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DIAMOND WIRE-SAWN SILICON WAFERS – FROM THE LAB TO THE CELL PRODUCTION

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Wafers for the PV industry are mainly sawn with a multi-wire slurry saw. This process is slow (it takes almost half a day to complete a cut) and generates a lot of waste: around half the silicon is sawn away and contaminating the slurry, and the wire is worn and has lost strength. After each cut, the slurry has to be cleaned from the silicon debris and the wire has to be exchanged. In contrast, sawing the wafers with a diamond-plated wire is faster, requires only a cooling liquid that is easy to filter from silicon debris and uses a wire that can be kept for several cut. But this new sawing technique only has a chance to develop if the solar cell production lines developed for slurry sawn wafers is capable of processing these diamond-plated wire sawn wafers efficiently. This study focused on the differences of surface properties of wafers cut via a slurry wire-saw and via a diamond-plated wire-saw. From these surface differences, it is possible to explain the differences in cell processing behaviour and to update the cell production line. Finally, it is shown that wafers sawn with a diamond-plated wire can give cells that are as efficient as the slurry sawn wafers, which validates this new diamond-plated wire wafering method for the production of solar cells.
Keywords: c-Si, wire saw, texturisation

1 INTRODUCTION

The mainstream wafering technology is currently slurry wire-sawing: the silicon blocks are cut by the action of a smooth steel wire on which an abrasive slurry is poured [1, 2, 3]. This slurry is made of a fluid – usually polyethylene glycol (PEG) – and of abrasive particles – usually silicon carbide (SiC). The action of the particles cut the silicon into wafers, but also wears the wire, which has to be changed after each cut. This process is fairly slow (almost half a day) and generates a lot of wastes: the worn steel wire, but also the slurry that contains silicon debris that have to be taken out before the slurry is used again. An alternative to this method is emerging in the form of diamond-plated wire cutting [4, 5]. The same saw is used for slurry wire-sawing, but the wire is replaced by a wire on which diamond particles have been attached and the abrasive slurry is replaced by a cooling liquid. It provides many advantages, like a higher productivity, an easier recycling of the cooling liquid (as all the particles have to be removed in order to have a refreshed liquid, in contrast to the standard abrasive slurry where the small silicon debris have to be removed, but the coarser SiC particles have to be kept), and a lower wear of the wire (the diamonds only are wearing off, but much slower than the steel wire used for slurry wafering), which can be used for many cuts. Furthermore, the wafering with a diamond-plated wire is much faster than the slurry wafering, increasing the productivity of the wire-saw. However, the surface of the wafers produced with this new technology is different and this method is suited for the PV industry only if it requires a minimal upgrade of the solar cell production lines. This study concentrates on the fundamental surface differences between a slurry sawn wafer and a diamond-wire sawn wafer.

2 EXPERIMENTAL METHOD

Monocrystalline (001), 125x125 mm^2, pseudo-square ingots were separated into two batches. One batch was cut with a slurry wire saw into 200 µm thick wafers as reference, the other with a diamond-wire saw into 200 µm thick wafers [6]. These wafers were analysed and characterised before being processed into solar cells at Q-Cells SE. The analysis consisted into a study of the topography (with SEM pictures and optical roughness measurements), an EDX chemical analysis and a Raman analysis of the surface, a study of the KOH texturisation behaviour, and finally a characterisation of the cell efficiency.

The SEM analysis was made with a Tescan Lyra SEM and the EDX spectra were taken with a Hitachi S-4800 FEG SEM. The Raman spectra were acquired with a Dilor XY800 with a 514 nm laser and a spot size of 1 µm. The Raman spectroscopy allows to measure the crystalline phases present on the sample, as silicon can be present not only in the stable diamond lattice that is well known, but can also be present in the form of meta-stable phases like nanocrystalline Si-III and Si-XII that are formed when the sample is slowly relaxing from high pressure, or amorphous silicon that is formed when the relaxation was fast [7, 8, 9, 10]. Furthermore, it is also possible to measure the stress on the sample by measuring the displacement of the peaks towards higher or lower wavelengths.

The roughness and TTV of the wafers were measured with a MircoProf chromatic white light profilometer from Fries Research & Technology. The roughness was measured on 5 non sequential wafers over 5.6 mm long profiles, as recommended by the norm ISO 4287. The TTV was measured on profiles perpendicular to the wire direction, also on 5 non sequential wafers for each wafer type.

The wafers were finally processed into solar cells on an industrial production line by Q-Cells SE. Each batch consisted of around 50 wafers. The properties of each cell were finally measured in-line at the end of the production.

3 RESULTS

3.1 SEM analysis

Samples from both wafer types were analysed. Typical surface of the wafers are shown in Figure 1. The

surface of the slurry sawn wafer (Fig. 1.a) is typical from this sawing process: a rough surface can be seen, with no indication of the wire direction during sawing. On the contrary, the surface of the diamond-wire sawn wafers (Fig. 1.b) shows smooth parallel grooves done by the diamond particles scratching the surface. These smooth grooves are sometimes interrupted by chips that were broken off, leaving a rougher surface. On the side of the grooves, slumps of silicon can also be seen. On both surfaces, cracks are not visible. The surface of the diamond-wire sawn wafers shows that the diamond particles are scratching the surface over long distances, possibly giving rise to a thicker oxide layer. EDX measurements were done at low accelerating voltage (3 kV) to enhance the detection of the oxide. As a reference, a sample of (001) silicon with a 20 nm thermically grown oxide layer was taken, as well as a slurry sawn wafer. Figure 2.a shows spectra for the 20 nm thick reference: the silicon peak (at 1.8 kV) is clearly visible, as well as the oxygen peak (at 0.5 kV). The slurry wafer (Fig. 2.b) shows a small, but distinguishable oxygen peak, that should correspond to a oxide thickness around 1 nm. The spectrum from the chipped-off region of the diamond-wire sawn wafer (Fig. 2.c) presents an oxygen peak equivalent to the one on the slurry sawn sample. The spectrum taken on the groove (Fig. 2.d) shows a slightly larger oxygen peak, but still much smaller than the one of the reference spectrum, meaning that the oxide layer is barely thicker than on the chipped-off regions in its thickest regions. The magnitude of variations of the oxygen peak on the diamond-wire sawn wafer corresponds roughly to the magnitude of variations that can be observed on the slurry sawn sample, implying that the oxide layer thickness on both types of samples are comparable.

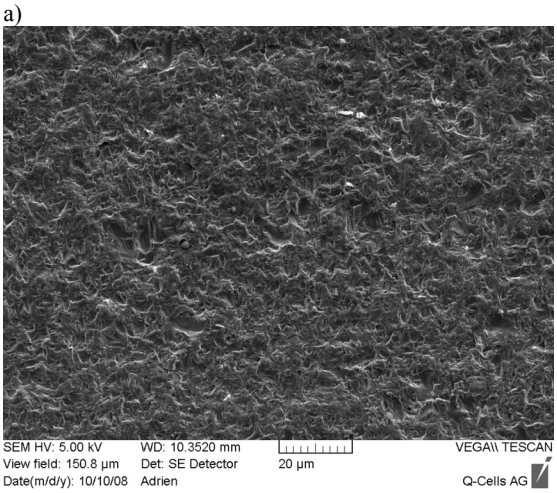
3.2 Raman analysis

As silicon is brittle and as the smooth grooves cannot be explained by a melting-quenching of the surface leading to the formation of a thick oxide layer, the samples were analysed with a Raman spectrometer to check for a phase transformation. It is known that when scratched at low load, silicon undertakes a phase transformation rendering it ductile [7]. This results in a layer of amorphous silicon or – if the scratch is slow enough – into a mixture of amorphous and metastable phases (called Si-XII and Si-III), in the same fashion as the phase transformation seen during nanoindentation [8]. When the indenting (or scratching) tip is pressed on the silicon, it induces a high local pressure, transforming the brittle silicon into a ductile phase (called Si-II). Upon unloading, this ductile phase in not stable and transforms into a mixture of amorphous and metastable silicon phases, which relative importance depends on the indentation parameters [9].

The Raman analysis of the wafers showed that there is only crystalline silicon present on the slurry sawn wafers, but that amorphous silicon is present on the diamond-wire sawn wafers. As it was already seen with the SEM, two types of surfaces are present: the rough parts, where material was chipped off, are only made of stable crystalline silicon (Fig. 3.a), and the smooth grooves, where amorphous silicon (and sometimes also metastable phases) is present (Fig. 3.b). A map of the surface of a diamond-wire sawn wafer (Fig. 4.a) was made by taking an array of spectra and fitting them to a mix of a Gauss distribution and a Lorentzian distribution for the amorphous silicon and a Lorentzian distribution for the crystalline silicon. The thickness of the amorphous layer was measured, by taking electron back-scattered diffraction (EBSD) patterns of a wafer cross-section, to be between 200 and 600 nm.

Furthermore, Raman spectroscopy allows to measure the stress level of the crystalline silicon with the movement of its peak to higher (when the silicon is in compression) or lower (when the silicon is in tensile stress) wavelengths. A map of the stress is presented in figure 4.b. It shows that the amorphous silicon induces a compressive stress into the crystalline silicon beside it and that the small chipped-off regions on the side of grooves are under a tensile stress.

a)



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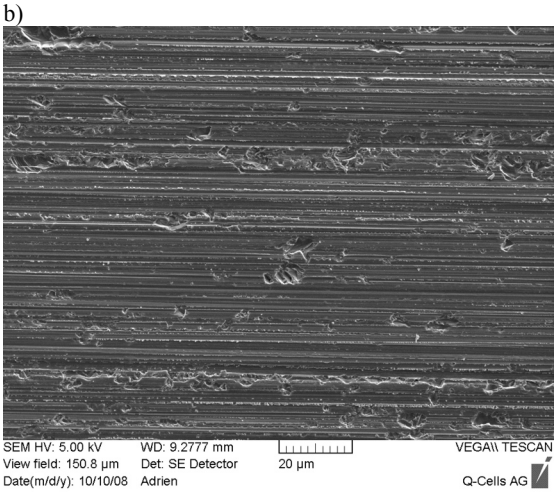


Figure 1: SEM image of the surface of a) a slurry sawn wafer. The surface is rough, but direction of the wire during sawing is not visible. b) Surface of a diamond-wire sawn wafer. Grooves indicating the direction of the wire during sawing can be seen. These grooves are mostly smooth, but traces of chips that broke off the surface can be seen.

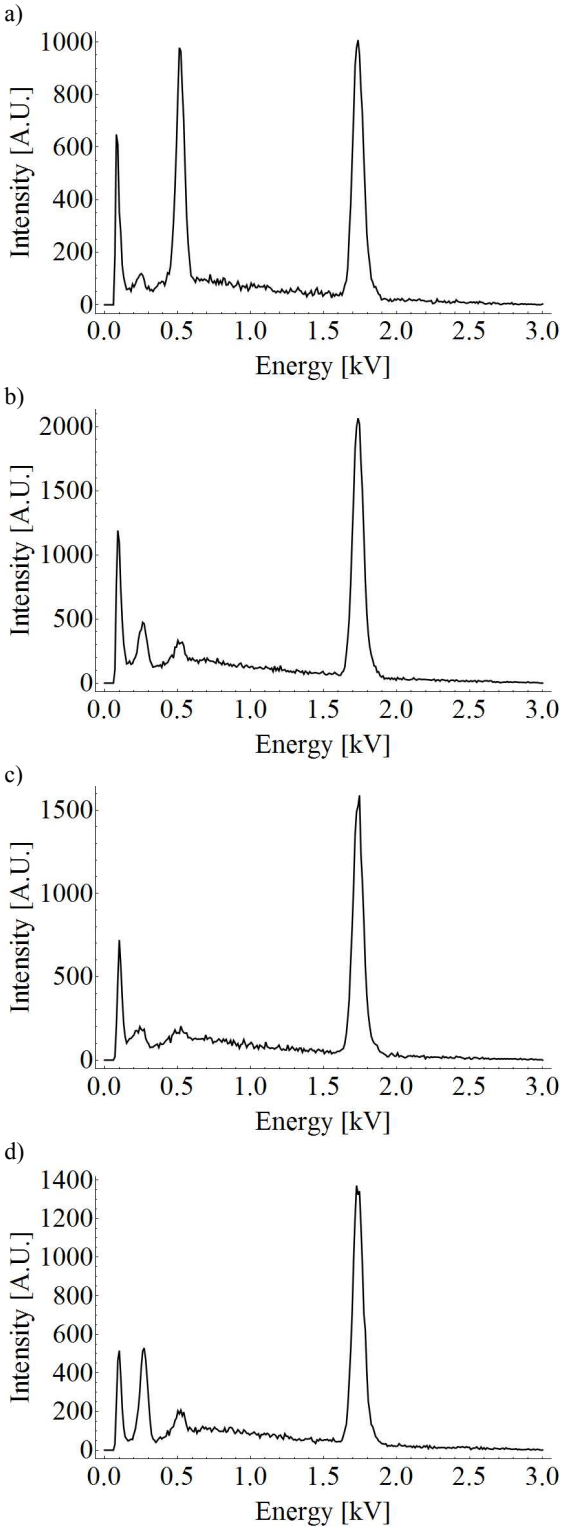


Figure 2: EDX Spectra of the surface. The oxygen peak is around 0.5 kV and the silicon peak is around 1.8 kV. a) a reference sample with 20 nm of oxide, b) the surface of a slurry sawn wafer, c) in a region were silicon chipped off a diamond-wire sawn wafer, d) In a smooth groove of a diamond-wire sawn wafer, where the oxygen peak is slightly larger than on chipped-off regions.

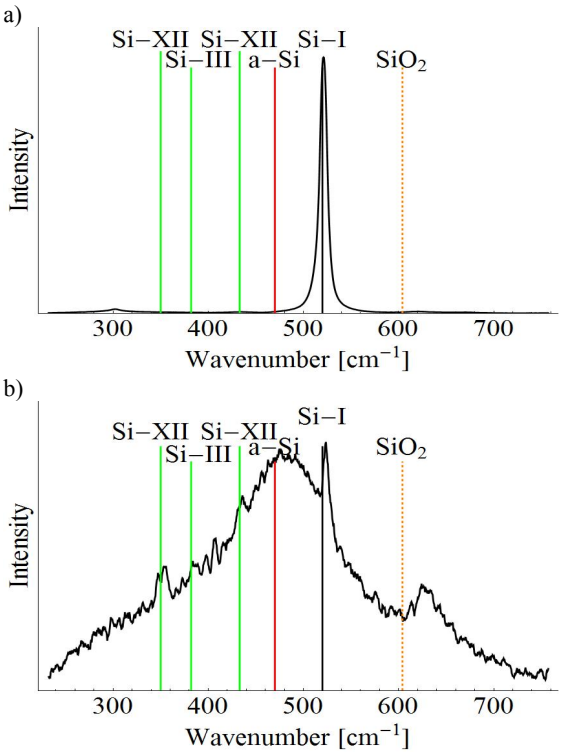
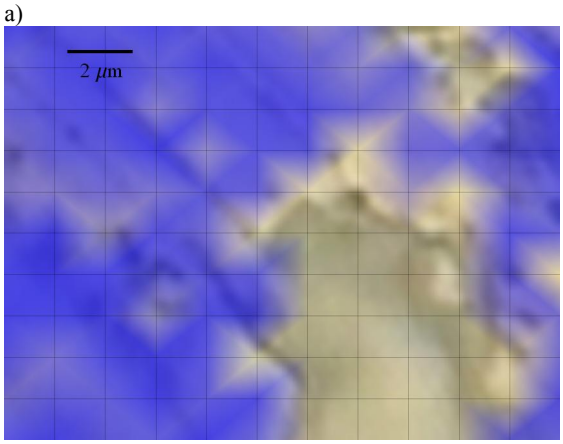


Figure 3: Raman spectra of a) a chipped-off region and b) a smooth groove. Only crystalline silicon can be seen in the chipped-off region and mostly amorphous silicon can be seen on the groove.

a)



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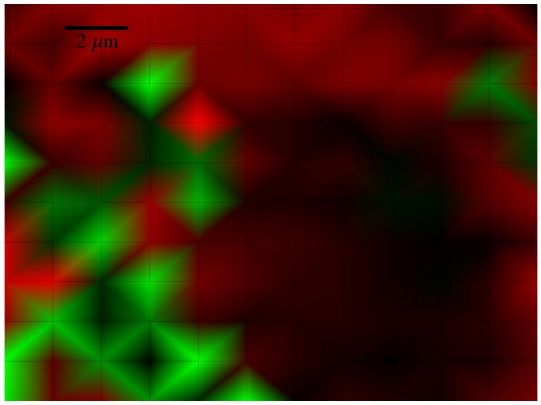

Figure 4: a) a map of the amount of amorphous silicon is superimposed to an optical micrograph. The blue regions indicate an important amount of amorphous silicon, and the transparent regions indicate an absence of amorphous silicon. It can be seen that the chipped-off region does not present any trace of amorphous silicon, but the regions where the grooves are present are amorphous. b) map of the stress in the crystalline silicon at the same region than a). The red indicate a compressive, the green a tensile stress and black indicates an absence of stress.

3.3 Roughness analysis

Comparing the roughness of the wafers, several differences exist between the two types of wafers. The surface of slurry sawn wafers are typical of a three-body abrasion process [11] and do not show a strong influence of the roughness measurement direction, but the diamond-wire sawn wafers present a surface typical of a two-body abrasion process, with a strong anisotropy of the topography. Furthermore, the roughness of the slurry sawn wafers diminishes between the entrance of the wire into the ingot and its exit. This is not the case for the diamond-wire sawn wafers: the roughness stays constant on the whole path of the wire (Fig. 5). But at the wafer scale, the surface of the diamond-wire sawn wafers show larger thickness difference compared to slurry sawn wafers. This is due, for some part, to the fact that the diamond-wire sawn wafers were cut with the wire going back and forth and a fast feed rate, thus making hills at each wire direction inversion (Fig. 6), but this occurs more often than the large thickness variation that are measured, so that it cannot explain most of the thickness variation. The slurry sawn wafers are cut with the wire going in one direction only, and do not present a regular thickness variation pattern.

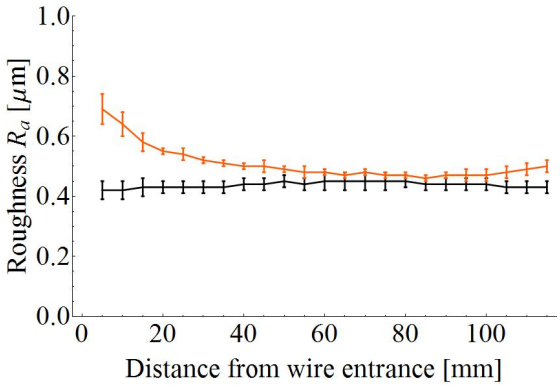

Figure 5: Roughness (measured perpendicularly to the wire direction) of a slurry sawn wafer (in red) and of a diamond-wire sawn wafer (in black). In contrast to the classical slurry sawn wafers, the diamond-wire sawn wafers do not show an evolution of the roughness with the distance from the wire entrance.

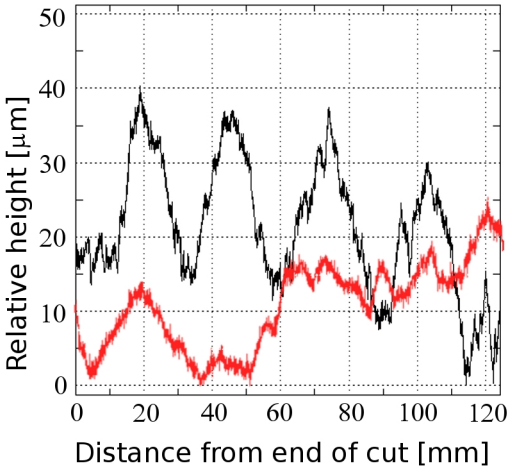

Figure 6: Profile of a slurry sawn wafer (in red) and a diamond-wire sawn wafer (in black) in a direction perpendicular to the wire direction. The changes in wire directions are clearly marked on the diamond-wire sawn wafer, making a large thickness difference.

3.4 Etching of wafers

The first step of the solar cell production consists of a texturisation to increase the absorption of light. On mono-crystalline wafers, it is done by an anisotropic etching, forming pyramids on the surface of the wafers. The thickness of silicon etched away is detrimental to determine the size of these pyramids, and thus their efficiency in light-trapping. For the slurry sawn wafers, a standard etching time is defined to produce a surface that absorbs light well enough. It is not the case of diamond-wire sawn wafers: after standard etching time, the thickness decreased by only one third of what was

expected and the surface was reflecting light too much. A second round of etching was necessary to have a well-developed enough texture. The relative etched depth of the wafers after each etching step is shown in figure 7. Based on C. Rohr [12], it seems possible that if the silicon is being sawn under other conditions, the wafers may have an etching rate comparable to standard wafers. These wafers then require the same etching procedure than slurry sawn wafers. But this work is still in progress.

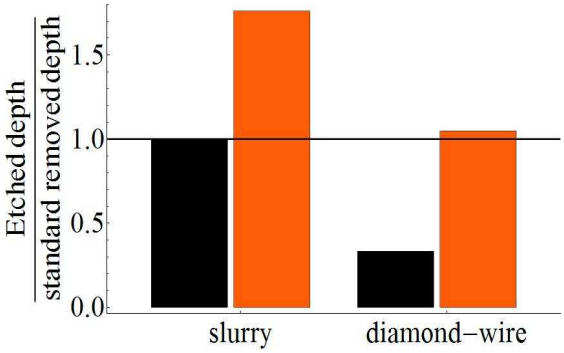

Figure 7: Relative etching depth after the etching process. In black: after the (standard) first etching. The diamond-wire sawn wafers were not etched as fast as the slurry wafers and had a high reflectivity. After a second etching (in orange) which does not occur in the standard production, they had a thickness comparable to the slurry wafers after one etch and an acceptable reflectivity.

3.5 Solar cell efficiency

The most important result to consider the validity of diamond-wire sawing to produce wafers is the efficiency of the solar cells. As expected from the etching process, the diamond-wire sawn wafers which were etched only once showed a lower efficiency compared to the slurry wafers (Table I). This cannot be imputed to the quality of the silicon, as both ends of the ingot were sawn with slurry and gave equivalent efficiencies (the samples are named Slurry A and Slurry B in Table I), but the middle part of the ingot – which was sawn with a diamond wire – gave lower efficiency. In contrast, the diamond-wire sawn wafers that were etched twice showed an efficiency comparable to the slurry wafers (that were etched once).

Table I: Efficiency of the solar cells.

	Slurry A	Diamond 2 etches	Slurry B	Diamond 1 etch
Efficiency	16.88%	17.07 %	17.03 %	16.21 %

4 DISCUSSION

The SEM pictures show that the surface of the wafers depends on the sawing method. The surface of slurry sawn wafers is made by a three-body abrasion process where the abrasive particles are free between the wire and the silicon ingot. They are indenting the surface, thus removing material and creating defects (cracks and roughness) [1, 2, 3, 13, 14]. With the diamond-wire sawing, the material removal process is different, as parallel grooves can be seen on the surface. This is typical of a 2-body abrasion mechanism. This calls for a complete change of paradigm, a different wear mechanism being not governed by the same parameters than the slurry sawing. One of the consequences is that the wafer surface roughness cannot be used as a mean to measure the sawing quality as with slurry sawing [13]. The slurry sawing can be related to indentation of the surface by the abrasive particles, which creates cracks and roughness that are correlated. On the contrary, the diamond-wire sawing process can be better thought of as scratching the surface, creating cracks, but also a region of phase transformation [7]. Gassilloud *et al* [7] found that scratching at a low load produced a smooth groove with either amorphous silicon on its surface, or a mixture of nanocrystalline metastable silicon and amorphous silicon if the scratching was slow. The surface of wafers sawn with a diamond-plated wire shows exactly the same topography, with mostly amorphous silicon inside the smooth grooves.

Sawing with a diamond-plated wire is much more efficient than slurry sawing. The sawing speed can be 3 times faster than usual slurry sawing speed [5]. Thus, a large flow of heat has to be extracted from the cutting zone by the coolant. If the heat extraction is not efficient enough – for instance at the vicinity of the diamond particle scratching the silicon – the silicon surface can be heated up, allowing for a thicker oxide layer to form. From the thickness of the oxide layer obtained on the diamond-wire sawn wafers, it can be concluded that the temperature of the surface was in the same range than the one of the slurry sawn wafers.

The difference in sawing mechanism also explains the difference in the etching process. The slurry sawn wafers are free of amorphous silicon and only have a thin native oxide on the surface. On contrary, diamond-wire sawn wafers have an important fraction of the surface covered with a layer of amorphous silicon, and an oxide layer of comparable thickness with the one of the slurry wafers. Both the oxide layer and the amorphous layer act as masks when etching the wafers: thermal oxide is routinely used for structuring silicon, and Kawasegi *et al* [15] showed that a layer of amorphous silicon formed by scratching the surface with a diamond tip could also act as an efficient mask. They stated that the amorphous layer had an etching rate approximately 30 times slower than the (001) direction [15].

The oxide layer, only marginally thicker than the one of slurry sawn wafers – and not strongly varying – cannot explain the slower etching speed, but the amorphous layer, much thicker than the oxide layer, can explain the etching rate difference.

From a solar cell production point of view, the diamond-wire sawn wafers can be better suited than the slurry sawn wafers, as the thickness variation in the wire direction is lower. Indeed, as the wafer thickness is going to decrease, the thickness variation is going to be a more and more important factor. The diamond-plated wire, because the abrasive particles are bound to it and are wearing slowly, produces wafers that may have less TTV. Also, as Gassilloud *et al* [7] showed, it is possible to scratch silicon in an entirely plastic fashion, without any crack, if the scratching force is low enough. This would, if applicable to the wafering, provide wafers with only shallow cracks – thus much tougher than standard wafers – while still keeping an acceptable productivity. The main problem of the wafers described here is the large thickness variation perpendicular to the wire direction. This variation can indeed limit the wafer thickness decrease, but might be circumvented by a better control

of the process, from the wire diameter to the ingot feed speed control.

5 CONCLUSION

In this study, it was shown that the surface of diamond-wire sawn wafers is fundamentally different than the surface of slurry sawn wafers. The surface of the diamond-wire sawn wafers can be compared to nano-scratches of silicon. The shape of the smooth grooves and the presence of amorphous silicon is found both on the sawn wafers and on nano-scratches made on a polished wafer. The presence of amorphous silicon acting as a mask during the etching imposes a change in the etching protocol. It is possible to overcome this issue either by changing the etching protocol, or by increasing the etching time as it was done here. Alternatively, these problems might also be circumvented by changing the sawing conditions [12].

The cells obtained with the updated etching protocol showed an efficiency comparable to the slurry sawn wafers used as a reference. This indicates that it is possible to use diamond-wire sawn wafers to produce high quality solar cells without significant changes in the cell production line and validates the use of a diamond-plated wire as a possible cutting medium.

6 ACKNOWLEDGEMENTS

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7 REFERENCES

[1] H J. Möller, Adv. Eng. Mat. 6, No. 7, 501 – 513, 2004.
[2] H. J. Möller, phys. Stat. Sol. (a) 203, No.4, 659 – 669, 2006.
[3] M. Bhagavat, V. Prasad, I. Kao, Journal of tribology, 394, Vol. 122, 394 – 404, 2000.
[4] P. Tso, B. Yan, C. Lo, Materials Science Forum Vols 505-507, 1219 – 1224, 2006.
[5] Y. Kondo, N. Watanabe, D. Ide, et al. Proceedings of the 23rd EUPVSEC, Valencia, 1297 – 1301, 2008.
[6] J.-I. Bye, S.A. Jensen, F. Aalen et al. Proceedings of the 24th EUPVSEC, 2CV.1.40, 2009.
[7] R. Gassilloud, C. Ballif, P. Gasser, et al. Phys. Stat. Sol. (a) 202, No. 15, 2858 – 2869, 2005.
[8] A. Kailer, Y. G. Gogotsi, K. G. Nickel, J. Appl. Phys. 81 (7), 3057 – 3063, 1997.
[9] J. Jang, M.J. Lance, S. Wen, et al. Acta Materialia 53, 1759 – 1770, 2005.
[10] V. Domnich, Y. Gogotsi, Rev. Adv. Mater. Sci. 3, 1 – 36, 2002.
[11] K. Adachi, I. M. Hutchings, Wear 255, 23 – 29, 2005.
[12] Private communication, C. Rohr, 2009.
[13] A. Bidiville, K. Wasmer, J. Michler, et al. Proceedings of the 22nd EUPVSEC, 2007.
[14] A. Bidiville, K. Wasmer, J. Michler, et al. proceedings of the 23rd EUPVSEC, 1311 – 1315, 2008.
[15] N. Kawasegi, N. Morita, S. Yamada, et al. Nanotechology 16, 1411–1414, 2005.