Ultra-Low Power Mixed-Signal Design Platform Using Subthreshold Source-Coupled Circuits

Armin Tajalli and Yusuf Leblebici
Microelectronic Systems Lab. (LSM)
Ecole Polytechnique Fédéral de Lausanne (EPFL), CH-1015 Lausanne, Switzerland
Email: {armin.tajalli, yusuf.leblebici}@epfl.ch

***Abstract*—This article discusses system-level techniques to optimize the power-performance trade-off in subthreshold circuits and presents a uniform platform for implementing ultra-low power power-scalable analog and digital integrated circuits. The proposed technique is based on using subthreshold source-coupled or current-mode approach for both analog and digital circuits. In addition to possibility of operating with ultra-low power dissipation, because of similar basis for constructing analog and digital parts, a common power management unit could be used for optimizing the power-performance of the entire mixed-signal system. Some circuit examples have been provided to show the performance of the proposed circuits in practice.**

I. Introduction

The demand for implementing ultra-low power systems in a cost-effective manner typically creates a set of conflicting constraints at the circuit level that complicates the design process [1]. This trend could be seen more clearly in digital domain where process engineers, circuit designers, and system level developers work together to achieve the desired specifications [1],[2]. In system level, high-level techniques such as dynamic voltage-frequency scaling (DVFS) scheme or dynamic body biasing have been proposed to optimize the circuit operating conditions with respect to the work load [1]-[3]. On circuit and process level, devices with optimized parameters (such as threshold voltage, gate oxide, doping density, etc.) along with complicated circuit topologies are used to minimize the dynamic and static power consumption of the circuits [4], [5]. The tight tradeoff exists among process parameters and circuit performance, calls for a close collaboration between circuit designers and process engineers [5].

Through technology scaling, leakage current and process variation increases rapidly which makes the design of power-efficient circuits very challenging [3], [5]. Ultra-low power circuits which are using subthreshold CMOS building blocks are very sensitive to process variations mainly due to the exponential I-V characteristics of the devices [6]. This property has encourages designers to work on above-threshold region instead of subthreshold regime in order to mitigate the process sensitivity problem. Generally a precise control on the circuit supply voltage is required to adjust the power consumption and speed of operation with respect to the work load [7], [8].

In this work, a unified approach for implementing ultra-low power integrated circuits will be introduced, based on subthreshold source-coupled or current-mode techniques. Employing this technique for implementing ultra-low power digital circuits have been already introduced in [9], [10]. Here, the idea is extended for constructing mixed-signal circuits and systems with possibility of having a uniform and common power-frequency management scheme for both parts. It should be noted that the goal is not to propose a complete replacement for the conventional CMOS topology, yet the proposed approach is well suited specially for ultra-low power scalable performance mixed-signal circuits. The main features of this approach could be summarized as the following:

- Subthreshold source-coupled logic (STSCL) circuits are used to reduce the circuit power dissipation well below the subthreshold power dissipation of CMOS circuits. This improvement is especially more pronounced in low activity rate systems [11].
- This family of circuits are less sensitive to the process and temperature variations. Due to their differential topology, supply voltage variation has a minor effect on circuit performance.
- It is possible to implement analog building blocks with compatible power-frequency behavior and construct complicated mixed-signal integrated circuits.
- A uniform and common power management scheme for both analog and digital sections can be used to optimize the system performance.
- This type of circuits exhibit a very low sensitivity to supply voltage variation. This is in stark contrast to the CMOS logic circuits where speed and power dissipation are both depending very critically on supply voltage. This property is especially important in applications where supply voltage can vary considerably during the operation, such as circuits based on energy harvesting and energy scavenging.

In the following, the concept of developing subthreshold source-coupled circuits is explained and practical examples are given.

II. Subthreshold Source-Coupled Mixed-Signal Circuits

In most of ultra-low power applications such as sensor networks and biomedical implants, the system consists of both analog and digital parts. Generally in such mixed-signal systems, the digital part is responsible for processing the raw data extracted by the analog part and there is a continuous interaction between these two sections. Therefore, to optimize

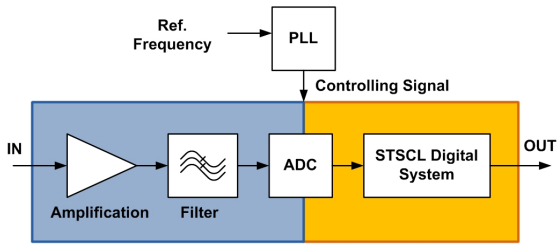

Fig. 1. Concept of an ultra-low power mixed-signal circuit using source-coupled circuit with adjustable power consumption versus frequency of operation.

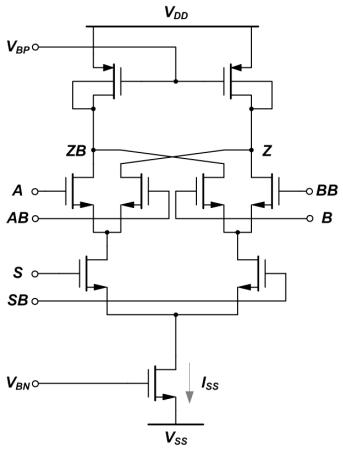

Fig. 2. Generic subthreshold source-coupled logic (STSCL) circuit [9].

the energy-performance balance in such systems, it is necessary to include both sections in the optimization process.

Figure 1 illustrates a conceptual mixed-mode circuit constructed using source-couple circuits. The main advantageous of using such a system is that a unique controlling unit could be used to tune the operating condition of the entire system and hence optimize the performance of the entire system. This is mainly because of using a common base topology for analog and digital parts, as will be explained in the following.

A. Subthreshold Source-Coupled Logic (STSCL)

1) Circuit Topology: Figure 2 shows a generic STSCL circuit could be used for ultra-low power applications [9]. While the logic operation takes place in current domain and in NMOS switching network, the output current will be converted to voltage using load resistances. In case the power consumption is very low, very high-valued load devices with enough output swing are required to provide enough voltage swing at the output [10]. The PMOS load devices in Figure 2 with shorted bulk-to-drain are implementing the required high-valued load resistances.

2) Power-Delay Tradeoff: In conventional CMOS circuits, the power-delay tradeoffs are linked to the supply voltage, V_{DD}, and process parameters such as gate oxide thickness, t_{ox}, and threshold voltage, V_T [12]. However, in STSCL topology the tradeoffs are more relaxed and speed of operation depends only on the tail bias current of each cell, I_{SS}. The circuit performance as well as the noise margins are virtually independent of the supply voltage [11]. As it is shown in [11], this topology can show comparable performance with respect to the conventional CMOS topology when the power dissipation of CMOS circuit is mostly dominated by the leakage current.

Assuming that the longest logic depth in a system operating at f_{op} is N_L, then the power consumption of an STSCL cell placed in the longest path can be calculated by:

$$P_{STSCL} = k \cdot N_L \cdot f_{op} \cdot V_{DD} \tag{1}$$

where $k = 2 \ln 2 V_{SW} C_L$, depends on voltage swing at the output of the proposed STSCL gate, V_{SW}, and loading capacitance, C_L. Based on (1), in a specific design with defined V_{SW} value, the power dissipation of the digital circuitry can be adjusted linearly with respect to the operating frequency. As shown in Figure 1, this can be done by a phase-locked loop (PLL) circuit.

Regarding (1), one important issue with STSCL topology is that the circuit power consumption depends on logic depth. Therefore, building circuits with deep logic depths can cause a considerable increase in power dissipation. Some remedies for reducing logic depth and improving power efficiency of STSCL circuits is proposed in [13]. A similar technique has been used in this work to reduce the power consumption of the digital circuitry, explained in Section III-B.

Figure 3 compares the relationship between design and process parameters in CMOS and STSCL topologies. It can be seen that there is a tight tradeoff among process, design, and performance parameters in CMOS topology. This tradeoff is more relaxed in STSCL topology. Interestingly, process parameters do not affect the STSCL circuit dynamics as severely as in the CMOS case. Therefore, they can be selected independently to reduce the circuit stand-by (leakage) current. For example, high V_T tail bias transistors could be used (MB in Figure 2) in order to control precisely the tail bias current [11]. Also, transistors with thick gate oxide can be used in STSCL circuits to help achieving a negligible gate leakage current without degrading performance. This is especially important when the tail bias current reduce s to few pico-Amperes and hence any source of leakage current needs to be very carefully treated.

One of the most important features of the current-based STSCL topology is the effective decoupling of the power dissipation from voltage swing, and thus, from noise margins. This fact allows the circuits to be designed and optimized for specific operating conditions without violating other constraints, in contrast to conventional CMOS logic operating in subthreshold. Note that the tail bias current becomes a completely independent design parameter that can be set individually to achieve a certain delay constraint (and hence, to determine the power dissipation), without any connection to the supply voltage nor the noise margins. Another important fact is that the tail bias current of such STSCL circuits can be

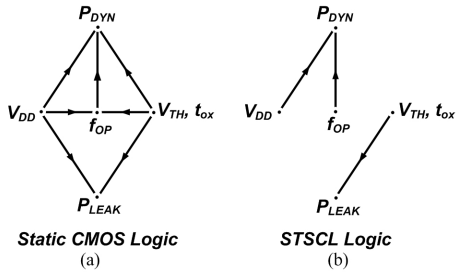

Fig. 3. Tradeoffs in design of digital integrated circuits based on: (a) conventional CMOS topology, (b) subthreshold source-coupled logic (STSCL) topology.

controlled very precisely using a current mirror and a replica bias generator. Note that this precisely controllable tail bias is the only current consumption of the entire circuit, as opposed to the unpredictable subthreshold leakage currents that must be taken into account in all CMOS circuits.

B. Power Scalable Analog Circuits

Current-mode approaches for implementing analog integrated circuits have been popular mostly because of their inherent speed advantage [18]. Even in low-power applications where MOS devices are mostly biased in subthreshold regime, current-mode circuits exhibit a good power-speed performance [19]-[21].

In this work, the aim of using subthreshold current-mode approach is to implement very low power circuits with scalable power-frequency performance. As mentioned before, scalability is mainly interesting for power management purposes. The exponential I-V characteristic of MOS transistors in subthreshold regime provides this possibility to scale their bias current in a very wide range while the bias voltages are changing proportional to logarithm of current [19]. This property makes them very suitable for power scalable applications.

There are many challenges in design of scalable analog circuits. By scaling the current in analog circuits, voltage bias levels should remain on acceptable condition. Moreover, special care needed to be taken into account to keep some other parameters such as frequency response of the circuit within desirable limits. For example, some parameters such as gain and phase margin should remain unchanged while unity gain bandwidth (UGBW) needs to be scaled with respect to the bias current [23]. These requirements typically render the design of scalable ultra-low-power analog circuits more challenging than digital circuits.

Simple source-coupled analog circuits such as single stage differential amplifier are good examples for widely scalable analog circuits. Some techniques for using source-coupled circuits for implementing widely adjustable analog circuits have been introduced in [17], [22], and [23].

The design example explained in Section III shows how source-coupled circuits could be successfully used for implementing some power scalable analog circuits.

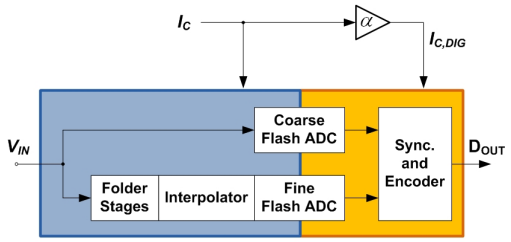

Fig. 4. The proposed scalable folding and interpolating ADC.

III. Design Example: Folding and Interpolating ADC

A folding and interpolating analog-to-digital (ADC) data converter topology has been selected to demonstrate the proposed approach for implementing mixed-signal circuits. Figure 4 illustrates the block diagram of this ADC. Compared to a fully parallel flash ADC, this topology needs fewer number of comparators and hence consumes less power with smaller silicon area occupation [14]. A coarse flash ADC extracts the few most significant bits (MSBs) of the input signal and a folding and interpolating scheme is used to extract the rest of bits [15].

In this work, STSCL topology is used to construct the digital part of the ADC. This part converts the output of coarse and fine ADCs to final digital outputs. For the analog part which consists of coarse and fine ADCs, a current-mode approach has been employed. In this way, it is possible to operate the circuit in very low bias currents and at the same time have a wide tuning range.

A controlling bias current adjusts the power consumption of analog and digital parts of this ADC with respect to the sampling frequency, f_s. The bias current of digital part, $I_{C,DIG}$, is a fraction of bias current of analog part, I_C.

A. Analog Building Blocks

1) Topology: Current-mode folding and interpolating first was introduced in [14]. Figures 5(a) and 5(b) show the circuit schematic of the folder and interpolator, respectively. Based on Fig. 5(a), the input voltage is converted to differential current. The output current is composed of three different parts, two of the equal and the third one is two times more than the others. Therefore, the folder stage is merged with the first interpolator. The outputs of the first stage are then applied to the current-mode interpolator circuit shown in Fig. 5(b). In this work, the interpolation factor is 8. Therefore, in addition to the first interpolation stage which is merged with the folder stage (Fig. 5(a)), two other interpolation stages based on Fig. 5(b) have been used. As long as the devices remain in subthreshold regime, the bias current and hence the frequency response of both circuits could be scaled in a very wide range. The circuit is designed for medium accuracy (6 to 8b), low-frequency (sub MHz range), biomedical applications where power dissipation is very critical. To have a wide tuning range and at the same

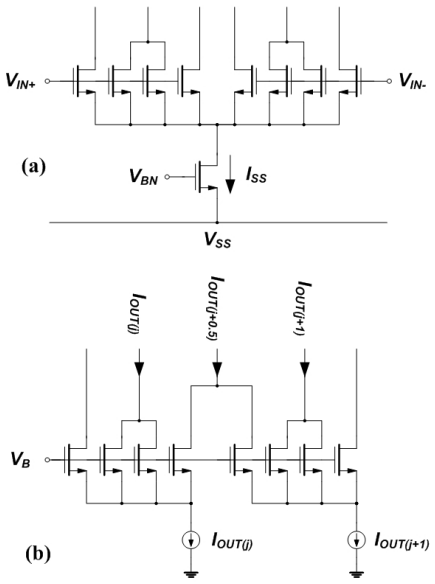

Fig. 5. Current mode implementation of: (a) folder, and (b) interpolator stages.

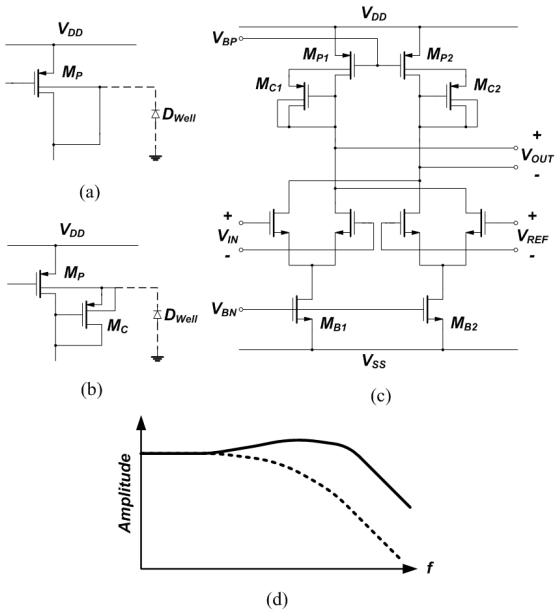

Fig. 6. (a) High valued load resistance. (b) Decoupling the parasitic capacitance of the well-substrate from output node. (c) Subthreshold pre-amplifier stage, (d) improvement of frequency response through parasitic capacitance decoupling.

time low power consumption, all the MOS devices are biased in subthreshold regime.

2) Comparator: Comparators are critical components in design of a FAI ADC. To reduce the sensitivity of the circuit to comparator offset, a low gain pre-amplifier stage is used in front of the comparator. The pre-amplifier used in this work is based on a single stage double differential amplifier as shown in Fig. 6. To have a wide frequency tuning range, the topology of the pre-amplifier is selected to be similar to the STSCL gates shown in Figure 2 where all the transistors are biased in subthreshold. Illustrated in Fig. 6(a), the reverse biased diode of the nwell-to-substrate PN junction (D_{Well}) appears directly at the output of pre-amplifier, and hence reduces the circuit bandwidth. To decouple this capacitance from the output node, a very high-valued load resistance has been added in series to the bulk-drain of the load devices. This resistance can be implemented by MC as illustrated in Fig. 6(b). Using this technique, the double difference preamplifiers (Fig. 6(c)) and comparator stages have been implemented. In each transition, the parasitic capacitance due to D_{Well} charges and discharges with a delay due to the RC delay constructed by resistance of MC and capacitance of D_{Well}. This structure acts as a zero in pre-amplifier transfer function and can improve the speed of circuit response as illustrated in Fig. 6(d).

3) Resistor Ladder: To design a power-frequency scalable ADC, it is also necessary to implement a very-low power and precise resistor ladder (Fig. 7(a)) with scalable equivalent resistivity of the components. Scalability of the resistivity helps to adjust the power consumption of this part of circuit with respect to the sampling frequency.

Using conventional techniques, it is not possible to reduce the power consumption of this part below 1μW since the required resistance will be very large. Meanwhile, the resistivity of the ladder should be adjustable with respect to the sampling frequency. To implement a high valued resistance for resistor ladder, the topology shown in Fig.7(b) can be used [17], [10]. In this topology, MR exhibits a very high resistivity which can be controlled over a very wide range by adjusting the source-gate voltage (V_{SG}) of this device. In Fig. 7(c), MLS is used

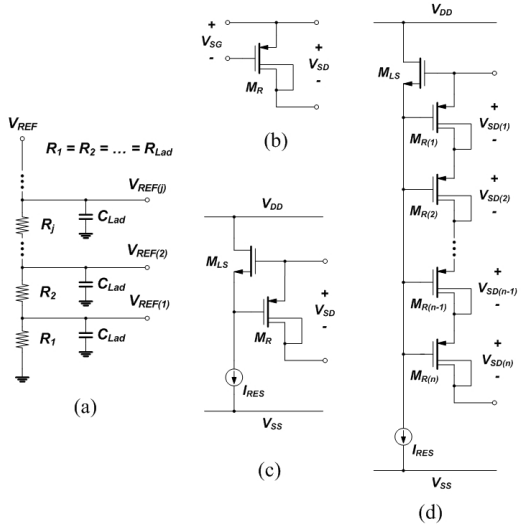

Fig. 7. Low power resistor ladder implementation: (a) Ideal resistor ladder used to generate reference voltages. (b) high-value resistance based on subthreshold PMOS device, (c) biasing the proposed high-value resistance where the resistivity can be adjusted through I_{RES}, (d) compact resistor ladder sharing the same biasing circuitry for more than one resistance.

to adjust the V_{SG} of MR by tuning I_{RES}. Therefore, each resistance is constructed by two MOS devices and a current source. When the number of resistors in the ladder is high (for example 256 for an 8-bit flash ADC), then the power consumption due to the controlling part (MLS and I_{RES}) can significantly be increased. Figure 7(d) shows a remedy to reduce the number of required controlling part by sharing MLS and I_{RES} among more than one resistance.

B. Digital Circuitry

The outputs of fine and coarse sub-ADCs need to be merged to construct the final output bits. Also, the outputs of the coarse sub-ADC need to be synchronized with the outputs of the fine sub-ADC after error correction [14]. In the first step, at the output of coarse sub-ADC, the majority detector circuits are used to remove the possible bubbles at the output thermal code. Then the thermal code is converted to Gray code and finally to binary codes.

Here, STSCL topology has been used to implement the digital encoder circuit. To improve the power efficiency of STSCL digital part, two techniques have been employed:

- Using stacked NMOS differential pairs in the switching network to construct compound logic operations [10]. In this way, it is possible to merge the functionality of two or more STSCL gates in only one gate and reduce the power dissipation and area, simultaneously [13].
- Using pipelining technique that reduces the logic depth to practically one gate as described in [10], [13], and [16].

Figure 8 illustrates how these two techniques have been employed to design an STSCL majority cell. Stacking of three layers of NMOS differential pairs help to do desired complicated the logic operation in only one stage. Meanwhile, a latch has been used at the output of majority cell for implementing pipelining technique. When the clock signal is high, the logic circuit is in evaluation phase and when clock goes low, the evaluated value will be kept at the output node for the rest of clock period. Therefore, the next stage can start its evaluation phase. As mentioned before, using pipelining can help to reduce considerably the power dissipation of STSCL circuits when logic depth is deep.

Bias current of digital circuit is a fraction of bias current of analog part, and hence the same controlling system could be used for both parts. This scheme considerably simplifies the control of power consumption in digital part. Also, using large enough transistor sizes can minimize the effect of current mismatch both in analog and digital parts [10].

C. Simulation and Experimental Results

Simulation results show that the encoder can operate in a wide range of frequencies by adjusting the bias current of the gates. Figure 9(a) shows the maximum frequency of operation of the encoder as a function of the tail bias current of the STSCL gates. Pipelining has helped to improve the power-delay performance of the circuit as explained in [10]. The bias current of the digital circuit is set to be a fraction of the bias current of the analog section, therefore, a separate controlling

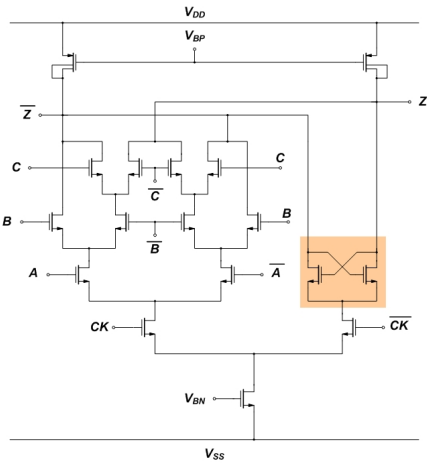

Fig. 8. Current-mode realization of the majority detector cell.

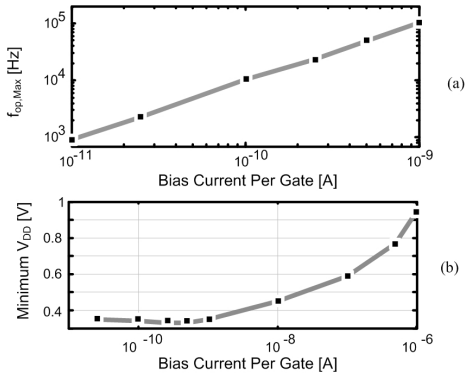

Fig. 9. (a) Simulated maximum operation frequency of the digital section as a function of tail bias current per gate. (b) Simulated minimum required supply voltage for digital part versus tail bias current per gate.

unit is avoided. The encoder circuit consisting of 196 STSCL gates.

Figure 9(b) illustrates the minimum supply voltage of digital part with respect to the gate tail bias current. For tail bias currents below 10nA, the supply voltage could be reduced below 0.5V. When tail bias current goes below 1nA, the supply voltage can be reduced to 0.35V, maintaining a signal swing of 200mV. However, as mentioned earlier, the choice of the supply voltage level does not have any impact on the operation speed and the noise margins..

Figure 10 shows the photomicrograph of the prototype test chip fabricated in 0.18μm CMOS technology. The total active area of the circuit is 0.6mm^2. The bias current of analog and digital parts are controlled externally with respect to the sampling frequency. The sampling frequency of the proposed ADC can be adjusted from 800S/s to 80kS/s where the power consumption is scaling proportional to the sampling frequency from 44nW (digital part: 2nW) to 4μW (digital part: 200nW) with ENOB of 6.5. The adjustment of power dissipation with respect to sampling frequency is achieved by changing the reference bias current. As can be seen, power dissipation of

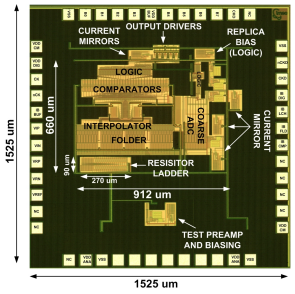

Fig. 10. Photomicrograph of the ultra-low-power ADC chip implemented in 0.18μm CMOS technology.

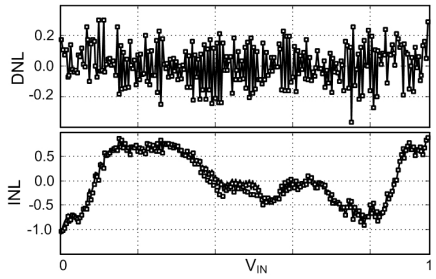

Fig. 11. Measured differential non-linearity (DNL) and integral non-linearity (INL).

digital part is negligible with respect to the total circuit power consumption. To have the same performance using CMOS logic circuits, a separate precisely controlled supply voltage would be needed.

Figure 11 shows the measured integral non-linearity (INL), and differential non-linearity (DNL) of the proposed FAI ADC which are 1.0LSB and 0.4LSB, respectively. As both digital and analog parts are based on differential topology, the sensitivity of the circuit to supply voltage variations is very low, and can be changed from 1.0V to 1.25V. An internal replica bias circuit controls the biasing condition of different parts of the circuit to minimize the effect of process, supply voltage, temperature (PVT) variations.

IV. Conclusions

It is shown that subthreshold source-coupled circuits can be used to implement very-low power and power-frequency scalable mixed signal circuits. The power scalability of this type of circuits is especially important for power management purposes. Using a common basis for the design of analog and digital parts provides the possibility to adjust the power-frequency performance of the entire mixed-signal system using a single controlling unit. Using this technique, a folding and interpolating ADC consisting of analog and digital sub-blocks has been implemented and tested, which serves as a realistic test-bed for the ultra-low-power mixed-signal design approach presented in this paper. Such an approach could be very useful in emerging applications such as sensor networks and biomedical systems.

References

[1] C. Piguet, *Low-Power Electronics Design*, CRC Press, 2005.

[2] M. Horowitz, T. Indermaur, and R. Gonzalesz, "Low-power digital design," *IEEE Int. Symp. Low Power Electron. Design*, pp. 8-11, Oct. 2004.

[3] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimandi, "Leakage current mechanisems and leakage reduction techniques in deep-submicrometer CMOS circuits,", *Proceeding of the IEEE*, vol. 91, no. 2, pp. 305-327, Feb. 2003.

[4] K. Roy, A. Agrawal, and C. H. Kim, "Circuit techniques for leakage reduction", in *Low-Power Electronics Design*, Editor C. Piguet, CRC Press, 2005.

[5] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

[6] S. Hanson, and et al., "Exploring variability and performance in a sub-200-mV processor," *IEEE J. of solid-State Circuits*, vol. 43, no. 4, pp. 881-891, Apr. 2008.

[7] E. Alon and M. Horowitz, "Integrated regulation for energy-efficient digital circuits," *IEEE J. Solid-State Circuits*, vol. 43, no. 8, pp. 1795-1807, Aug. 2008.

[8] Y. K. Ramadass and A. P. Chandrakasan, "Minimum energy tracking loop with embedded DC-DC converter enabling ultra-low-voltage operation down to 250 mV in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 1, pp. 256-265, Jan. 2008.

[9] A. Tajalli, E. Vittoz, Y. Leblebici, and E.J. Brauer, "Ultra low power subthreshold current mode logic utilizing a novel PMOS load device concept," in Proc. *European Solid-State Circuits Conf. (ESSCIRC)*, pp. 304-307, Munich, Germany, Sep. 2007.

[10] A. Tajalli, E. J. Brauer, Y. Leblebici, and E. Vittoz, "Sub-threshold source-coupled logic circuit design for ultra low power applications," *IEEE J. of Solid-State Circuits*, vol. 43, no. 7, pp. 1699-1710, Jul. 2008.

[11] A. Tajalli and Y. Leblebici, "Leakage current reduction using sub-threshold source-coupled logic," *IEEE Trans. on Circuits and Systems-II: Express Briefs (Special Issue on Nanocircuits)*, vol. 56, no. 5, pp. 347-351, May 2009.

[12] S.-M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits*, McGraw-Hill, 2003.

[13] A. Tajalli, E. J. Brauer, and Y. Leblebici, "Ultra low power 32-bit pipelined adder using subthreshold source-coupled logic with 5fJ/stage PDP," *Elsevier Microelectronics Journal*, vol. 40, no. 6, pp. 973-978, Jun. 2009.

[14] M. P. Flynn and D. J. Allstot, "CMOS folding A/D converters with current-mode interpolation," *IEEE J. of Solid-State Circuits*, vol. 31, no. 9, pp. 1248-1257, Sep. 1996.

[15] S. Limotyrakis, K.-Y. Nam, and B. A. Wooley, "Analysis and simulation of distortion in folding and interpolating A/D converters," *IEEE Trans. on Circ. and Systems-II: Analog and Digital Process.*, vol. 49, no. 3, pp. 161-169, Mar. 2002.

[16] M. Mizuno, and et al., "A GHz MOS adaptive pipeline technique using MOS current-mode logic," in *IEEE J. of Solid-State Circuits*, pp. 784-791, vol. 31, no. 6, Jun. 1996.

[17] A. Tajalli, Y. Leblebici, and E.J. Brauer, "Implementing ultra high value tunable CMOS resistors," *IEE Electronics Letters*, vol. 44, no. 5, pp. 349-350, Feb. 2008.

[18] H. Khorramabadi and P.R. Gray, "High-frequency CMOS continuous-time filters," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, pp. 939-948, Dec. 1984.

[19] E. Vittoz and J. Fellrath, "CMOS analog integrated circuits based on weak inversion operation," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 3, pp. 224-231, Jun. 1977.

[20] M. H. Cohen and A. G. Andreou, "Current-mode subthreshold MOS implementation of the Herault-Jutten Autoadaptive network, "*IEEE Journal of Solid-State Circuits*, vol. 27, no. 5, pp. 714-727, Jun. 1992.

[21] A. G. Andreou, and et al., "Current-mode subthreshold MOS circuits for analog VLSI neural systems," *IEEE Journal of Solid-State Circuits*, vol. 2, no. 2, pp. 205-213, Mar. 1991.

[22] A. Tajalli, and Y. Leblebici, "Linearity improvement in biquadratic transconductor-C filters" *IEE Electronics Letters*, vol. 43, no. 24, Dec. 2007.

[23] A. Tajalli and Y. Leblebici, "A widely-tunable and power-scalable MOSFET-C filter operating in subthreshold," to be appear in *Custom Integrated Circ. Conf.*, San Jose, USA, Sep. 2009.