

New Approach for SOI Pixel Sensor, Analysis and Implementation

THÈSE N° 4440 (2009)

PRÉSENTÉE LE 2 OCTOBRE 2009

À LA FACULTÉ SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
INSTITUT DE GÉNIE ÉLECTRIQUE ET ÉLECTRONIQUE - GROUPE KAYAL
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

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Suisse
2009

Acknowledgment

HERE I am at the finish line of a long term project, where I have come to interact with people from all around the globe. It is time to express my gratitude for all those with whom I have not only worked with but also have shared a part of my life for the past six years. I would like first of all to thank my thesis advisors Maher KAYAL and Jean-Michel SALLESE for their guidance that helped me to put back on track the project after inevitable derailings, things we encounter very often in any research work. I would like also to thank them for their trust in me as well as their support at many instances of the work.

I would like to thank the office mates with whom I have shared not only an office but also some thoughts (philosophical for many of them), jokes, comments, lunches, stress and difficult moments. I will go chronologically, Marija BLAGOJEVIC, Danica STEFANOVIC, Sergio PESENTI, Ira NAGEL and Laurent FABRE.

My thanks go also to Marija BLAGOJEVIC and Sergio PESENTI for their support during my very first year in the lab, where I have been working on independent projects with them. Their expertise helped me develop a better view in a field that was new to me.

In addition to the research work, we had assistantship work we share among the group. This too allowed interactions with the lab people. Under this category I would like to thank especially Danica STEFANOVIC and Ira NAGEL whose passion for education and perfection will always amaze me.

Also rememberable are the lunch breaks with Didier BOUVET and Patrice BEAUD and later on with Daniel GROGG, Dimitris TSAMADOS and Pierre-Yves PFIRTER especially when we tackled world wide financial and political issues. Nor shall I forget the discussions and the exchange of recipes with the italian group in the lab, especially with Donatello ACQUAVIVA and Giovanni SLAVATORE.

Without the little chit chat here and there and the moments of comics spent with the people around in the lab, the work environment would become unbearable. For these moments I would like to thank in the order of appearance during my typical day at the lab, Andrea AJBL, Cédric MEINEN, Laurent FABRE, Fabrizio LOCONTE, Diana CIRESSAN then at the coffee break at 9:30 sharp Adil KOUKAB, Marc PASTRE, Paulo DAL FABBRO, then comes after the coffee throughout the day Sylvain MARECHAL, Imre KOVACS, Raymond SUTTER, François KRUMME-NACHER, Nicolas PILLIN, Luca DE MICHELIS, Livio LATTANZIO, Anupama ARUN, Matthieu BOPP, Nenad CVETKOVIC and Montserrat FER-

NANDEZ. My special thanks go for the secretaries Marie HALM, Isabelle BUZZI and Karin BELLARDINELLI-BORCARD not only for the perfect administrative work they do, but also for the organization of the social events of the lab. Also to remember the discussions we have numerous times made at the early coffee break.

Special thanks goes to Roland JAQUES and Joseph GUZZARDI for the continuous technical support at any time of the day and sometimes from remote places!

I would like to thank my friend and associate Jari CURTY for his patience and understanding especially during the last phase of the thesis.

Last but not least I would like to thank my parents and brother for their love and the trust they have put in me and the help they provided me to nurture my curiosity all the way through.

To my mom Marie, my father Bahige
and my brother François.

وقل لمن يدعي نبي العلم فلسفة
حفظت شيئاً وغابت عنك أشياء

أبو النّوّاس

Abstract

SILICON on Insulator (SOI) is an interesting alternative to bulk silicon for the fabrication of integrated circuits due to its advantages with respect to the junction leakage, low switching noise coupling, high temperature immunity, low voltage and low power applications. Recently, SOI transistors have also been used in high speed CPU's due to their high switching performances and their reduced power consumption. Another application where high performances and even higher densities are needed are dynamic memories (DRAM) where floating body SOI MOSFETS were used as an 1T memory node. Using the floating body as a charge storage reduces the unit cell size and drastically increases the bit density and the storage capacity.

However, despite technical advances in SOI technology, it has rarely been exploited in optical sensing and imagery. The main reasons are the expected low optical conversion efficiency due to the relatively thin silicon film thicknesses, well below $1\ \mu\text{m}$ and the slow time constants due to slow recombinations at the junctions. In addition, the slim active region reduces the optical bandwidth of such sensors as longer wavelengths are absorbed deeper (and in the case of SOI probably in the buried oxide layer).

Despite these major handicaps, it was shown recently that an SOI MOSFET based phototransistor could detect light intensities as low as $5\text{mW}/\text{m}^2$. However, previous work addressed only low light intensities neglecting the slow transients drawbacks. Moreover, as for most fully and partially depleted SOI MOSFET's based photodetectors, it is the drain current variation due to light absorption that was used as a measure of photon densities (for instance the $5\text{mW}/\text{m}^2$ generates 50 fA of photocurrent). Such variations are hard to measure with the needed resolution as such currents are close to the noise levels of any amplifier.

This research project proposes a new measurement technique that does not rely on direct quantification of the photocurrent and hence overcomes the problems inherent to noise and low current variations. In addition to that, this novel technique solves the problem of slow drain current recovery time inherent to the slow recombinations at the junctions.

This technique relies on the transient charge pumping used to remove continuously photogenerated charges from the electrically insulated body of the MOSFET. Then, since the transistor is always maintained in equilibrium conditions, this approach will get rid of any transient effect occurring in the partially depleted SOI MOSFET.

Also presented in this work is an extension of this technique to any float-

ing body MOSFET. We presented also measurement of bulk P-MOSFET whose n-well was left floating and showed that the behaviour was similar to that of a floating body SOI MOSFET. Still using the transient charge pumping to remove extra charge from the floating n-well.

Finally, An SOI circuit implementation of this technique was presented. This circuit takes advantage of some of the properties of the floating body SOI MOSFET to implement a first order delta sigma modulator at the pixel level without substantially reducing the fill factor. The first order delta sigma modulator in each pixel, can improve the resolution and offer a direct digital output without the need of an ADC.

Keywords: Silicon on insulator (SOI), phototransistor, partially depleted, charge pumping, delta-sigma modulation, digital pixel sensor (DPS), active pixel sensor (APS), floating body, floating N-well, photo-generation, recombination, photon shot noise, charge pumping noise.

Résumé

SILICON on Insulator (SOI), littéralement “silicium sur isolant“, représente une alternative à la technologie silicium classique dite “bulk“ pour la fabrication de circuits intégrés. Les avantages du SOI se situent dans les faibles courants de fuites des jonctions, les bruits de découplage ainsi que l’immunité aux hautes température. La technologie SOI est davantage utilisée dans des applications faible tension et faible consommation et à haute fréquence, comme c’est le cas pour les unités centrale (CPU). Une autre application intéressante concerne les memoires vives appelées DRAM où l’on utilise le transistor à substrat flottant comme capacité de charge à la place d’un condensateur, ce qui permet d’atteindre des densités d’intégration plus élevées.

Malgré les progrès technologiques de la SOI, on trouve très rarement des détecteurs optiques de haute performance. Les chercheurs sont découragés non seulement par la faible efficacité optique, qui est essentiellement due à la faible épaisseur du film de silicium inférieur au $1\mu\text{m}$, mais aussi par des constantes de temps relativement longues qui sont dues aux faibles taux de recombinaisons dans les jonctions source-body et drain-body. De plus, l’épaisseur du film de silicium réduit l’efficacité pour les plus longues longueur d’onde qui sont principalement absorbées dans l’oxide enterré.

Ces limitations techniques n’ont pas empêché l’avancement dans ce domaine. Un détecteur optique basé sur un phototransistor SOI a également pu détecter des faibles intensités lumineuses allant jusqu’à $5\text{mW}/\text{m}^2$. Cependant, la problématique de la constante de temps subsiste encore: le temps de réaction du dispositif reste inacceptable pour la plupart des applications. Toutes les solutions qui ont amélioré l’efficacité optique des phototransistors SOI, partiellement ou totalement déplétés, mesurent un photocourant (une variation du courant du drain) pour évaluer la densité de photons qui a été absorbée (une illumination de $5\text{mW}/\text{m}^2$ génère un courant de 50 fA seulement). Cette faible variation de l’amplitude est difficilement mesurable par un circuit intégré car elle est proche du niveau du bruit d’entrée du circuit d’amplification.

Dans ce contexte, ce projet de recherche propose une nouvelle technique de mesure qui ne repose pas sur la quantification exacte de la variation du courant de drain (le photocourant) mais plutôt sur le maintien d’une valeur fixe de celui-ci.

Cette technique de mesure utilise le “transient charge pumping” pour recombinaison continuellement les charges photogénérées dans le “body” flottant du MOSFET. Comme le transistor est constamment maintenu dans

un état d'équilibre, cette approche s'affranchit des effets transitoires qui ont lieu dans un MOSFET SOI partiellement déplété. Ainsi, cette solution s'affranchit des problèmes dûs aux bruits de circuit d'amplification ainsi que de la constante de temps qui sont des facteurs limitatifs.

Egalement, cette approche peut être étendue à tous les types de MOSFETs dont le substrat est flottant. Des mesures réalisées sur un PMOSFET de type bulk dont le caisson N est laissé flottant révèle un comportement identique à celui du MOSFET SOI avec "body" flottant. En effet, il a été démontré que la technique du "transient charge pumping" est également applicable à un tel dispositif pour recombinaison des charges en excès existant dans le caisson.

Enfin, l'implémentation d'un circuit utilisant la technologie SOI a été présentée. Ce circuit utilise les propriétés du transistor SOI à "body" flottant et implémente un modulateur delta sigma du premier ordre au niveau du pixel, occupant une surface négligeable par rapport à celle du phototransistor. Avec un modulateur delta sigma dans chaque pixel, la résolution du signal à la sortie a été accrue. De plus un modulateur delta sigma présente une sortie qui, par nature, est numérique, ce qui évite d'avoir à réaliser un convertisseur analogique numérique à la sortie du système.

Ainsi, à travers ce travail de thèse, nous avons pu démontrer que la technologie SOI associée à une technique de mesures innovante devenait une alternative intéressante à la technologie CMOS-bulk pour les capteurs optiques.

Mots-clés: Silicon on insulator (SOI), phototransistor, partiellement déplété, charge pumping, modulation delta-sigma, digital pixel sensor (DPS), active pixel sensor (APS), body flottant, N-well flottant, photogénération, recombinaison, photon shot noise, bruit de "charge pumping".

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Introduction

1.1 Silicon on Insulator

SILICON On Insulator CMOS is becoming a major player in existing VLSI systems. Designers are attracted to this technology because of its suitability for low power applications using low supply voltage. Along with the progress in CMOS processing technology, the CMOS device has been scaled down serving two purposes, low voltage supply and higher densities. Allowing to achieve a computing power similar to that achievable 25 years ago with 10,000 times less power consumed. (figure 1.1 adapted from [44]). This trend is continuing according to Semiconductor Industries Association (SIA) leading to smaller and smaller geometries for the transistor and forcing circuit designer to design with lower voltages.

Owing to the oxide layer underneath the structure, SOI devices have lower current leakage, less parasitic capacitances which results in higher speed performance of the SOI CMOS compared to the bulk counterpart. Figure 1.2 (adapted from [2]) shows a comparison between an SOI and a bulk CMOS inverter using a $0.35\ \mu\text{m}$ transistors. As we lower the supply voltage the power dissipated in the inverter drops in both cases as well as the delay performances; however, the SOI CMOS is less affected by the scale down of the voltage, implying that SOI technologies are better suited for low voltage circuits.

Generally, SOI CMOS outperforms the bulk CMOS by about 25% in speed performance at a reduced power consumption. Along with the improved speed performance, circuit designers would like to keep power consumption down too. Figure 1.3 (adapted from [10]) shows that the

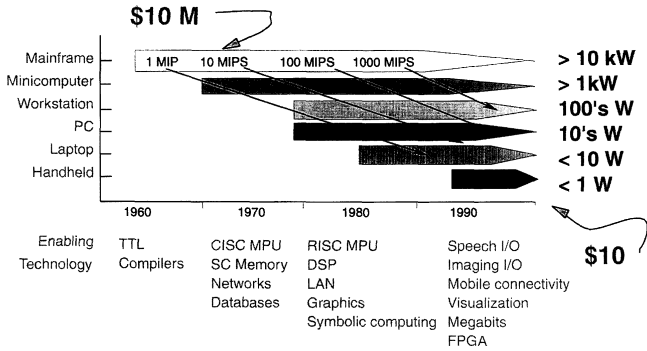


Figure 1.1 Trend on Power Consumptions during the past 40 years

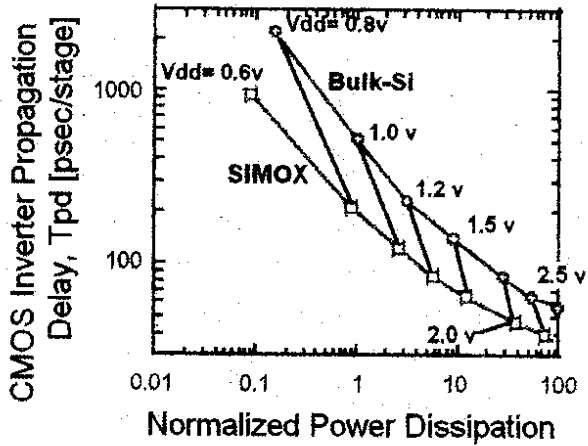


Figure 1.2 Propagation delay versus normalized power consumption

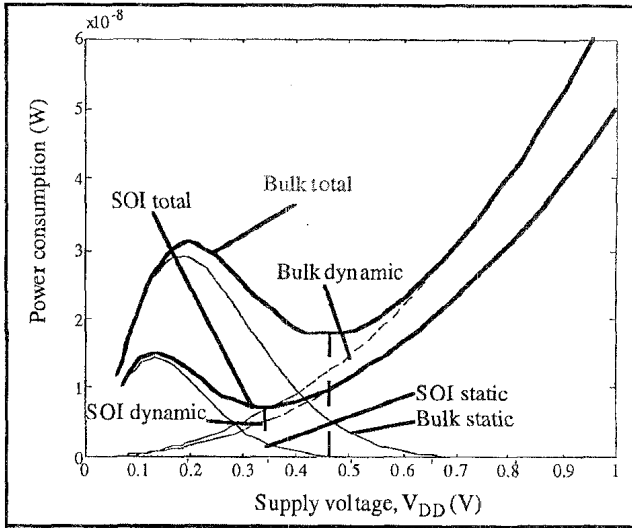


Figure 1.3 Power consumption versus supply voltage

SOI CMOS has a lower static power consumption as well as a lower dynamic power consumption and the latter is because of the smaller parasitic capacitances of the SOI CMOS. All of these factors show that for the future trends SOI technology is a good candidate to replace the bulk especially that the SOI CMOS technology is similar to the bulk CMOS counterpart except for the starting silicon wafer. There are essentially two major of techniques: Separation by Implantation of Oxygen (SIMOX) and the wafer bonding methods.

1.1.1 The Bulk MOS

Basic Structure

The basic idea of the MOS transistor dates back to the early 1930's with the patent of J.E. Lilienfeld. However, the MOS did not become popular until the early sixties when techniques of reliably growing oxide were developed and the basic theories of operation were established. The simplified structure of an n-channel MOS transistor is shown in Figure 1.4. The transistor is formed on a p-type silicon called the body or substrate which is lightly doped typical concentrations range between 10^{16} and 10^{18} cm^{-3} . At the center of the structure a thin layer of silicon dioxide (sometimes simply called oxide) is grown with thicknesses varying from 1 to 10 nm. On top of this oxide a low resistivity electrode called the gate is added. Usually the gate is made by a polycrystalline silicon also

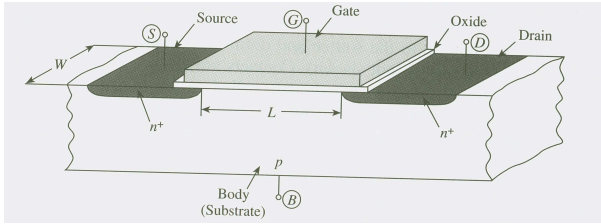


Figure 1.4 Simplified structure of an n-channel MOS transistor

called polysilicon or simply poly. The two n^+ regions on the sides of the gate are what we call drain and source of the transistor. The gate is acting as a mask against the implant that dope the drain and source region, which makes a self aligned doping to the gate. The depth of these regions are between $0.04 \mu\text{m}$ and $0.2 \mu\text{m}$. Due to the heavy doping of these regions some diffusion takes place and we can see some diffuses laterally under the gate. The region between the drain and the source is called the channel and is characterized by W and L which are the width and length respectively. These values varies largely from transistor to another depending on circuit design needs. Often the n-channel and p-channel MOSFET transistors are called nMOS and pMOS transistors respectively. Using CMOS (complementary MOS) technology both nMOS and pMOS can coexist on the same chip, this is possible thanks to a technique called LOCOS (Local oxidation of silicon). With this a gradual increase of the silicon dioxide thickness is possible, resulting in the so-called "bird's beak" shape as shown in figure 1.5. The thick layer of oxide is used to prevent the accidental formation of a parasitic channel underneath it in case a metal line was passing above it. In addition to this heavily doped "channel stops" are made under this thick oxide. As we can see in figure 1.5 all the nMOS transistors will share the same p substrate, the pn junction formed by the source and the drain on one side and the p substrate on the other side is kept in reverse bias mode by connecting the p substrate to the lowest potential in the circuit. The pMOS transistors are formed in a separate n-well as shown in figure 1.5. This n-well is connected to the highest potential in the circuit to keep the pn junction formed by the n-well and the p substrate in reverse bias. An oxide layer called passivation layer is put on top of all the devices to protect them from their environment. In figure 1.6 we see a technique which is becoming prevalent to isolate nMOS from pMOS transistor and is called the *shallow-trenchisolation*(STI). A "trench" filled with oxide separates devices from one another without compromising performance. The advantage of this technique is that the devices can be packed closer

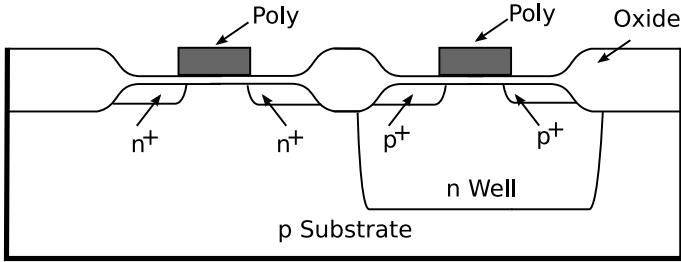


Figure 1.5 Simplified CMOS LOCOS process

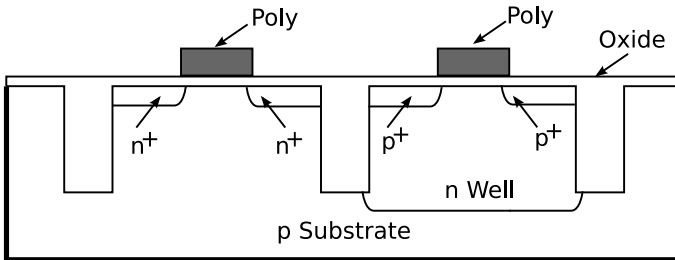


Figure 1.6 Simplified CMOS shallow-trench isolation process

together without causing any latch up problem.

Qualitative description of operation

In this section and for the sake of example we will take the n-channel shown in figure 1.4. If sufficiently high positive voltage is applied at the gate, the holes are repelled from the surface and electrons are attracted to the surface. These electrons can easily enter either or both of the n^+ . This situation is called *inversion* as the p-type, which is naturally abundant with holes, has now more electrons. Now when a potential V_{ds} is applied across the channel, the electrons will be accelerated as they enter from the source and they leave through the drain. This corresponds to a current flowing from the drain toward the source. In the next subsection we will show how this current behaves as a function of the gate and the drain voltages.

MOS transistor characteristics

Let's take a look at the main characteristics of a MOS transistor. This is summarized by figure 1.7 where the drain current is plotted versus V_{ds} with V_{gs} as a parameter and in figure 1.8 where the drain current

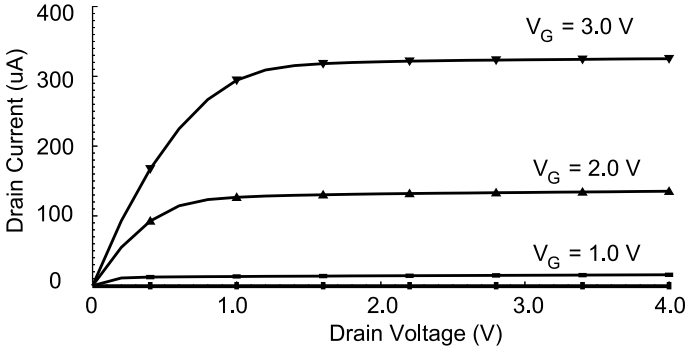


Figure 1.7 I_D - V_{DS} characteristics with V_{GS} as parameter for a specific device

is plotted versus V_{gs} . The inversion of the channel can be seen in figure 1.8 where the different inversions have been marked in terms of V_{gs} . The weak inversion region can be seen in the graph for gate voltages much lower than the threshold voltage V_{th} . This mode of operation is becoming more and more attractive as circuit designers are more confronted with Low power and low voltage applications. In this mode of operation the current is mainly due to diffusion of carriers, while in the strong inversion case the drift of carriers is the major contributor to the current. The moderate inversion is a mixture of both where both drift and diffusion of carriers contribute to the current.

1.1.2 The SOI MOS

As stated in section 1.1.1, it was said that the MOS was originally invented in the early 1930's. The patent filed of Lilienfeld stated that a piece of semiconductor which constituted the active part of the device was a thin film deposited on an insulator. Some consider this MOSFET as Semiconductor on insulator device (SOI) and thus SOI dates back to the first MOSFET ever built. Figure 1.9 depicts a simplified view of an SOI MOSFET.

The fabrication process of SOI CMOS is similar to that of the bulk CMOS, except at the wafer fabrication stage, where the silicon oxide layer has to be incorporated to the wafer. We can differentiate two main methods of wafer fabrication: the Separation by Implantation of Oxygen (SIMOX) and Wafer-Bonding.

The Separation by Implantation of Oxygen (SIMOX) is the process that creates SOI through implantation, most of which use the oxygen implantation. This implantation takes place before the CMOS processing.

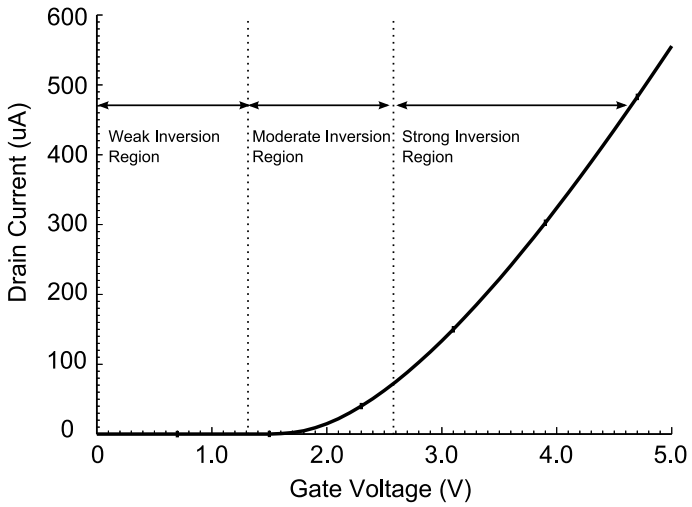


Figure 1.8 I_D - V_{GS} characteristics

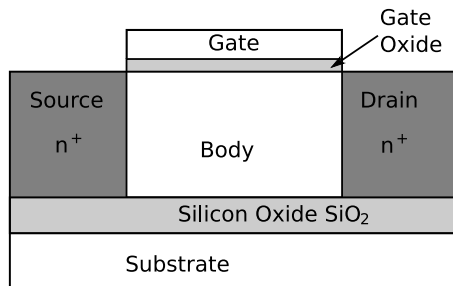


Figure 1.9 Simplified view of an SOI MOSFET

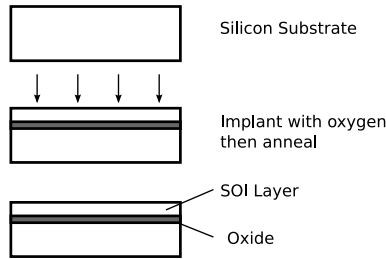


Figure 1.10 Preparation of SOI using SIMOX process

High energy oxygen is sent deep below the silicon wafer surface, the doses used are about 200 times higher than those used for ion implantation doping. The second step is annealing which takes place at 1300C for 6 hours. During this stage the silicon dioxide is formed and recrystallization of the damaged epitaxial layer due to high energy implantation takes place. Typical thicknesses of the oxide layer ranges from 50 to 500 nm with a uniformity of $\pm 2.5\text{nm}$. The thickness of the silicon film above this dioxide layer is 40 to 70 nm for a fully depleted material and 100 to 200 nm for the partially depleted material. Figure 1.10 shows an SOI wafer made using the SIMOX process.

Wafer-bonding methods for preparing SOI wafers have basically the same process sequence. The active wafer is bonded to a handle wafer. In most of the cases both are oxidized, this is followed by an annealing to strengthen the bonds between the two wafers. Finally comes the thinning process which ranges from grinding to chemical etching going through plasma assisted chemical etching, selective etch and implant-enhanced wafer splitting.

Physical Thinning and etch back

This is the most mature process for SOI wafer bonding, however this is the least economical in terms of raw material. As for most wafer bonding processes, 2 wafers one called the active and the second the handle, are bonded after oxidizing both of them. The active side which is used for the circuitry, is ground and thinned down to the desired thickness. However the uniformity is rather poor making it only useful for thick Silicon films. Figure 1.11

Smart Cut

Smart Cut was developed by SOITEC as a variant of the bonding technique. However with this method the active wafer is implanted with hydrogen protons at the depth of $1\mu\text{m}$. When annealed this creates a stress fracture. Afterward the active and handle wafer are bonded and the active wafer is split along the stress fracture. The unused portion of the active wafer can be reused, resulting in reduced costs over the

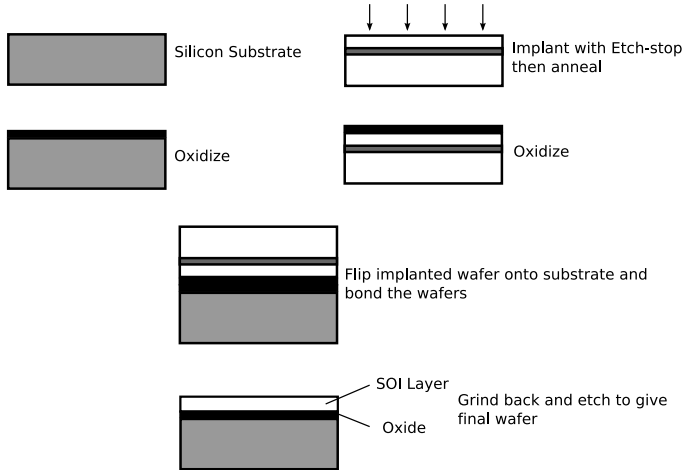


Figure 1.11 Etch-back process for creating SOI material

ground back described before. Figure 1.12

1.1.3 Body Tied SOI MOSFET

The body of an SOI MOS as opposed to the bulk MOS is deposited on a thick layer of SiO_2 called the BOX which effectively isolates the body of the MOS from the substrate and hence two configurations are possible: Either the body is left unconnected to any potential and the transistor is called floating body transistor or the body has a contact which can be connected to a known potential, which is called body tied. In this section we will examine the partially depleted MOS with the body tied to a known potential through a contact. We will also see the different body ties currently used.

Partially Depleted

An SOI MOS is said to be partially depleted when there is a neutral region below the gate, the thickness of the silicon film is larger than the depletion region, as shown in figure 1.13. For thicknesses smaller than the depletion the transistor is said to be fully depleted which we will discuss in the next sections. The behavior of partially depleted MOS is very similar to their bulk counter part, the neutral zone in SOI also called body corresponds to the local well in bulk. The differences are more important when the body is left floating, whose different effect will be discussed in section 1.1.4. These effects are undesirable especially for analog circuits. Adding a body contact to a partially depleted SOI

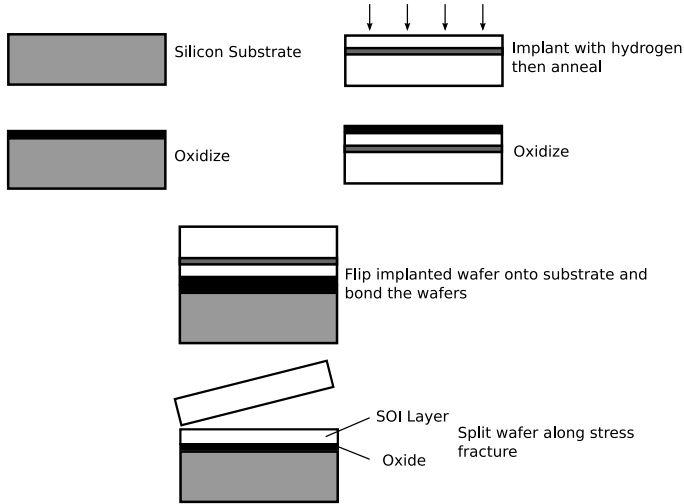


Figure 1.12 SOI wafer produced using the SmartCut® process

MOSFET eliminates these undesirable effects and makes it behave like a bulk MOSFET.

Type A. This type of contact is made up by a P implant in the active area of the source, this creates an ohmic contact with the channel of the transistor. It is necessary to have a metallic line connecting the N diffusion to the P hence the body potential is forcefully the same as that of the source. It is worth noting that such topology is not adapted to the design of pass gates or analog switches because the MOSFET structure

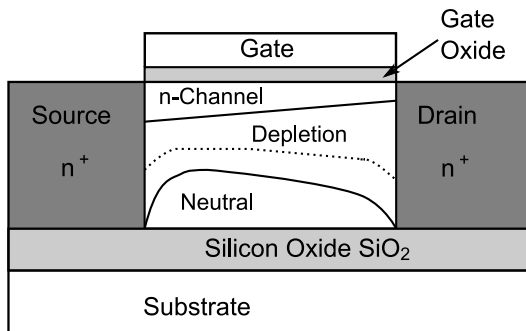


Figure 1.13 Neutral, depletion and the channel regions in a partially depleted SOI MOSFET

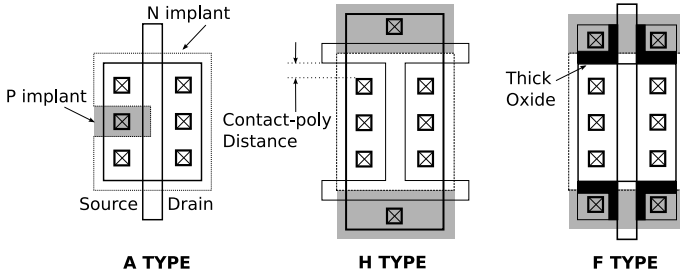


Figure 1.14 Different layouts of body contacts

loses its symmetry (Figure 1.14). If the body is connected to the source then for the case of nMOS, the switch would be on even if the control voltage is low at the gate and the input voltage is high at the source. This is because the body-drain junction is forward biased.

Type H. This contact, unlike type A, does not break the symmetry of the MOS. However, due to layout rules for the minimum distances between polysilicon and contact, minimum widths cannot be achieved. Yet small widths can be achieved with this type of contact. The effective width of the channel is better controlled than in the case of the A contact. Few parasitic elements are due to this contact like the parasitic channel and diodes shown in figure 1.15; furthermore, the efficiency of the contact is reduced due to the distributed resistance created between the substrate contact. This was circumvented by setting a maximum W/L ratio to 6. Throughout this thesis work the H type of contact was used for all analog circuits as it has the best control over the potential in the body of the transistor. In addition to that, the foundry had the most suitable model for this type of contacts (Figure 1.14).

Type F. This type of contact uses the thick oxide normally used for high voltage MOS. This oxide is most of time doped in P^+ to reduce the resistivity of the contact. This type does not suffer from parasitic channel (as the oxide of the gate gets thicker in the contact regions). However, their main disadvantage is their rather high leakage current at the reverse biased drain-body junction (Figure 1.14).

The phototransistors used in the proposed pixels are called floating body SOI MOSFETs, this is because their body is floating, in addition to this, those MOSFETs had no contacts at all. Whereas, the digital gates used were taken from the digital library provided by the foundry where the transistors have a body contact of type A.

The Partially depleted SOI MOSFET behaves like a bulk MOSFET when its body contact is connected to ground, if this contact was left electri-

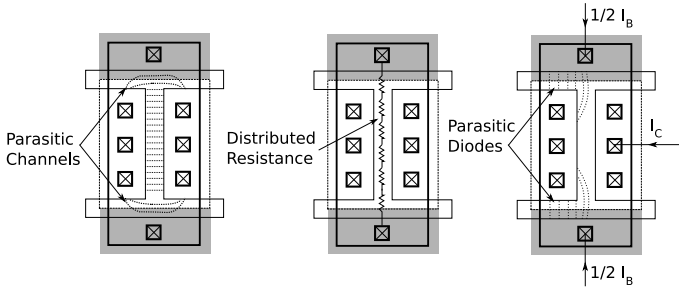


Figure 1.15 Parasitic elements of the H type contact

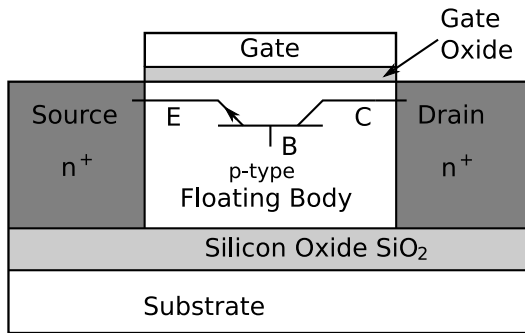


Figure 1.16 The parasitic bipolar device of PD-nMOS

cally floating then the partially depleted SOI MOSFET would still behave like a bulk MOSFET with the exception of two parasitic effects [11]: one called the Kink effect which we will detail in section 1.1.4 and the second is the presence of a parasitic open-base NPN bipolar transistor as shown in figure 1.16. The base is left open however, capacitive switching as well as leakage effects will combine to increase the body voltage and turn on the MOSFET. A typical example is that of a transmission gate where for instance the source and the drain were at a high potential so will the body drift to that potential too. Now suppose that the gate was low then the n-MOSFET should be off; however, when the source goes low the base-emitter diode will be forward biased therefore turning on the NPN transistor and causing a current to flow from the drain to the source. This can take few picoseconds to few milliseconds, until all carriers are swept from base region. This behavior can seriously impact the performance of both digital and analog circuits hence the need to use of body contact to connect the body to a fixed known potential.

1.1.4 Floating Body MOS

We have seen in the previous section the effect of the different types of body contact on the behavior of the partially depleted SOI MOSFET and the importance of tying the body to a known potential for the use of the transistor in analog and digital circuits. In this section we will see the effects of leaving this body floating electrically for both the partially and fully depleted SOI MOSFETs.

Partially Depleted

Kink Effect

The effect of impact ionization in a floating body SOI MOSFET is much more important than that of bulk CMOS device [18]. In the case of a partially depleted because there is a neutral zone in the body and the potential barrier at the source body junction is high, holes generated by the impact ionization are not evacuated from the body. For the case of an nMOS this increases the body potential, thus decreases the threshold voltage. As a consequence the drain current shoots up; however, this phenomenon is not unbound, as the body potential increases the potential barrier at the source body junction decrease and holes created by the impact ionization flow from body to source, allowing the body potential to reach a steady state. The impact ionization takes place when the lateral field in the channel created by the potential V_{ds} is large enough and normally this takes place near the drain junction when the transistor is in the saturation region. Figure 1.17 shows an example of the kink effect on a floating body SOI MOSFET. The kink effect is reinforced by the parasitic NPN bipolar transistor shown in figure 1.16. This kink effect is mainly visible for nMOS; however, pMOS are usually free of kink effect. This behavior is suppressed as the frequency increases [37], implying that it could be beneficial when designing RF circuits for SOI applications [47]. However, other suggested the use of source to body connection to minimize the effect of the parasitic bipolar transistor.

However, for many analog circuits like operational amplifiers and analog-to-digital converters and many others the kink effect should be suppressed. In addition to this, it is a phenomenon that cannot be easily modeled and implemented in circuit simulators [52]. Numerous methods are used to suppress this undesirable behavior. This can be done either by process optimization by minimizing the gain of the parasitic bipolar transistor or by body ties. The different body ties that were discussed in section 1.1.3 could apply. However, we have to keep in mind that those body ties are not perfect and that they exhibit parasitic resis-

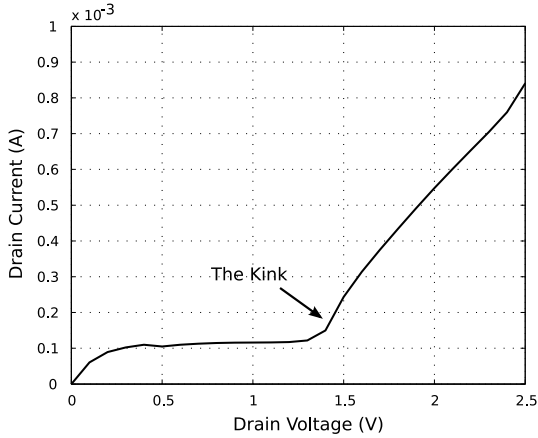


Figure 1.17 The kink effect in 100/1 PD-nMOS

tances, many foundries set a maximum W/L ratio to keep the parasitic resistance to minimum.

Light Effect

When Biased appropriately (in order not to cause any kink), a floating body SOI MOSFET exposed to light will increase its drain current by decreasing the threshold voltage due to accumulation of some photogenerated majority carriers inside the floating body this behavior was shown by [60]. When a floating body SOI MOSFET is actually illuminated by light some of the photons generate electron-hole pairs inside the body. These pairs get separated by the electric field in the depletion layer and at the source and drain junction, the electrons are evacuated through the channel while the holes will accumulate in the body (as it is electrically isolated) until the junctions body-source and body-channel become forward biased [40]). Figure 1.18 (adapted from [20]) shows the drain current variation for different light intensities. This figure shows also the slow decay of the drain current that is due to the slow recombination at the reverse biased source-body junctions. We recognize also another problem, the rather slow generation rate which is also a function of the illuminating light intensity and which is due to the rather low efficiency of the thin Si film of the floating body.

From this simple experiment we can foresee two major limitations to the utilization of the SOI phototransistor: the first is the low efficiency and the second is the slow decay of the photocurrent.

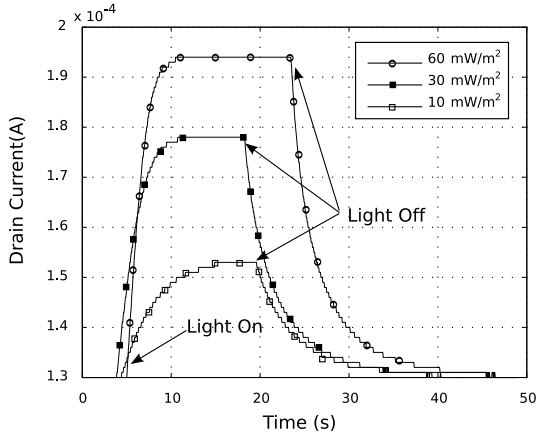


Figure 1.18 Drain current of a floating body SOI MOS when subject to a light pulse

Fully Depleted

In the fully depleted SOI MOSFET, the SOI film is far thinner than the depletion region width. The width of the silicon film is typically between few nanometers to few tens of nanometers. Thus there is no body region of the MOSFET to be charged and as a consequence no floating body effects like the kink effect, light effect and the history effect ([8]).

As a matter of fact, the fully depleted was designed as an effort to suppress the floating body effects. It may be assumed that the fully depleted SOI MOSFET are more suited for analog circuits implementation, as they have no kink effect and no history effect. The fully depleted SOI MOSFET have a steep sub-threshold slope and low parasitic capacitances making them suitable for low voltage, low power applications. An important advantage of the fully depleted SOI circuits is that, for the same bandwidth, they consume only about half the power of their bulk counter part.

However, because they do not have kink effects and are almost insensitive to light, the fully depleted SOI MOSFETs are not attractive for our specific (light sensing) application and therefore, only partially depleted SOI MOSFETs will be used throughout this project. Table 1.1 summarizes a comparison between the fully depleted and the partially depleted SOI MOSFET

	Partially Depleted SOI	Fully Depleted SOI
Floating Body	yes	no*
Active Silicon Thickness	$>0.15 \mu m$	$<0.1 \mu m$
Kink Effect	yes**	no
History Effect	yes	no
Source/Drain resistance	moderate	high
Manufacturing	reasonable	difficult
Power	low	very low

Table 1.1 Comparison between partially depleted SOI and the fully depleted SOI

* Floating body is not present in the saturation region of operation

** Kink effect is suppressed in some operational states

1.2 Photosensors

Optical absorption is the fundamental process which is exploited when converting optical energy into electrical one. Photosensors are the devices that implement this conversion. Thanks to the work done by Max Plank and Albert Einstein, we can describe the light by a quantum-mechanical particle formalism. The smallest unit of light intensity is a quantum-mechanical particle called a *photon*. Photons are used to characterize electromagnetic radiation in the optical range from infrared to ultraviolet spectrum.

Photons are characterized by their energy E , itself dependent on the wavelength .

$$E = h\nu = \frac{hc}{\lambda} = \frac{hc_0}{\lambda_0}. \quad (1.1)$$

Where h is Planck's constant, E is expressed in electron-volt (eV), c_0 is the speed of light in m/s and λ_0 is the wavelength in nm both in vacuum. Whereas c is the speed of light in a medium with index of refraction \bar{n} and λ is the wavelength in the same medium. A useful relation to get the energy of a photon at a certain wavelength is:

$$E = \frac{1240}{h} \quad (1.2)$$

Where 1240 is the result of the product c_0h .

We define the flux density as the number of photons incident per time unit on a unit area. The optical power P_{opt} incident on a detector with

an active area A , can be determined by the photon energy and the flux density:

$$P_{opt} = E\phi A = h\nu\phi A. \quad (1.3)$$

It is important to know the energy of a photon as it determines if it can be transferred to an electron allowing to pass from the valence band to the conduction band of a semiconductor. Indeed, an incident photon with energy larger than that of the bandgap (E_g) generates an electron-hole pair and the photon is absorbed. Photons with energies lower than E_g cannot be absorbed and the semiconductor is transparent for wavelengths longer than $\lambda = \frac{hc_0}{E_g}$. Another important parameter for photodetectors is the optical absorption coefficient α . This coefficient, which depends on the semiconductor, affects the efficiency of the generation of electron-hole pairs and thus the photocurrent. The absorption coefficient determines the penetration depth $1/\alpha$ of the light in the semiconductor material according to Lambert-Beer's law:

$$I(\bar{y}) = I_0 \exp(-\alpha\bar{y}). \quad (1.4)$$

The optical absorption coefficient is strongly dependent on the wavelength of the incident light, for wavelengths shorter than λ_c which corresponds to the bandgap energy ($\lambda = \frac{hc_0}{E_g}$) the absorption coefficient increase steeply according to the so-called *fundamental absorption*. Table 1.2 summarizes the absorption coefficient and intensity factors of silicon as a function of the most important wavelengths for a constant flux density of $\phi = I_0/\alpha = 1.58 \times 10^{18}$ photons/cm². (ehp/cm³ is the electron-hole pairs/cm³)

Although Silicon is not the optimal semiconductor regarding the optical absorption, it is widely used due to economical reasons.

1.2.1 Photodiodes the State of the Art

Typically, a photosensor consists of a photodiode and an amplifier with an input capacitance C_I and with an input resistance R_I . The equivalent circuit of a photodiode is shown in figure 1.19 together with the parasitic elements of the amplifier. These two elements define in general the major parameters of the photosensor like its speed, sensitivity and dynamic range. C_D is the space-charge region capacitance of the photodiode, I_{ph} current source is the photocurrent, R_D models the reverse bias leakage of the photodiode (also known as the dark current). The resistance R_L is a load resistance ;whereas, the series resistance

Wavelength	α	I_0
(nm)	(μm^{-1})	(ehp/cm ³)
980	0.0065	1.03×10^{20}
850	0.06	9.5×10^{20}
780	0.12	1.89×10^{21}
680	0.24	3.79×10^{21}
635	0.38	6.00×10^{21}
565	0.73	1.16×10^{22}
465	3.6	5.72×10^{22}
430	5.7	9.00×10^{22}

Table 1.2 Absorption coefficient α of silicon and intensity factors I_0

R_S cannot be neglected when the photocurrent has to flow through low doped regions, this is not the case for PIN photodiodes where the P and N regions are highly doped. Based on this model, we can determine the -3dB frequency

$$f_{3dB} = \frac{1}{2\pi(R_L//R_I)(C_D + C_I)} \quad (1.5)$$

for amplifiers with MOSFET input R_I is very large and can be neglected.

Then f_{3dB} can be rewritten as

$$f_{3dB} = \frac{1}{2\pi R_L(C_D + C_I)}. \quad (1.6)$$

The capacitance of the photodiode can be approximated for the case of a reverse biased abrupt PN junction as follows:

$$C_D = A \sqrt{\frac{q\varepsilon_r\varepsilon_0 N_{A/D}}{2} \frac{1}{\sqrt{U_D - U - (2k_B T/q)}}} \quad (1.7)$$

where

$$U_D = \frac{K_B T}{q} \frac{N_A N_D}{n_i^2} \quad (1.8)$$

For the case of a PiN photodiode, the capacitance is approximated to that of a plate capacitor (neglecting the boundary capacitance):

$$C_D = A \frac{\varepsilon_r \varepsilon_0}{d_I} \quad (1.9)$$

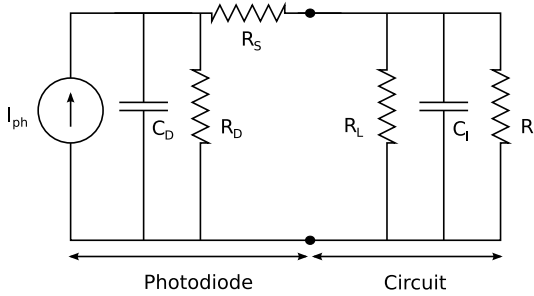


Figure 1.19 Small-signal equivalent of a photodiode with parasitic element of the amplifier

where d_I is the thickness of the intrinsic region and A is the area of the photodiode. $N_{A/D}$ is the doping concentration of the low doped side of a PN junction.

In the next subsection we will be interested only in CMOS integrated photodiodes.

CMOS Integrated Photodiodes

PN Photodiodes. A PN junction in the CMOS process is the simplest way to build a photodiode using the source/drain-substrate or the source/drain-well or even well-substrate junctions. The main disadvantage of such photodiode is the absence of an electric field in certain regions. In such regions, the slow diffusion of photogenerated charges determines the -3dB frequency of such photodiode. The source/drain-well junction are suitable for short wavelength (shorter than 600 nm) as they are shallow junctions and the short wavelengths have limited penetration capabilities as shown in table 1.2. On the other side the junction well-substrate is suitable for longer wavelengths (780-850 nm). Figure 1.20, shows an N^+/P -substrate photodiode. Besides the slow diffusion, the series resistance of the anode contact limits the speed of such photodiodes.

The parasitic capacity of the PN photodiode can be used as a storage to integrate and store photogenerated charges. This stored charge can be read later on to determine the intensity of the incident light. For this purpose in an initial phase, (also called the reset phase) the photodiode capacitor is charged to V_{DD} , then the diode is left floating. Exposure to light will discharge it gradually at a rate dependent on the intensity of incident light. This phase is commonly known as the integration phase. Next is the reading phase, the photodiode is connected to a charge sen-

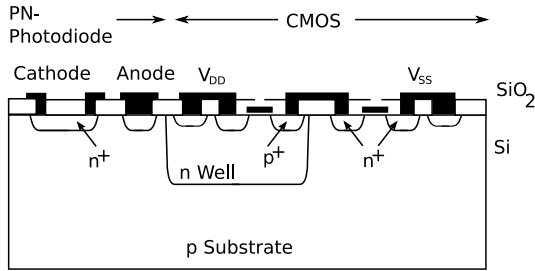


Figure 1.20 Cross section of a PN photodiode integrated in a one-well CMOS chip

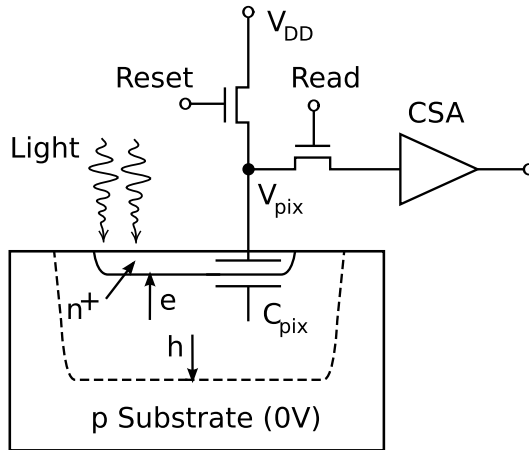


Figure 1.21 A PN photodiode in a pixel working in discharge mode

sitive amplifier which converts the charge into a voltage level that is converted to a digital value by an analog to digital converter (usually not associated to the pixel but rather to a complete column of pixels). Figure 1.21 shows the setup of a photodiode being used as a charge collector, specifically in discharge mode. This mode is advantageous as it allows the use of the electric field that build up during the reset phase.

PiN Photodiodes, A PiN photodiode is a photodiode with a intrinsic region between the N and the P regions (hence the name PiN). The incident photons are absorbed in the intrinsic region which is a lightly doped or undoped Si region.

Compared to the PN photodiode, a PiN photodiode has a thicker depletion region allowing it to collect more photogenerated charges and hence PiN photodiodes have higher quantum efficiency. The thicker de-

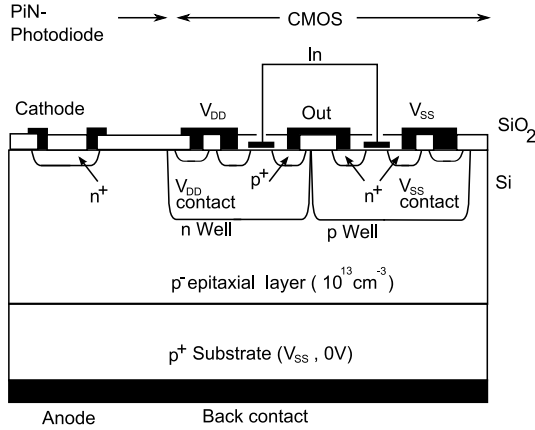


Figure 1.22 A cross section of a PiN photodiode in a CMOS process

pletion region leads also to a lower parasitic capacitance, thus this kind of photodiodes has a large bandwidth typically in the order of few tens of gigahertz. Those photodiodes are sensitive along the visible spectrum and the infrared as it is based on Silicon. Having these specifications this photodiode is ideal for high speed communication systems.

Figure 1.22 shows how a PiN photodiode can be integrated on the same die with MOSFET transistors using a CMOS process.

Charge-Coupled-Device, are basically closely spaced MOS capacitors whose capacity can be stored below one with the appropriate biasing for the gate under which the charges are stored as well as the surrounding gates. To transfer the charges from one gate to the other, one only needs to alter the biasing of the gates accordingly. An example of biasing for the storage and transferring the charges is given in figure 1.24. The light sensing part is always a photodiode which is the source of photogenerated charges that are transferred through the MOS capacitor. Figure 1.23 shows a typical array structure of CCD pixels, the charge is first transferred from the active area to the input gates, then a column wise transfers the charges to the output registers.

It is worth mentioning that 2 phase CCD's are also possible, these need an additional doping structure for generating an internal lateral electric field.

Active Pixel Sensor, the need to miniaturize has driven circuit designers to try to integrate the whole camera on chip. This means, we will need to have both the optical sensor and the signal process-

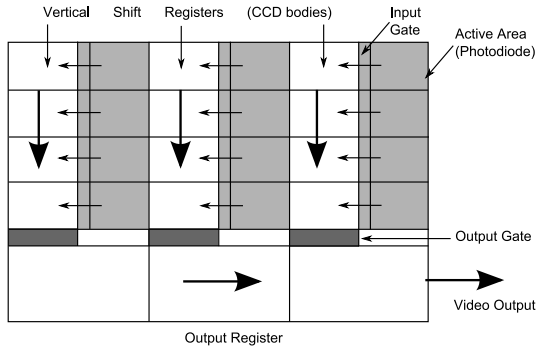


Figure 1.23 A block diagram of a CCD matrix

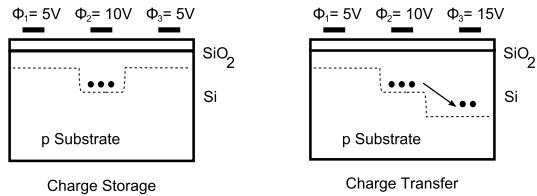


Figure 1.24 An example of biasing for charge storage and charge transfer in a charge-coupled device

ing circuits integrated on the same die (and specifically using the same CMOS process). The Active Pixel Sensor (APS) represents many advantages over the CCD the most important of them are the following:

- (i) random access
- (ii) nondestructive readout
- (iii) ease of integration with on chip electronics

Although CCD can be integrated with the electronics, some compromises will have to be made which will degrade the performance of the circuits. We can distinguish two types of active pixel sensors the *photo-gate* and the *photodiode*.

Figure 1.25 shows a block diagram of an array of APS pixels, showing the ease of access randomly to any of the pixel as opposed to the architecture of an array of CCD cells.

Photo-gate, with this kind of APS a charge transfer is needed from the photogate toward the storage region FD (figure 1.26). The pixel is selected by enabling the transistor S connecting the output of the source follower to column bus. The reset is done by enabling the transistor R. After the reset the charges generated by light at the photogate are transferred to the storage node FD. This creates a change of potential at the gate of the source follower which outputs the signal of the pixel

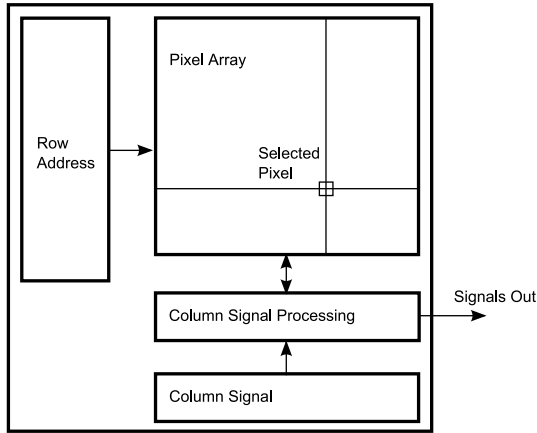


Figure 1.25 The block diagram of an array of APS pixels

Photodiode, with this kind of APS, the photodiode acts as a charge integrator too. This charge is then transferred to the charge storage through the transfer gate TG (figure 1.27), the rest of the circuit is similar to that of the photogate.

A quick comparison of both types of APS shows that the photogate type has a lower quantum efficiency, it also needs a larger area due to the additional transfer switch. Its advantages are lower noise and higher conversion gain due to a smaller floating node capacitance [6].

1.2.2 Phototransistors: the State of the Art

For applications with weak optical signal the use of photodetectors with built in amplifications are used, these photodetectors are called phototransistors. These can be divided in two groups the *bipolar phototransistor* and the *MOSFET phototransistor*.

Bipolar phototransistor, are usually done on a CMOS process without substantial modifications through the use of a floating well as a floating base of a PNP transistor, the P^+ of the source or the drain diffusions as the emitter and the substrate as the collector (figure 1.28). These phototransistors are used as common collector as the collector (the substrate in this case) is connected to ground.

The limitations of such a phototransistor are mainly :

- (i) low sensitivity to short and medium wavelengths due to the depth of the N-well P substrate junction
- (ii) a rather large base-collector capacitance due to the large base area.

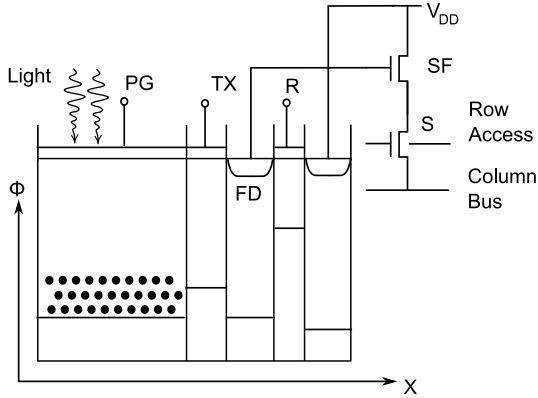


Figure 1.26 Pixel circuit of a photogate APS image

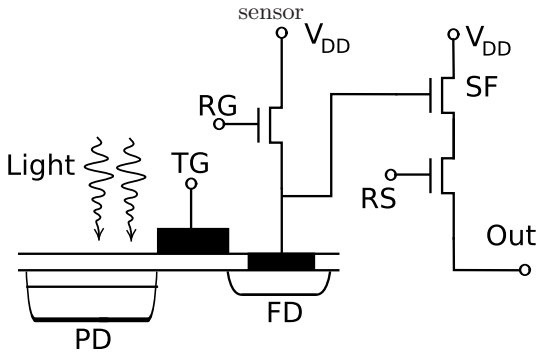


Figure 1.27 Pixel circuit of a photodiode APS image

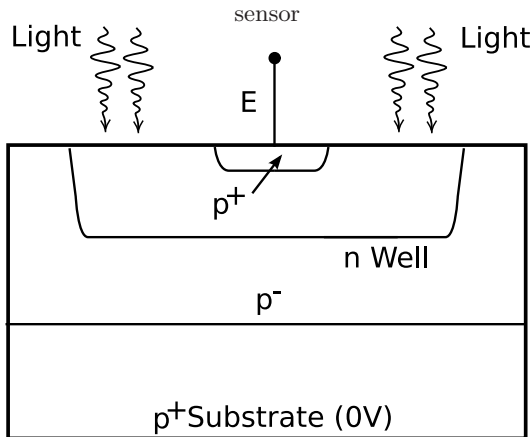


Figure 1.28 A cross section of a vertical bipolar phototransistor in a CMOS process

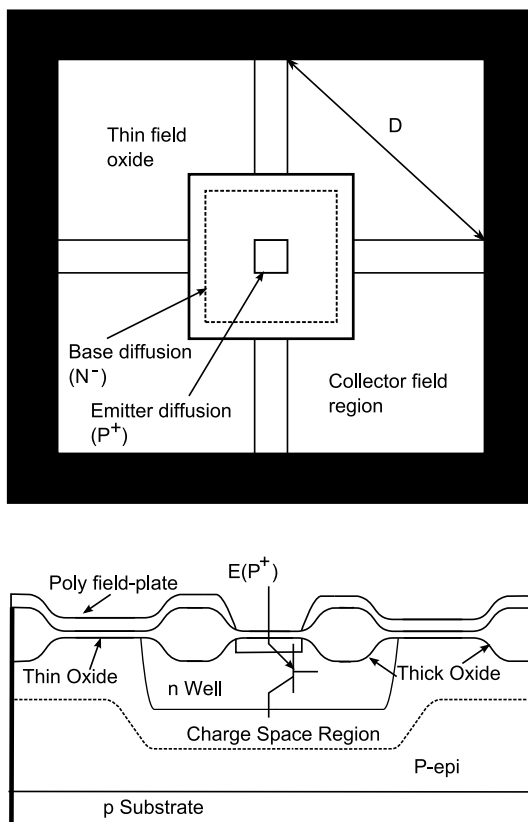


Figure 1.29 Cross section and layout of a PNP phototransistor with reduced Base-Collector capacitance

These disadvantages were overcome by the use of a polysilicon field-plate structure (shown in figure 1.29). This allows the reduction of the N-well base area, whereby the space-charge region below the plate and carrier diffusion in the areas not covered by the polysilicon are used for the collection of photogenerated charges. ([53])

As mentioned before the vertical bipolar (shown in figure 1.28) can only be used in a common-collector topology, however a lateral bipolar (shown in figure 1.30) can be freely used. These are also readily available in a standard CMOS process without modifications. However, they suffer from low current gain and lower collector efficiency than their vertical counterpart. [42] proposed modification to the structure to improve the performances of this lateral bipolar phototransistor.

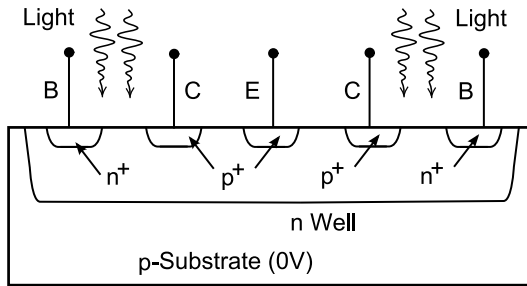


Figure 1.30 A cross section of a lateral bipolar phototransistor in a CMOS process

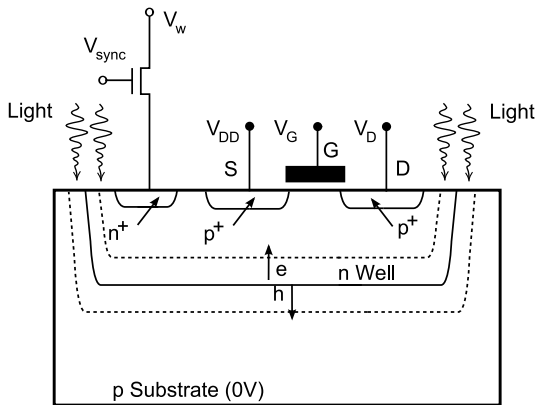


Figure 1.31 A cross section of a MOSFET phototransistor

MOSFET phototransistor, is a usual transistor, with the N-well left floating as is shown in figure 1.31. The incident light will generate electron-hole pairs that get separated by the electric field at N-well P substrate junction. The N-well will become charged negatively as the free electrons will drift to the N-well. This will change the threshold voltage and hence modulate the drain current. Some of the drawbacks of this phototransistor is that the dark current is also amplified with the signal, slow response due to space charge that extends some 1-2 μm away from the N-well which causes slow charge diffusion.

1.2.3 Techniques

Based on the electrical model of the photodiode, we can see that all the techniques of measurements are done by measuring and quantifying

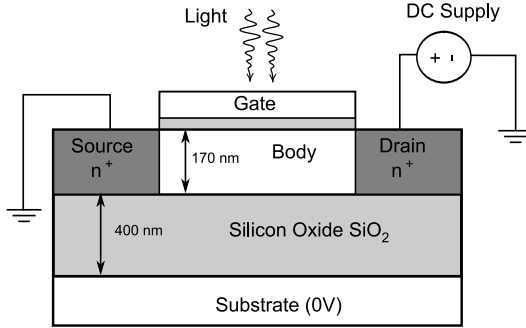


Figure 1.32 A schematic cross section of an illuminated SOI nMOS ([58])

the photocurrent that is a change in the current (or conversely in the voltage of a charged capacitor) and then amplify it. The challenges are to design an amplifier with the lowest input noise that would not mask the photocurrent or create the greater voltage change by minimizing the value of the integrating capacitor (and also taking care of the $\frac{KT}{C_D}$ noise due to switching the integrating capacitor).

1.3 SOI Photosensors

SOI photosensors range from the classical photodiodes to phototransistors just like in the bulk case, in the following section we will review the recent studies and researches in this field.

1.3.1 State of the Art

Lateral bipolar transistor in the floating body SOI. This was shown in [58]. In the setup shown in Figure 1.32 the sample is illuminated from the gate side. This creates electron hole pairs in the body. The electrons are evacuated through the positively biased drain, while the holes remain in the floating body. The positively charged holes in the body are responsible for the base current of the lateral bipolar which amplifies the drain current by a factor β . Note that the base which is nothing but the body is floating, and hence is not biased that's why the author named this topology as *self biased*. The base width of this parasitic bipolar transistor is the channel length of the SOI MOSFET. Figure 1.33 shows the current gain that is due to illumination for two channel lengths.(figure taken from [58]).

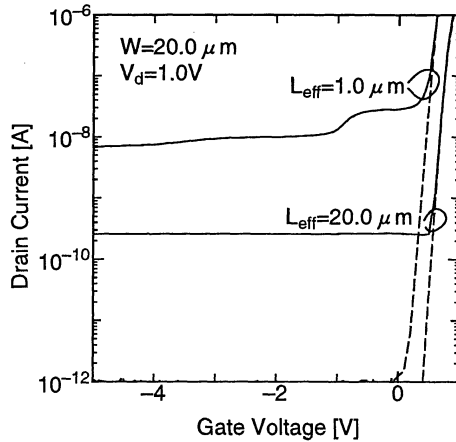


Figure 1.33 Current gain due to illumination for channel lengths $1\mu\text{m}$ and $20\mu\text{m}$. ([58])

Dark Current	Diode Responsivity	Conversion Gain	Output Swing	Dynamic Range
$< 50nAcm^2$	500 mA/w	$1\mu V/e$	$> 0.5V$	74dB

Table 1.3 Summary of performance of the hybrid APS

The authors in [57], have opted for a hybrid solution where the circuits are in SOI MOSFETs while the photodiode was built on the handle substrate. Figure 1.34 shows the structure adopted by the author to build an APS using both bulk and SOI on the same die. The performances of such an APS are summarized in the table 1.3

1.3.2 Our Phototransistor

The phototransistor we have used throughout the whole project, is a partially depleted floating body SOI MOSFET. The need for a partially depleted is motivated by the use of the neutral region to store the photogenerated holes that are responsible for the drain current increase through the change in the threshold voltage. The floating body is needed to store the charges otherwise they will be sunk through the source, for instance, for a body connected to the source. And finally the use of SOI is actually related to the above mentioned characteristics which cannot be found in a bulk process. The photogenerated charges will remain in the body even when light is switched off. As we can see in figure 1.18 the decay of the current is slow (time constant is in the order of sec-

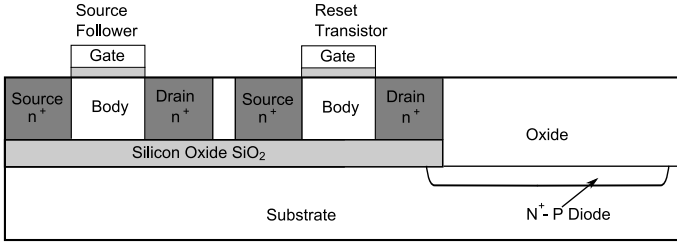


Figure 1.34 A schematic structure of the hybrid bulk/SOI CMOS APS([57])

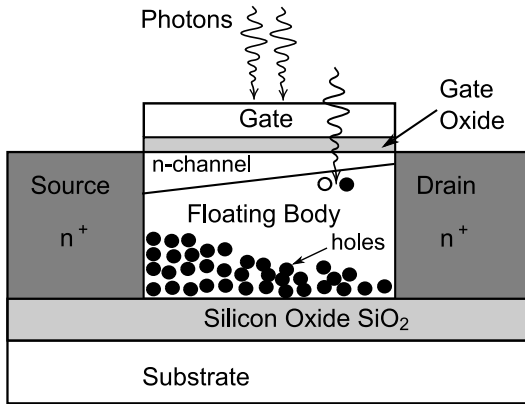


Figure 1.35 The photogeneration and storage in a PD floating gate SOI MOSFET

onds), and is due to the recombination of the holes at the reverse biased source-body and drain-body junctions.

In figure 1.35 we show how the electron-hole pairs are generated and how these photogenerated charges get stored in the floating body.

It is worth mentioning that the partially depleted SOI MOSFETs used in this research are devices optimized for mixed mode applications from the Xi10 of XFAB and not optically optimized for imaging applications. The specifications of such devices are shown in table 1.4. As shown in figure 1.35 the device performances were measured when it was illuminated from the front gate side, it is known that illuminating from the backside greatly improves the optical efficient by at least a factor of 2 [43].

Parameters	Symbol	Units	N-type	P-type
Gate Oxide	t_{oxf}	nm	25	25
Silicon Film	t_{si}	nm	250	250
Buried Oxide	t_{box}	nm	1000	1000
Channel Doping	N	$10^{16} cm^{-3}$	16	4
Mobility	μ	m^2/Vs	510	180
Body Factor	μC_{ox}	$\mu A/V^2$	82	32
Threshold Voltage	V_{T0}	V	1.7	-1.3
Body Factor Slope	n		2.3	1.5
Supply Voltage		V	5	5

Table 1.4 XFAB's partially depleted SOI MOSFET specifications

1.4 Conclusion

In this chapter we had a general review of what is being used currently in image sensing using both the bulk CMOS process as well as the SOI process. We have also seen the limitations that an SOI image sensor has, due mainly to the thin Si film to collect the incident photons. We have exposed the characteristic of the partially depleted floating body SOI MOSFET as well as the problems in having it used as a phototransistor.

The following chapters will discuss the technique used to overcome the two major limitations of the SOI phototransistor: the low optical efficiency and the slow decay due to the charged body.

Device Principles

2.1 Introduction

SILICON On Insulator, as we have seen in chapter 1, is being widely used in the fabrication of integrated circuits due to its advantages with respect to the low junction leakage, low switching noise coupling, high temperature immunity, low voltage and low power applications. More recently, SOI transistors have also been used in high speed CPU's [25] due to their high switching performances and their reduced power consumption. Another application where high performances are needed are dynamic memories (DRAM) where floating SOI MOSFETS were used as an 1T memory node. That drastically increased the density of unit cells and hence the storage capacity [34].

However, despite the technical advances in SOI technology, it has rarely been exploited in optical sensing and imagery [13], the main reasons being the expected low optical conversion efficiency due to the relatively thin silicon film thicknesses, well below $1\ \mu\text{m}$ and the slow time constants due to slow recombinations at the junctions. This slim active region reduces the optical bandwidth of such sensors as longer wavelengths are absorbed deeper (and in the case of SOI probably in the buried oxide layer). Even with such a handicap it was shown recently that an SOI MOSFET based phototransistor could detect light intensities as low as $5\text{mW}/\text{m}^2$ [12]. However, in this work, as it is the case for most of the works done on fully and partially depleted SOI MOSFET's based photodetectors, it is the drain current variation due to light absorption that was used as a measure of photon densities [15, 42, 58, 59, 35, 36, 43] (for instance in [12] the $5\text{mW}/\text{m}^2$ generates 50 fA of photocurrent). Such variations are hard to measure with the needed resolution as such currents are close to the noise levels of any amplifier.

In this chapter, we present a new measurement technique for low light intensity overcoming the problems inherent to noise and low current variations, and the problems of slow drain current recovery due to slow recombinations at the junctions in a floating body partially depleted MOSFET. In addition, an extension of this technique to any floating well bulk MOSFET is presented. Measurement results proved that a bulk PMOS with a floating N-well have the same behaviour as the floating body SOI MOSFET.

Essentially, when a floating body SOI MOSFET is exposed to light, some of the incident photons will be absorbed, generating electron-hole pairs inside the body. A fraction of these electron-hole pairs will get separated by the electric field in the depletion layers, i.e. below the channel, and at the junctions. Considering an N-channel device, electrons will drift to the drain whereas holes will remain in the body and will accumulate until the body-source and/or body-channel junctions start to be forward biased. Being electrically insulated, holes remaining in the body will decrease the threshold voltage that in turn will increase the drain current. This phenomena is very similar to the well known kink effect taking place in floating body SOI MOSFET's when relatively high drain to source voltages is applied [55, 28]. Usually in standard approaches the drain current magnitude is representative of the light intensity. However, here we intend to propose a new method based on the transient charge pumping technique [31]. This method consists in maintaining the drain current to a nominal value by removing the excess of photo-generated holes from the body. This can be achieved by recombining holes with electrons trapped on defects located near the Si/SiO_2 interface using the transient charge pumping. In the following sections, this new approach will be analyzed showing its effectiveness to measure light intensity from practical application and its main advantages in terms of speed, dynamic range and sensitivity.

2.2 The Effect of Light on a Partially Depleted Floating Body SOI MOSFET

We propose to analyze the effect of light on the drain current of a floating body SOI MOSFET. In particular, we will study the impact of the gate voltage on the electron-hole pair collect efficiency, which, to our knowledge, was never reported so far. Without loss of generality, we propose to investigate an N type floating body partially depleted SOI MOSFET. The silicon film thickness is 250 nm and is doped at about

10^{17}cm^{-3} and the gate oxide is 25 nm thick. The threshold voltage was measured and found to be close to 1.6V. In our experiment, the photo-transistor was illuminated from the 'top' with different wavelengths and the optical power density was measured using a calibrated photodiode. This configuration is obviously not optimized since incident light had then to cross all the passive layers and the gate contact before reaching the active body. Neither was the device itself as it was fabricated in a quite old technology (1 μm minimum channel length). Measurements circuits were not integrated on the chip and data acquisition was done through external circuits. In order to reduce the measurement time constants, we intentionally used a relatively large device with width and length of 100 μm and 1 μm respectively (nevertheless, the pixel active area is still equivalent to that of a 10/10 μm device).

2.2.1 The Effect of Light on Electrical Characteristics

As already reported in previous works [60], illuminating a PD SOI MOSFET will increase the drain current by decreasing the threshold voltage due to accumulation of some photogenerated majority carriers inside of the body. Electrons will drift to the channel and will be collected by the drain whereas holes will stay inside the body. Some of these electrons will leak through the body-source and body-channel junctions [60]. For a given wavelength (for instance with a green LED), we intend to evaluate the photogeneration rate (optical efficiency) of the SOI MOSFET by measuring the drain current drift with respect to time for a given light irradiance ($m\text{W}/\text{m}^2$). In order to avoid non linear effects, the photogeneration rate was extracted through the drain current variation at the onset of illumination ensuring that the operating point is almost constant. This was further confirmed in our experiments through the evaluation of the induced body potential variations. The gate voltage was in the range of 1.2 V to 2.0V and the drain potential was set to 0.3V in order to avoid electron-hole pair generation by impact ionization [55, 28]. An external low-noise high-gain current to voltage converter was connected to the source of the transistor, as shown in figure 2.12. This setup was used both to decrease the time response of the overall circuit and, due to the high gain of the amplifier, to set the source potential to zero volt (according to figure 2.1, a simple relation exists between the output voltage and the input current).

Figure 2.2 shows a typical dependence of the drain current (I_D) versus time when the device is illuminated with different light intensities. Under illumination the drain current increases until it reaches a 'steady state' value. This can be explained by a competition between (optically induced) hole generation and hole recombination rates at the junctions

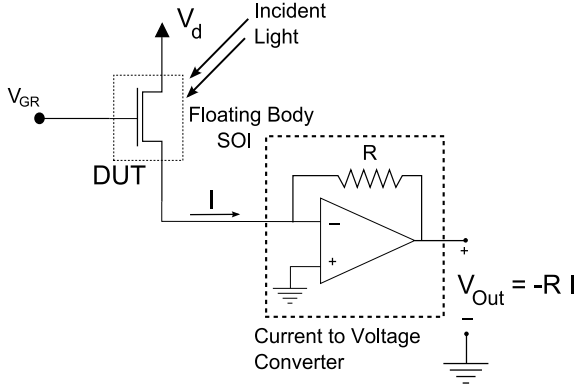


Figure 2.1 Circuit topology used in the light generation experiment

(mainly between body/source [55, 28] and body/channel [40]).

Indeed, accumulation of holes inside the electrically insulated body will increase the body potential. Conversely, increase in the body potential will induce recombination of these holes at the forward biased junctions. Since recombination rate of hole inside the junctions varies exponentially with the body potential, an equilibrium state will be reached after a given time depending on the light intensity. Now, after switching-off the light, the transistor is in non-equilibrium and the excess of holes will then recombine through junction leakage. This will reduce the body potential and hence the drain current, giving rise to the slow transient decay on figure 2.2. In our case, the switch off time constant could exceed 10 seconds, which is obviously not acceptable for practical applications (the reason for slow decay comes from the vanishingly small recombination rate for low values of the body potential. It is worth noticing that the apparent fast decay observed in [58] was due to the fact that the authors did not wait long enough to recover a *true* steady state. In our case this would lead to unacceptable errors especially when low intensities are measured).

2.2.2 Impact of the Gate Voltage on Charge Separation

Since electron hole pairs separation is governed by the built-in electric fields in the depletion regions, we expect that the gate voltage will have an impact on the collect efficiency of holes by affecting the depletion layer below the channel. We measured the effect of the gate voltage on the photo-induced drain current variation by illuminating the transistor with a green light ($\lambda = 550nm$), with an incident power of $5mW/m^2$.

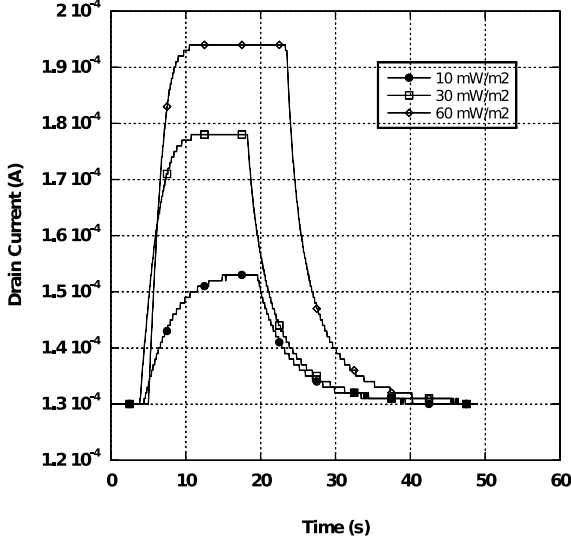


Figure 2.2 Time dependence of the drain current of a floating body partially depleted SOI MOSFET when subjected to a light pulse

Then, we computed the current slopes evaluated at the onset of illumination for different gate voltages from 1.2V to 2.0V, while keeping V_{DS} at 0.3 volt. Figure 2.2 shows both the dark drain current and the drain current variation due to the illumination of the transistor with a light irradiance of $5mW/m^2$. Apparently, for a given illumination intensity, the current variation always increases with the gate voltage. However, since the relation between current and body charge density depends on the inversion level of the channel, we have to convert the current into body charges.

Based on the EKV formalism [41, 39] and provided gate, source and drain potentials are maintained constant with respect to an external reference, we can explicit the relations that govern the relation between the body charge density and induced drain current variations in a floating body partially depleted SOI MOSFET.

Let's first normalize the currents and charges to $2n\mu C_{ox}U_t^2$ and $-2nC_{ox}U_t$ respectively with n varying between 1.1 and 1.7 from strong to weak inversion and normalizing potentials to the thermal voltage [39], we obtain:

$$i = (q_S^2 + q_S) - (q_D^2 + q_D) \quad (2.1)$$

Where i , q_S and q_D represent the normalized current and normalized source and drain charges. In addition, normalized charges and potentials

are also linked by [41]:

$$\ln(q_{S,D}) + 2q_{S,D} = \frac{v_g - v_b - v_{T0}}{n} - (v_{s,d} - v_b) \quad (2.2)$$

where $v_b, v_g, v_{s,d}$ are the body, gate, source and drain normalized potentials, and v_{T0} is the normalized threshold voltage evaluated at $v_b = 0$. Differentiating equations 2.1 and 2.2 we obtain:

$$di = (2q_S + 1)qd_s - (2q_D + 1)dq_D dq_{S,D} = \frac{n-1}{n} \frac{q_{S,D}}{1 + 2q_{S,D}} dv_b \quad (2.3)$$

leading to:

$$di = (q_{S0} - q_{D0}) \frac{n-1}{n} dv_b \quad (2.4)$$

where q_{S0} and q_{D0} are calculated from equation 2.2 with $v_b = 0$. In addition, the normalized body charge can be expressed as a function of the source and drain charges and of the body potential (gate, source and drain voltages are constant).

From [41], the local depletion charge is given by:

$$dq_B(x) = -\frac{n-1}{n} (dq_i(x) + \frac{1}{4n^2} dv_b) \quad (2.5)$$

where $dq_i(x)$ is the perturbed inversion charge density. The total depletion charge variation is then obtained by integrating equation 2.5 from source to drain and using the spatial dependence of $dq_i(x)$ given by [41]. We will not explicit these relations. However, assuming a low drain to source voltage we can assume a uniform charge density along the channel and with equation B.6 in [41], we can write the body charge variation dq_B as a function of the inversion charge evaluated at the source and of the body potential variation dv_b :

$$dq_B \approx -\frac{n-1}{n} (dq_{S0} + \frac{1}{4n^2} dv_b) \quad (2.6)$$

Finally, replacing dv_b in equation 2.6 with the expression of the current variation in equation 2.4, we get:

$$\Delta q_B \approx \frac{-1}{q_{S0} - q_{D0}} \frac{n-1}{n} \left[\frac{q_{S0}}{1 + 2q_{S0}} + \frac{1}{4n^2} \right] \Delta i \quad (2.7)$$

The threshold variation dV_T can also be derived based on the variations of the body charge dq_b .

From [41] we have

$$q_B = \frac{\gamma\sqrt{\psi_s}}{2nU_T} \quad (2.8)$$

Differentiating equation 2.8 we obtain:

$$dq_B = \frac{\gamma}{4nU_T} \frac{1}{\sqrt{\psi_s}} d\psi_s \quad (2.9)$$

We also have that

$$V_T = V_{FB} + \psi_s + \gamma\sqrt{\psi_s} \quad (2.10)$$

After differentiating equation 2.10 and replacing $\frac{d\psi_s}{\sqrt{\psi_s}}$ by the expression found from equation 2.9 we get

$$dv_T = 2n\sqrt{1 - \frac{4}{\gamma^2}(V_{FB} - V_{T0})} dq_B \quad (2.11)$$

where dv_T is the normalized threshold voltage variation.

Figure 2.4 depicts the curves of the variations of both the body charge and the threshold voltage based on the measured currents (shown in figure 2.3) and the following equations respectively:

$$\Delta q_B \approx \frac{-1}{q_{S0} - q_{D0}} \frac{n-1}{n} \left[\frac{q_{S0}}{1+2q_{S0}} + \frac{1}{4n^2} \right] \Delta i \quad (2.12)$$

$$\Delta v_T = 2n\sqrt{1 - \frac{4}{\gamma^2}(V_{FB} - V_{T0})} \Delta q_B \quad (2.13)$$

These curves reveal that, whereas the gate voltage (V_G) is increased, the body charge density and the threshold voltage start to decrease for V_G below 1.4 volts, and then increase when V_G exceeds 1.6 volts. Such observation, which was never reported so far to our knowledge, is most likely a combination of two opposite effects. A possible explanation would be that increasing the gate potential repulses additional photo-generated holes from the gate, implying that they will recombine more efficiently at the junction, hence reducing their concentration with respect to lower V_G . However, further increase in the gate voltage also generates a higher electric field and widens the depletion width under the channel. This in turn will strengthen the electron-hole pair separation efficiency increasing as a result the hole density in the body. Then

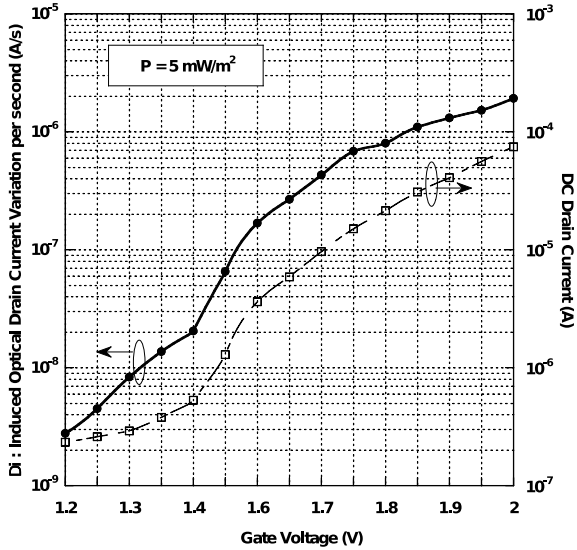


Figure 2.3 Measured DC drain current and measured current regeneration rates versus the 'reading' gate voltage (V_{GR}) for a light intensity of 5 mW/m^2 .

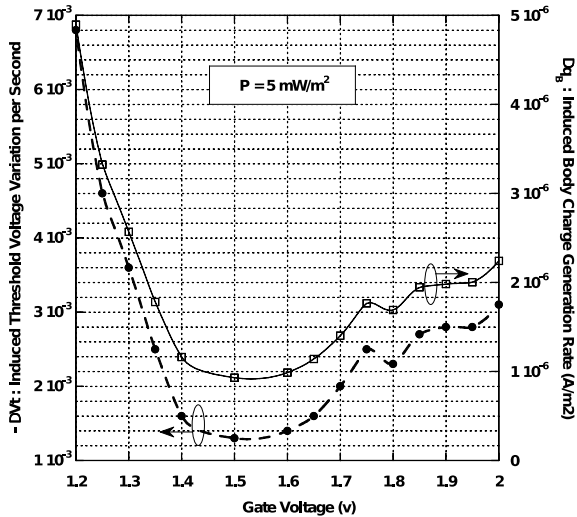


Figure 2.4 Charge regeneration rate and threshold voltage variation versus the 'reading' gate voltage (V_{GR}) for a light intensity of 5 mW/m^2

the question would be, should the PD SOI photo-MOSFET be used in weak or in strong inversion for an optimal sensitivity? In fact, the choice of the best operating point will depend on the technique used to measure light intensity. If the current is the key parameter, then we would probably get the higher sensitivity by setting the MOSFET in weak inversion since the current will vary exponentially with the body potential V_B . However, if we wish to evaluate the charge density, the situation might be different and needs to take into account the hole removal rate.

2.3 Charge Pumping

Traditionally charge pumping is a technique used to get not only the density of traps at the Si/SiO_2 interface, but also their energy distribution and even also the mean value of the capture cross section of electrons and holes [4, 17, 14, 9, 46]. In this section we will review the different parameters that affect the charge pumping in both bulk and SOI MOSFET. In section 2.4 we will focus on the more general aspects of charge pumping and the some specific elements for the charge pumping applied to a bulk MOSFET. Section 2.5 will detail a transient charge pumping technique adapted for SOI floating body MOSFETs.

2.4 Standard Charge Pumping in Bulk MOS

Let's consider for now on that the transistor is a NMOS, the conversion to the case of a PMOS is straight forward. The basic setup to measure the interface trap density for a bulk MOSFET transistor is shown in figure 2.5. Essentially, we need to keep the V_{ds} potential low enough to avoid regeneration of charges by impact ionization. (In addition to that we need to make sure the source-bulk junction is reverse biased). Then, when the gate is pulsed from inversion to accumulation, minority carriers trapped at the interface traps will recombine with majority carriers attracted toward the gate during the accumulation phase. This will generate a bulk current that will be proportional to the interface trap density, the frequency of charge pumping and the transistor gate area. Basically, the charge pumping consists in applying a low voltage at V_{ds} then sweep the gate from low accumulation to high saturation causing a recombination of holes with electrons trapped at the interface traps, creating a substrate current. The form of this pulse is shown in figure 2.6, if we keep the amplitude, the frequency and the rise and fall times

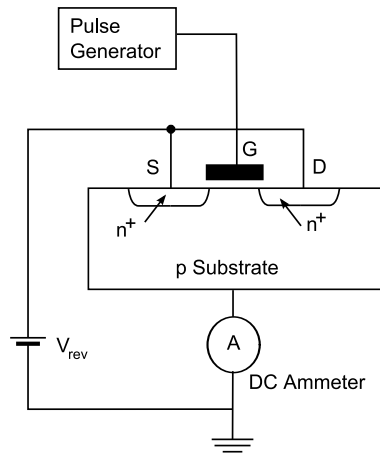


Figure 2.5 Basic experimental setup for charge pumping measurements

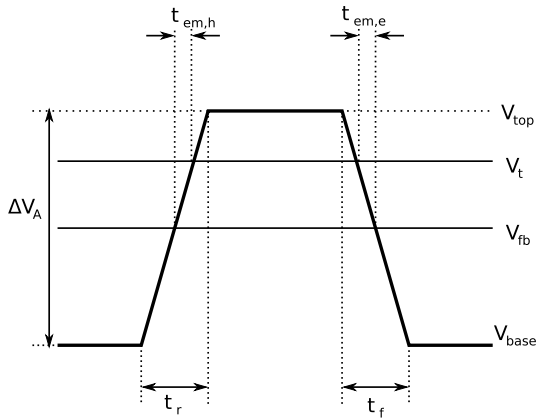


Figure 2.6 Parameters of the pulse applied at the gate

of the pulse unchanged but we only change the base low and high levels of the pulse we will obtain 5 different regions of operations which affects the substrate current. The different modes are shown in figure 2.7.

Region 1 ($I_{cp} = I_{cp,max}$). In this region the low base (V_{base}) is lower than V_{fb} , the flatband voltage (V), and the high level (V_{top}) is higher than V_t , the threshold voltage. The substrate current is at its maximum, this means that the charges are transferred from the drain and the source through the fast interface traps to the substrate. The author in [24] showed that the substrate current due to the charge pumping is given by:

$$I_{cp} = 2\overline{D_{it}}qfA_GkTln(v_{th}n_i\sqrt{\sigma_n\sigma_p}\sqrt{t_{em,e}t_{em,h}}) \quad (2.14)$$

The times $t_{em,e}$ $t_{em,h}$ are emission time constants of electrons and holes respectively that enter in emission and capture process of carriers during the rise and fall of the pulse at the gate as shown in figure 2.6. D_{it} is the interface trap density ($cm^{-2}ev^{-1}$), f is the frequency of the charge pumping, while the other symbols used in the above equation hold their usual meaning.

Region 2 and 3 ($I_{cp} = 0$). In region 2 as shown in figure 2.7 V_{top} and V_{base} are lower than the flat-band one. For this case there is never inversion and traps are always filled with holes, therefore there is no recombination with electrons. In region 3 however, traps are always filled with electrons and no holes are attracted toward the traps at the Si/SiO_2 interface. In both cases the substrate current represents only the leakage current from the drain and the source.

Region 4 and 5 ($0 < I_{cp} < I_{cp,max}$). These are the transitions regions. In region 4 the substrate current increases gradually to reach $I_{cp,max}$ at $v_t - \Delta V_A$ where ΔV_A is the amplitude of the charge pumping pulse. The electron concentration increases when V_{top} is higher than V_t creating an inversion layer which fills all the traps. From this it is understood that the transition region 4 is shaped by the recombination process in weak inversion. Similarly, the falling edge in region 5 is located at V_{fb} since the recombination current disappears when the channel can no longer be flooded with holes.

2.5 Transient Charge Pumping in Floating Body SOI MOSFET

The floating body SOI MOSFET has no electrical contact to its body and hence the measurement of traps density cannot be made through

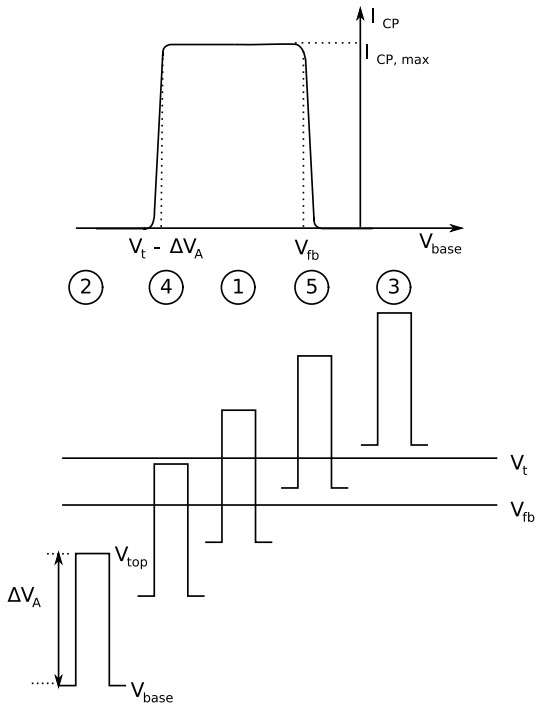


Figure 2.7 The five operating regions by changing the pulse low and high levels

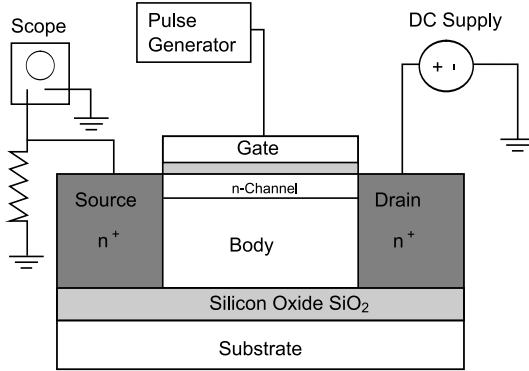


Figure 2.8 Setup for charge pumping a partially depleted floating body SOI MOSFET

the measurement of the substrate current. This should be done on the drain current instead. A typical setup for such measurement is shown in figure 2.8. Using this method, majority carriers are removed from the floating body through recombination of holes at the interface traps. This reduction causes a decrease in the drain current that is relatively large due to the transistor amplifying effect. Hence, the change in the drain current corresponds to the density of traps at the Si/SiO_2 interface and to the number of available holes in the substrate.

Actually, the decrease in the number of majority carrier (holes) in the floating body decreases its potential, increasing the threshold voltage which in turn decreases the drain current. According to the author in [33], cumulative charge pumping pulse could lead to a considerable shift in the threshold voltage as the floating body is electrically insulated. Figure 2.10 shows the drain current change after a series of charge pumping pulses and the cumulative effect on the threshold voltage which can be seen through the continuous decrease of the drain current. A shift of about 200mV in the threshold voltage after a series of charge pumping pulses is reported (Figure 2.9).

However, this phenomena is limited by the number of holes in the body when these are less than the number of traps at the interface. It was also shown in [32] that the number of traps at the interface is related to the change in the drain current and it can be written as :

$$\delta I_s = \frac{N_{it} g_m q}{C_{ox}} \quad (2.15)$$

Where C_{ox} is the capacitance of the gate dielectric, g_m is the transconductance, q is the elementary charge and δI_s is the change in the drain

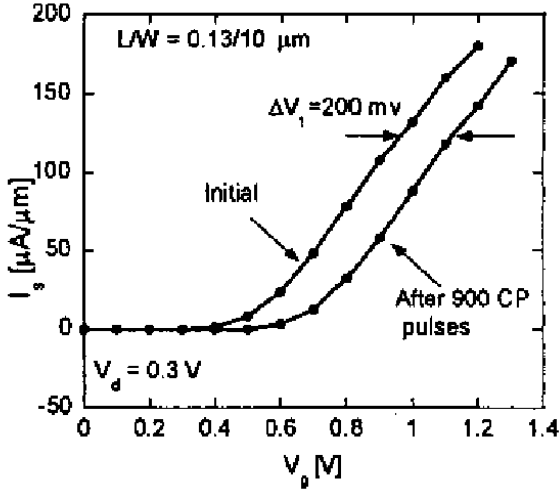


Figure 2.9 Drain current measured before and after charge pumping showing a shift in the threshold voltage (adapted from [33])

current due to charge pumping. As mentioned previously, in the case of bulk MOSFET both the base and high voltage parameters (V_{base} and V_{top}) are critical for the charge pumping efficiency (i.e. the value of I_{cp} in figure 2.7). The author in [33] explored experimentally the effect of the base level of charge pumping pulses (keeping the amplitude constant) on the drain current change in a floating body SOI MOSFET. For the SOI MOSFET used (a floating body SOI MOSFET with $L = 0.13 \mu\text{m}$ and $W = 10 \mu\text{m}$), a maximum is reported when the base level is -1V with a pulse amplitude 1.5V ($V_a = 1.5\text{V}$). Figure 2.11 show the results of such measurement [33].

In summary compared to the bulk charge pumping, the charge pumping in a partially depleted floating body SOI MOSFET has a cumulative effect making the number of pulses (or in other words the frequency) applied an added parameter to the technique. The other parameters are not only the base and high levels of the pulse but also the rising and falling speeds of the pulse.

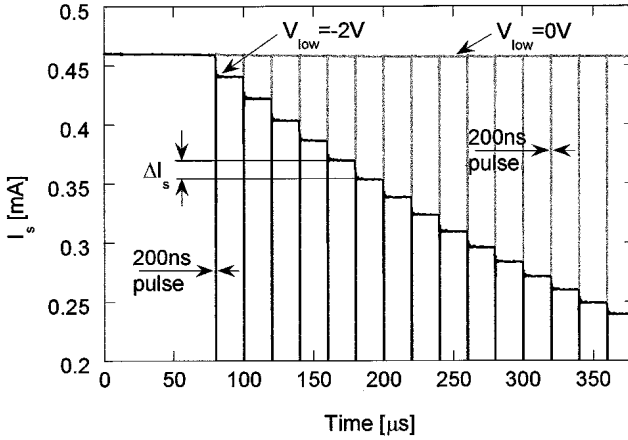


Figure 2.10 Decrease in the drain current measured for an NMOS with $L/W = 0.25/25 \mu\text{m}$ for $V_{low} = -2\text{V}$ and 0V (adapted from [33])

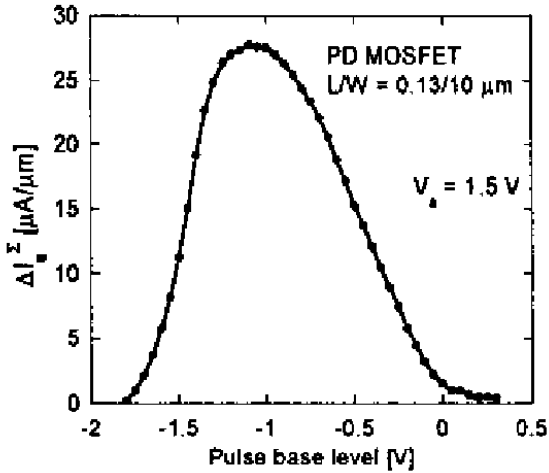


Figure 2.11 δI_s after 200 charge pumping pulses as a function of pulse base level for an NMOS with $L/W = 0.13/10 \mu\text{m}$ and $V_a = 1.5\text{V}$ (adapted from [33])

2.6 The Transient Charge Pumping as a New Light Sensing Technique

In this section, we propose to recall basics of transient charge pumping using it to measure electron-hole pair photo-generation rates.

2.6.1 Transient Charge Pumping and Optical Intensity Measurement

Transient charge pumping (TCP) in PD SOI MOSFETs with floating body was proposed by Okhonin et. al. [31]. In fact, this technique consists of pulsing the gate of the SOI MOSFET between two potentials, namely 'high' and 'low' gate voltages (V_{GH} and V_{GL}), in order to create alternatively inversion and accumulation in the channel. During inversion, some electrons in the channel will fill traps located at the Si/SiO_2 interface. Reverting to accumulation, holes present in the body of the MOSFET will now move at that interface where some of them will recombine with trapped electrons. This will reduce the number of holes in the floating body and thus will increase the threshold voltage. Consequently, the drain current will decrease [31]. Details of charge pumping principles on bulk MOSFET are discussed in [24] and in section 2.3. According to [24], the charges removed after a pulse of the charge pumping per unit area are given by

$$Q_{CP} = \overline{D}_{it} 2qkT \ln(v_{th} n_i \sqrt{\sigma_n \sigma_p} \sqrt{t_{em,e} t_{em,h}}) \quad (2.16)$$

where D_{it} is the interface trap density and $t_{em,e}, t_{em,h}$, are the emission time of electrons and holes respectively, as for the other symbols they hold their usual meanings. Note that even though this relation was derived for bulk MOSFET, it can still be used for PD SOI MOSFET if the body potential is maintained at 0 volt. As will be discussed later, the specific technique that we will use ensures that this condition will always be satisfied (the body potential variation was verified to be lower than 1 mV during the experiments). During the charge pumping period and for a given set of electrical parameters, the number of holes that will recombine with electrons is then a fixed quantity. Provided the transistor state does not drift with time, holes removal rate should be proportional to the charge pumping (CP) frequency. On the other hand, the main effect of light is to generate excess of holes inside the floating body. Since both processes have opposite effects, we propose to evaluate light intensity through the number of CP pulses needed to remove the photo-generated holes. This could be achieved as follows: after each pulse of CP, the gate voltage is set to an intermediate 'reading' value noted V_{GR} and the current is compared to its (steady state) value measured at dark. As long

as the current is higher than the 'dark' value - meaning that there is still an excess of holes in the body - the gate voltage is pulsed between V_{GH} and V_{GL} . Such sequence should be repeated continuously until the drain current drops below the steady state value. Consequently, the apparent frequency of the CP keeps increasing until the value of the drain current is less than or equal to that of the dark. Therefore, the CP frequency needed to maintain the device in the given steady state is representative of the light power that illuminates the device. It is important to notice that in addition to set the 'reading' state, V_{GR} also modifies the 'dynamic' steady state of the transistor since the system aims at keeping a body potential to zero. Then, as V_{GR} directly impacts the depletion region of the MOSFET, we expect that it will also affect the CP efficiency. In order to characterize in details this new method for light sensing, we now propose to investigate the influence of major electrical parameters (V_{GH}, V_{GL}) on the CP efficiency.

2.6.2 Calibration of the CP

Choice of V_{GH} and V_{GL} Potentials

Efficiency of the charge pumping is the measure of how effectively holes recombine with electrons in the channel after a pulse cycle. Recombination of holes depends on both the shape and the values of V_{GH} and V_{GL} , as in classical bulk MOSFETs [24]. These values are important since they are related to the sensitivity of our photo-detector (note that there is an upper limit since holes removed from the body can never exceed active interface traps density). In our experiment (whose setup is shown in figure 2.12), we pulsed the gate with rectangular signals (period of $10\mu s$, rising and falling times of $1\mu s$) with high and low gate voltages varying between $V_{GH} = 4.4V$ and $V_{GL} = 1V$, which corresponds respectively to inversion and depletion modes (note that $V_T = 1.6V$) (a typical CP pulse is shown in figure 2.13).

This rather 'high' value for V_{GL} is unusual since it doesn't match with accumulation as it is usually accustomed for in charge pumping. However, this was chosen to achieve low recombination rates (as will be discussed later, it is worth noticing that even though accumulation is not attained, the CP is still active). In our measurements the choice of V_{GH} and V_{GL} values were based on the needed efficiency of the charge pumping to maintain the drain current constant during illumination. Having fixed the values of V_{GH} and V_{GL} , we are left with the frequency of charge pumping as the only tunable parameter. In addition, in order to avoid any charge generation due to impact ionization, a relatively low voltage was applied on the drain, namely 0.3 volt. However, as pointed

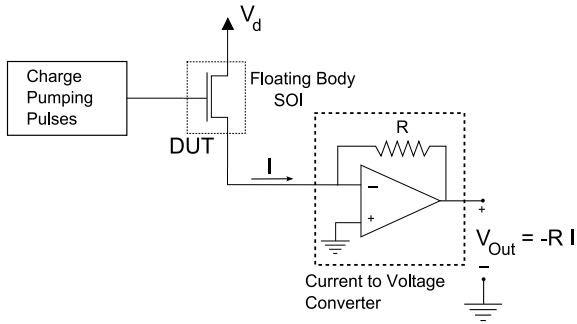


Figure 2.12 Circuit topology used in the charge pumping experiment

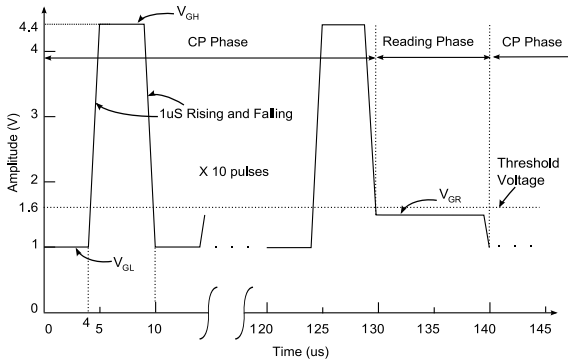


Figure 2.13 An example of the CP pulses applied at the gate of the transistor

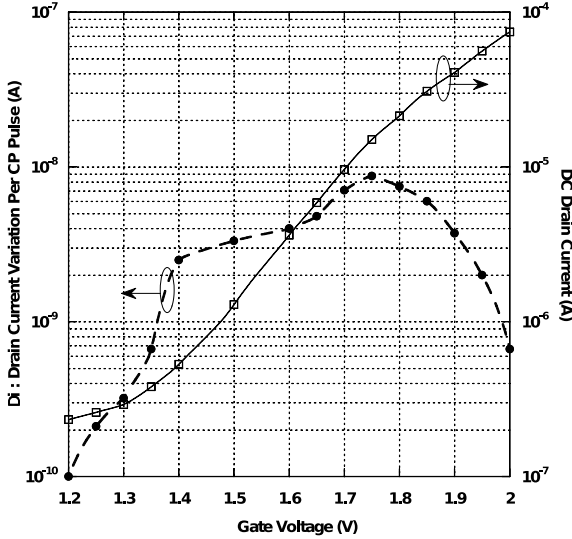


Figure 2.14 DC drain current and its variations as a function of the 'reading' gate voltage (V_{GR}) after the application of a single charge pumping pulse

out previously, we can also wonder if the reading voltage V_{GR} can also affect the charge pumping efficiency, given that this could affect the effectiveness of photogenerated holes (figure 2.4).

Influence of the Reading Voltage V_{GR}

The number of charges removed during each charge pumping pulse is calculated from the drain current variation together with the procedure explained in section 2.2.2. The change in the drain current per pulse, plotted together with the dark drain current on figure 2.14, was obtained after applying a series of 1500 pulses to the device, and then reapplying the V_{GR} to read the drain current.

This number of pulses was applied before the reading phase to insure a large enough drain current changes measurable with the external circuit (figure 2.12). These constraints would not normally be followed were the readout circuits integrated together with the phototransistor on the same die. For instance, after applying 1500 charge pumping with $V_{GH} = 4.4V$ and $V_{GL} = 1V$ ($V_{GR} = 1.8V$), the relative variation of the current was lower than 5.9%, supporting that the shift of the operating point is negligible. (Note that Okhonin [31] measured large current variation in their paper. However, the situation was quite different since

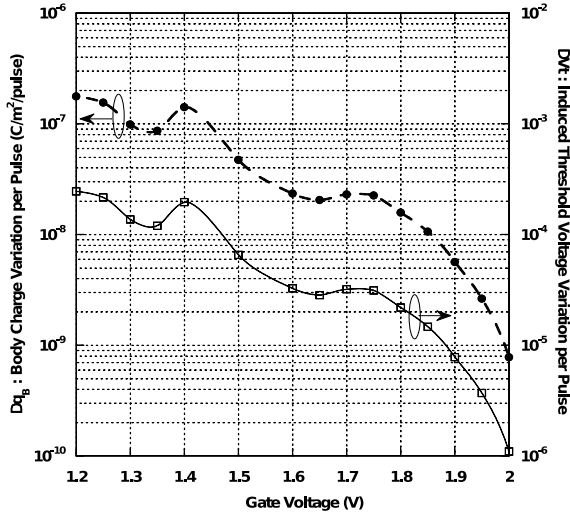


Figure 2.15 Charge recombination and threshold voltage variation as a function of the 'reading' gate voltage (V_{GR}) after the application of a single charge pumping pulse

CP was applied on a sample that was in 'overshooting' state, meaning that there was an excess of holes in the body subsequent to some impact ionization). Figure 2.15 reveals that there is a quasi-monotonic decrease of the CP efficiency when V_{GR} increases, except when the value is close to 1.4 volts, in that case a slight peak is observed. Since V_{GR} also represents the steady state of the MOSFET, this overall decrease is explained by the lower number of available holes since the depletion region is extending deeper in the floating substrate as V_{GR} increases. Eventually, the device starts to be almost fully depleted above 2 volts, hence lowering considerably the charge pumping effect as shown on figure 2.14 and figure 2.15. As will be discussed later, this effect, which is a manifestation of the partially to fully depletion mode can be interesting for our application.

2.6.3 Optical Intensity Measurement

Before applying any CP pulses to the SOI MOSFET, the gate potential was fixed at V_{GR} in order to ensure that the device is in a steady state (this is important to avoid any history effect [55, 28] in the measurements). Then, the phototransistor was illuminated with a certain light intensity (the wavelength was $\lambda = 550nm$ in our case) and a CP pulse was applied, followed by the reading phase ($V_G = V_{GR}$). In figure 2.16, we depict the CP frequency that is needed to recover the 'dark'

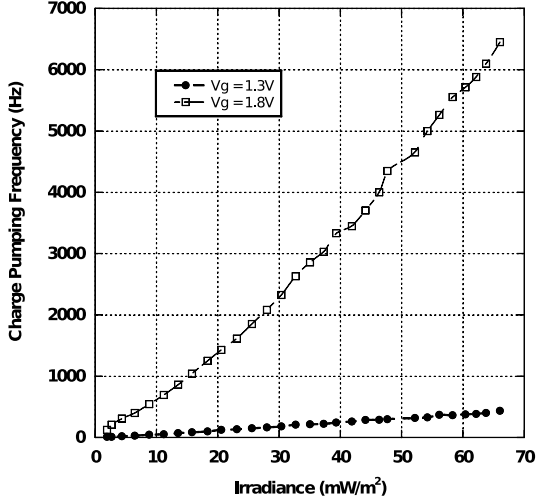


Figure 2.16 Charge pumping pulses needed to compensate excess of majority carriers (holes) generated for a given light irradiance (squares: $V_{GR}=1.8$ volts, dots: $V_{GR}=1.3$ volts)

value of the drain current during illumination for two values of V_{GR} . For instance, for a light intensity of $40\text{mW}/\text{m}^2$, such frequency was found to vary from 250 Hz for $V_{GR} = 1.3\text{V}$ up to 3450 Hz for $V_{GR} = 1.8\text{V}$.

In addition, since the 'reading' gate voltage V_{GR} influences both the collect and the recombination of holes, there may be an optimum depending on the specific application that is pursued. From the generation rate (due to illumination) and the recombination rate (due to charge pumping) - see curves on figure 2.4 and figure 2.15- it is possible to calculate the time separating two CP pulses needed to compensate the generated holes for a given light intensity. Following this approach, the maximum light intensity that can be measured is obtained when the number of charges photogenerated during the charge pumping period start to exceed the number of holes that are removed by the same charge pumping pulse. Then, since the minimal period that can be obtained with the charge pumping corresponds to the charge pumping pulse duration (see figure 2.13), we can deduce the maximum light intensity that can be measured. This only requires the knowledge of a frequency that corresponds to a given light intensity, assuming that there is a linear dependence between frequency and light intensity, as it will be discussed in section 2.8. This upper limit for the light power that can be quantified will depend on the charge pumping parameters used in our experiment

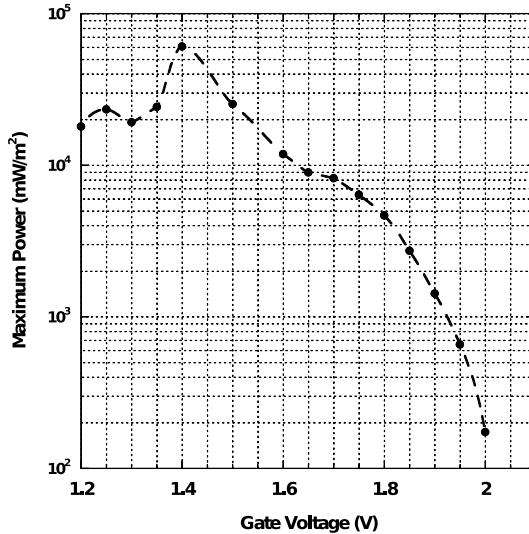


Figure 2.17 Maximum light irradiance as a function of the 'reading' gate voltage

(V_{GH} , V_{GL} , V_{GR} , frequency). In particular, figure 2.17 illustrates the influence of V_{GR} . The higher dynamic range is obtained for a V_{GR} equal to 1.4 volts. Conversely, the maximum sensitivity is achieved for $V_{GR} = 2$ volts where the charge pumping is not very efficient whereas the photo generation is still relatively high (see figure 2.4). In that way we can monitor precisely the amount of charges we are removing, leading to a better control.

Note that since CP recombination and optical generation rates are both directly proportional to the MOSFET area, reducing the device dimensions will not affect the correspondence between CP and luminance.

2.7 The Effect of Light on a Photo-MOSFET

We have briefly seen in section 1.2.2 the MOSFET phototransistor where the N-well is left floating and the photogenerated charges are separated at the junction N-well, P-substrate. The N-well will be negatively charged by the electrons inducing a change in the threshold voltage, while the holes will be evacuated by the substrate. The reason for which we are interested in this device, is that it resembles to a floating body SOI MOSFET.

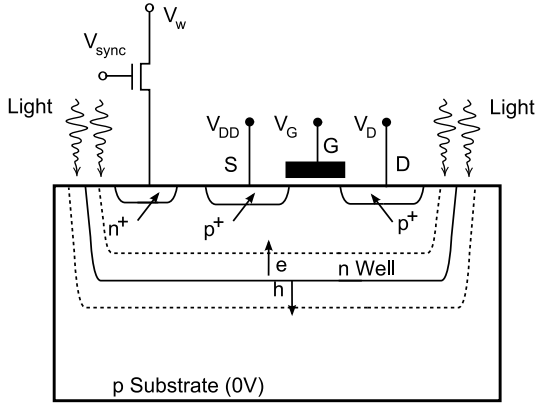


Figure 2.18 MOSFET phototransistor cross section

2.7.1 Principle

The basic principle of a MOSFET phototransistor is very similar to that used for the floating body SOI as discussed in section 2.2. The floating N-well of the MOSFET is similar to the floating body of the SOI MOSFET. In order to improve the isolation of the N-well, the P-substrate would have to be slightly negative, this would also improve the collection of photogenerated electron-hole pairs, as the electric field at the junction is higher. Once the electron-hole pairs are separated the electrons will remain in the body causing its potential to change. This would in turn, change the threshold voltage which affects the drain current. In contrast with traditional techniques, we will not measure the change in the drain current, but rather try to relate this to the frequency of charge pumping that is needed to keep the drain current constant even though the phototransistor is illuminated. The cross section of a MOSFET phototransistor is shown in figure 2.18 the N-well would be similar to the floating body of an SOI except that the separation of electron-hole pairs are taking place at all the interface surface between the N-well and the p-substrate. Whereas, the floating body SOI, the separation is taking place at the junctions and the channel, so the collection efficiency is higher for the bulk MOSFET case.

2.7.2 Light Measurement Technique

The technique used for the bulk MOSFET is similar to the one proposed for its SOI counterpart. The Charge pumping recombines the electrons in the N-well with the trapped holes at the gate side. Removing the extra electrons from the N-well reduces the body potential and

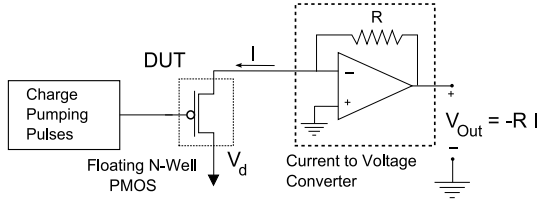


Figure 2.19 Circuit topology used to measure the drain current of the floating N-well PMOS

therefore increases the threshold voltage. Subsequently the drain current will decrease accordingly. With every pulse of charge pumping statistically the same number of electrons is removed from the N-well. This is different from the charge pumping applied for a bulk MOS where the recombination of electrons with the holes creates a bulk current, while the drain current remains unaffected. It is important for this technique to have the effect of charge pumping on the drain current otherwise it would be difficult to measure the amount of charges that were evacuated from the floating N-Well.

So instead of quantifying the photocurrent, as is usually done, we will measure the frequency of charge pumping needed to maintain the drain current constant, this allows a more accurate measurement as was shown in the floating body SOI MOSFET case in section 2.6.1. Results of such a measurement technique will be shown in section 2.7.3.

2.7.3 Measurements Results

For these measurements, the minimum length of the chosen technology is $0.35\mu m$, the threshold voltage of which is 650 mV. The sample used was a PMOS with a floating N-well, its length and width are $0.35\mu m$ and $35\mu m$ respectively.

The circuit setup depicted in figure 2.19 was used to measure the drain current. The drain voltage of the sample $V_D = -300mV$ to avoid the kink effect which is also present in a floating N-well MOSFETs. The gate voltage was adapted according to which channel inversion was needed. The source potential was set to zero volts by the fact that it is connected to a virtual ground of the setup shown in figure 2.19. The P-substrate (the handle silicon) was connected to zero volts, this minimizes the leakage current in the reverse biased junction N-well,P-substrate.

The light used was a calibrated green LED with wavelength $\lambda = 550nm$, varying the intensity of which was done by varying it biasing current.

The first measurement was conducted to demonstrate that a floating N-well to a bulk MOSFET is what a floating body is to an SOI MOSFET. Indeed, a photocharged N-well modifies the threshold voltage of

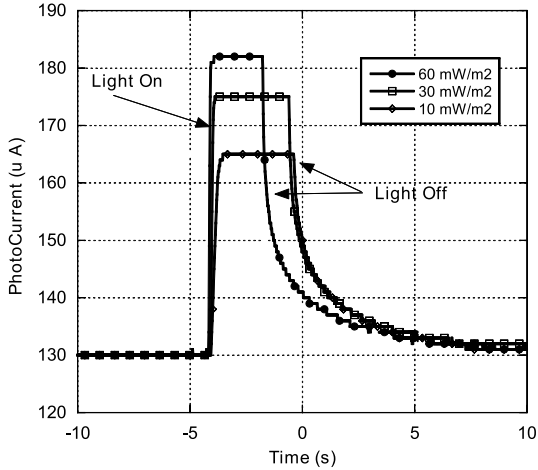


Figure 2.20 Time dependence of the drain current of a floating N-well bulk P-MOSFET when subjected to a light pulse

the PMOS which in turn modifies the drain current. The higher the illumination power the faster the generation rate and the higher the new *steady state*. This can be shown in figure 2.20 as we increase incident light power from 10mW/m^2 to 60mW/m^2 both the steady state and the slope of the currents have increased. Also similar to a floating body SOI MOSFET, slow recombinations at the junctions means slow drain current decay, something that is not desirable for common image sensing applications. Usually a MOS analog switch is used to discharge the floating N-well; however, this switch adds to the capacitance of the N-well making its voltage variation to the same illumination smaller. In addition to smaller voltage dynamics, the analog switch will contribute to the noise in the floating N-well by a factor of KT/C due to switching the integrating capacitor. In this experiment, the gate voltage was set to -800mV , which gives a DC current of $130\mu\text{A}$, the same DC current that biased the SOI phototransistor for a similar experiment (in section 2.2.1).

The second set of experiment was to find the relation between the intensity of incident light and the needed frequency of charge pumping to maintain the drain current constant. As stated before the incident light will tend to increase the drain current, where as the transient charge pumping will tend to decrease the drain current. If both are applied at the same time, and the photogenerated charges are equal to that re-

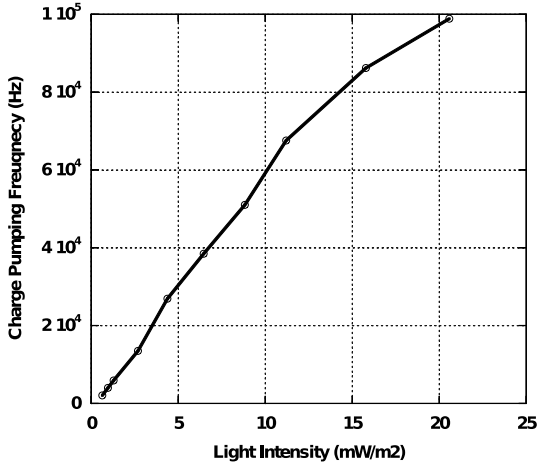


Figure 2.21 Charge pumping pulses needed to compensate excess of majority carriers (electrons) generated for a given light irradiance when biased in moderate inversion ($V_{GR} = -700mV$)

moved by the applied charge pumping pulse at a certain frequency then the drain current would remain constant. Figures 2.21 and 2.22 show the frequencies needed when the phototransistor is respectively in moderate and strong inversion. In both cases, the linearity was respected and what is more important is that low light intensities were measurable ($0.2mW/m^2$ for the strong inversion case and $0.6mW/m^2$ for the moderate inversion case).

2.8 Discussion

In this section we propose to discuss what are the main advantages and limitations of this sensing technique when using a PD SOI MOSFET as photodetector. Using the floating body SOI MOSFET in a 'standard' way, i.e. by measuring the change in the drain current, suffers from various drawbacks. Among them is the slow recovery time constant (see figure 2.2) which is not very attractive for common image sensing applications. A solution to overcome this effect would be to create a new contact directly to the body of the MOSFET in order to evacuate the excess of majority carriers (holes in our case). This solution is comparable to the reset phase of regular photodiodes before any measurement.

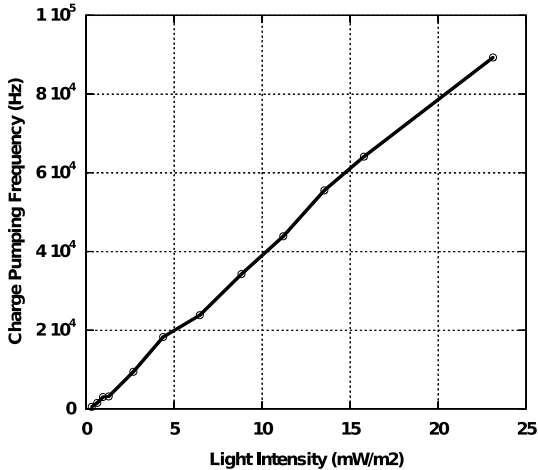


Figure 2.22 Charge pumping pulses needed to compensate excess of majority carriers (electrons) generated for a given light irradiance when biased in strong inversion ($V_{GR} = -900mV$)

However, it requires an extra MOS transistor used as a switch in order to isolate the body of the SOI photodetector during the 'sensing' phase. This direct contact of the switch transistor on the body of the SOI MOSFET will generate an additional leakage path and a substantial parasitic capacitance (and hence a lower change in body potential). Conversely, when using the charge pumping, we also benefit from this unique operation mode that can be viewed as a continuous discharging of the photon induced charges. This can be understood as an inherent integration time which has the property to adapt self consistently according to the light intensity. For instance, if the phototransistor is illuminated with a weak light, the current comparator will take more time before triggering the CP pulses. Conversely when a high power light is used, the threshold is reached faster. In addition, keeping the transistor in one defined state (when the transistor deviates from its 'dark state', the CP pulses will try to cancel out this offset) avoids any drift from weak to strong inversion during the data acquisition, minimizing non-linear effects in the photoresponse. Looking at figure 2.16, we can see that the relation between light intensity and charge pumping frequency that is needed to get the drain current back to its pre-illumination value is almost linear. Moreover, from the relatively low removal rate measured at higher gate potentials, the charge pumping frequency is higher for V_{GR} of 1.8 volts compared to 1.3 volts. Then, in terms of sensitivity, choosing a high V_{GR} allows for a better resolution whereas a lower V_{GR} can be used

Wavelength (nm)	Normalized Efficiency
675	0.06
575	0.134
550	0.267
420	1

Table 2.1 Normalized photogeneration efficiency measured at different wavelengths for a power density of $200mW/m^2$

to measure relatively high optical intensities. A power density as low as $2mW/m^2$ at a wavelength of 550 nm, corresponding to a charge pumping frequency close to 10 Hertz, could be measured. To our knowledge, there is no data reported in the literature for illuminations as low as $2mW/m^2$ which supports that this method can offer an interesting alternative to more classical strategies. Further, the effect of the light wavelength on the photodetector was analyzed. The maximum efficiency was obtained for 420 nm emission. Relative efficiencies for different wavelengths are listed in table 2.1.

For a given gate voltage V_{GR} , it is possible to estimate the probability that an incident photon will generate an additional hole in the body of the SOI MOSFET since the number of holes removed during a cycle of charge pumping is a known quantity. For instance, when the gate potential is set to 1.8 volts, we estimate the overall efficiency for the conversion of incident photons into excess body holes to be close to 0.1% for the wavelength 550 nm. Note that ideally, a higher sensitivity is expected when removing the silicon substrate down to the buried oxide and then illuminating the device from the backside. However, direct comparison with existing SOI photo-sensors is difficult mainly because we use a different technique of measurement. In addition, integration times are not fixed but, as discussed earlier, they vary self consistently according to the incident light power. A major advantage of this technique is that it can accurately measure low light intensities, simply by inducing long integration times. From the sensing circuit solution, the CP technique also offers some advantages: instead of requiring a high precision analog to digital current converter, here we simply compare a current to a fixed value and we directly generate a stream of digital pulses through the charge pumping activation. Typically the readout circuit would be a current comparator that compares the drain current to the dark current of the same cell. This comparator's output triggers

the CP pulses, hence forcing a reduction in the sensor current until the steady state value is reached. The output of the current comparator is digital by nature, so there is no need for an A/D converter to make the conversion into the digital domain. To some extent, this method is close to the sigma-delta approach widely used in single bit A/D converters. Besides the advantages of such method, there are some limitations. One of them would be the need for a high precision reference current source if high sensitivity is needed. According to figure 2.3, current variations as low as 3 nA, corresponding to a light intensity of $5mW/m^2$, should be detected. This represents a variation of the SOI MOSFET current of 1%. Another limitation concerns the use of this sensor in high data rate communication and ultra fast optical detection. Indeed, due to its mode of operation that rely on a closed-loop like regulation, the system may have a relatively long time constant, depending on the light intensity, but that is at least equal to the CP period. In our case, this would represent some tenth of micro-seconds, but could be substantially lowered in a fully integrated design solution. With this respect, future architectures co-integrating the sensing circuitry with the SOI MOSFET should allow enhancing the overall device performances and reducing the elementary cell area.

2.9 Conclusion

A new method to measure the intensity of light in a floating body partially depleted SOI MOSFET has been proposed. The method is based on collecting the photo-generated charges in the floating body of a partially depleted SOI MOSFET and removing them using the transient charge pumping technique. Interestingly, enhancement of the device sensitivity is simply obtained by monitoring gate potential, without requiring any layout modification. Based on our measurements, we found an optimum efficiency in terms of device sensitivity as low as $2mW/m^2$. Finally, this new concept seems to be very promising since it opens new applications for highly sensitive SOI based photo-detector that is fully compatible with standard CMOS technology.

Circuit Principles

3.1 Introduction

CURRENTLY, many of the SOI image sensors are based on an accurate measurement of the photocurrent that is generated by the incident light. This traditional technique suffers from two major drawbacks: the first is that the signal level is too low to be measured by an on chip circuit with sufficient signal to noise ratio (50 fA of photocurrent for $2mW/m^2$ [12]). The second disadvantage is the slow time recovery (10 seconds for the samples shown in [20]) in partially depleted SOI devices leading to a rather slow device, something not always attractable to many applications. However, the new technique explained in chapter 2 allows intensities as low as $2mW/m^2$ to be detected without having to accurately quantify the corresponding photocurrent.

The absorption of light taking place in the floating body of an illuminated SOI MOSFET generates charges trapped in the body, creating a decrease in the threshold voltage, leading to an increase in the drain current. These extra photogenerated charges in the body are then slowly evacuated through the reverse biased junctions at both the drain and the source [55] causing the slow decay in the drain current once the light is removed. However, this slow recombination rate impedes the phototransistor for most imaging applications since this is related to the device recovery time. As was discussed in chapter 2, transient charge pumping can remove extra charges from the floating body by pulsing the gate voltage producing a change in the channel current. Based on this observation, we proposed in chapter 2 the use of transient charge pumping to evacuate the extra charges and showed that the number of charges evacuated is roughly proportional to the number of pulses applied on the gate [21].

Using the technique developed in chapter 2 and based on the model derived in [19] a practical implementation of a complete readout circuit for the SOI sensor of interest is then proposed and discussed in this chapter. The basic idea of the circuits consists of a current comparator continuously comparing the current of the phototransistor with a reference value set to the drain current of the phototransistor in dark. When illuminated, the phototransistor drain current will increase. As long as the drain current under illumination is higher than that of the reference (dark current), the comparator enables the charge pumping pulses on the phototransistor gate. When the photocurrent drops below the reference value, the comparator stops the pulses and the drain current is free to increase again (if the phototransistor is to be illuminated). The output of the comparator is then a pulse width signal modulated by the intensity of light. In this chapter, we propose two different circuits both based on the same principle just described. One circuit, called the synchronous circuit, relies on an external clock to synchronize the circuit through the different phases of the readout. Another circuit, called asynchronous, is clocked through the charge pumping pulses applied on the phototransistor gate. In this chapter, we will show how the use of a floating body SOI transistor along with a current comparator reverts to a *natural* first order delta-sigma modulator. Section 3.2 reviews quickly the general concept of delta sigma modulators, then in section 3.3 both architectures (synchronous and asynchronous) are explained as well as the comparator and the dimensioning of the different transistors. Section 3.4 shows the measurements for both circuits discusses the measurements and compares the performances. Section 3.5 presents the improvements that can be brought to the proposed system. Finally, in section 3.6 a matrix architecture using the presented pixels is proposed.

3.2 Delta Sigma Theory

3.2.1 In General

In this section we will briefly explain what a delta-sigma modulator is and how it can be used for analog to digital conversion along with some of the basic design elements.

A delta sigma modulator has three important components as is shown in figure 3.1.

1. A loop filter or a transfer function $H(z)$
2. A clocked quantizer
3. A feedback digital-to-analog converter (DAC)

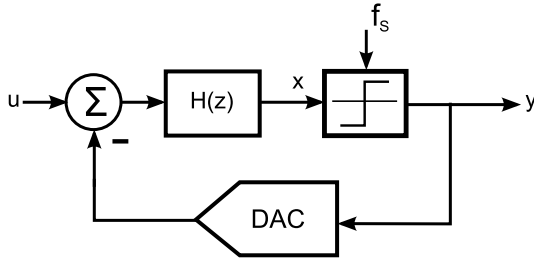


Figure 3.1 Basic components of a delta sigma modulator

Among the three major components of a delta sigma modulator the quantizer is the only non-linear component. This makes the mathematical model of such a system very complicated to investigate, however we can still explain the basic idea of delta sigma modulators as follows:

The analog input signal is modulated into a digital word sequence whose spectrum approximates that of the analog input well in a narrow frequency range; however, outside this band of interest the signal is noisy. This noise comes essentially from the quantization of the input analog signal, and the loop filter that *shapes* the quantization noise away from the band of interest. The circuit shown in figure 3.1 can be linearized by replacing the non-linear component (the quantizer) by an adder which adds to the signal a quantization noise independent of the input signal u as shown in figure 3.2. This assumes that the quantizer gives the exact discrete representation of its input, then the output y can be written in terms of the two inputs u and e as follows:

$$Y(z) = \frac{H(z)}{1 + H(z)}U(z) + \frac{1}{1 + H(z)}E(z) \quad (3.1)$$

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \quad (3.2)$$

where $STF(z)$ and $NTF(z)$ are the so-called signal transfer function and the noise transfer function. From the equation 3.1 we see that the poles of $H(z)$ become the zeros of $NTF(z)$, and that for any frequency where $H(z) \gg 1$,

$$Y(z) \approx U(z)$$

this means that the input ($U(z)$) and the output ($Y(z)$) spectra are in agreement at frequencies where the gain of $H(z)$ is large.

The above is based on the assumption that the added noise e at the quantizer in figure 3.2 is white and uncorrelated with the input u . The first assumption is often true, the second one is never exactly true; however, this model yields correct qualitative predictions of the performances. The reduced quantization noise is over a narrow bandwidth, that is a

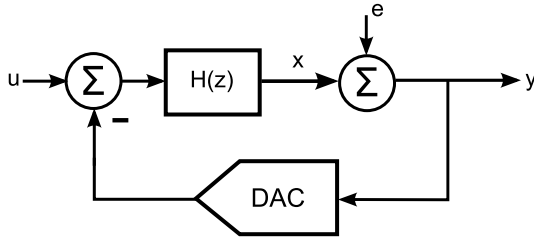


Figure 3.2 Linearizing the quantizer in a delta sigma modulator

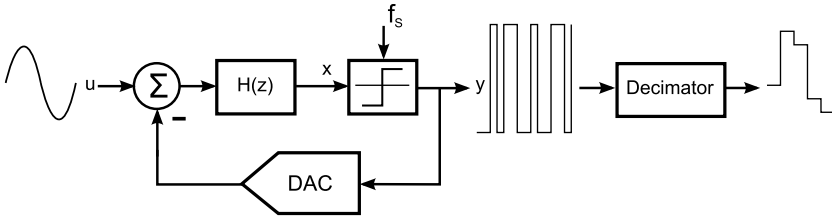


Figure 3.3 Linearizing the quantizer in a delta sigma modulator

bandwidth much smaller than f_s the sampling frequency. If we desire to have a high resolution, then the signal should be bandlimited to a value much smaller than f_s . This means for a signal with Nyquist sampling frequency of f_N , this means that $f_N \gg f_s$. This defines what is known as the oversampling ratio:

$$OSR = \frac{f_s}{f_N} \quad (3.3)$$

In order to convert the high speed low resolution quantizer output to multibit output samples at the Nyquist rate a decimator is used as shown in figure 3.3. The second function of the decimator is to filter out the noises that are outside the band of its filters. The subject of decimators is not covered in this thesis as the desired format of the output is a digital bitstream similar to the output of the quantizer. The figure 3.3 shows a complete signal flow in a delta sigma modulator at both the time domain and the frequency domain.

In the next section we will apply the same principles applied in this section to a first order delta sigma modulator and we will see the performance parameters.

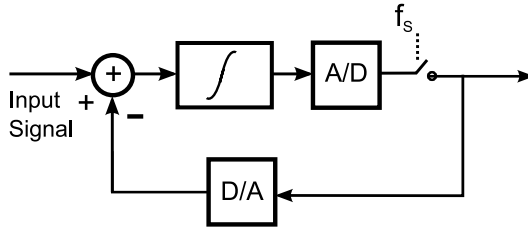


Figure 3.4 A diagram of a first order delta sigma modulator

3.2.2 First Order Delta Sigma

The basic structure of a first order delta-sigma modulator consists of an integrator, a one bit analog to digital converter and a digital to analog converter in the feedback path (figure 3.4).

The input to the integrator is the difference between the input signal and the feedback signal. The one bit analog to digital converter is built with a comparator performing the quantization of the integrator output. The digital to analog converter in the feedback loop is an analog switch, alternating between two analog values based on the binary output of the comparator. Usually, this output is followed by a decimation filter which yields a more accurate representation of the input signal. Such a modulator has the average of its input signal equal to that of the output as the integrator has an infinite DC gain. The performances of a delta-sigma modulator are dependent on the oversampling ratio defined as:

$$OSR = \frac{f_s}{2f_0} \quad (3.4)$$

Where f_s is the sampling frequency and $2f_0$ is the Nyquist frequency. Based on this parameter as well as the order of the delta-sigma modulator, it was shown [27] that the maximal signal to noise ratio has the following form:

$$SNR_{max} = \frac{3}{2}\pi(2L+1)\frac{OSR^{2L+1}}{\pi} \quad (3.5)$$

Where L is the order of the modulator. From this, the number of effective bits could be deduced based on the following formula.

$$Effective\ bits = \frac{SNR_{max} - 1.76}{6.02} \quad (3.6)$$

If we take, in our case, the first order modulator, we find a maximum of 80 dB of signal to noise that can be achieved with an OSR of 1000

[27].

Because of the coarse conversion of its 1-bit comparator one would think that the quantization noise would be high in this modulator reducing the resolution of the measurement. However, if we take a look at the s -domain representation of such a system (figure 3.4) we see that it applies spectral shaping to the quantization noise (taking place at the 1-bit comparator). If we model the quantization error as an input noise after the integrator, the noise transfer function (NTF(s)) has the form

$$\frac{Y(s)}{N(s)} = \frac{s}{s+1} \quad (3.7)$$

which is a high pass filter shifting the undesirable quantization noise at high frequency outside the band of interest. While the signal transfer function (STF(s)) has the form

$$\frac{Y(s)}{X(s)} = \frac{1}{s+1} \quad (3.8)$$

which is a low pass filter and hence keeping the signal in the band of interest, pushing to a higher frequency the noise associated with the error of quantization that means the error done at the comparator stage does not affect the resolution of the pixel.

Model Simulation

The first order delta sigma modulator discussed in section 3.2.2 can be simulated in Matlab using the model shown in the aforementioned section. The adder and the integrator blocs are a simple addition, while the comparator is a comparison with a reference. In order to simulate the behavior of the system, at the input we supply a sine signal at a frequency $f_0 = 10Hz$ with some white noise. The input signal is shown in figure 3.7. For this input the delta-sigma outputs a stream of 1's and 0's whose power spectral density is shown in figure 3.5. From this figure one can deduce the quantization noise shaping of the first order (20 dB/decade), the oversampling ratio (OSR) used for this experiment was 2500, which puts the sampling frequency at $f_s = 50kHz$. Finally we can see that what limits the performance is the white noise that was added to the input signal with a signal to noise ratio of 70dB. One would expect more than 70 dB with an OSR = 2500 based on equation 3.5. On the contrary, with an OSR = 50 (shown in figure 3.6) we can see the signal to noise ration (SNR) is limited to about 60 dB. The noise floor, in this case, is set by the quantization noise of the 1-bit comparator.

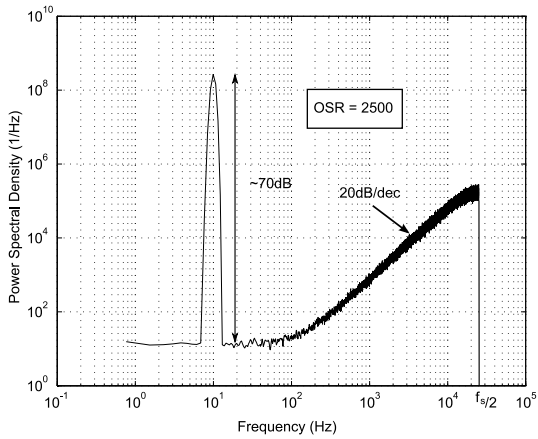


Figure 3.5 Power spectral density with an OSR of 2500

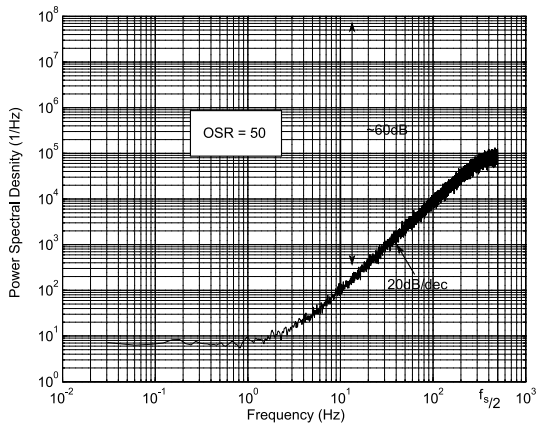


Figure 3.6 Power spectral density with an OSR of 50

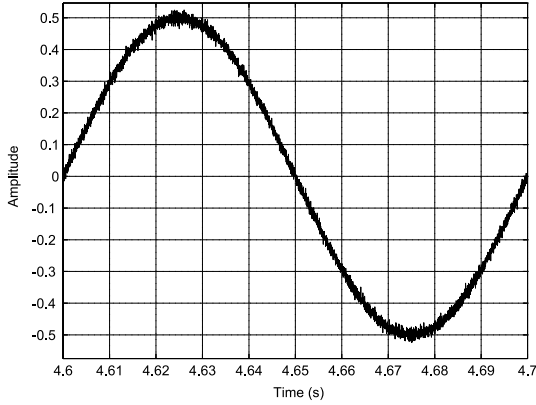


Figure 3.7 Input signal pure sine with added white noise (SNR = 70 dB)

3.3 Proposed Circuits

3.3.1 Model and Simulations

Modelling the Photogeneration and the Transient Charge Pumping

As we have seen in chapter 2, the charge pumping as well as the photogeneration are physical phenomena that cannot be modeled in a circuit simulator since this is an important variable of the MOSFET compact models. However, both phenomena cause a change in the body potential by changing the amount of charges stored in the floating body. Unfortunately, body charges are not primitive variables in compact models, in contrast to voltage and current that can be handled by CAD tools as external variables. Therefore, we will use electrical modules of the simulator to modulate the body potential as needed. The floating body SOI MOSFET has an electrically isolated body. Its body can be modeled as an ideal capacitor storing charges. Therefore, there exists a correspondence between potential and charges. This is exactly what will be used for the charge pumping simulation. Using the partially depleted floating body SOI MOSFET transistor in a circuit simulator by connecting the body to a current source, which intensity is equal to the photogeneration rate, imply that changes in body potential and drain current will be equivalent to that experienced by the phototransistor exposed to light. This electrical approach can then be used to model the photogeneration in a floating body of partially depleted SOI MOSFET. On the other hand, in order to simulate the charge pumping, which is essentially a

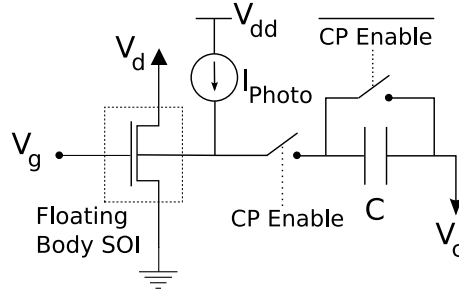


Figure 3.8 Block diagram showing the model of the photogeneration and charge pumping

technique to remove the majority carriers from the body, we propose to discharge a capacitor connected to the body. Then the charges removed per cycle can be written as:

$$Q = C(V_{body} - V_c) \quad (3.9)$$

As we can see, charges removed are dependent on the body potential V_{body} . To ensure that the amount of charges stored on the capacitor are independent of V_{body} , one side of the capacitor is connected to a relatively high negative potential ($V_c = -5V$) in order to be insensitive to mV body potential variations and equation 3.9 can be rewritten as:

$$Q \approx C(-V_c) \quad (3.10)$$

Since in the real case the source-body and drain-body junctions exhibits some leakages leading to a slow discharge of the body, it is important to use the MOSFET model that accounts for these leakages and this indeed was our approach.

Before any new charge pumping phase, a discharge phase is needed to reset the capacitor. However, we must ensure that charges removed by the capacitor are equal to that removed by a single pulse of charge pumping. This is achieved by setting the right value of the capacitance C . Figure 3.8, shows the setup used to simulate both the photogeneration as well as the charge pumping pulses. In this setup the reference current I_{ref} is set to $45\mu A$, the capacitor C is 2aF corresponding to a charge of $100nC/m^2$ per one CP pulse. I_{photo} is a sine wave of frequency 50Hz and amplitude of 20fA with a DC offset of 40fA corresponding respectively to $10mW/m^2$ and $20mW/m^2$.

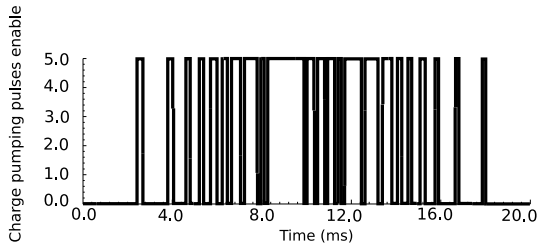


Figure 3.9 The pulse width modulation output of the current comparator.

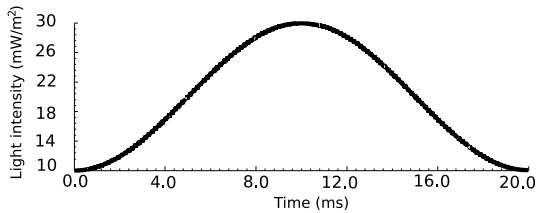


Figure 3.10 The input light signal to the pixel.

System Simulation

Now that we can model the photogeneration and the recombination of charges in the body of the transistor in a circuit simulator, we are ready to simulate the complete system. The basic concept of our cell is to compare the current of the phototransistor with a reference current. Whenever the photocurrent is larger than the reference current, the output of the comparator goes to logic 1, enabling the generator of charge pumping pulses. Figure 3.9 shows the output of the comparator when a sine modulated light (figure 3.10) is illuminating the phototransistor. We can see that as light intensity increases, the enable duration gets larger, enabling more charge pumping pulses to remove more holes from the body and hence decreasing the current.

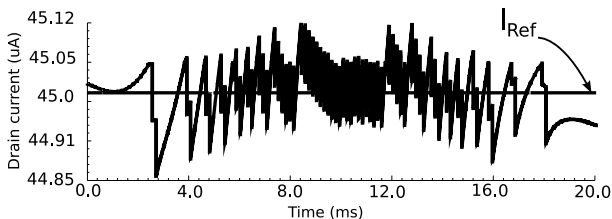


Figure 3.11 The drain current in the phototransistor as a function of time.

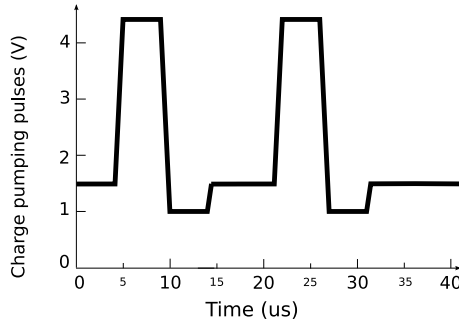


Figure 3.12 Typical charge pumping pulses applied on the phototransistor.

Effectively the drain current will oscillate around the reference current as shown in figure 3.11. As long as the photocurrent is below this threshold value (I_{ref}), no charge pumping pulses are applied on the gate of the phototransistor.

When I_{ref} is exceeded, due to the charging of the body, charge pumping pulses (shown in figure 3.12) will then be applied to the gate, forcing the removal of the photogenerated holes and subsequently reducing the drain current. If this new value of the drain current is still exceeding the reference, additional charge pumping pulses will be applied, causing another decrease in the drain current. This step will be repeated as long as the drain current is larger than the reference one. Once it gets below, the comparator disables the charge pumping pulse generator. One would expect to have symmetrical output current generated by a symmetrical light pulse, but this is not the case due to the fact that the charge pumping pulses and their enabler are not synchronized. In the event where the incident light generates too many charges that cannot be compensated by the stream of charge pumping pulse, holes will accumulate in the body and the body potential will continuously increase.

This in turn will increase the drain current as shown on figure 3.13a. Note that when this light is switched-off, the system will need sometime to reestablish the steady state due to the very large hole concentration in the body. In our case, the time the system needs to stabilize is close to 1ms. This light intensity represents then an upper limit for the dynamic range of the pixel. However, a simple solution consists in increasing the charge pumping frequency. Figure 3.13b confirms that increasing the frequency from 6.6 kHz up to 10 kHz allows recovering a full control of the pixel, thus offering a simple mean to extend the dynamic range.

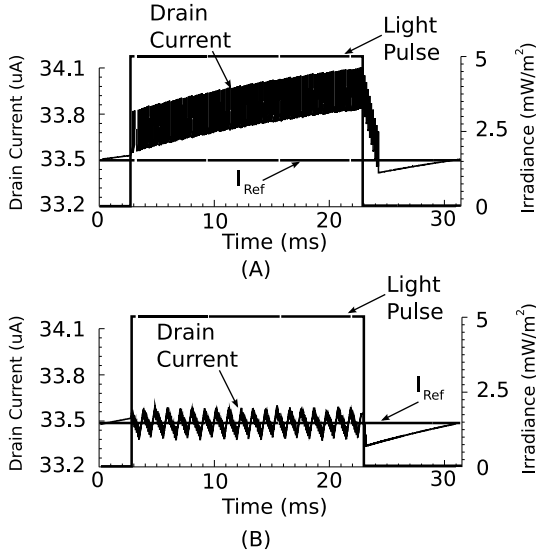


Figure 3.13 (A) an insufficiently low charge pumping frequency of 6.6KHz (B) a sufficient charge pumping frequency of 10KHz

3.3.2 Synchronous Pixel

Figure 3.14 shows the block diagram of the synchronous pixel presented in [22].

In this configuration, the output of the current comparator V_{out} is fed to the input of a memory element (typically a D flip-flop) which is clocked at the sampling frequency. The output of the memory element controls the gates of analog switches, switching the gate of the phototransistor between the charge pumping pulses and the gate reading voltage. The circuit has 2 phases per cycle, the reading phase and the charge pumping phase explained as follows:

During the reading phase, a reading voltage (V_{GR}) is applied at the gate leading to a given drain current (the drain is kept at a low voltage of about 0.3V to avoid generation due to impact ionization, also known as the kink effect in a floating body transistor). At this stage the comparison between the reference current and the drain current of the phototransistor takes place. At the end of this reading phase the output of the current comparator had enough time to stabilize its output which is then latched by the D flip-flop. During the charge pumping phase, the gate of the phototransistor is either pulsed or kept at the reading voltage (V_{GR}) depending on the latched output of the previous reading

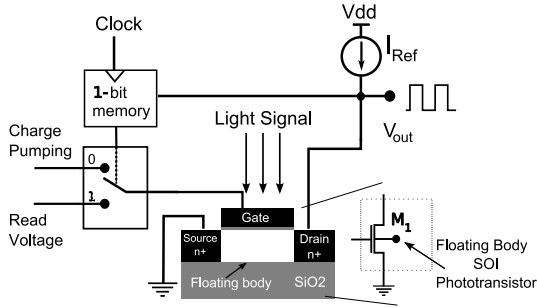


Figure 3.14 Block diagram of the synchronous pixel

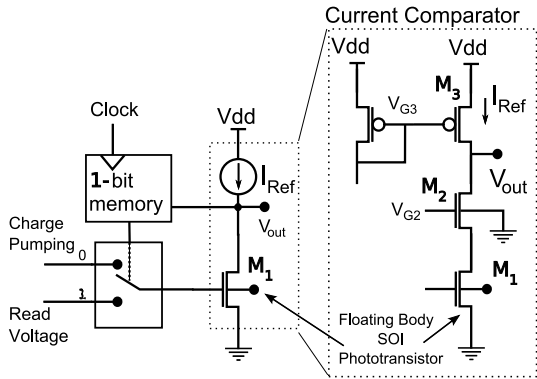


Figure 3.15 Synchronous pixel architecture

phase. In this phase, in order to minimize current consumption when the charge pumping is in the inversion phase, the drain of the phototransistor is disconnected from the circuit. This is done by switching off the transistor M_2 (figure 3.15).

(Note that leaving the drain floating does not affect the efficiency of the charge pumping pulse). The charge pumping pulses will then remove some extra charges and tend to bring the body potential V_b back to its initial value (typically 0 V). One important aspect is that the reference current source used by the comparator does not have to be of high resolution. As a matter of fact, and in contrast with *standard* techniques, a drift in the reference current is translated into a drift in V_b , however the relation light intensity frequency of pulses would still be the same. This technique is then very robust and should be less sensitive to current mismatch issues in a matrix structure. However, in addition to the *classical* mismatch coming from geometry and process dependent parameters (V_T , C_{ox} , mobility ...) fluctuations in the trap density will also generate some mismatches in regard to the charge pumping effect. Even

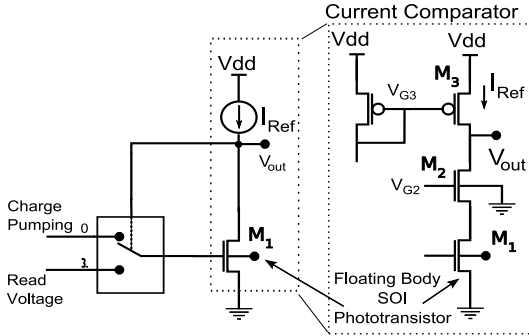


Figure 3.16 Asynchronous pixel architecture

though this requires a detailed investigation that cannot be addressed in this work, it is worth mentioning that the threshold voltage also depends on the trapped charge density in the oxide through the flat band voltage. Mismatch in charge pumping and V_T should then share some common origin. Then improving matching of the threshold voltage should also improve the matching of the charge pumping.

3.3.3 Asynchronous Pixel

In this setup shown in figure 3.16, the output of the current comparator is not fed to a memory element, but rather directly to inverters that control the gates of analog switches having the same functions as in the synchronous pixel. This circuit has 2 phases per cycle, but it differs from the synchronous pixel architecture in its instantaneous decision in the reading phase (with a small delay in the order of 10ns) applied on the switch moving from one phase to another depending on the output of the comparator.

The first phase is a reading phase during which the output is initially high when the phototransistor is not illuminated, meaning that the drain current of the phototransistor is lower than the reference current (I_{ref}). When illuminated, the drain current may rise above the reference value and then the output of the comparator goes low switching on the charge pumping pulses; otherwise, the pixel will remain in the reading phase. In the second phase, the charge pumping pulses are applied on the gate of the phototransistor following 2 states: the inversion state and the accumulation state. When in the inversion case, a rather high V_{GCP} (higher than V_{GR}) is applied, the comparator output remains at logic 0. This keeps the voltage V_{GCP} applied on the gate. When in the accumulation case, the V_{GCP} applied is much lower than the V_{GR} , and then the comparator output will be logic 1, switching the gate voltage

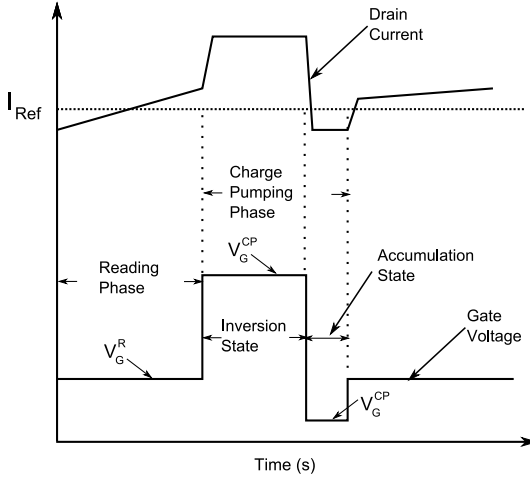


Figure 3.17 Asynchronous pixel timeline

from V_{GCP} to V_{GR} . This brings back the circuit into the reading phase. Figure 3.17 shows the timeline of the different control signals of this pixel.

3.3.4 Current Comparator Transistor Sizing

The phototransistor used in our circuit is a floating body SOI NMOS with a channel length of $1\mu m$ and a width of $100\mu m$ [21] (see Fig. 3). During the reading phase, the device is biased with a drain current $I_D = 15\mu A$ and the gate voltage is set to $V_{GR} = 1.4V$ [21]. The drain current of M1 is buffered through the device M2 acting as a current follower (figure 3.15). The threshold current is generated by a current mirror that is biased by a current $I_{bias} = I_{ref} = 15\mu A$. The gate voltage of M2 (V_{G2}) is set to get the M1 drain voltage at $0.3V$ thus avoiding the impact ionization phenomena. The V_{dd} of the chosen technology (Xi10 module from Xfab) is $5V$ with a threshold voltage of $1.6V$ and a minimum channel length of $1\mu m$. During the reading phase, the potential V_D should be stable to guarantee a stable drain current. At least, variations in V_D , i.e. ΔV_D , should not cause the comparator output change state. From a simple analysis, a variation in V_D will induce a variation in the drain current ΔI_D given by:

$$\Delta I_D = g_{ds1} \Delta V_D \quad (3.11)$$

This in turn can be related to a variation in the threshold voltage ΔV_T through [41]

$$\Delta I_D = \frac{g_{m1}}{n-1} \Delta V_T \quad (3.12)$$

From equations 3.11 and 3.12 we obtain a correspondence between the threshold and drain voltage variations through the transistor voltage gain definition:

$$\Delta V_D = \frac{g_{m1}}{g_{ds1}(n-1)} \Delta V_T = A_V \frac{1}{n-1} \Delta V_T \quad (3.13)$$

Typical values of ΔV_T that induce switching in the comparator were measured to be about 1 mV. Therefore, acceptable corresponding ΔV_D variations would be of the order of 10mV in our case. Note also that the stability in the drain potential is only needed at the beginning of the reading phase, once the output of the comparator has stabilized at a certain state, V_D will no longer vary.

Then a variation ΔI_D in the drain current will cause a variation of the source potential of M2 which identifies to ΔV_D 3.15.

In addition the transistors M1 and M2 satisfy the following relations:

$$\Delta I_D \propto g_{m2} \Delta V_D = \frac{g_{m2}}{n} \Delta V_D \quad (3.14)$$

where g_{m2} is the transconductance of M2.

$$\Delta I_D = g_{mb} \Delta V_b = g_{m1}(n-1) \Delta V_b \quad (3.15)$$

where "n" is the body factor and is equal to 2.3 in our case [39], and ΔV_b is the body potential variation due to holes generation in the body.

Combining equations 3.14 and 3.15 and given that M1 and M2 have the same lengths and the same drain current, the following relation can be written

$$\frac{\Delta V_D}{\Delta V_b} \propto \frac{g_{m1}}{g_{m2}} \frac{n-1}{n} \quad (3.16)$$

When the pixel is biased in strong inversion, the ratio of equation 3.16 can be written as

$$\frac{\Delta V_D}{\Delta V_b} \propto \frac{n-1}{n} \sqrt{\frac{W_1}{W_2}} \quad (3.17)$$

where W_1 and W_2 are the widths of the transistors M1 and M2 respectively.

The ratio of equation 3.17 is always greater than but close to 1, because

Transistor	Gate Voltage (V)	Width (μm)	Length (μm)
M1	1.4	100	1
M2	2.2	10	1
M3	3.1	35	1

Table 3.1 Summary of the transistors dimensions

M1 is always larger than M2 for a high fill factor. When biased in weak inversion equation 3.16 can be written as

$$\frac{\Delta V_D}{\Delta V_b} \propto \frac{n-1}{n} \quad (3.18)$$

The ratio in 3.18 is always lower than 1 and is independent of the sizes used for M1 and M2. It is always desirable to keep this ratio as large as possible to make V_b independent from the variations of V_D . In weak inversion this ratio is dependent only on the technological parameter "n", hence in this mode of operation the stability of V_D is independent of the dimensions of M2. The PMOS transistors of the current mirror shown in figures 3.15 and 3.16 were sized to get the best matching. Table 3.1 summarizes the different design parameters for the current comparator.

3.4 Circuit Measurements

3.4.1 Principles

In general, we are interested in the power spectral density of a signal because it carries the information of signal to noise ratio (SNR) one of the most important performance measure of an electronic system. In addition to that, a delta-sigma system is known to shape the quantization noise, hence one is interested in the frequency domain representation of the time domain output stream of bits. For this end, the most common tool to use is the discrete Fourier transform (DFT). A DFT can be implemented using a *fast Fourier transform* (FFT) when the signal is represented by N discrete uniformly separated samples ($y(n) = \hat{y}(t)|_{t=nT_s}$, $n = 0 \dots N-1$, $y(n) \in \mathbf{R}$)

$$Y(n) = \sum_{k=0}^{N-1} y(k) e^{j2\pi kn/N}, n = 0 \dots N-1 \quad (3.19)$$

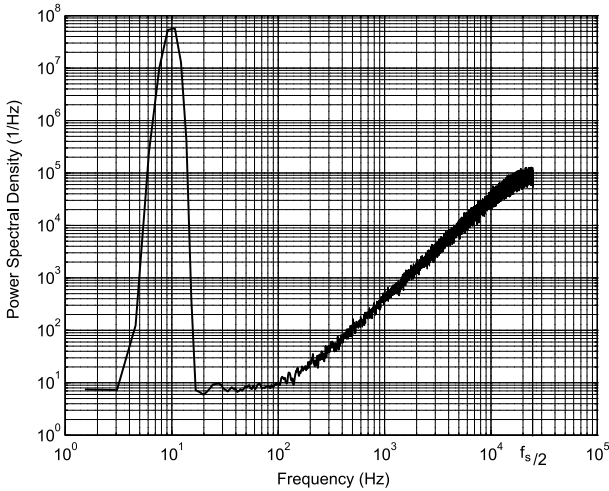


Figure 3.18 The PSD of a tone at 10Hz with the window blackmanharris

This power spectrum is defined for $N/2+1$ uniformly spaced frequency points between 0 and the frequency $f_s/2$ (known as Nyquist rate). Therefore, each frequency point, called also frequency bin, is of width f_s/N , hence it is important to collect the maximum number of samples N to have a good resolution. Being a representation of the real power spectrum, the FFT has limitation that we will detail in this section.

Leakage and windowing. When the input signal frequency does not fall exactly in the center of frequency bin, then leakage will result. Instead of a sharp dirac-like spike in one spectrum bin, the tone will be spread over adjacent bins. This occurs because of the limited number of samples that were taken from the signal. The FFT of finite number of bins is similar to that of an infinite number of data multiplied by a rectangular window that is 1 for the duration of the finite set of bins and 0 elsewhere. In the frequency domain, this corresponds to a convolution of the Fourier transform of the rectangle $(\sin x)/x$, with the infinite power spectrum. The leakage can then be controlled by the spectrum of the chosen window. It is sufficient to multiply the data with a specific window before applying the FFT. [23] lists many examples of windows figures 3.19 and 3.18 shows the outcome of both the *hamming* and the *blackmanharris* windows respectively. Compare the PSD's where a window was used to a one where no window was used (figure 3.20).

Averaging. There is a second reason for which the FFT is not an accurate representation of the actual power spectral density: the FFT at

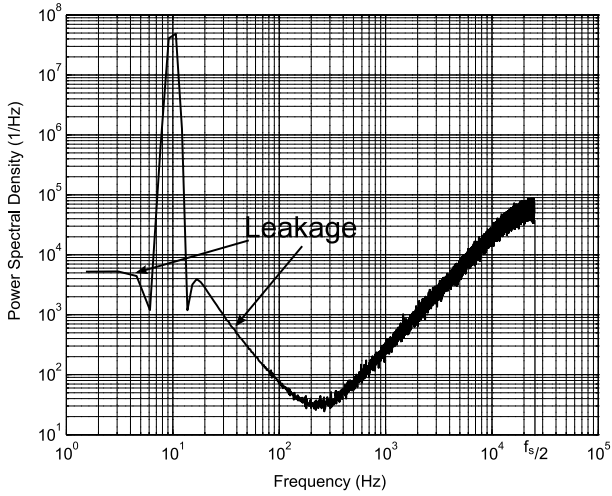


Figure 3.19 The PSD of a tone at 10Hz with the window hamming

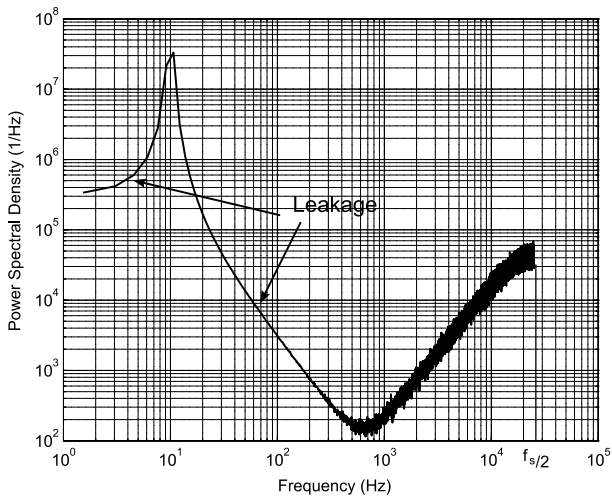


Figure 3.20 The PSD of a tone at 10Hz with the no windowing of data

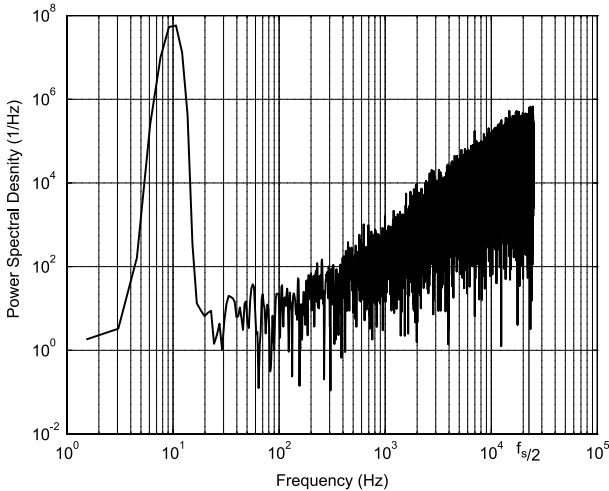


Figure 3.21 The PSD of a tone at 10Hz with no averaging of PSDs

a single frequency is an estimate of a continuous function over a range of frequencies centered at f_n and having a width of f_s/N . The estimates have a standard deviation of 100% of the real values. This can be reduced by taking K successive sets of N samples and averaging them, the standard deviation will then be reduced by a factor of \sqrt{K} . Figures 3.21 and 3.22 show respectively a PSD with no averaging applied and with $K = 50$ successive measurements.

3.4.2 Performances

Both circuits shown in figure 3.15 were integrated using partially depleted SOI MOSFETs (body tied except for the phototransistor). To characterize such a system, we supplied the bias for the reference current; the value chosen for this current depends on the inversion level of the phototransistor. The supply voltage, as well as the reading gate voltage V_{GR} were supplied from external sources. The pulses of charge pumping were generated from an external pulse generator (note that this could be integrated as well). The non active part of the circuit was protected by a top layer metal, so the incident light illuminates only the phototransistor. A calibrated green LED was used as a light source, varying its current to modulate its light intensity. In all of the experiments the reference current is placed just above the DC current of the phototransistor when biased by V_{GR} . It is shown in [21] that the sensitivity

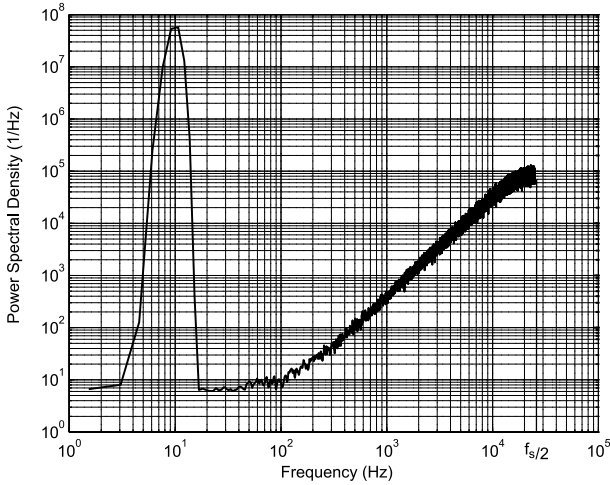


Figure 3.22 The PSD of a tone at 10Hz with 50 PSDs averaged

and the efficiency of the charge pumping are related to the inversion of the MOSFET channel. Thus, to characterize the minimum and the maximum sensitivities for the pixel we need to consider it in different inversion regions. The minimum intensity is evaluated when the output of the comparator is high and not changing in time. The maximum intensity is obtained when the comparator output is always low, implying that we are constantly removing charges, but not enough to regain the steady state current. The minimum and maximum intensities were measured in the cases where the phototransistor was in weak inversion and moderate inversions. The choice of the inversion of the phototransistor has an impact on the bias and reference current level in the pixel. For weak inversion, we used $1.2\mu A$ and for moderate inversion $15\mu A$. Respectively in weak and moderate inversion, we obtained for the synchronous pixel, $30mW/m^2$, $1650mW/m^2$ and $3mW/m^2$, $2800mW/m^2$. Whereas, for the asynchronous pixel, the minimum and maximum intensities were respectively $6.4mW/m^2$, $2193mW/m^2$ for moderate inversion and $25.6mW/m^2$, $2915mW/m^2$ for the weak inversion. Figure 3.23 shows the relation between the light intensity and the frequency of charge pumping applied on the gate of the phototransistor for both the synchronous and the asynchronous pixel. Except for the intensities between 45 and $55mW/m^2$, this dependence is found to be almost linear. This was already observed in former experiments [19], and is confirmed in the readout circuit operation.

Figure 3.24 shows the power spectral density (PSD) of the output

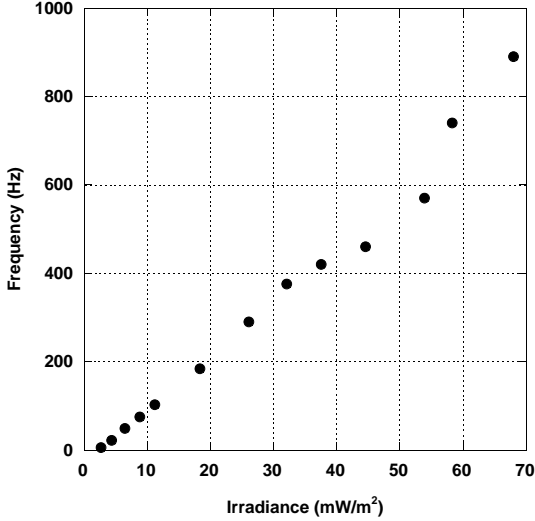


Figure 3.23 Measured frequency of charge pumping needed to compensate light induced charges

of both the synchronous and asynchronous pixels when illuminated by amplitude modulated light at a frequency of 10Hz. In the band of interest the signal to noise ratio (SNR) is measured to be 47dB for the synchronous pixel, and 52dB for the asynchronous one when the phototransistors are biased in moderate inversion. Figure 3.25 shows the PSD of both architectures when the phototransistors are biased in weak inversion: the SNR for the synchronous pixel is 44dB and 50dB for the asynchronous one.

These results are summarized in table 3.2, 3.3 and 3.4 for different inversions levels. It is shown in [21] that the generation rate is dependent on the power of the incident light. This means the pixel has a maximum frequency over which the signal is distorted or loses precision. This is due to the delay of the generation rate which can be slower than the rate of change of the light signal. In an ideal case, the time needed to switch on the charge pumping is dependent on the number of photons absorbed to make the drain current of the phototransistor slightly higher than the reference current. This depends on the incident power (P_{light}) for a given wavelength. From this we can write

$$t_{switch} = E_{threshold} / P_{light}.$$

To find the maximum frequency of the input light signal, it is necessary to satisfy the switching speed relation

$$f_{switchMax} = OSR * f_{signalMax} \text{ to guarantee a given signal to noise ratio (SNR), hence } f_{signalMax} = P_{light} / (E_{threshold} OSR).$$

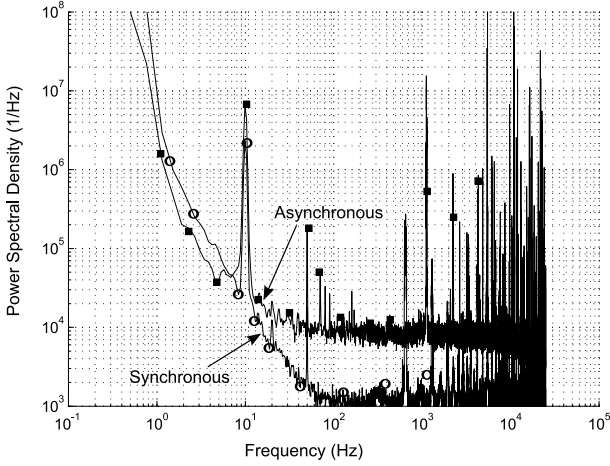


Figure 3.24 Measured power spectral density of both pixels biased at moderate inversion

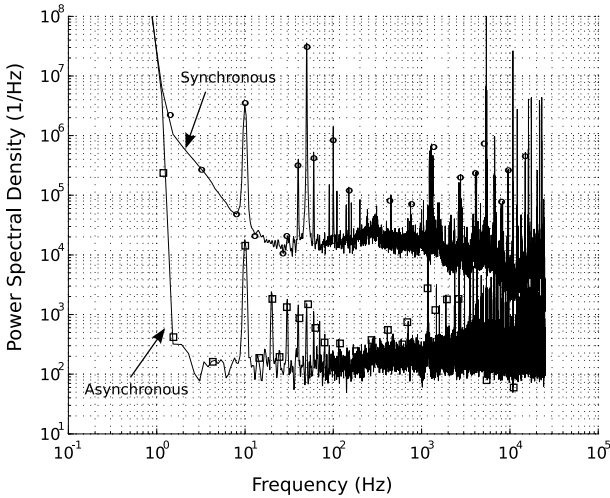


Figure 3.25 Measured power spectral density of both pixels biased at weak inversion

Channel Inversion	Synchronous Pixel (dB)	Asynchronous Pixel (dB)
Weak Inversion	35	41
Strong Inversion	59.4	61

Table 3.2 Dynamic range for the proposed pixels

Channel Inversion	Bias Current (μA)	Sensitivity (mW/m^2)	Maximum irradiance (mW/m^2)	Resolution (bits)
Weak Inversion	1.2	30	1650	7
Strong Inversion	15	3	2800	7.5

Table 3.3 Summary of results for synchronous pixel

Channel Inversion	Bias Current (μA)	Sensitivity (mW/m^2)	Maximum irradiance (mW/m^2)	Resolution (bits)
Weak Inversion	1.2	25.6	2915	8
Strong Inversion	15	6.4	2193	8

Table 3.4 Summary of results for asynchronous pixel

It is worth mentioning that $E_{threshold}$ mainly depends on how close the dark drain current of the phototransistor and the reference current can be without switching the comparator. On one side, this can be a measure of the sensitivity of the comparator, on another side it can be a measure of the sensitivity of the phototransistor. However, these effects could not be separated in our circuit. $E_{threshold}$ can be deduced by applying a pulse of light at different power levels (P_{light}) then by measuring the time needed to start the charge pumping pulses (t_{switch}). $E_{threshold}$ as a function of the irradiance is shown in figure 3.26. The dependence is almost linear with respect to light irradiance, except at very low power. The leakage taking place at the junctions, that can no longer be neglected, may be responsible for this deviation from linearity.

Another important parameter for any image sensor is the dynamic range, which is the maximum measurable incident light power divided by the sensitivity. Given that the sensitivity and maximum irradiance are dependent on the bias of the phototransistor, the dynamic range for weak and moderate inversion were measured for both pixel architectures the result of which is shown in table 3.2.

3.4.3 Comparison Sync-Async

1)**Ratio of surfaces** The main differences between the synchronous and asynchronous pixels are in the digital part architecture. The synchronous pixel has a synchronous D flip-flop not present in the asynchronous one. In our case, and because we used a $1\mu m$ SOI technology, the D flip-flop has an area of $68\mu m \times 44\mu m$ with respect to a total area of the synchronous pixel of $100 \times 100\mu m^2$. Then the ratio of the area of the asynchronous pixel to that of the synchronous pixel is of about 0.7. However, the shrinking technology mainly shrinks the digital but

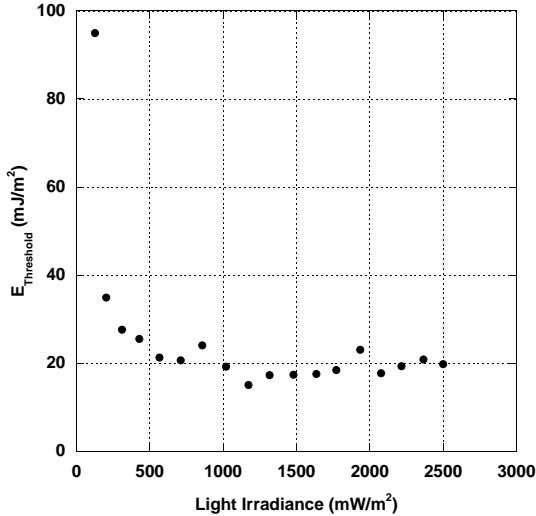


Figure 3.26 Measured energy needed to switch the comparator as a function of the incident light power

not the analog part, and thus this ratio will tend to 1.

2) **Complexity** The asynchronous circuit does not need any memory element in the pixel, thus reducing the complexity inside the pixel itself compared to the synchronous one. Because it does not need a clock signal (the phases are clocked by the charge pumping pulses) the matrix made up of asynchronous pixels has a simpler interconnects between the different pixels, (no clock signal is routed to all the pixels like it would be for the matrix made up of synchronous pixels.)

3) **Performances** Both circuits have a relatively good dynamic range when biased in moderate inversion, however their performances degrades when biased in weak inversion. This can be improved in the asynchronous circuit by adapting the bias current according to the incident light. So for low intensity light we would bias the phototransistor in moderate inversion. As the intensity of light increases we would then decrease the biasing current where the phototransistor can detect higher intensities of light. As for the sensitivity, both circuits have the same order of sensitivity. However, the asynchronous outperforms the synchronous pixel for the maximum intensity. It is mainly due to the fact that the synchronous circuit does not apply the charge pumping pulse instantaneously but rather waits for the right edge of the clock to enable the pulses. In contrast, the asynchronous circuit applies the decision of the comparator rather instantaneously on the enabling switches. For the same reason we find that the resolution of the asynchronous pixel is a

bit higher. Finally, it is worth noting that the above mentioned performances will be boosted once an optically optimized phototransistor is used.

3.4.4 Discussion

Using the floating body SOI MOSFET in a *standard* way (i.e. by measuring the change in the drain current) suffers from various drawbacks. Among them are the slow recovery time constant which is not very attractive for common image sensing applications and the relatively small photocurrent (in the order of pA). Taking advantage of the floating body SOI MOSFET where the device itself acts as analog adder, integrator and a digital to analog converter we can design a first order delta-sigma modulator by simply adding a current comparator to the system. The latter allows us to improve drastically the precision of the pixel reaching a measured SNR of about 50dB without additional signal processing of the input signal.

Moreover, since the output of the pixel is the output of the current comparator (figure 3.14), the circuit works also as an analog to digital converter, taking advantage of the first order delta-sigma modulator built around the floating body SOI MOSFET. Eliminating the need to add a column wise A/D converter, we reduced the overall power consumption of a matrix made up of the synchronous or asynchronous pixels.

In the previous section, we have seen that the pixel can be operated in both moderate and weak inversion. When high sensitivity is needed, the SOI phototransistor should be used in moderate inversion by using a reference current of $15\mu A$. Meanwhile, in our case, lower power consumptions can be achieved, when the SOI phototransistor is in weak inversion. This choice reduces the current consumption by at least a factor of 10. The bias current of the phototransistor is the major contributor to the power consumption of our pixel, neglecting both the dynamic and static power consumption of the digital part. The former can be neglected due to low switching frequency (typically 50KHz).

In the case of synchronous circuit, the DC current is flowing only half of the time during the reading phase (during the charge pumping phase the phototransistor is disconnected from the comparator). Using a 5V CMOS technology, the power consumption is then $37.5\mu W$ per pixel. If we assume a matrix of 1000×1000 pixels and the reading done one row at a time then the total power consumption is $37.5mW$ for the moderate inversion case and $2.5mW$ for the weak inversion case. The case of the asynchronous is even better, because the pixel is in the reading phase for less than half of the time. The matrix of pixels designed in [7] is a 90×90 pixel sensors (APS) consumes about 4.2mW while operating at

30 fps. Another solution with direct digital output from the pixel was proposed in [29] where the pixel has a DC current of $1.6\mu A$ which is comparable to the bias current we have in the weak inversion case.

In both proposed architecture, there is no need for a high precision current source. Actually, a drift in the reference current would only mean a change in the potential of the floating body of the SOI MOSFET; however, the relation between the light intensity and the PWM output of the current comparator will be unaffected.

It is worth mentioning, that the phototransistor used was not optimized for light sensing applications. The technology was optimized for mixed signals circuits. In [21] the measured optical efficiency was about 0.1% for the green LED. In addition, further improvements could be achieved by scaling down to smaller technologies, which reduces junction leakage and improves the fill factor without affecting the behavior of the phototransistor. If we compare the resolution of both pixel architectures to the theoretical ones, we find some reduced performances. This can have 2 possible origins:

The first one is leakage of stored charges from the body of the transistor through the junctions. This phenomenon becomes important especially at low light intensities (especially that the optical efficiency was computed to 0.1% [21]). To confirm this, we simulated an ideal first order sigma-delta modulator with no leakages in its integrator and we got what is shown in figure 3.27. Then, adding some leakage to its integrator led to a reduction of the SNR due to a raise in the noise floor. The higher the leakage, the higher the noise floor as shown in figure 3.27.

The second one is the noise due to the Poisson distribution of incident photons. The author in [45] showed that in order to have at least 40dB of SNR 10,000 electrons are needed to be stored. For light irradiance of $5mW/m^2$, we computed a quantity of about 1000 electrons per second stored in the body of the phototransistor. This would lead to a SNR lower than 40 dB. (One of the factors for which this quantity is low is due to the low optical efficiency (0.1% optical efficiency)). Even though the collected quantity of electrons is lower than 10,000 electrons (about 5500 electrons are needed to switch the comparator output state based on the measurements shown in figure 3.26), we still have an SNR which is higher than 40 dB. In fact, a repeated number of measurements (50 in our case) are needed to obtain a smooth looking power spectral density curve. This is equivalent to averaging the different measurements thus reducing the standard deviation of the photon noise by a factor of $\sqrt{50}$ yielding to an SNR of about 54 dB for the moderate inversion case. This could explain why in the measured PSDs the SNRs are actually better than 40 dB and in addition to that one can conclude that the major source of noise for such a system is indeed the photon shot noise.

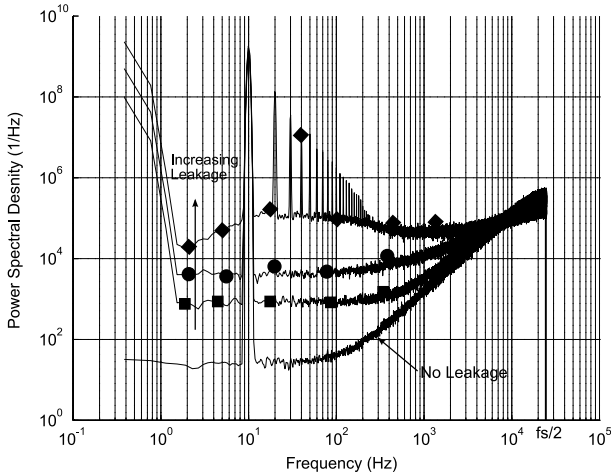


Figure 3.27 Simulation of the effect of leakage of an integrator on the Signal to Noise Ratio (SNR)

3.5 Improvements and Outlook

3.5.1 Leakage

In section 3.4.4 we have seen the effect of leakage in the integrator on the performance of the system. This leakage is due mainly to recombinations taking place in the floating body of the phototransistor. Solutions to such a problem can be on two levels, electrically or technologically.

Electrically. Keeping the potential of the body close to zero helps keeping the junctions in reverse bias and hence keeps the leakage to a minimum. To keep the potential of the body close to zero, one would need a sensitive current comparator. The latter would trigger the charge pumping pulses as early as possible before having a substantial rise in the body potential.

technologically. Even if the body potential is close to zero, recombinations would still take place. Using smaller technologies help reducing the leakage currents. In addition, technologies like the ones used for DRAMs, where the leakage is also a problem, could also be used to reduce the leakage.

3.5.2 Optical Efficiency

As stated in the section 3.4.4, the optical efficiency was about 0.1% which is relatively low. It is worth mentioning in here that no optical optimizations were applied on the phototransistors used in this work, like

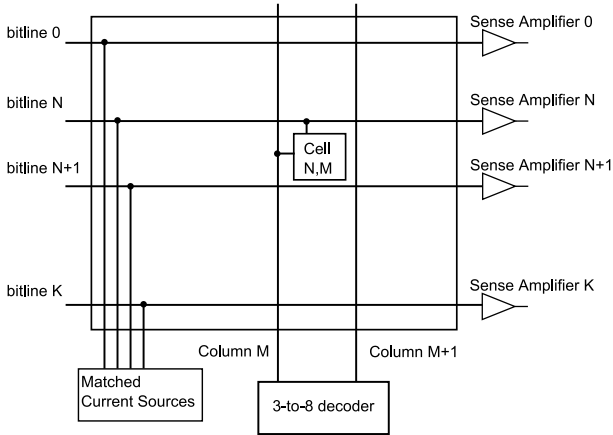


Figure 3.28 The matrix of the proposed pixel

microlenses and so on. One way to improve the collection of photons by the phototransistor, is to use back illumination after etching down to the BOX (Buried Oxide, which is transparent). The author in [56] have shown experimentally that there is at least a factor of 2 improvement compared to the frontal illumination. In his experiment the author in [56] had samples where the gate was of polysilicon. In contrast our samples have salicide gates, the salicide process involves the reaction of a thin metal film with silicon in the active regions of the device, ultimately forming a metal silicide contact through a series of annealing and/or etch processes. Therefore, we expect to have even better improvements on the efficiency compared to *top - side* illumination.

3.6 Matrix

The pixel architectures proposed in section 3.3 can be used to build up a matrix. We will restrict our study to an 8×8 pixel matrix. Figure 3.28 shows a schematic view of the matrix, a 3-to-8 decoder enables a column of pixels at a time, so the reading is done column wise. The current reference is a matched current source whose schematic is shown in figure 3.33, with a design done as is explained in [5]. The current source is shared per bitline, a voltage sense amplifier (figure 3.35) will buffer and amplify the voltage changes on each bitline. A layout of the proposed pixel is shown in appendix A with all relevant dimensions.

Read	Comparator Output	Switch Control
OFF	LOW	Enable Charge Pumping Voltage (V_{GCP})
OFF	HIGH	Enable Reading Gate Voltage (V_{GR})
ON	LOW	Enable Reading Gate Voltage (V_{GR})
ON	HIGH	Enable Reading Gate Voltage (V_{GR})

Table 3.5 Control logic for the switches that select the gate voltage of the phototransistor

3.6.1 Reading Algorithm

The reading algorithm for this matrix is a bit different from the random access readings of usual APS matrix. The reading is done column wise, that is the pixels in one column are selected by the 3-to-8 decoder which triggers the following actions on all pixels of the same column:

- Connect the phototransistor to the reference current source of the bitline
- The comparator makes the decision
- The decision is latched by a D flip-flop (in the case of the synchronous pixel only)
- Based on this decision, a 1 or a 0 logic is applied on the bitline which is connected to the input of the sense amplifier

The voltages V_{GCP} (the charge pumping pulse 3.12) and V_{GR} (the reading gate voltage) are distributed to all the cells of the matrix through a 2 line bus. Switches in each pixel control which of the two voltages is applied on the gate of the phototransistor. The control logic of these switches is summarized by table 3.5.

The first 2 entries in table 3.5 means that when a cell is not selected by the 3-to-8 decoder, either V_{GCP} or V_{GR} is applied on the gate based on the decision of the comparator. The last 2 entries means that the cell will be in a reading state and the V_{GR} is applied on the gate. Figure 3.29 shows the control logic and the corresponding gate voltage.

The waveform of the charge pumping pulses applied are shown in figure 3.30. During the reading phase all the columns are read and the decision of the comparator is made.

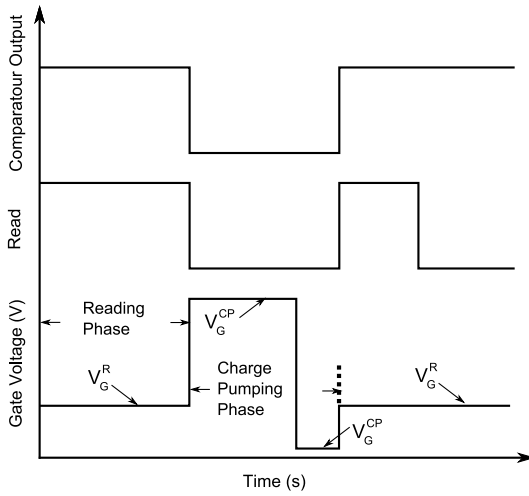


Figure 3.29 control logic and the corresponding gate voltage

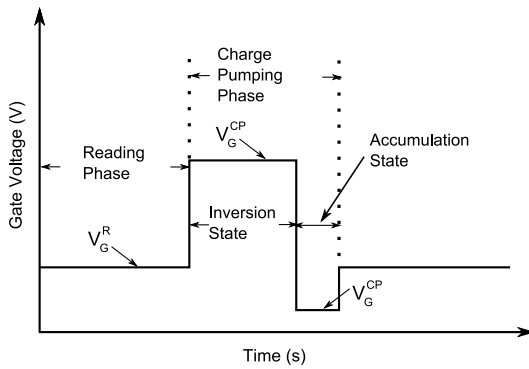


Figure 3.30 Waveform of the charge pumping pulses applied at the matrix cells

3.6.2 The Reference Current Source

We have seen in section 3.3.2 a pixel with a current source for the reference current and the phototransistor; however, this reference current can also be shared among different pixels provided they do not use it at the same time. This is the case as the reference current is only needed in the reading phase (section 3.3.2) while in the charge pumping phase the phototransistor is disconnected from the current source to minimize current consumption. Hence, and given the architecture we have adopted, only one pixel is in the reading phase on a given bitline. Therefore, it is possible to share this current source on the same bitline which greatly simplifies the architecture.

The matching of the current sources among all the cells is not crucial due to the delta sigma modulator that filters out this mismatching offset (this will be detailed in chapter 4); however, we have chosen to adapt a matched topology for extra immunity.

The bitline is connected to the output of the comparator whose potential is expected to swing between 0 and V_{dd} . At the same time the output of the current source is also connected to the bitline; therefore, the output of the current mirror would experience a large swing. Despite the large swing the current mirror should be able to copy the current from the current source to the bitline with the maximum fidelity. Moreover, the output impedance of this current source should be large in order to preserve the high gain of the cascode transistor (M2 in figure 3.33). One of the current mirrors architecture that best matches these specifications has been well studied in [5]. We will next see how this architecture fits our specifications and why a simple cascode current mirror (figure 3.32) would not fulfill all of the desired specifications for this application. I would like first to review how a simple current mirror works, then the cascode mirror will be studied.

Figure 3.31 shows a basic schematic view of a current mirror. The input current I_{bias} is injected into the drain of the diode connected transistor (M1). This transistor is always in saturation as its V_{ds} is always bigger than $(V_{gs} - V_T)/n$. The injected current will impose a gate voltage

$$V_{gs} = \sqrt{\frac{I_{bias} 2n}{\beta}} + V_{T0} \quad (3.20)$$

This gate voltage is copied to transistor M2, having the same gate voltage we expect to get $I_{out} = I_{bias}$. However, due to mismatches between the input voltage (V_{in}) and the output one (V_{out}) the current I_{out} is not exactly I_{in} . This error can be minimized if the transistors M1 and M2 were cascoded.

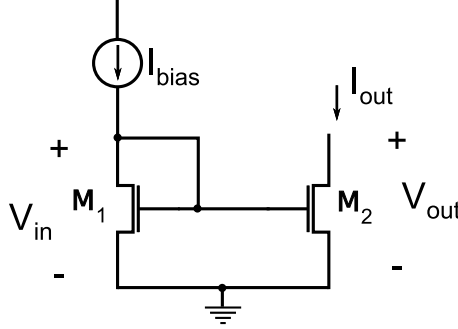


Figure 3.31 A simple current mirror

The simple cascode studied in [5] and shown in figure 3.32 was always biased in strong inversion and based on this the authors derived some conditions for the transistors dimensions and drawn some consequences. Essentially they showed that the output resistance of this cascode mirror decreased as we drive the transistor into deep strong inversion hence there should be a trade off as it is desirable to have a rather large output resistance. The trade off is done using the factor $N = \sqrt{A_C/A_M}$ where $A_C = \sqrt{W_3/L_3} = \sqrt{W_4/L_4}$ and $A_M = \sqrt{W_1/L_1} = \sqrt{W_2/L_2}$ which is inversely proportional to g_{m4}/g_{ds4} . Whereas the output resistance of this cascode mirror has the following form:

$$r_{out} = \frac{1}{g_{ds2}} \left(1 + \frac{g_{m4}}{g_{ds4}} \right) \approx \frac{1}{g_{ds2}} \frac{g_{m4}}{g_{ds4}} \quad (3.21)$$

while the overdrive of the gate voltage can be written as :

$$V_{gs1} - V_T = \frac{N}{1+N} (V_{BC} - V_T) \sqrt{\frac{I_{in}}{I_{in,max}}} \quad (3.22)$$

It would be more flexible to have the bias voltage V_{BC} increasing with the input current to guaranty that the transistors remain in strong inversion, because the output current of the current mirror will vary considerably. The latter condition is set by the tests we will do on the phototransistor in weak, moderate and strong inversion. Typically the weak inversion current of the phototransistor is about $1\mu A$. To have this functionality the author in [5] showed that the new circuit should respect the following relation derived from the condition that M1 transistor is in saturation.

$$V_{bc} = V_T + \frac{1+N}{N} \sqrt{\frac{2I_{in}}{KA_M}} \quad (3.23)$$

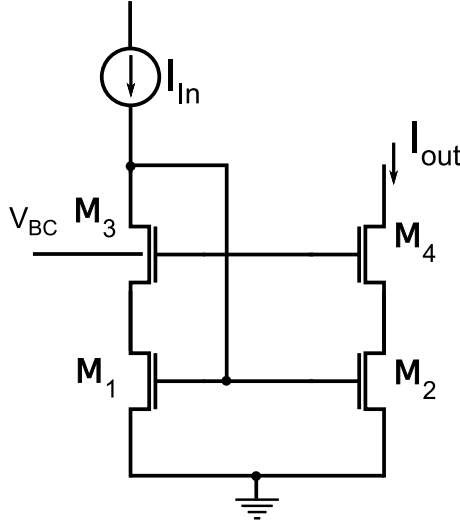


Figure 3.32 A simple cascode current mirror

where $K = \mu C_{ox}$ Equation 3.23 is satisfied by the schematic shown in figure 3.33. In this schematic transistor M7 is in saturation and hence its V_{ds} is as follows:

$$V_{ds7} = \sqrt{\frac{2I_{in}}{KA_B} \left(1 - \sqrt{\frac{A_B}{A_8}}\right)} \quad (3.24)$$

where $A_B^{-1} = A_7^{-1} + A_8^{-1}$
from equation 3.24 we find that equation 3.23 is fulfilled if

$$N = \sqrt{\frac{A_M}{A_B} - \sqrt{\frac{A_M}{A_8}}} \quad (3.25)$$

Also according to [5], to have the minimum input voltage (which is attractive for our application as the bitline swings between 0 and V_{dd}). it is advantageous to choose a large A_8 , we chose 16 in our case. $A_M = 3.65$ so $A_8 \approx 4A_M$ and $A_7 \approx A_M/2$. Having A_M , A_7 and A_8 from equation 3.25 we can find $N \approx 3$ and then $A_C \approx 10$

In terms of layout, the current mirror is made in one block, and the current is distributed to the different bitlines as is shown in figure 3.28. Although this might increase the parasitic capacitance of the bitline, this is more immune than distributing the gate voltages of the current mirrors should they be located nearest to the bitline. This is because the

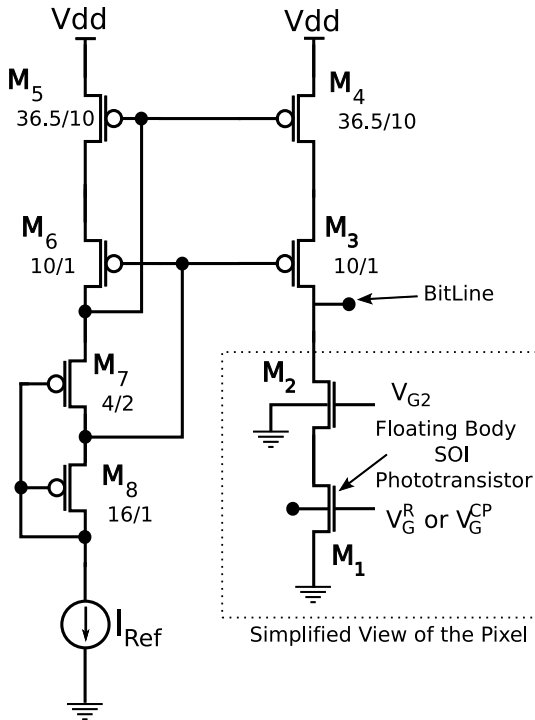


Figure 3.33 Schematic of the current reference used for the matrix

gate voltage drop among all the bitlines will be different creating more mismatches in the reference current.

3.6.3 Voltage Sense Amplifier

As we have seen in figure 3.28 the bitlines are long lines running from the cell toward one side of the matrix, those lines have large parasitic capacitances. This slows down the signal transition, a voltage sense amplifier detects the slightest change in the line and amplifies it speeding up the transition of the line. A sense amplifier is usually used especially for that purpose in DRAM, there are 2 kinds of sense amplifier: the voltage sense amplifier, which detects a variation in voltage. And a current sense amplifier which detects the variation of the current along the bitline. In our case and because the variation on the bitline is a voltage, we will use a voltage sense amplifier.

Sense amplifiers, are monostable circuits, just before the comparison they are brought and held into the unstable state (shown in figure 3.34)

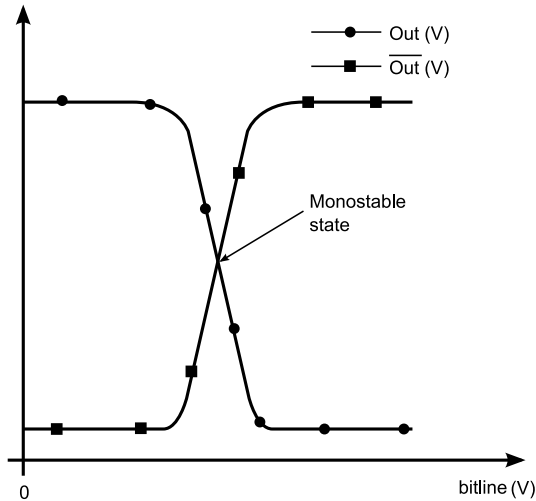


Figure 3.34 Sense amplifier output as a function of the input voltage at the bitline

and depending on the input on the bitline the output is allowed to move to one of two stable states. In figure 3.35, we show the voltage sense amplifier we have used in the matrix architecture. The En signal turns on the sense amplifier by turning on transistor M5. Transistor M6, when turned ON, brings and holds the output at an unstable state, when En goes low the output is allowed to change to the stable state which depends on the input voltage of the bitline. In order to create a bigger voltage gap between the differential input transistors M1 and M2, the input at M1 is inverted. Figure 3.36 shows a simulation of two possible scenarios (when the bitline goes high, or goes low).

3.7 Conclusion

A novel architecture of a pixel taking advantage of the physical properties of a floating body partially depleted SOI MOS was proposed. The device takes up the functions of an adder, integrator and a digital to analog converter in a delta sigma loop. The use of delta-sigma increases the resolution of the output signal to 7.5 bits which is otherwise unattainable due to the very low optical efficiency of the SOI phototransistor. The measurements done on the proposed pixels have shown that it was capable of detecting low intensities of light as low as $3mW/m^2$ with an acceptable dynamic range of about 60 dB. In addition to improved

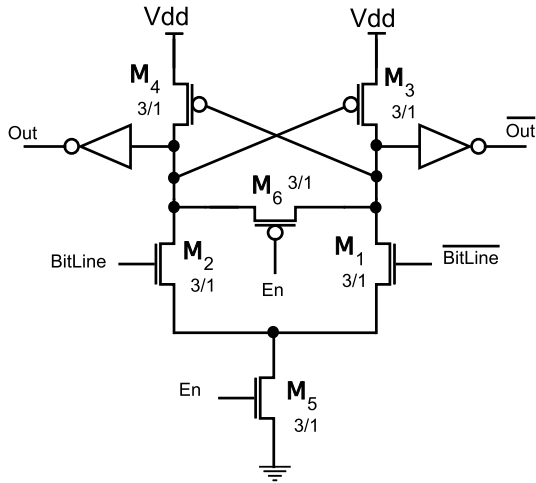


Figure 3.35 Voltage sense amplifier

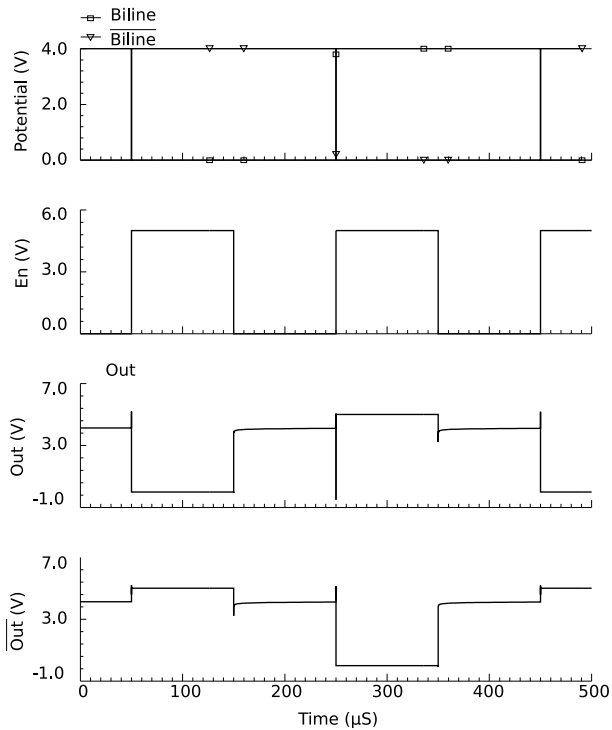


Figure 3.36 A simulation of the proposed voltage sense amplifier

resolution and high sensitivity, each pixel has a readily available digital output (PWM output of the current comparator) eliminating the need to add an ADC per column. This reduces the total power consumed by a matrix allowing it to be used in low power applications.

Noise Sources

4.1 Introduction

IN almost all of the electronic systems, noise with its different natures and sources define the limits of the system, like the sensitivity, dynamic range and other performance measures. In this chapter we will take a look at some of the noise sources to which the pixel or more specifically the current comparator branch is subject to (i.e. the transistors M1, M2 and M3 of the comparator branch in figure 4.1). In section 4.3, simulations of a first order delta-sigma modulator model with the different noise sources included will be shown. Section 4.4 will discuss the result of the simulation and will try to relate them to the measurements shown in section 3.4 of chapter 3.

4.2 All the Noise Sources

The noises of our current comparator branch can be divided into three groups, the reference current noises, the cascode noises and the phototransistor noises. In the following subsections we will show that the noises of the current reference are totally filtered out by the delta sigma loop. The noise sources of the cascode transistor (M2 in figure 4.1 are less important than those of the phototransistor itself due mainly to the high gain and this will be shown in section 4.2.2. On the other side, the phototransistor used in this work is a partially depleted SOI MOSFET. Therefore, one would expect to have flicker (also known as $1/f$) and white noise. Because it was used as a photosensitive device, noise related to generation and recombination in the floating body is

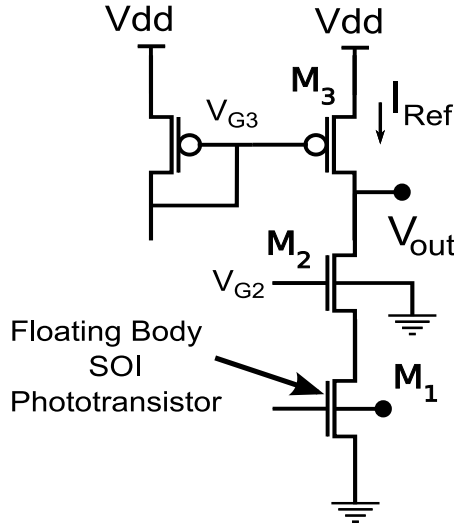


Figure 4.1 The comparator branch in both synchronous and asynchronous architecture

expected to be a noise source too. This kind of noise is also seen as the fluctuation of electron-hole pair generation due to light. Another noise related to light, or specifically to the Poisson distribution of photons will be more important as we intend to detect light intensities as low as $5mW/m^2$ (equivalent to about 5000 photogenerated electrons). An additional source of noise come into play in this work and it is charge pumping noise. Throughout this report we assumed that every pulse of charge pumping removes exactly the same amount of holes from the body; however, this is not exactly true as the number of traps at the Si/SiO_2 interface fluctuate in time (and space). In the following subsections we will detail about the sources and effect of each of these noises on the performance of our system.

The power spectral density of a current noise will be denoted by $S_i(f)$, this quantity has a unit of A^2/Hz . But we often use the square root of the power spectral density instead given in A/\sqrt{Hz} . For a noise voltage v_n , one can similarly define a power spectral density denoted by $S_v(f)$ having units in V^2/Hz or its square root power spectral density in V/\sqrt{Hz} .

4.2.1 White and Flicker Noise of the Reference Current

The noises generated by the reference current transistors (transistor M1 in figure 4.4) can be considered as noises acting on the linear

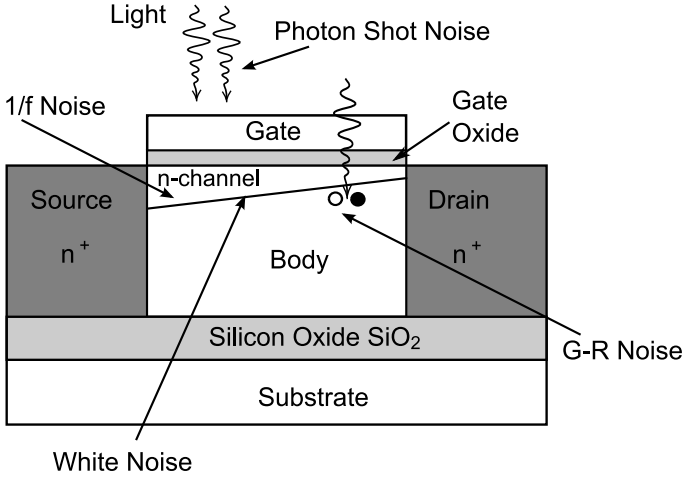


Figure 4.2 Sources of noise in an floating body SOI phototransistor

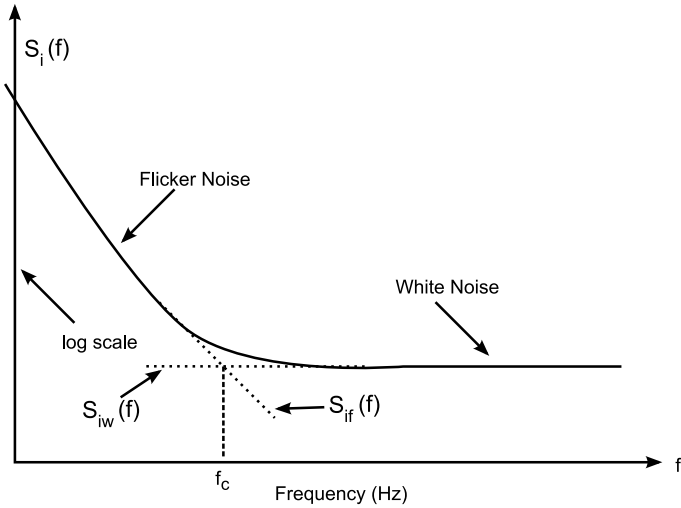


Figure 4.3 Typical plot of the drain-noise current power spectral density versus frequency

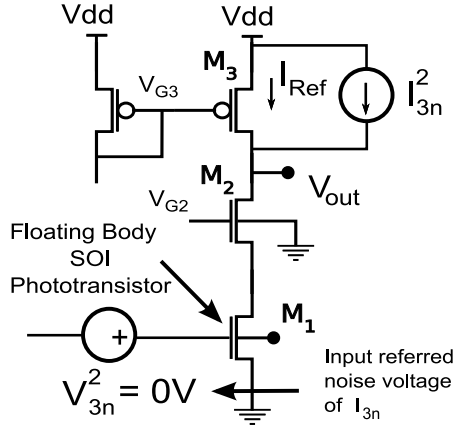


Figure 4.4 Noises generated at the current reference are filtered by the delta sigma modulator

quantizer of the delta-sigma. Therefore, all the noises coming from the reference transistors and even those in the band of interest, can be added to the quantization noise and together will be shaped by the delta-sigma loop. The shaping is of the first order, as the delta sigma system that we have is of the first order (only one integrator at the floating body SOI MOSFET). This makes the system even more reliable and robust to mismatches in the current reference in a matrix structure of the described pixel. This means that an offset in the current source will once again (we have also seen immunity of the system to such mismatches in section 3.3.2) be filtered out and hence does not deteriorate the performance of the overall matrix of pixels.

4.2.2 Cascode Noises

The noises generated at the cascode (M2 in figure 4.5) are not filtered by the delta sigma loop and they do appear as part of the signal; however, this noise gets attenuated by the large gain that is due to the cascode.

Taking the small signal of the circuit shown in figure 4.5 we can write at node V_d the following equation as the relation between the current in the cascode and the input voltage at the gate of the phototransistor:

$$g_{m1}V_{in} - V_d g_{ds1} + g_{m2}V_d = 0 \text{ with } i_2 = g_{m2}V_d \tag{4.1}$$

from equation 4.1 we can get the voltage noise source at the input

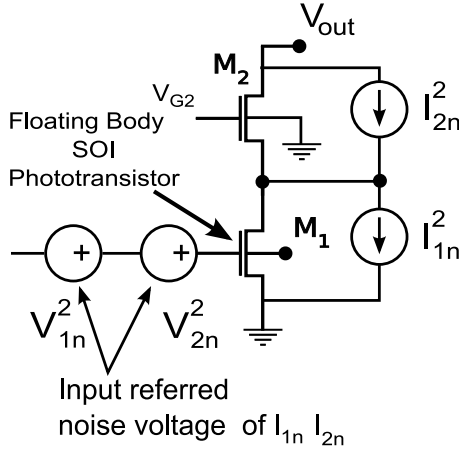


Figure 4.5 Noises generated at the cascode and the phototransistor

V_{2n}

$$\frac{V_{2n}^2}{i_{2n}^2} = \frac{1}{g_{m1}^2} \left[1 - \frac{g_{ds1}}{g_{m2}} \right]^2 \quad (4.2)$$

meanwhile the relation between the noise current source of the phototransistor and the input noise voltage is :

$$v_{1n}^2 = \frac{i_{1n}^2}{g_{m1}^2} \quad (4.3)$$

This confirms the need to concentrate on the different noises coming from the phototransistor itself as all of the noises are added to the signal and most of all they are in the same band as the signal, making them difficult to filter out by the delta sigma loop.

4.2.3 Flicker Noise

The flicker noise, also known as $1/f$ noise, is dominant in low frequencies as is shown in figure 4.2. It got its second name $1/f$ from the fact that its power spectral density is proportional to the inversion of the frequency. $1/f$ noise in MOS has been the subject of several studies presenting several theories for the origin (and sometimes conflicting) of this noise. In here we will present briefly the main conclusions of the two dominant theories.

The first theory attributes this noise to the random fluctuation of the number of carriers in the channel due to fluctuations in the surface potential. The fluctuations of the latter are caused by the traps at the Si/SiO_2

interface which traps and releases carriers randomly [1, 30, 26, 3]. From this theory the power spectral density of such a noise can be formulated as follows:

$$S_{vf}(f) = \frac{K_1}{C_{ox}^2} \frac{1}{WL} \frac{1}{f^c} \quad (4.4)$$

The exponent c is between 0.7 and 1.2 for an n-channel device. K_1 is independent of the bias but dependent on fabrication parameters. Lower values of K_1 are found in cleaner fabrication processing.

From equation 4.4 we can deduce the power spectral density of the drain current noise because the equivalent voltage noise appears in series with the gate of the MOSFET. Thus it is sufficient to multiply the voltage noise source by g_m to obtain the corresponding current noise.

$$S_{if}(f) = g_m^2 S_{vf}(f) \quad (4.5)$$

The second theory attributes the cause of $1/f$ noise to mobility fluctuations, due to carrier interactions with lattice fluctuations [49, 16, 51, 50]. Based on this theory it is suggested that the power spectral density for the equivalent input noise voltage is:

$$S_{vf}(f) = \frac{K(V_{GS})}{C_{ox}} \frac{1}{WL} \frac{1}{f} \quad (4.6)$$

The $1/f$ noise whose voltage spectral density is given by equation 4.4 (or equation 4.6), is generated at the phototransistor. So this noise can be an additional voltage at the gate of the noise free phototransistor. Note that the photogeneration taking place at the body of the phototransistor can also be simulated by a voltage source at the gate. Hence, for the simulation the $1/f$ noise should be added to the input signal. The $1/f$ noise, as shown in figure 4.3, is predominant at low frequencies and typically the signals that are inputted to our system are at low frequencies too. It is expected then to have the $1/f$ noise appearing at the output of the delta-sigma.

4.2.4 White Noise

The white noise in a MOSFET is actually thermal noise, this noise has been well studied for the MOS [38]. The most significant source is the noise generated in the channel. It was proved in [48] that for long channel MOSFETs operating in saturation, the channel noise can be modeled by a current source connected between the drain and the source as shown in figure 4.6, having a current spectral density as:

$$\bar{I}_n^2 = 4kT\gamma g_m \quad (4.7)$$

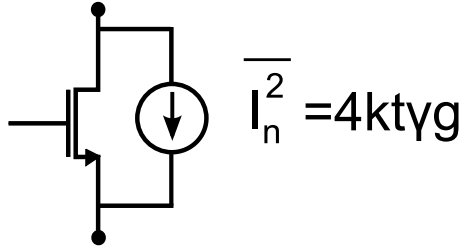


Figure 4.6 Thermal noise of a MOSFET

The coefficient γ has a value of $2/3$ for long channel MOSFETs. This kind of noise is predominant at higher frequencies where the contribution of the pink noise becomes negligible as is shown in figure 4.3. The frequency at which both are equal is called the corner frequency and is evaluated at:

$$f_c = \frac{K}{C_{ox}WL} \frac{3}{8KT} g_m \quad (4.8)$$

The white noise can also be modeled as a voltage noise source at the gate of the phototransistor and this noise source has the following form:

$$\overline{V_n^2} = \frac{4kT\gamma}{g_m} \quad (4.9)$$

It is expected to get the white noise of this phototransistor at the output of the delta-sigma loop as it is also present at the input in the same band as the flicker noise and the signal. Because the flicker and the white noise are in the band of the signal they will not be filtered out by the delta-sigma loop; therefore, one has to reduce them on the input side that is on the phototransistor. Increasing the width of the phototransistor reduces both noises and improves the fill factor as well.

4.2.5 Charge Pumping Noise

The charge pumping noise is due to the fact that the number of traps at the Si/SiO_2 is fluctuating. It is known that this fluctuation may also be the cause of the flicker noise. Some also argue ([1, 30, 26, 3]) that the noise due to charges being trapped and released from the traps at the Si/SiO_2 interface have a dependence of the form:

$$S_i(f) \propto \frac{1}{f^\alpha} \quad (4.10)$$

Where α is a factor varying from 0.7 to 1.5. [54]

The charge pumping noise, because it affects the number of charges it removes from the body, can be considered as if coming with the input signal of the system. Moreover, and because it is very much related to the same physical phenomena that causes $1/f$ noise we will later on simulate it as a $1/f$ noise.

4.2.6 Photon Shot Noise

This kind of noise occurs when the number of photons is small enough to give rise to statistical fluctuations in measurements. To give a numerical example, an intensity of light of $5mW/m^2$ is equivalent to 1 million photons on average, however due to low optical efficiency of our samples only 1000 of them would reach the thin Si film and would create on average 1000 electron-hole pairs. The photon noise will approach a normal distribution for a large number of photons as they have a Poisson distribution. The standard deviation of the photon noise is \sqrt{N} , where N is the average number of photons collected. correspondingly the signal to noise ration (SNR) of the signal of light having on average N photons will be $SNR = \sqrt{N}$. As the number of collected electrons gets large so does the SNR of such a signal. From the measurement results shown in figure 3.26 shown in chapter 3 one can deduce the average number of electrons that were photogenerated leading to a switch in the output state of the comparator causing few charge pumping pulses to be applied on the gate of the phototransistor. This energy gives an average number of 5500 electrons, this means that the SNR is about 43 dB.

4.3 Noise Simulations

For the purpose of simulation, a Matlab code was used to describe a first order single bit delta sigma modulator. The input signal is a sine wave with frequency of 10Hz. The noise sources described in section 4.2 were added one at a time to the signal. In order to reduce the standard deviation of the FFT of the output signal, we repeated the simulation for 50 times and averaged the FFT.

4.3.1 Current Reference Noise Sources Simulation Results

As mentioned in section 4.2.1, the noises generated at the current source reference are filtered out by the delta sigma modulator, because these noises add up to the quantization noise. The latter is naturally shaped by the modulator and pushed to higher frequency, outside the

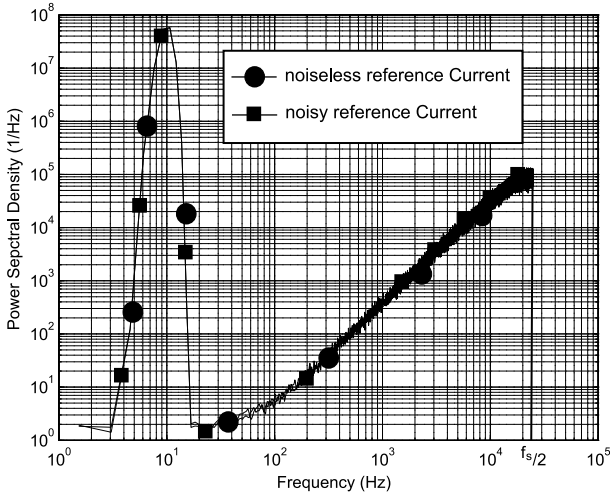


Figure 4.7 Current source noises totally filtered by the delta sigma modulator

band of interest. A simulation of a noise free quantizer in a delta sigma modulator along with a quantizer which reference is fluctuating due to a white and a flicker noise are shown in figure 4.7. The performance, and especially the signal to noise ratio of the system did not degrade.

4.3.2 Phototransistor Flicker Noise Simulation Results

Now that we have shown that the noises at reference current and the cascode are of little importance we will show hereafter the simulation results of the different noise sources on the output of the delta sigma modulator. In this section, we have added the $1/f$ noise to the 10Hz sine wave input. One can see from the graph in figure 4.8 that the output stream of 1's and 0's has also the $1/f$ noise. Therefore, to suppress the $1/f$ noise one should not count on the delta sigma loop, for this other solutions should be studied.

4.3.3 Phototransistor White Noise Simulation Results

White noise is characterized by the fact that it is present at all frequencies and among them the band of interest of our signal which is for this simulation at 10Hz. We added to the noiseless sine wave a white noise and we simulated the delta sigma modulator. As we can see in figure 4.9 the white noise raises the floor noise of the output effectively reducing the SNR of the system. The purpose of this simulation is only qualitative as we do not have the MOSFET's noise parameters; however,

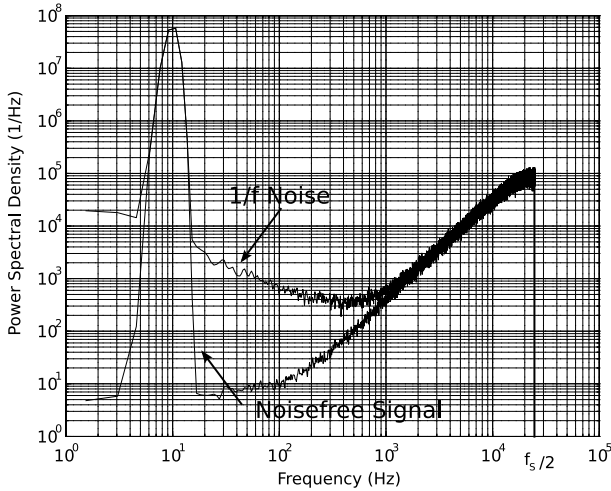


Figure 4.8 Flicker noise at the phototransistor is not filtered by the delta sigma modulator

this shows clearly that the delta sigma modulator cannot filter out the phototransistor white noise.

4.3.4 Charge Pumping Noise Simulation Results

As was stated in section 4.2.5 the charge pumping noise is similar to $1/f$ noise, hence we will use the $1/f$ noise source used for the flicker noise. Even though this noise is generated at the feedback loop of the delta sigma modulator it will be added as is with no attenuation at the input signal (and being in the band of the signal it will not be filtered out). Unfortunately, we do not have any data concerning the noise level of this phenomena. Therefore, the simulation of this noise will only be qualitative, showing the behavior of the delta-sigma modulator when a $1/f$ noise is present at its input.

4.3.5 Photon Shot Noise Simulation Results

This type of noise becomes important when the intensity of light measured is very low, which is the case in our pixel. This noise can be added to the signal as a white noise having a normal distribution with average the number of electrons (N) we need to switch the output state of the comparator and a standard deviation of \sqrt{N} . Then we re-simulate the delta sigma modulator and as was expected this noise do not get filtered by the as it is in the band of the signal. However, if we repeat the same measurement 50 times the standard deviation of the

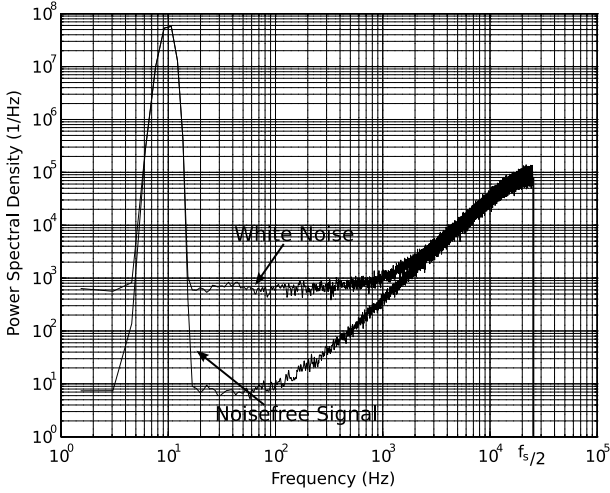


Figure 4.9 Thermal noise of the phototransistor is not filtered by the delta sigma modulator

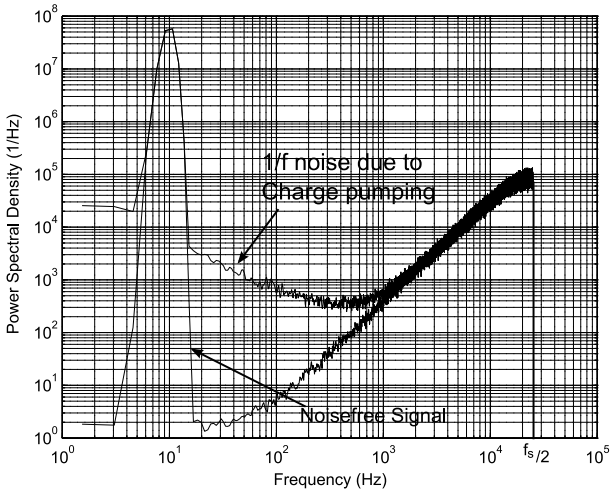


Figure 4.10 Charge pumping noise of the phototransistor is not filtered by the delta sigma modulator

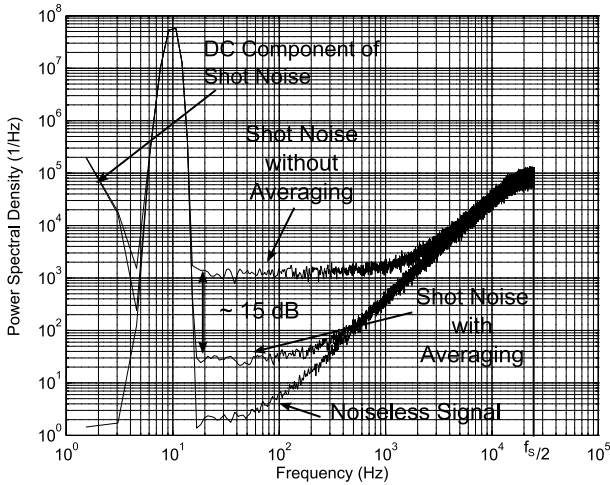


Figure 4.11 Photon shot noise is not filtered by the delta sigma modulator

shot noise is reduced by a factor of $\sqrt{50}$ thus improving by 15dB the SNR of the output signal.

4.4 Discussion

We have seen qualitatively the behavior of the pixel under different noise sources to which it might be subjected to, we can divide them into two groups: those that can be filtered by the delta sigma modulator and those that cannot. It is important to know that having a first order delta sigma modulator reduces the number of noise sources with which one has to deal with.

4.4.1 Noises Filtered by the Delta Sigma Modulator

The noises that can be filtered by the delta sigma modulator are essentially the noises coming from the current reference circuitry as those are assimilated to quantization noise. Therefore, there is no need to worry about the noises coming from this circuit. In addition to that, in a matrix structure, the offset existing between different current references for different pixels can be considered as a flicker noise. This means that this offset will be pushed to higher frequencies outside the band of interest, hence with this architecture we were able to suppress a fixed pattern noise, the offset in the current reference.

4.4.2 Unfiltered Noises

The noises that do not get filtered are mainly those generated in the phototransistor or those that are due to the low light intensity. Therefore, one needs to find a way to minimize their effect mainly by sizing the phototransistor accordingly or using repeated measurements for the shot noise.

As we can see from the measurements (figure 3.24) the major contributor to the noise in the band of interest is mainly the flicker noise which shows more of $1/f^2$ trend. Unfortunately we do not know the origins of this noise, i.e. we do not know if this is the charge pumping noise having the $1/f$ noise or the flicker noise of the phototransistor itself. For this it would have been useful to measure the $1/f$ noise level of the phototransistor in dark and with no charge pumping pulses applied. Especially that for the technology used the noise parameters are supplied by the foundry. Now if we suppose that the flicker noise is that of the phototransistor, in order to minimize it, it would be judicious to make the phototransistor area as big as possible. This solution is in harmony with the objective of having a high fill factor for the pixel.

As for the photon shot noise, one is tempted to increase the sensitivity of the phototransistor; however, even if we increase the sensitivity the number of electrons in the body of the phototransistor responsible for changing the comparator output state would be unchanged. Therefore, it would be more suitable to do repeated measurement and then average them. In order to be able to repeat measurements it would be necessary to have an even higher sampling frequency.

4.5 Conclusion

In this chapter we have seen the noise sources that come into play in the proposed architecture. We have also seen that some of the noise sources do not contribute to the noise at the output of the circuit, the noises of the current reference for instance. Meanwhile, the noises that are generated at the phototransistor level are not filtered by the delta sigma modulator and hence one has to deal with them at the design level, like using a large area for the phototransistor to reduce its $1/f$ noise.

Conclusion

5.1 Thesis Outlook

THIS thesis work have presented a new technique to quantify the irradiance of the incident light on a partially depleted SOI phototransistor.

This new technique improves considerably the sensitivity of such a phototransistor, allowing it to detect low light intensities ($2mW/m^2$). With such intensities the lower bound is now set by the photon shot noise. Furthermore, the floating body is maintained at zero volt, avoiding therefore the slow transients of the floating body phototransistor.

With such a technique, a delta sigma modulator can be built around the phototransistor in order to improve the resolution and filter out the quantization noise of the 1-bit current comparator. Therefore the delta sigma loop allows us to use a minimum number of transistor for the current comparator.

On the other hand, some capabilities of the floating body SOI MOSFET could be put in use. For instance, the charge retention and integration, or charge elimination through charge pumping also to minimize on the number of transistors used and hence maximize the fill factor. The noise study of the proposed pixels showed immunity to some of the major sources of noise both temporal and spacial. The latter is useful for building a matrix of the proposed pixels. This is why we were able to propose an architecture of a matrix as well as a reading algorithm for the matrix where the pixel was the core of the matrix cells.

Based on the same technique developed for a floating body SOI MOSFET, the same measuring technique was shown to be applicable to a bulk CMOS phototransistor. The device structures were proposed and the behavior of such a system was explained.

5.2 Main Contributions

The Main contributions of this work can be summarized as follows:

- The development of a novel technique of light intensity measurements allowing high sensitivity ($2mW/m^2$ with the device, the circuit reached $5mW/m^2$) with unoptimized phototransistor.
- The provision of the essential physical background to efficiently use this technique.
- The design and implementation of two pixel architectures that implements in SOI the proposed technique, and implements elegantly a delta sigma modulator.
- The study of all noise elements that would limit the performance of the proposed pixels .
- The development of a matrix architecture and its corresponding reading algorithm, although it has not yet been tested to provide its performance.
- The extension of the technique for bulk transistor and proposed a phototransistor topology that could be a valid candidate.

5.3 Future Work

Although we did a big step in developping and implementing the readout technique and also in proposing a matrix architecture, a lot can still be done.

Even though we proposed a matrix, unfortunately we were unable to measure it before handing in this report. We have 2 matrices of 8×8 pixels each, one having the synchronous pixel as basic cell and the other has the asynchronous one.

The noise study made in this work lack the measurement of the noise of the phototransistor. This step is needed because the foundry did not provide the values of any of the noise parameters. With the noise measurements we will be able to identify if the $1/f$ noise appearing in the output signal is due to the flicker noise of the phototransistor or the charge pumping noise or both.

In this work we proposed to use large phototransistor to minimize the flicker noise effect; however, this is not the only way to reduce this kind of noise. In *standard* APS we use what is called correlated double sampling (CDS), although this technique cannot be directly applied in our

case, we believe, that something similar to correlated double sampling could improve this noise figure.

Also in this work, we prepared the bulk phototransistor topologies and measured them, the results are encouraging as they show the same behaviour as their SOI MOSFET counterpart. The next step would be to propose the pixel that implements the readout technique. Then do all the study that was done for its SOI counterpart, like the noise study to determine the limiting noise figures. Afterwards, propose a matrix of this pixel. Although competition will be tough in bulk technologies, we believe the performances of this technique applied to the proposed bulk phototransistor will be quite competitive.

Appendix

A.1 Matrix Layout

The photo shown in figure A.1 is that of a matrix of synchronous pixel. The technology used have a $1\mu m$ of minimum channel length, three metal layers and one polysilicon layer. The phototransistor has the dimensions of $1\mu m$ by $100\mu m$ and the total area of pixel (phototransistor, the logic and the current comparator) is $100 \times 100\mu m^2$. The area of the digital part account for 75% of the total area. The pitch between the pixels is $135\mu m$. It is worth noting that this matrix layout was designed to show the feasibility of the matrix using the proposed pixel, and hence the optimization of the design parameters of the matrix were not our goal.

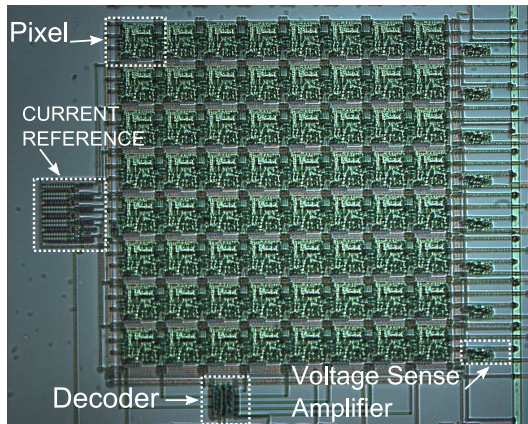


Figure A.1 Layout of the matrix of the synchronous pixel

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Publications

Journal

Published in The Journal of Solid-State Electronics:

"High Sensitivity PD SOI MOSFET Phototransistor Using Transient Charge Pumping."

L. Harik, J-M. Sallese and M. Kayal.

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"SOI Pixel Based on a Floating Body Partially Depleted MOSFET in a Delta-Sigma Loop."

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"Floating N-Well Photo-MOSFET Using Transient Charge Pumping."

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EuroSensors XXIII 2009:(Submitted for review)

"Noise Study for an SOI Digital Pixel Sensor."
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