Resistless ion implantation of sub-µm scale features through nano-stencil

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The fabrication of micro and nano devices using standard processing techniques is mainly based on the pattern transfer of designs onto a substrate. These standard techniques use pre-patterned resists that selectively expose certain parts of the substrate either to a material deposition or implantation or to an etching process. The use of resist processes implies the coating, exposure, development and removal of the resist and also imposes certain restrictions regarding the materials and substrates to pattern. In this contribution we demonstrate the use of silicon nitride membranes with apertures as shadow masks for localized ion implantation of silicon dopant impurities. This technique has been already used to perform projection ion beam lithography [1], where sub-micrometric resolution has been achieved. In our case, we use standard ion implantation equipment in order to demonstrate this resist-less process that, in addition to provide a high resolution, can allow processes that otherwise would not be possible, such as implanting pre-patterned substrates with high steps or fragile membranes.

For this work, chip-size (1x1 cm2) stencils have been used. The membranes were made out of silicon nitride (500 nm in thickness). The dimensions of the different apertures in the membranes were ranging between 600 nm and several tens of microns. The fabrication of the stencil chips is a well established process described elsewhere [2]. The chips were gently placed on the wafers to be implanted and a standard implantation of phosphorus (E = 100 keV, Dose = $2 \cdot 10^{15}$ cm^{-2}) was performed (Fig. 1). The energy of the implantation must be chosen consequently with the thickness of the membrane, being the latter larger than the penetration depth during implantation. After lifting the stencils off the substrate, an oxidation followed by an annealing was performed (10 min @ 850ºC in O_2 + 30 min @ 1000ºC in N_2).

Inspection with SEM and AFM of the implanted substrate shows an apparent loss of dimensions of around 300 nm (Fig. 2), which is much smaller than what could be expected, given the fact that the diffusion length for the given annealing conditions is of the order of 1 µm. The smallest replicated features are dots of around 900 nm in diameter (Fig. 2.c). The electrical behaviour of the implanted wells has been tested, obtaining a good behaviour as resistances (Fig. 3) and also as diodes (Fig. 4).

The presented technique proposes a new concept for the fabrication of electronic devices, given that now a complete resistless fabrication process could be performed to obtain features and devices in the sub-micrometric regime.

[1] P. E. Mauger, A. R. Shimkunas, J. C. Wolfe, S. Sen, H. Loschner, G. Stengl; Journal of Vacuum Science & Technology B (1992)
[2] G.M. Kim, M.A.F. van den Boogaart, J. Brugger; Microelectronic Engineering (2003)

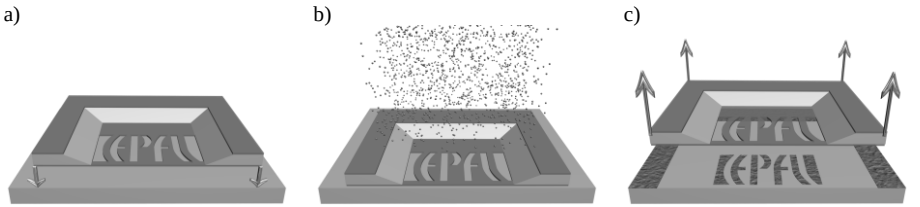

Figure 1. Schematics of the process. (a) A chip with structured membranes (silicon nitride membranes with apertures) is placed on a substrate (p-type Si wafer). (b) Ion implantation of phosphorus ions is performed. (c) The chip is lifted revealing the implanted zone.

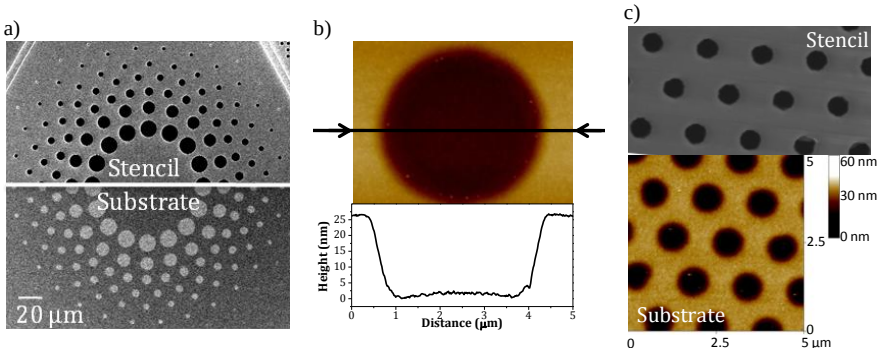

Figure 2. a) SEM micrographs of a stencil (top) and the correspondent substrate after implantation and annealing. b) Topography AFM image of a 3 µm diameter circle implanted in the silicon. The profile is showing a step of around 25 nm that corresponds mainly to the Si consumption during impurities activation and oxidation, and subsequent oxide etching. c) SEM micrograph of nano-stencil and topography AFM picture of the corresponding patterns. The loss of dimensions (around 300 nm) is in this case (600 nm holes in the stencil) more significant than for the micrometrics apertures.

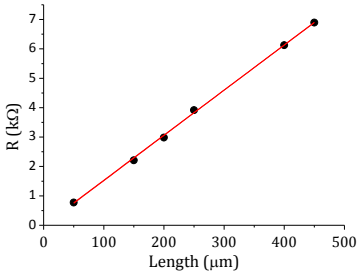

Figure 3. Resistance of doped silicon wires as a function of length, showing high linearity.

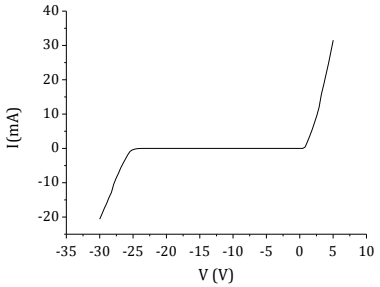

Figure 4. I-V curve of a several diode-like structures fabricated by implanting through stencil.