Optimization of amorphous silicon thin film solar cells for flexible photovoltaics

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We investigate amorphous silicon (*a*-Si:H) thin film solar cells in the *n-i-p* or substrate configuration that allows the use of nontransparent and flexible substrates such as metal or plastic foils such as polyethylene-naphtalate (PEN). A substrate texture is used to scatter the light at each interface, which increases the light trapping in the active layer. In the first part, we investigate the relationship between the substrate morphology and the short circuit current, which can be increased by 20% compared to the case of flat substrate. In the second part, we investigate cell designs that avoid open-circuit voltage (V_{oc}) and fill factor (FF) losses that are often observed on textured substrates. We introduce an amorphous silicon carbide *n*-layer (*n*-SiC), a buffer layer at the n/i interface, and show that the new cell design yields high V_{oc} and FF on both flat and textured substrates. Furthermore, we investigate the relation between voids or nanocrack formations in the intrinsic layer and the textured substrate. It reveals that the initial growth of the amorphous layer is affected by the doped layer which itself is influenced by the textured substrate. Finally, the beneficial effect of our optical and electrical findings is used to fabricate *a*-Si:H solar cell on PEN substrate with an initial efficiency of 8.8% for an *i*-layer thickness of 270 nm. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2938839]

I. INTRODUCTION

The fabrication of thin film silicon solar cells in the *n-i-p* (nip) configuration allows the use of nontransparent substrates such as plastic sheets or metallic foils. This strategy is used in production by different companies such as Fuji Electric,[1] Canon,[2] and Unisolar.[3] All of these have reported high initial efficiency on cells and module level, between 13% and 15% for cells, by using multijunction devices with layers deposited at elevated temperature (250–350 °C) on polyimide sheets or metallic foils. Here, the final goal of our investigations is to master the deposition of high efficiency devices with low temperature processes, i.e., below 200 °C, on polyethylene-naphtalate (PEN) or polyethylene-teraphtalate (PET) substrates with a textured surface. A similar approach is also followed by AIST (Ref. 4) and Utrecht University[5] but with *p-i-n* (pin) configuration. The major strengths of PEN or PET sheets are the cost per square meter, lower than iron free glass, the possibility to use roll-to-roll processes which allows the deposition of hundreds of meters of solar cells in one run,[6] and finally the light weight, reduced fragility, and flexibility of the modules which reduce the storage and transportation costs. Additionally, by combining *a*-Si:H with microcrystalline silicon in a tandem micromorph configuration, significant increases in efficiency are possible. Roll-to-roll processing of thin film silicon is, hence, a technology that is ideal for companies that seek to be a cost leader in the future photovoltaic market.

This paper discusses one way to lower further the cost of thin film amorphous silicon solar cells (*a*-Si:H) on PEN substrate by increasing their stabilized efficiency. This can be achieved with the introduction of textured substrates which enhance the light trapping in the cell and by developing tandem structures.[6–8] It was already shown that the current density (J_{sc}) can be increased on textured plastic substrates,[6] but this increase was accompanied by a reduction of open-circuit voltage (V_{oc}) and fill factor (FF). Indeed, the interaction between substrate morphology and plasma enhanced chemical vapor deposition (PECVD) growth of thin films is critical for most *a*-Si:H and μc-Si:H solar cells, and first hints toward a better understanding have been given only recently.[9,10] Indeed, the optimum structure for nip solar cell, taking into account the needs for a strong light trapping and a suitable growth of the nip devices, is not yet known. The first part of the paper will focus on the relation between the surface morphology of the substrate and the J_{sc} in the nip cells. For this study, we develop textured zinc oxide (ZnO) back reflectors, where the roughness (size) and the morphology (shape) can be adjusted independently with the deposition time[11] and a plasma surface treatment,[10] respectively. In the second part of the paper, the study concentrates on the cell design in order to increase open-circuit voltage (V_{oc}) and FF on textured substrate. In the nip configuration, the *n* layer is the first deposited layer and therefore influences the growth of the subsequent layers. Microcrystalline *n*-layer (*n*-μc) is a good candidate because the layer can be doped efficiently and it has a low absorption coefficient, but its growth is also strongly influenced by the substrate material.[12] Here, we report on a strong dependence of the *n*-μc on the substrate morphologies. In pin solar cell, Pellaton-Vaucher[13] suggested that amorphous *n* layer is robust, in other words the deposition parameters have only small influences on the electrical characteristics of the layer. We apply this concept to the nip

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configuration by introducing an amorphous carbide layer (*n*-SiC) which is robust with respect to the deposition parameters and to the substrate morphologies. Furthermore, the addition of carbon increases the gap and gives higher V_{oc} than amorphous Si (Ref. 14) and microcrystalline Si layers without carbon. Furthermore, we describe how the benefits of the *n*-SiC layer can be used fully in the solar cell. We propose a surface treatment to enhance the transparent conductive oxide (TCO)/*n*-SiC contact and the introduction of a buffer layer to reduce the band discontinuities between the intrinsic and the *n*-SiC layer. Finally, by applying the benefits of our findings, we show that a flexible *a*-Si:H solar cell on PEN substrates with initial efficiency with 8.8% can be achieved. The low absorber layer thickness of 270 nm in this device guarantees reduced losses due to light induced degradation.[15]

II. EXPERIMENTAL

We develop processes compatible with plastics such as PEN and PET. Light trapping is achieved by replication of a texture onto the plastic substrate, as described by Bailat *et al.*,[6] or can be given by the deposition of a rough TCO directly on plastic or on glass for development purposes. The flat and textured plastic substrates are coated with Cr–Ag–ZnO stacks deposited by a roll-to-roll process in a large area multisource sputtering system at the Fraunofer Institute für Elektronenstrahl und Plasmatechnik (FEP), Dresden.[16] For reference purposes and for cells development, we also use glass substrates (Schott AF 45) coated with Cr–Ag–ZnO deposited with our in-house sputtering system. The silver can be deposited at room temperature. In this case the surface of the layer is flat. When deposited at high temperature (hot silver), the partial crystallization of the layer results in a rough surface. The chromium is an adhesion layer, the silver serves as back reflector and electrical contact for the solar cell, and finally the ZnO protects the silicon layer from diffusion of metallic atoms in the active layers, and it enhances the optical matching of the back reflector.[17] Additionally, we develop new back reflectors, for which flat silver on glass or on PEN is coated with a rough low pressure CVD (LP-CVD)-ZnO followed by a plasma surface treatment similar to that described by Bailat *et al.*[10] The silicon films are deposited by plasma enhanced chemical vapor deposition (PECVD) at very high excitation frequency (VHF, 50–150 MHz) on PEN or glass substrates with opaque reflector. The gases used for the deposition are silane (SiH_4), hydrogen (H_2), methane (CH_4), phosphine (PH_3), and trimethylboron for the *n* and *p* doped layers. In order to keep the process fully compatible with plastic substrates, the deposition temperature is kept below 200 °C. This limits the possibility to change the gap of the intrinsic layer. Nevertheless, the gap can still be influenced with the dilution ratio ($[H_2]/[SiH_4]$).[18] In the following, the dilution of the *a*-Si:H intrinsic layer equals 2, except when something else is specified.

As transparent front contact, boron doped zinc oxide (ZnO) is deposited by LP-CVD-ZnO.[11] It consists of ZnO deposited under conditions which result in a textured surface with a root mean square (rms) roughness of about 70 nm for a "standard" 2 μm thick layer.

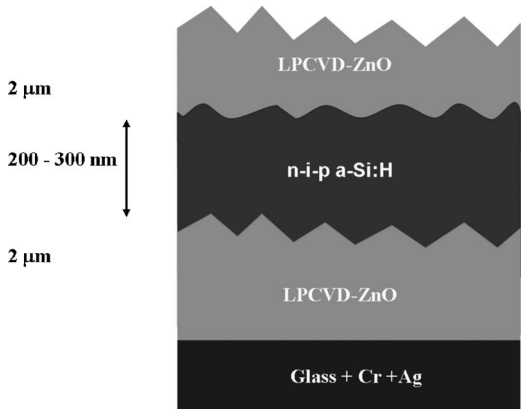

FIG. 1. Structure of the nip solar cell on glass substrate.

V_{oc} and FF are obtained from current-voltage (*IV*) measurements performed at 25 °C under AM1.5 solar spectrum with a dual-lamp solar simulator (Wacom WXS-140S-10). The external quantum efficiency (EQE) curve is given at short circuit condition except when something else is specified. The current density (J_{sc}) is calculated from the EQE by convolution with the AM 1.5 solar spectrum and by integrating over the wavelength range of 350–800 nm. This method avoids uncertainties in the determination of the solar cell surface area, which is typically 0.25 cm^2. The cell is completely isolated (front TCO and Si layers etched), and the measurements are performed without encapsulation, antireflection coating, or silver grid on top of the front TCO. Finally, we measure the rms roughness of the different substrates with an atomic force microscope (Burleigh, Vista-100). Focused ion beam is used for the preparation of cross-sectional samples for transmission electron microscopy (TEM), using the procedure described elsewhere.[9]

III. RESULTS

A. Substrates

In the first part of the paper, we investigate the effect of the surface structure on the nip cell properties. We work on LP-CVD-ZnO substrates which allow us to vary independently the dimensions and the shapes of the surface texture: The surface of LP-CVD-ZnO consists of pyramidal structures whose size varies with the deposition time.[11] A subsequent surface treatment is used to change the morphology.[10] Therefore, two degrees of freedom are available to investigate light trapping in *a*-Si:H solar cells.

For the development, the design of the solar cell is kept as simple as possible. The structure, Fig. 1, consists of glass/Cr/Ag/LP-CVD-ZnO/μc *n*-layer/*a*-Si:H/μc *p*-layer/LP-CVD-ZnO. The whole cell thickness is below 300 nm, and here the dilution of the intrinsic layer is 6. Figure 2 shows the results of a series where the feature size of the substrate has been varied. It plots the current density at a reverse bias of −1 V for wavelengths between 550 and 800 nm as a function of the rms roughness for the different sub-

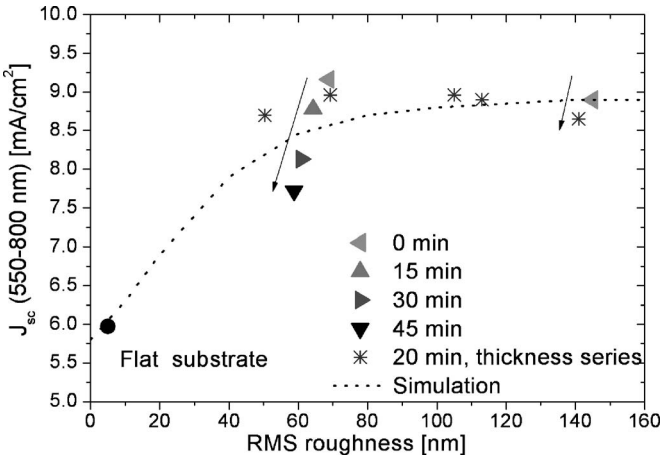

FIG. 2. Current density (at −1 V) between 550 and 800 nm of the *n-i-p a*-Si:H solar cell on ZnO-LP-CVD/flat Ag substrates with different surface features, shapes, and sizes. The stars indicate substrates with different ZnO grain sizes and with a standard plasma treatment of 20 min. The dashed line represents simulations obtained with SUNSHINE. The left oriented triangles are untreated substrates and the up, right, and down triangles are treated with 15, 30, and 45 min, respectively. A point for a flat substrate is added for reference (circle).

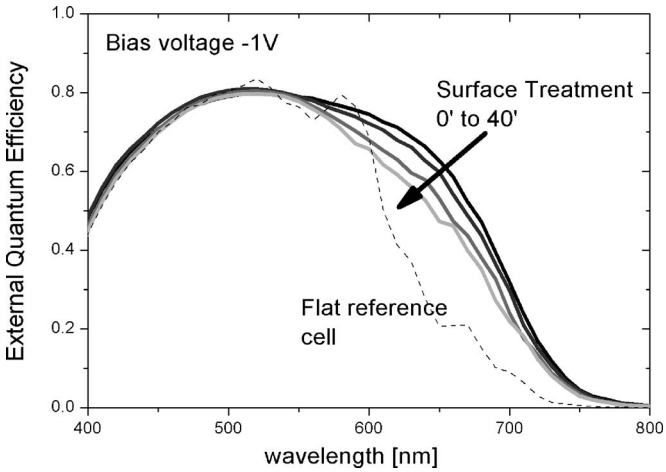

FIG. 3. EQE for different back reflector structures after different times of surface treatment (solid line, black to light gray for increasing treatment time) of the ZnO LP-CVD and a flat reference (dashed line).

strates. Choosing this particular wavelength range better emphasizes the light scattering effect in the solar cell, and the reverse bias ensures collection of all photogenerated charge carriers independent of the actual cell performance. The figure shows little variation of the current in the rms range from 50 to 140 nm. This saturation behavior is also found by simulation by using the modeling software SUNSHINE (University of Ljubljana[19]). The software implements a semiempirical model based on the scalar scattering theory and allows the simulation of multilayer system with various roughnesses and scattering capabilities of each interface. However, the trend of the simulation still indicates a slight increase in current with increasing rms over 100 nm, whereas the experimental thickness series shows a small diminution of current with increasing rms over 100 nm. We observe that there is an optimum for the light scattering which is around 70 nm corresponding to lateral dimension of 360 nm, but the simulation does not reproduce this result. We think that the simple linear increase in haze with rms in the semiempirical theory overestimates the amount of light scattering in this case.

Figure 3 shows the EQE at −1 V of cells starting from the same LP-CVD-ZnO substrates, but with different treatment times. In this series, the collected current is reduced from 13.9 to 12.6 mA/cm^2. Figure 3 shows that the current loss is due to reduced collection in the wavelength range from 550 to 800 nm which depends strongly on the light scattering properties of the substrate. Table I summarizes the solar cell parameters V_{oc}, FF, J_{sc}, and the efficiencies of the series in treatment time. The table shows that the treatment slightly reduces the rms roughness from 69 to 59 nm. This suggests that for a given size of the ZnO texture, the treatment modifies the morphology of the substrate rather than the height of the pyramids. The details of the morphological changes have been studied by Bailat *et al.*[10] for the case of microcrystalline solar cells in pin configuration. It was observed that the plasma treatment transforms the valleys between the pyramids from a V shape to a U shape, as schematically illustrated in Fig. 4. The reduced light trapping in the cells on treated substrates is not desired because of its lower current density, but we find that the treatment dramatically improves V_{oc} and FF, resulting in improved efficiencies of the cells. Table I shows that the V_{oc} difference between the cells on standard flat substrate and on nontreated substrate amounts to 178 mV. These results show that the shape of the substrate can lead, similarly to the case of the pin μc-Si cells, to dramatic changes of the cell electrical characteristics. From the balance between optical gain (V shape) and reduction of V_{oc} and FF losses (U-shape), the optimum substrate is found to be the most treated one. Note in Fig. 2 that the morphology changes of the substrate have a much stronger impact on the light scattering in the solar cell than the rms or feature sizes of the substrate.

B. *n* layer

In the second part of the experimental section, we evaluate the influence of the *n*-layer on the V_{oc}. The state-of-the-art nip solar cells are usually prepared with a *n*-μc layer deposited directly onto the substrate, as it is the case for the cells presented in Sec. III A. This configuration can give good results on flat substrate thanks to the high doping efficiency of microcrystalline layers and the low absorption of the microcrystalline material. However, we observe that the *n*-μc layers can have different properties depending both on the substrate texture and on the material. This effect can be seen in Table I, it shows that the plasma treatment increases strongly the V_{oc} and decreases the difference in carrier collection (EQE at 0 and −1 V). The TEM micrographs, Fig. 5–7, show that the texture of the substrate can influence the growth of the silicon layer. All these micrographs are obtained on cells with a *n*-μc layer. The flat substrate image, Fig. 5, shows a uniform and homogenous deposition of the *n*, *i*, and *p* layers. Figures 6 and 7 reveal the appearance of voids and nanocracks in the layers grown on the textured substrates. Two effects are visible, the first is the porosity of

TABLE I. Solar cell parameters for different back reflectors.

Plasma treatment [min]	0′	15′	30′	45′	Flat
Efficiency	5.4	6.6	7.1	7.2	6.6
V_{oc}(mV)	710	772	821	846	888
FF (%)	59	66	69	69	67
J_{sc}(mA/cm^2)	13.0	13.0	12.6	12.3	11.0
J_{sc}(−1 V)(mA/cm^2)	13.9	13.7	13.1	12.6	11.1
rms (nm)	69	64	61	59	

n-μc layer and the second is the apparition of voids and nanocracks in the Si. Figure 6 shows the appearance of a defective region starting in the valley of the LP-CVD ZnO and propagating through the entire intrinsic layer. In Fig. 7, the micrograph represents a zoom of the n/i interface in a μc-Si:H solar cell on a textured substrate. We clearly see the appearance of voids in the *n* layer. The valley of the pyramids is also a start of defective region in the microcrystalline material. In order to ameliorate the problems related to the defective material in the microcrystalline *n*-layer, we develop an amorphous *n*-layer with the addition of methane (*n*-SiC). It was shown by Hamakawa[14] that the carbon in the *n* layer increases the V_{oc} and the efficiency of the *a*-Si:H solar cell. Our *n*-SiC has a high optical band gap of 2.4 eV, determined with the Tauc plot method.[20] At room temperature, the dark conductivity of the *n*-SiC layer is 2×10^{-5} $(\Omega\ \mathrm{cm})^{-1}$ which is similar to the value given by Hamakawa *et al.*[14] The activation energy is 388 meV. Figure 8 compares the V_{oc} of nip solar cells with microcrystalline and carbide *n*-layers deposited on the rough LP-CVD ZnOs, with all the other parameters kept constant. The trend lines show that the decrease in V_{oc} from strongly treated to untreated substrate is less pronounced for the carbide *n*-layers (full lines) than for microcrystalline *n*-layers (dashed line). In the case of the untreated substrate, which yield the highest current, the increase in V_{oc} with the *n*-SiC layer is more than 170 mV (882 against 710 mV for the *n*-μc layer). Even for the fully treated substrate, the *n*-SiC layer gives a better V_{oc} (900 mV) than microcrystalline layer (878 mV) does.

C. Interface treatment

The benefit in V_{oc} of the *n*-SiC is now clear, but the potential of that doped layer is only fulfilled if a low contact resistivity between the ZnO and the *n*-SiC is achieved. In Fig. 9, the *IV* curve of the cell with the *n*-SiC (dashed black line) shows a strong serial resistance which lowers the FF to 59%. To overcome the contact resistance problem, we introduce an interface treatment between the ZnO substrate and the *n*-SiC. This is carried out with plasma conditions close to the deposition of microcrystalline *n* doped layer, but the deposition time is kept below or close to the incubation time. In Fig. 9, the *IV* curve compares a cell with and without the treatment. The absolute 6% gains in FF demonstrate the improved contact resistance between ZnO and *n*-SiC layer. This procedure is capable of improving the contact resistance, either by applying it for a short time which is effectively a treatment or by applying it for an extended time which actually results in the growth a microcrystalline layer without amorphous nucleation phase. The treatment is preferred because it diminishes the optical losses.

D. Buffer layer at *n*/*i* interface

In this section, we discuss the introduction of 20 nm thick buffer layer in order to enhance the interface between the *n*-SiC and the intrinsic layers. The buffer layer is deposited with a dilution ratio of 9 which has two effects. It increases the band gap of *a*-Si:H, which should act as a graded interface between the *i*-layer and the *n*-SiC layer, and reduces the density of defects at the n/i interface.[18,21,22] Figure 10 shows the efficiencies of the cell with and without buffer layer for different surface treatment times on the ZnO LP-CVD. Table II gives the solar cell characteristics for a 12 min surface treatment applied on the substrate. The gain due to

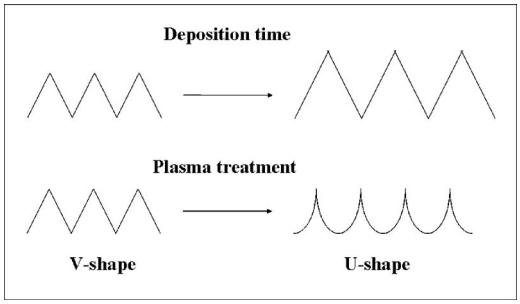

FIG. 4. Substrate morphology changes from small to big pyramids with deposition time, and from V-shape to U-shape with the surface treatment.

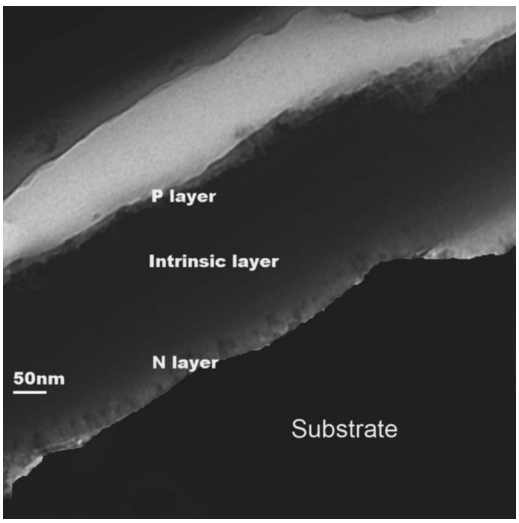

FIG. 5. Cross-sectional TEM micrograph of *a*-Si:H solar cell on a flat substrate. The substrate has been shaded for the sake of clarity.

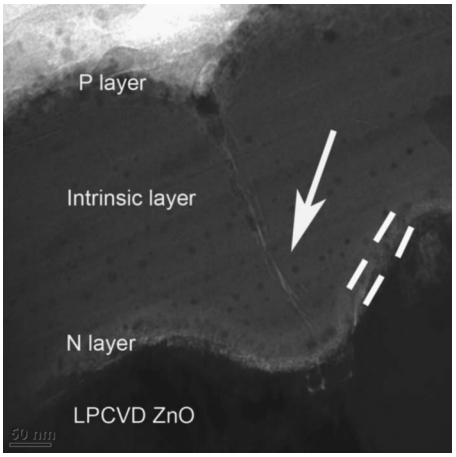

FIG. 6. Cross-sectional TEM micrograph of *a*-Si:H solar on rough LP-CVD ZnO.

the buffer layer is mostly in FF (63.4%⇒67.6%) and slightly in V_{oc} (885 mV⇒895 mV). The buffer layer at the n/i interface increases by 9% the relative efficiency of the cell (8.0%⇒8.7%). The *IV* curve in Fig. 11 does not tell if the gain in FF is a collection improvement close to the maximum power point or a reduction of shunt or series resistance. The distinction between these effects is possible with the variable illumination measurements.[23] Table III indicates that the difference in FF loss between the cells is mainly due to series resistance. In fact, the impact on the FF due to shunt resistance (R_{sh}) is negligible for both cells because a R_{sh} as high as 1.7×10^5 Ω cm^2 has no impact on the FF of an *a*-Si:H solar cell. The collection voltage (V_{coll}) is similar for both cells (12.5 compared to 13) and thus has the same FF impact. However, the series resistance (R_s) differs significantly, 5.3 versus 7.8 Ω cm^2. Merten *et al.*[24] defined the R_s under 3 suns illumination as follows:

$$R_s = \left.\frac{dV}{dJ}\right|_{J=0}.$$

The evaluation then implies FF reductions, from the ideal case of 75%, of 8.0% and 11.7%, respectively. The difference of 3.7% (11.7%–8.0%) explains almost completely the

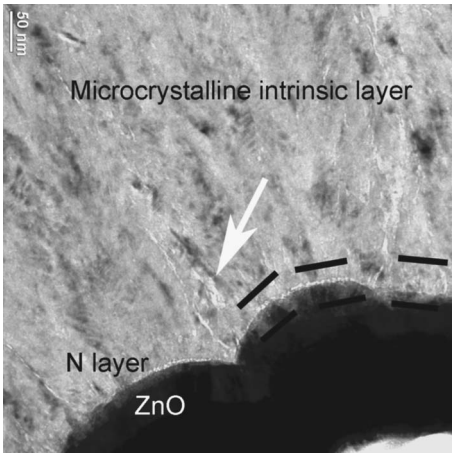

FIG. 7. Cross-sectional TEM micrograph of a μc-Si:H cell on textured substrate coated with 80 nm of sputtered ZnO.

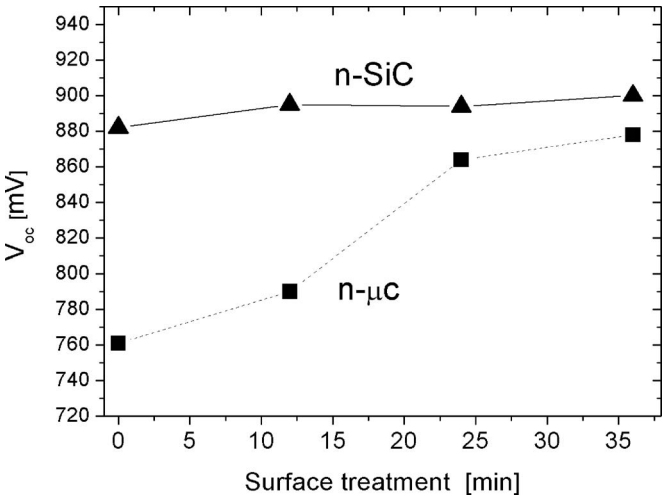

FIG. 8. Open-circuit voltage (V_{oc}) comparison of nip cells with a microcrystalline *n*-μc (dashed line) and an amorphous *n*-SiC layer (full line). The substrate is a rough LP-CVD ZnO/flat Ag deposited on glass, with different surface treatment times.

observed value of 4.2% (67.6%–63.4%) FF deviation between the two solar cells in Table III. Nevertheless, further optimization of the devices is required with the *n*-SiC layer. Indeed, in our laboratory R_s values around 2–3 Ω cm^2 are routinely achieved for pin *a*-Si:H solar cells on highly textured substrates.

E. Amorphous solar cell

Here, we apply the findings of the previous sections to flexible solar cells where the glass substrate has been replaced by PEN. We compare a flat PEN+silver+70 nm ZnO and a flat PEN+silver+textured LP-CVD ZnO as back reflectors, see Fig. 12. The EQEs are shown in Fig. 13 where a glass hot silver+70 nm sputtered ZnO has been added for reference. The results of Table IV show a relative increase of 20%–25% in efficiency on the rough substrates compared to the flat substrate. An initial 8.8% efficiency for an *a*-Si:H cell on plastic substrate is obtained.

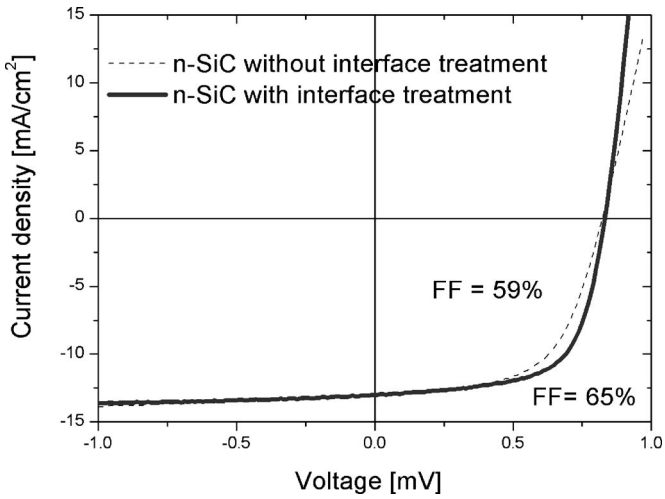

FIG. 9. Comparison of the *IV* curves of *a*-Si:H solar cell with (plain curve) and without (dashed curve) an interface treatment at the ZnO/*n*-SiC interface.

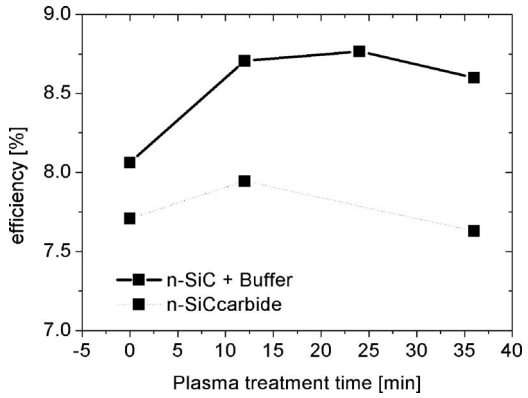

FIG. 10. Efficiencies of *a*-Si:H solar cell with and without buffer layer at the *n*/*i* interface.

TABLE II. Solar cell parameters with and without buffer layer at *n*/*i* interface for a 12′ surface treatment applied to the LP-CVD ZnO substrate.

Buffer layer	Yes	No
Efficiency (%)	8.7	8.0
V_{oc}(mV) (mV)	895	885
FF (%)	67.6	63.4
Current (mA/cm^2)	14.4	14.2

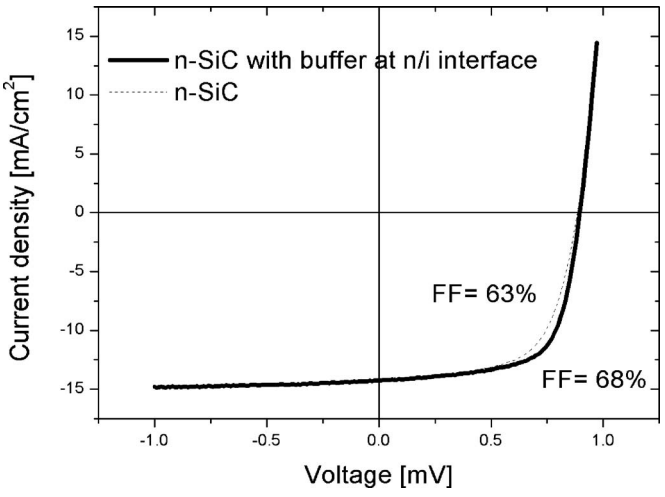

FIG. 11. *IV* curve of *a*-Si:H solar cells with (plain curve) and without (dashed curve) buffer layer at the *n*/*i* interface.

TABLE III. Parameters determined from the variable illumination measurements on cells without and with buffer layer.

Buffer layer	Yes	No
V_{coll}(V)	12.5	13.0
R_{sh}(kΩ cm^2)	170	1580
R_s(Ω cm^2)	5.3	7.8

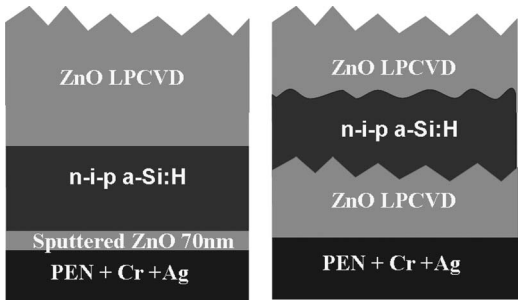

FIG. 12. Structure of the nip solar cell on plastic with a flat (left) and rough (right) back reflectors.

IV. DISCUSSION

The development of the nip solar cell on our back reflector consisting of flat Ag and LP-CVD ZnO gives valuable insight into the effect of the substrate texture on optical and electrical properties of nip solar cells. This substrate reduces texture mediated plasmon absorption[25–27] in the metallic back reflector and thus diminishes the optical losses, but thanks to the LP-CVD ZnO, it supplies a sufficient amount of roughness for light trapping in the absorber. Similarly, it has been reported in a pin solar cell[28] that the configuration with a smoothed metallic back reflector has optical advantages compared to rough back reflector. Nevertheless, for an industrial application the goal is to have a texture embossed in the PEN, then deposition of silver and also a thin 70 nm ZnO as the back reflector. Indeed, previous work[6] has shown that high current in *a*-Si:H cell is also achievable in such configuration. In a preliminary study, we also find that thin Ag/ZnO back reflector on textured substrate can yield high current, and, in addition, we are able to improve the electrical parameters compared to Bailat *et al.*[6] We achieve initial efficiency of 8.1% with 14.5 mA/cm^2, 871 mV, and 64% of FF on plastic substrate with a thin Ag/ZnO back reflector. However, when varying the thin back reflector, we find that we are more sensitive to plasmon effect, and that the cell result depends strongly on the thin layer thicknesses and properties.

Our results show that, even for simple single-junction

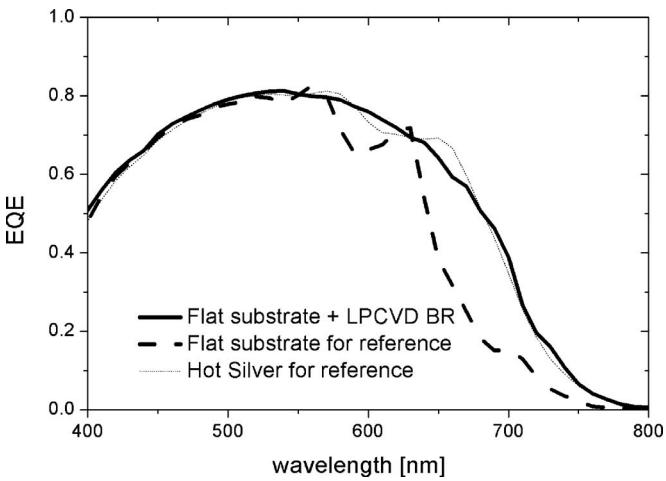

FIG. 13. EQE of the *a*-Si:H on flat substrate with LP CVD back reflector and LPCVD ZnO front contact.

TABLE IV. *a*-Si:H solar cell parameters for different back reflectors: ZnO LP-CVD, flat PEN, and a glass hot silver with LP-CVD front TCO.

Back reflector	ZnO LP-CVD	Flat	Hot silver
J_{sc}(mA/cm^2)	14.3	12.3	14.2
V_{oc}(mV)	888	895	915
FF (%)	70	66	69
Efficiency (%)	8.8	7.3	9.0

a-Si:H devices, a complex interplay between substrate morphology, chemistry, and subsequent *n*-layer takes place. It has been shown in the past that thin microcrystalline layers are sensible to the substrate material,[12] and we clearly find that it is also sensitive to the morphology of the substrate (Table I and Figs. 6 and 8). We think that the sensitivity of the *n*-μc layer comes from growth competition between adjacent grains. The valley of the sharp V-shape textured of LP-CVD ZnO results in a defective material which increases the defect density at the *n*/*i* interface and results in the formation of voids and cracks in the amorphous material, as shown in the TEM micrographs and reported elsewhere.[26,29,30] For pin μc-Si cells, Python *et al.*[9] reported in detail how these defective regions affect the performance of the solar cell. Presumably, the presence of two different kinds of electronic defects is favored by the *n*-μc layer. First the porosity of the defective areas at the *n*-*i* interface results in the creation of additional dangling bonds which increases the interface recombination center density. Second, the cracks or voids initiated in the μc-Si layer are contamination routes for dopant and/or impurities atom, which can be incorporated in the active layer. In contrast, we see that on a flat or smooth substrate high V_{oc} of 890 mV can be achieved, and the micrograph on the flat substrate shows a uniform deposition without voids in the *n*-μc and in the subsequent layers.

Our solution to avoid V_{oc} losses on textured substrates which are compulsory for light trapping is to utilize an amorphous *n*-SiC layer which is clearly less sensitive to the substrate morphology and material. Furthermore, the *n*-SiC layer achieves very good results on textured substrate. We demonstrate that high V_{oc}, over 900 mV, can be achieved with a low dilution intrinsic layer ($[H_2]/[SiH_4]=2$). In pin solar cell, Poissant[31] has compared *n*-μc and amorphous *n*-layers in single-junction *a*-Si:H solar cells. They reported significantly smaller activation energy for *n*-μc compared to amorphous *n* layer but a similar potential in the *a*-Si:H solar cell. Here, we report that the amorphous *n*-SiC layer can have advantages compared to fully carbon-free and microcrystalline doped layer. The gap of the microcrystalline material is assumed to be 1.1 eV, and it has low activation energy of about 0.02 eV. The carbide *n* layer has a larger gap, 2.4 eV, and higher activation energy of 0.39 eV. The higher gap can diminish optical losses in the doped layer and the band alignment can be favorable for the V_{oc}, as illustrated in Fig. 14. In this figure, we assume for *n*-μc similar band discontinuities as reported in Ref. 31, and for the *n*-SiC, we suppose that they are distributed between the valence and the conduction band, but it is so far not possible to distinguish to which

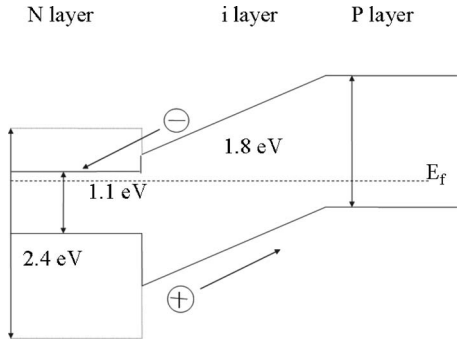

FIG. 14. Band diagram of a nip solar cell with *n*-SiC (dashed lines) and microcrystalline *n* layer (plain lines).

extent. This creates a barrier for the holes and the electrons in the valence and conduction bands, respectively. We suggest that the blocking barrier in the valence band repels the holes from the defective interface area and reduces retrodiffusion of the holes in the doped *n*-layer. Hence, the *n*-SiC layer enhances the collection of the charge carriers.

The limitation of a quality thin film silicon solar cell is often driven by the quality and structures of its interfaces. Here, the efficiency of the nip solar cell is clearly enhanced by a buffer layer at the *n*/*i* interface, from 7.9% to 8.8%. The buffer layer is highly diluted with H_2 which promotes a better quality and a higher band gap material.[18,21,22] In Sec. III D, we demonstrated that the buffer layer improves slightly the V_{oc} and reduces mainly the series resistance of the *a*-Si:H solar cell and thus improves the FF of the *a*-Si:H solar cell. We suppose that the higher gap buffer layer reduces the band discontinuity in the conduction band, which was previously mentioned, and thus enhances the collection of the electrons close to the *n*/*i* interface. In Fig. 15, we represent the band diagram of the nip stack with *n*-SiC layer. We include (dashed line) the effect of the buffer layer with a higher band gap; the effect is exaggerated for the sake of clarity. Based on previous work on the *p*/*i* interfaces,[32–34] we assume that the increased buffer band gap is reported in the conduction band. The buffer layer reduces the barrier for the electrons and thus reduces the series resistance of the cell, which is observed experimentally in Sec. III D. A similar buffer layer at the *n*/*i* interface has been studied in the pin case by Sakai *et al.*[32] but without significant improvements. The discrepancy between their and our observations could be explained because they use a carbon-free amorphous *n* layer,

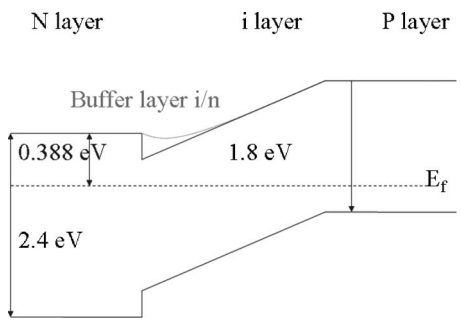

FIG. 15. Band diagrams of a nip solar cell with (full lines) and without a highly diluted buffer layer (dashed line).

and thus no barrier was created at the n/i interface. Furthermore, from a comparison to the results of Tawada *et al.*[35] for a *n*-SiC, it appears that our *n*-SiC layer can be doped more efficiently. This will result in a lower activation energy (300 meV) and a superior conductivity $[10^{-3}\ (\Omega\ \mathrm{cm})^{-1}]$. In addition their gap is about 0.1–0.2 eV lower which could deteriorate part of the benefits of the *n*-SiC layer.

The contact between the carbide *n*-SiC layer and the ZnO potentially introduces a high series resistance in the solar cell. A solution already exists for the pin case[36] where the best contact with the ZnO/TCO is accomplished with a microcrystalline *n* doped layer. We show that the microcrystalline *n* treatment provides a good contact in the nip configuration. We think that the treatment can improve the contact resistance by changing the chemical properties of ZnO surface, but no actual deposition of a microcrystalline silicon layer is needed to improve the contact resistance. Furthermore, it demonstrates that very thin n-μc treatment can be applied directly on the ZnO without deteriorating its properties, and it achieves good contact between ZnO and *n*-SiC layer. The drawback of this double *n* layer (n-μc+*n*-SiC) is the optical loss due to the increased thicknesses of the total doped layer. This has only minor consequences. First of all because the n-μc layer is thin, the deposition time is kept below or close to incubation time. Second, the absorption coefficient of a microcrystalline layer is small for the light that reaches the layer, at wavelengths between 550 and 800 nm. In addition, the higher gap of the *n*-SiC layer limits the losses in the doped layer.

V. CONCLUSION

In this paper, we report on the achievement of simultaneously high J_{sc} and V_{oc} on textured substrates and the optimization of nip *a*-Si:H solar cell on flexible substrate. We find optimum substrate morphology for light trapping and develop a cell design that simultaneously maintains good V_{oc} and FF. The benefits of an amorphous carbide *n* layer are fully implemented in the *a*-Si:H solar cell on PEN substrate with the demonstration of an initial 8.8% efficiency, for an intrinsic layer thickness of 270 nm.

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