Micro Photovoltaic Modules for Micro Systems

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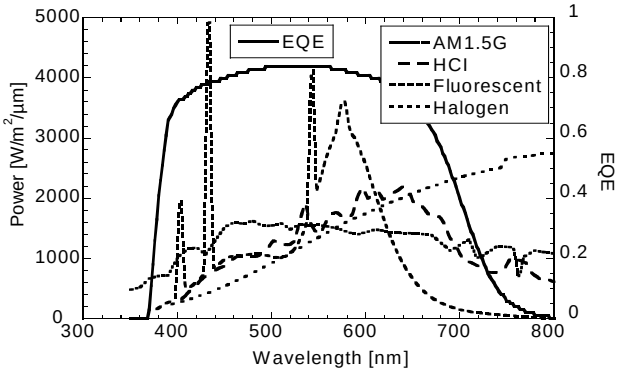
ABSTRACT

Amorphous silicon based solar modules are very attractive for the powering of various microsystems for both indoor and outdoor applications. This technology offers a lot of flexibility in terms of module design, output voltage, shape, size, choice of substrates and offers also the possibility to embed sensors such as photodiodes. This paper focuses on the development of micro-solar modules with area $\leq$0.15 cm^2. Several micro-modules with output voltage of up to 180 V (for a total area of 0.1 cm^2) were designed and fabricated. The performance limitation introduced by the segment monolithic interconnection and the design of the latter is presented and discussed. An example of a micro-module with a total size of 3.9x3.9 mm^2 developed for a micro-robot with dual voltage outputs and embedded photodiodes is also presented.

INTRODUCTION

Development of various types of Microsystems (e.g. autonomous micro-systems, sensor networks, micro-robots, etc) requires the parallel development of energy scavenging solutions. Given the energy consumption of most devices, the use of photovoltaic module is a valuable option for many applications [1]. In this context, amorphous silicon (a-Si:H) solar cell technology using micro-fabrication processes offers several advantages. Efficiency values higher than the ones of typical c-Si cells can be obtained due to the more optimal value of the band gap of a-Si:H for most cases of indoor illuminations; for example, an efficiency of 23% can be obtained for a-Si:H in the case of fluorescent light illumination as illustrated in Fig. 1. Voltage and current values can be tailored to the application needs with monolithic interconnections of the module segments, and additional sensors can also be integrated on the same substrate. Furthermore, the solar module can also be designed in any shape in order to maximize the use of the available area. Finally, fabrication on flexible substrate is also possible.



Light source	Efficiency
AM1.5G	10.4%
Metal halide HCI	14.8%
Halogen	6.1%
Fluorescent	23.0%

Figure 1. Light spectra for sun AM1.5G and various indoor illumination sources (metal halide HCI, fluorescent and halogen lamps) adjusted for the same short-circuit current I_{sc} as for AM1.5G. The external quantum efficiency (EQE) of 0.25 cm^2 a-Si:H cell (cf. Fig. 2b) is also plotted. The corresponding cell performances for all illuminations sources are indicated in the table for the same I_{sc} of 15.9 mA/cm^2, assuming that fill factor FF of 74.3% and open-circuit voltage V_{oc} of 886 mV are the same for all sources (as plotted in Fig. 2a for AM1.5G).

In this paper several examples of a-Si:H based micro photovoltaic modules are presented. Modules with a total area ≤15 mm^2, developed on glass wafers using micro-fabrication procedures (including photolithography). The monolithic interconnections of the module segments add parasitic serial and parallel resistance and, as the segments size is reduced, may critically affect the module performance. Therefore various interconnection geometries have been tested and compared in order to devise design rules. For the same purpose, high voltage modules were also designed and fabricated. The analysis of the performance of these high voltage modules offers additional information for optimizing interconnection schemes.

Finally, the practical development of solar modules for an application in micro-robotics led to a further optimization of the design and processing and illustrates the potential of this technology for energy scavenging for micro-systems.

EXPERIMENTAL

All micro photovoltaic modules have been fabricated on 4" borofloat glass wafers. For these modules, the same cell structure was used as for large photovoltaic cells, namely glass/ZnO:B/p-a-Si:H/i- a-Si:H/n- µc-Si:H/ ZnO:B configuration. ZnO:B transparent conductive oxide (TCO) layers were deposited by LP-CVD (low pressure chemical vapor deposition); details on the deposition technique can be found in Refs. 2, 3. P-i-n diodes were deposited by Very High Frequency plasma-enhanced chemical vapor deposition (VHF PE-CVD) at 40 MHz and 200°C in a KAI S or KAI M reactor [4]. Thicknesses of the front ZnO layer and of the i-layer were 2 µm and 270 nm, respectively. For large reference cells a back contact using a 2 µm thick ZnO:B layer and a white paste was used while for micro-modules, Al contact pads were further evaporated, covering also the back thin (50 nm thick) ZnO:B.

Finally for some of a the micro-modules, a 200 nm thick SiO_x passivation layer was deposited by VHF PE-CVD and opened by photolithography on the Al contact pads. Cell patterning for monolithic interconnection of the segments or for additional implementation of photodiodes in the modules was performed by photolithography and etching steps. Mask design and alignment precision was better than 3 µm. Wet etching using diluted HCl acid was used for the front ZnO:B contact, dry etching using SF_6/O_2 mixture was used for the a-Si:H and SiO_x layers while the back ZnO:B/Al back contact was patterned using Al etch solution.

Typical current-voltage I(V) under illumination of reference cells (co-deposited with the micro-modules) as well as external quantum efficiency (EQE) curves are given in Fig. 2. These reference cells were systematically deposited together with the micro-modules.

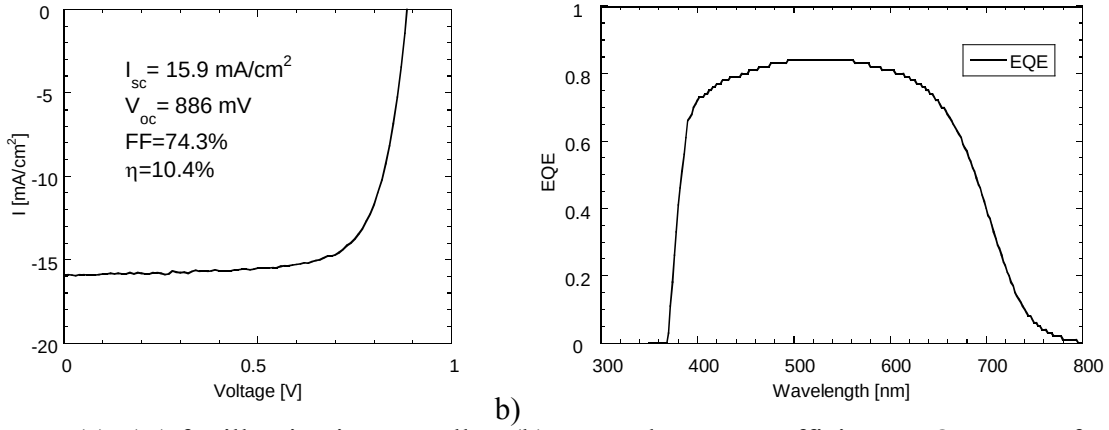


Figure 2. (a) I(V) for illumination as well as (b) external quantum efficiency EQE curves for 0.25 cm^2 reference cells deposited under similar conditions as for the micro-modules.

I(V) was measured either under (at 100 mW/cm^2) using a 2 light sources Wacom solar simulator (for relatively large solar cells) or on an illumination test bench using an halogen lamp

with IR filter with an illumination adjusted to give an identical current for a-Si:H reference cells as under the solar simulator (the actual illumination was approximately 100 kLux).

RESULTS AND DISCUSSION

For standard large area a-Si:H solar modules, every layer is deposited on the entire substrate surface and then pattern by laser scribing in order to isolate the individual cells and realize the monolithic serial interconnection. In the present case of micro-modules fabrication, we have more freedom in terms of the stacking of the various layers, as well as for the definition of the active layer. As illustrated in Fig. 3, the active area of each module segment can be defined either by the ZnO layer (Fig. 3b) or by the metallic back contact (Fig. 3a, c). An overlapping of the a-Si:H layer on the ZnO one is also possible. All stacking configurations shown in Fig. 3 have been tested and compared.

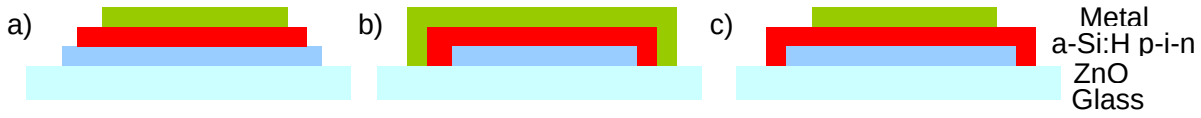


Figure 3. Schematic side view of the possible stacking of the layers to form module segments.

The monolithic interconnection implies that the metal back contact of each segment must at some point of the segment periphery cover the side of the p-i-n diode layer stack before reaching the ZnO front contact of the adjacent segment. The rather conductive back contact layer is therefore expected to create a shunt between the p- and n-layer of the diode, as illustrated in Fig. 4. In large area modules, this local shunt usually plays a negligible role on the module performance, due to the relative large distance between this local shunt and the active area. For micro-modules this shunt is expected to reduce considerably the performance as the active area of segment is decreased. Several interconnection schemes have therefore been designed and tested to study the effect of the gap between the position of the side of the a-Si:H layer stack (expected position of the shunt, as see in Fig. 4) and the active area and the effect of the width and length of the interconnection area (contact area between the ZnO and metal back contact).

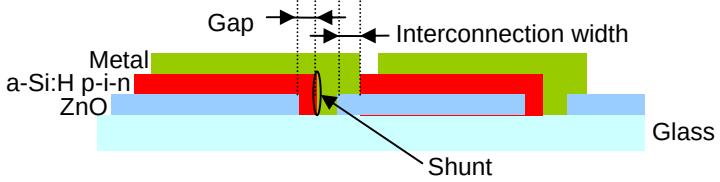


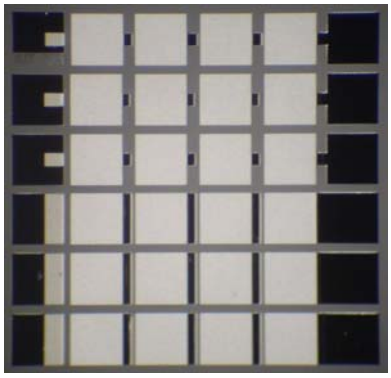
Figure 4. Schematic side view of the interconnection between two segments and position of the expected shunt.

Test modules

In order to study various layer stacking configurations, as well as interconnection designs, test structures as shown in Fig.5a were fabricated. Each test structure comprised 6 modules of 4 segments, with 2 length of the interconnection area on a 3x3 mm^2 total area. The width (15 µm) of the interconnection was the same for all modules and the gap between the interconnection area and the active area was changed from 10 to 40 µm. One set of test structures was designed with an active layer define by the ZnO top contact (Fig. 3b) and a second with an active layer defined by the bottom metallic contact (Fig. 3c).

I(V) characteristics of the different structures show very little differences which are within the scattering of the results under the used light illumination used (see experimental details). No significant change in parallel or serial resistance was observed. However, a large scattering of the performance was observed from run to run (see Fig. 5.b) indicating that such small monolithic interconnections are quite sensitive to the quality of the processing (alignment errors, under-

etching of the layers, etc). Nevertheless, slightly better yields were obtained on structures with a higher interconnection length and on some of them very high performance could be obtained with FF better than 72% (cf. Fig. 5b).

a) 

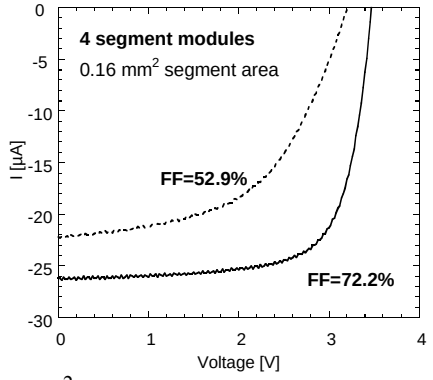
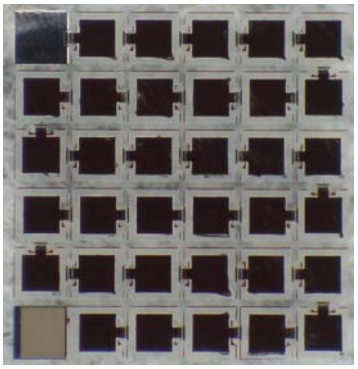
b) 

Figure 5. (a) Picture of the back of a test structure (3x3 mm^2 total area) with 6 modules of 4 segments with identical active area but various interconnection design, and (b) I(V) characteristics measured on two similar modules from 2 different deposition and processing batches. Dark areas of the picture correspond to flat aluminum area (mainly bonding pads) while white area correspond to Al deposited on rough surface (due to ZnO roughness).

High voltage modules

In order to further study the effect of segment size and interconnect on the performance, several modules were designed with number of segments ranging from 23 to 223 segments on the same 3x3 mm^2 total area. The geometry of the interconnection was kept constant for all modules. Two examples of modules are shown in Fig 6.

a) 

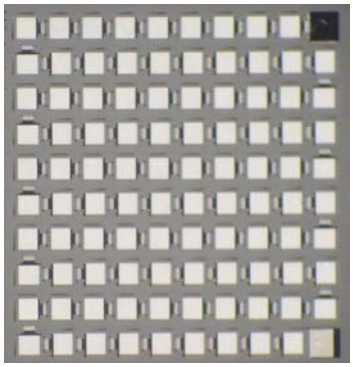
b) 

Figure 6. (a) Front side (glass side) picture of a module with 34 segment and (b) back side (module side) picture of a module with 98 segment fabricated on 3x3 mm^2 total area.

V_{oc} may be limited by the parallel resistance when the photo-generated current is reduced. In our case, the anticipated presence of a shunt in the interconnection (i.e. a fixed parallel resistance) should be revealed if one reduces the segment area. As seen in Fig. 7, no limitation in V_{oc} is noticed as the segment size is decreased down to 800 μm^2 under 100 kLux illumination and a maximum voltage of 180 V is obtained for 223 segments. From this behavior, one can conclude that the interconnection does not introduce large shunts, in agreement with the observation done on the test structures. In Fig. 7, one can also observe that the optimization of the processing led to a significant improvement in the reproducibility in the fabrication of those modules. Nevertheless, measurement of the I(V) characteristics should be carried out to quantitatively evaluate the parallel resistance introduced by the monolithic interconnection.

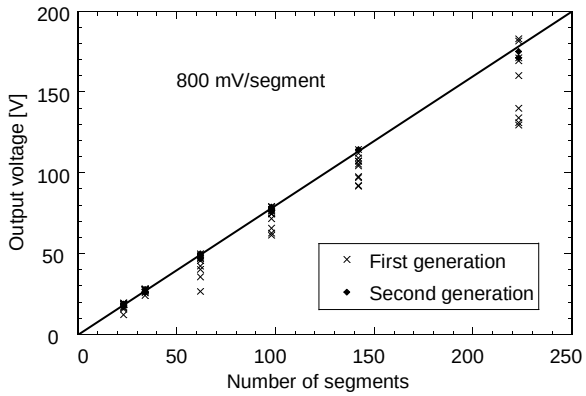


Figure 7. Open circuit voltage V_{oc} as a function of the segment number (and a fixed total module size of 3x3 mm^2) for 2 different generations of modules. The bold solid line corresponds to an output voltage of 800 mV/segment under approx. 100 kLux illumination. First and second generations share the same module designs; the change illustrates the progress in the processing.

Micro-system modules

For a specific application in micro-robotics (European project I-Swarm [5], cf. Fig. 8c), a modules with two voltage sources (1.5 and 3.3 V) as well as two photodiodes had to be integrated on a 3.9x3.9 cm^2 glass substrate. The robot comprises a locomotion and sensing module, an IR communication module, a power and sensor module as well as an ASIC (application specific integrated circuit) for the robot control. The solar module was designed to deliver a power of ca. 1 mW for the 3.3 V source and 0.5 mW for 1.5 V source under 100 kLux illumination from a HCI metal halide light source. The same device structure as for the test modules was used and in this context several inter-connection designs were also compared. The segment areas for the "high" voltage (HV), "low" voltage (LV) and photodiodes are 5.2, 0.9 and 0.039 mm^2, respectively. A schematic electrical diagram of the two voltage sources, as well as pictures of the fabricated modules, are shown in Fig. 8.

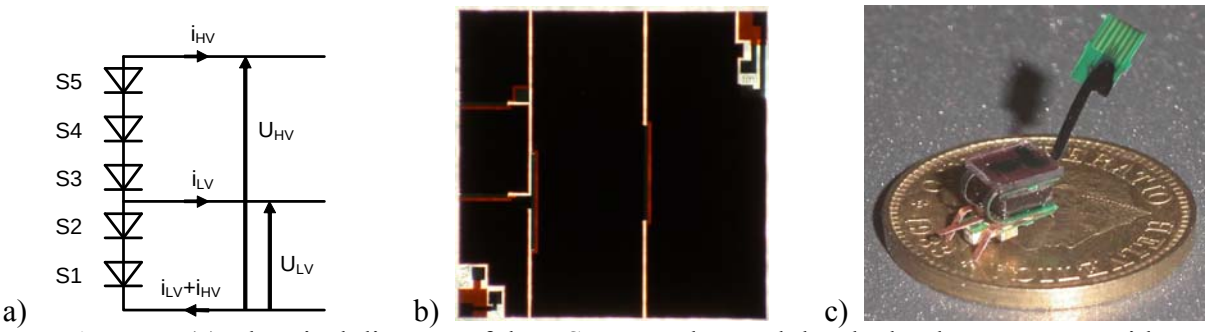
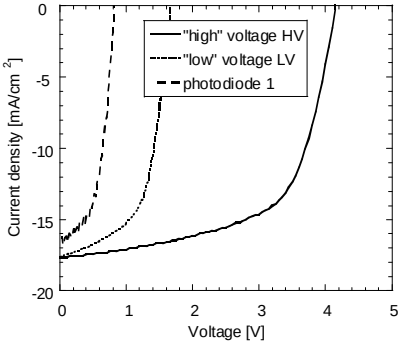


Figure 8. (a) Electrical diagram of the I-Swarm solar modules dual voltage sources with 5 segments in series, (b) front side (glass side) picture of a module and (c) picture of an autonomous microrobot developed in the framework of the I-Swarm project on a Swiss 5 cent coin. The 3.9x3.9 mm^2 solar modules can be seen on the top with 2 photodiodes in the corners. The flexible connector is used for initial programming and testing of the robot and is then cut away.

As already observed for the test structures, very limited effect of the stacking and definition of the active area was observed. Nevertheless a slightly better yield was obtained with an active area defined by the bottom Al contact and an a-Si:H layer overlapping the ZnO top contact (see Fig. 3c). Most of the fabricated devices exhibited rather high serial resistance, mostly due to an insufficient interconnection area. Best results were obtained by increasing the interconnection

width to 40 µm, and by choosing a length of 1200 µm for HV segments and 600 µm for LV ones. Nevertheless, the length was found to have less effect. Module characteristics of the best modules are plotted in Fig. 9. We can observe that the serial resistance is still limiting the performance (mostly with a reduction of the fill factor FF). A further increase of the interconnection area as well as the implementation of small bus bars are expected to further improve the behavior.



	HV	LV	Photo 1	Photo 2
I_{sc} [mA]	0.159	0.911	0.0065	0.0065
V_{oc} [V]	4.157	1.667	0.822	0.828
FF	0.613	0.572	0.517	0.522
Power[mW]	0.41	0.87	0.0028	0.0028

Figure 9. Current density I(V) as a function of voltage of the HV, LV voltage sources as well as for one photodiode (the I(V) of second photodiode not shown here is almost identical) of a I-Swarm solar modules under 100 kLux illumination (halogen lamp). The corresponding short-circuit I_{sc}, open-circuit voltage V_{oc}, FF and output power are also indicated.

CONCLUSIONS

Several micro solar modules with total area of 3-15 mm^2 were designed and fabricated on glass substrates using micro-fabrication processes. Monolithic interconnection and flexibility of the cell design allow for a wide range of module output voltage values. Even though the interconnect design of the device is critical for the performance, the latter is more dependant on the fabrication process that the geometry itself. It is observed that in most case these small modules are limited by serial resistance due to small interconnections and small connection pads.

High voltage modules able to generate up to 20 V/mm^2 under 100 kLux illumination have been successfully fabricated. No limit in the voltage density was so far found. This type of modules may have applications for example in MEMS (micro electromechanical systems), electrostatic or piezoelectric actuators. The fact that this type of device can be deposited on various types of substrates is an asset.

Finally, micro-modules for a micro-robot application were designed and successfully fabricated. This example illustrates the possibility of this a-Si:H technology to tailor the output voltage to the needs of the application and to allow also the integration of sensors such as photo-diodes. It also highlights the potential of this technology for various micro-system powering.

ACKNOWLEDGMENTS

The authors acknowledge J.-M. Breguet of the Robotic System Laboratory of the Ecole Polytechnique Fédérale de Lausanne and the EU project I-Swarm for financial support.

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