Image Sensors Based on Thin-film on CMOS Technology: Additional Leakage Currents due to Vertical Integration of the a-Si:H Diodes

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ABSTRACT

Image sensors based on thin-film on CMOS technology (TFC) have been developed. In this approach, amorphous silicon (a-Si:H) detectors are vertically integrated on top of a CMOS readout chip so as to form monolithic image sensors. In order to reduce as far as possible the dark current density (J_{dark}) of the TFC sensors, we have focused on analyzing and understanding the behavior of J_{dark} in this type of detectors. Edge effects along the periphery and at the corners of the pixel, due to the non planar configuration of the vertically integrated photodiodes, are found to be responsible for an increase of the dark current. A new and adapted solution for the minimization of J_{dark} is proposed, which combines the use of a metal-i-p a-Si:H diode configuration with a deposition on top of an unpassivated CMOS chip. Values of J_{dark} as low as 12 pA/cm^2 at a reverse polarization of V = -1 V are measured on such TFC sensors.

INTRODUCTION

The vertical integration of a thin-film a-Si:H detector on top of a dedicated CMOS integrated circuit is an attractive solution to enhance the performances of the resulting monolithic sensors. This approach is useful in the field of visible light imaging [1, 2]. In fact, TFC (Thin Film on CMOS) technology, where the pixel readout-electronics does not share the die area with the photodiode array allows one to reach high geometrical fill factors ($FF = A_{eff}/A_{pix}$). This fact combined with the high quantum efficiency of a-Si:H in the visible spectral range enhances the sensitivity of the device [3, 4]. Image sensors based on this technology have been developed in our laboratory showing geometrical fill factors up to FF = 92 % and increased sensitivity (S > 60 V/(µJ/cm^2) between 575 and 659 nm).

In order to extend the dynamic range and to enable low light level detection, a very low J_{dark} value is a key issue [5]. In the case of planar large area a-Si:H n-i-p photodiodes (several mm^2) the lower limit for J_{dark} is given by the thermally-generated charge in the intrinsic layer. The density of thermally-generated current depends on various factors: the deep defect density, the mobility gap of the semiconductor material and the width of the i-layer [6]. For a 1 µm thick diode with a low dandling bond density (<10^{15} cm^{-3}) and an optical band gap of 1.8 eV, one is able to estimate the thermally generated current density which is in the range of 1 to 10 pA/cm^2. Such low values were confirmed by experimental measurements of J_{dark} on millimeter size test structures deposited on glass [7, 8].

However, in the case of vertical integration, because of the small size (40x40 µm^2) and the non planar configuration of the pixels, additional leakage currents which lead to an increase in J_{dark} have been observed [7, 8]. In this paper the nature of these leakage currents is analyzed and discussed: Edge effects along the periphery and at the corners of the pixel, linked to the presence of a passivation layer surrounding the pixels (inset Fig.1), are found to be responsible for this

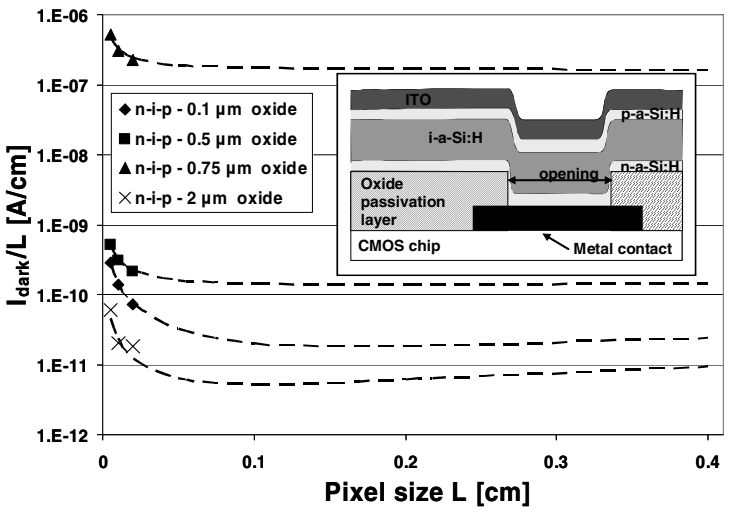

Figure 1: Dark current linear density (I_{dark}/L) in function of the pixel size L for 1 µm thick n-i-p diodes measured at -1V with different oxide passivation thicknesses. Dots correspond to experimental data and dashed lines to trend lines using equation (2). Inset: Schematic cross section of a pixel.

increase. Thanks to a simple model which is used to analyze the measured J_{dark} values in function of the detector size, the presence of a ''corner effect'' is demonstrated. The occurrence of this effect at the pixel corners, as well as the one of a peripheral effect along the pixel edge is confirmed by electron beam induced current (EBIC) analysis of a TFC sensor.

In order to minimize these effects, responsible for the observed increase of J_{dark}, different approaches have been evaluated. This led to the choice of a new and adapted solution which combines the use of a metal-i-p a-Si:H diode configuration, with a vertical integration on top of an unpassivated CMOS chip. With such a TFC sensor a value as low as 12 pA/cm^2 has been measured on a 40x40 µm^2 pixel at V = -1 V.

EXPERIMENTAL DETAILS

All results reported in this paper have been obtained on a-Si:H sensors deposited in a Plasma Enhanced Chemical Vapor Deposition reactor, at a frequency of 70 MHz.

In order to study the effect of non planar pixel geometry, specially designed test structures, so called "chip-like'' structures, mimicking the TFC pixel configuration, with small-size pixels (40 to 1000 µm side lengths) were fabricated by photolithography.

Two different dedicated types of CMOS chips have been used in this paper. A first one has been designed by CERN (''AFP chip'' [9]) and used for the EBIC analysis. The second type is a 64 x 64 pixels CMOS chip designed by CSEM. More details on the fabrication of the TFC image sensors can be found in Ref. [3, 8]

RESULTS AND DISCUSSION

As mentioned before, due to the non planar configuration of the pixels, additional leakage currents have been observed. To be able to reveal the presence of these additional contributions and study there nature, a simple model has been used (which is an extension of a previous work [10]). It is assumed that the sensor's dark current consists of three components. For square sensors of side L we have:

$$I_{dark} = j_1 \cdot L^2 + 4j_2 \cdot L + j_3 \qquad (1)$$

The term j_1 corresponds to a bulk contribution due to thermal generation in the intrinsic layer that scales with the area of the detector. The second component j_2, proportional to the sensors perimeter, is related to edge effects along the pixel periphery.

Finally, the third component j_3 is a ''point like'' contribution, independent of the pixel size L, which could be in relation with a corner effect. One can obtain a simple but powerful tool, for the graphical analysis of measured data, by writing Equ.1 in the following form:

$$I_{dark}/L = j_1 \cdot L + 4j_2 + j_3/L \quad (2)$$

In fact, by plotting the measured I_{dark}/L in function of the pixel size L the contribution of the three components j_1, j_2, j_3 can easily be distinguished. In this case, j_1 corresponds to the slope. The intercept at L = 0 indicates $4 \cdot j_2$. The term j_3 provokes the bending of the curve for small pixel size L.

In Fig.1, the experimental data measured on ''chip like'' test structures, with different oxide thicknesses (i.e. non planarity) and for 1 µm thick n-i-p vertically integrated diodes, are presented. The most important observation is the bending of the curves for small pixel sizes, which is a clear evidence of the presence of a point like component j_3. In all cases, the data can't be fitted properly with only bulk and peripheral components that are obviously present, and it is necessary to add the j_3 term to obtain the observed bending of the fitting curve. Even though this leads to the conclusion that in addition to the bulk effect, a peripheral and a ''point like'' effect are present; this doesn't explain their nature. In particular it is not obvious that the latter is related to an effect taking place at the square pixel corners. However it is already evident that these additional effects appear when vertically integrating the a-Si:H detectors on top of a non planar configuration pixels (inset Fig.1). This can be pointed out because of the influence of the passivation thickness on the relative J_{dark} values measured (Fig.1 and more detailed in Ref. [3])

To reveal the nature of j_2 and j_3, a TFC sensor (''AFP chip'') has been observed with a Scanning Electron Microscope (SEM) and an Electron Beam Induced Current (EBIC) analysis has been performed on it. Due to the encountering of the two perpendicular a-Si:H growth flank, one from the bottom of the pixel (metal contact) and the other from the passivation side wall, an edge forms along the periphery of the pixel (see also Fig.3c). This ''growth edge'' can clearly be observed in the SEM image of Fig.2b. At the pixel corners, three growth flanks meet each other, leading to the formation of some kind of ''crack'', as it can be seen in the zoom of Fig.2c.

Using the electron beam of the SEM it is possible to scan the pixel, while inducing at the same time an output voltage, proportional to the generated current. An EBIC contrast image of a pixel is shown in Fig.3 together with the corresponding cross scan of the EBIC output signal. We can observe a bright zone corresponding exactly to the ''edge growth'' seen in Fig.2; a sharp EBIC signal peak is present at this position. In each corner a bright zone (i.e. a high EBIC signal) extending along the ''cracks'' is also detected.

It is supposed that the electric field is locally higher, and , hence, the collection is better, due to a point effect provoked by the presence of the ''growth edge'' along the periphery and the ''cracks'' at the corners. Because of the well known Poole-Frenkel effect [6, 11], the leakage current is locally enhanced in those parts of the pixel. However this local field enhancement doesn't seem to be sufficient to completely explain the observed behavior; thus we think that an additional phenomena is present. At the corner and along the peripheral edge growth, at the interface where the different a-Si:H growth flanks meet each others, we suspect that the defect density is much higher than in the bulk regions.

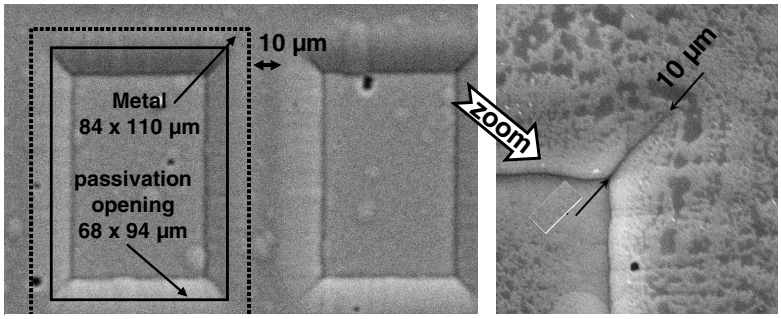

Figure 2: SEM image of an ''AFP chip'' pixel (top view) and zoom on the pixel corner. The dashed line corresponds to the metal area and the black line to the opening in the passivation.

As it is know from other works [11], or can be easily simulated, the thermally generated current is related to the defect density. Therefore a local enhancement of the defect density will induce in the concerned region a peak of thermal generation, i.e. an additional contribution to the leakage current to the bulk component. Combining the effect of a locally higher electric field and defect density at the corners and along the periphery of the pixels, the origin of the components j_2 and j_3 used in equation (1), (2) can be explained. We must stress that the presence of a step, induced by the passivation surrounding the pixel, is responsible for the apparition of the ''growth edge''; and thus concerns the particular case of vertical integration onto a non planar CMOS chip. Finally, the term j_1 is simply the constant contribution of the central part of the pixel, the bulk current (Fig.3a).

To eliminate or at least reduce the peripheral and the corner leakage current components, different solutions have been evaluated:

1. Larger opening in the passivation than the metal contact [3]
2. Chemical-mechanical polishing (CMP) or dry etching of the passivation layer
3. passivation layers (''unpassivated chip'')
4. Suppression of the n-layer of the n-i-p a-Si:H vertically integrated diode (''metal-i-p '')

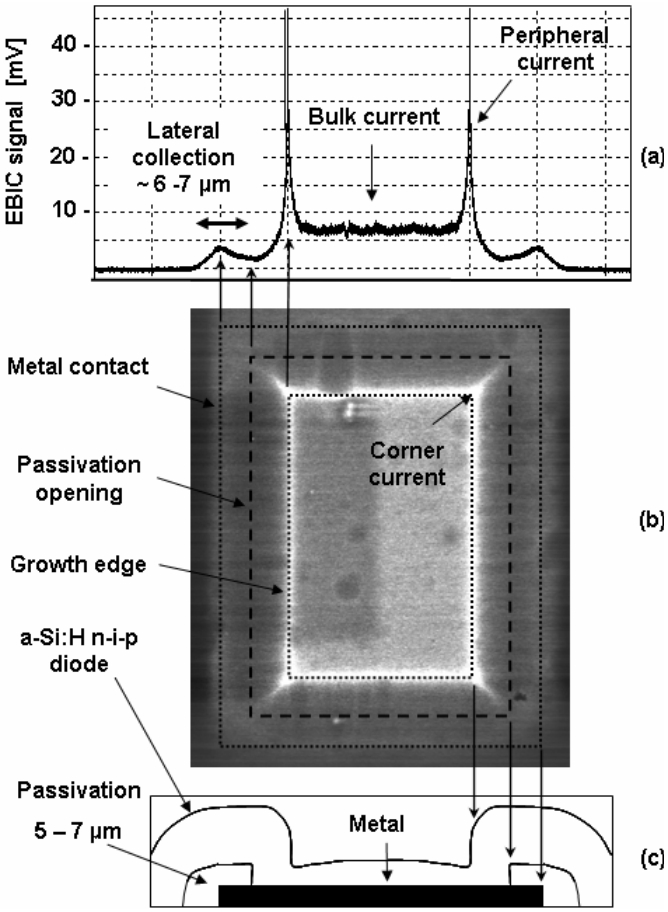

Figure 3: (a) EBIC signal profile induced by scanning the TFC pixel with the electron beam. (b) EBIC contrast image, the bright zones correspond to high output signal. (c) Schematic cross section of a pixel with the passivation overlapping the metal contact, i.e the passivation opening is smaller than electrode area.

The first approach consists to create a larger opening than the metal contact area in the passivation. By doing so, the zone where the edge and corner effect takes place is pushed away from the electrode; therefore less leakage current is collected, thus reducing J_{dark}. This has been reported and detailed in one of our previous work [3].

In both cases, with CMP or dry etching pretreatment of the CMOS chip, a reduction of the J_{dark} has been observed, proving experimentally that any solution aiming at removing the passivation is beneficial in terms of dark current. Unfortunately those two planarization solutions aren't ideal to implement on isolated single chips (as processed in this work) and therefore difficult to reproduce. To avoid the inconveniences of the presence of the passivation layer and the need of removing it, the only valid alternatives left are: either to get from the CMOS foundry a chip without the last passivation steps of the process or to modify the a-Si:H detector so as to be less sensitive to the presence of the oxide step. This has led to the development of a metal-i-p type diode. The idea, in this case, is to suppress the bottom conducting n-layer with the aim of

avoiding the conduction path between the side walls of the passivation step and the metal rear contact of the pixel; i.e. limiting the collection of the additional leakage current from the zones affected by the ''edge growth'' problems.

In fact, by comparing the experimental data obtained on both vertically integrated 1 µm thick metal-i-p and n-i-p type ''chip-like'' test diodes, the effect of n-layer suppression can be revealed (Fig.4). On one side, the n-i-p type diode is characterized by the bending of the curve indicating the presence of the corner effect. One the other side, for the metal-i-p diode, the absence of the bending for small pixel sizes is clearly observed. This means that the effect of the j_3 component is suppressed or at least minimized, i.e. a highly reduced corner effect is obtained with such a modified detector. Integrating this type of metal-i-p diode directly on top of a CMOS chip, we observe, as expected, a reduction of the measured J_{dark}. This can be seen by comparing the results obtained on a TFC sensor in the n-i-p diode and the passivated chip configuration, with the one measured in the metal-i-p and passivated TFC chip configuration (Fig.5, black and crossed squares).

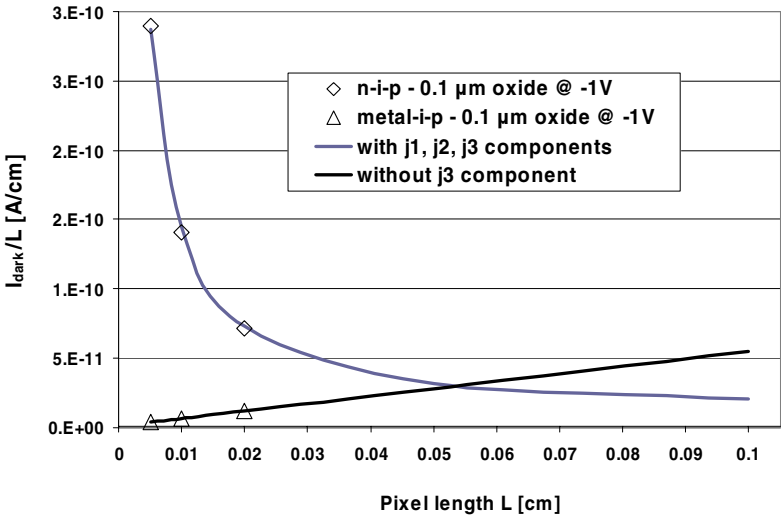

Figure 4: Dark current linear density (I_{dark}/L) in function of the pixel size L comparison for 1 µm thick n-i-p and metal-i-p diodes measured both at -1V with 0.1 µm oxide passivation thickness. Dots correspond to experimental data and dashed lines to trend lines using equation (2).

A further reduction of J_{dark} has been achieved by using the unpassivated chip. With an n-i-p diode as well as with the metal-i-p type diode, J_{dark} is lower when vertically integrating the diode on the CMOS chip without any passivation. The best results are obtained for the combination of the metal-i-p type diode deposited on top of the unpassivated chip (Fig.5 black dots). This choice allows us to attain a value of 20 pA/cm^2 for J_{dark} (measured at room temperature (RT) and V = -1 V, in the as deposited state, on a 40x40 µm^2 pixel).

Finally a comprehensive characterization of this metal-i-p on unpassivated TFC sensor has been carried out leading to the following synthesized results:

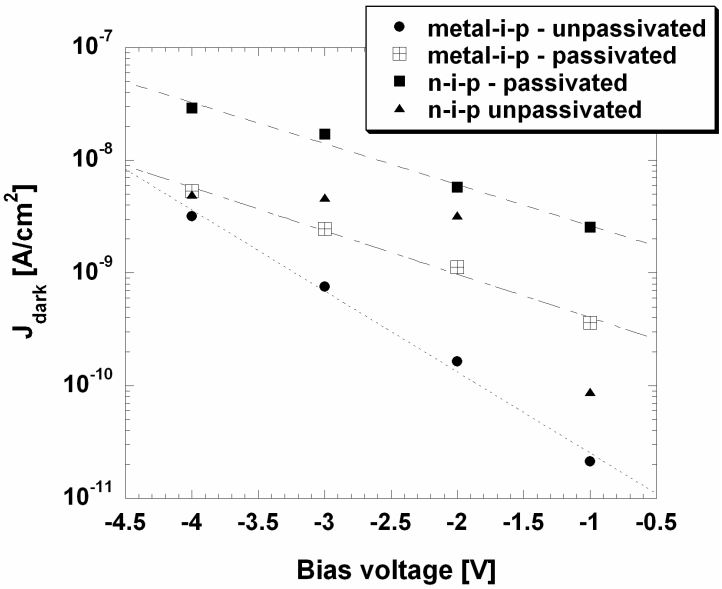

Figure 5: Dark current density J_{dark} in function of the bias voltage for different configuration of TFC chip

- J_{dark} = 12 pA/cm^2 after thermal annealing at 180°C for 1h30 (measured at RT, V = -1V)
- Stabilized J_{dark} = 200 pA/cm^2 after 250 hours of light soaking under AM1.5 at 50°C (measured at RT, V = -1V)
- Temporal noise TN = 1.08 mV and Fixed Pattern Noise FPN= 3.1 mV; noise being limited by TFA chip readout electronics and not by the a-Si:H metal-i-p diode.
- Dynamic range DR = 61 dB, limited by the saturation of the output signal, i.e. the amplification gain.
- Linearity L = 99% at 650 nm over 3 orders of magnitude.
- Sensitivity of S > 60 V/(µJ/cm^2) between 575 and 660 nm, corresponding to an external quantum efficiency EQE > 85 %, that could be easily improved in the blue region, by optimizing the ITO front contact and the p-layer thicknesses.

CONCLUSIONS

In this paper, the authors present a new and adapted solution to reduce the J_{dark} of TFC image sensors for non planar CMOS technology.

A graphical tool using a three components equation for I_{dark} (j_1, j_2, j_3, bulk, peripheral and point like terms respectively) is proposed to analyze the J_{dark} experimental data measured on test structures. Thanks to this simple approach the presence of a point like effect is evidenced.

It is found that, in the particular case of vertical integration of a-Si:H detectors on to of a non planar CMOS chip, the presence of a step, induced by the passivation surrounding the pixel, is responsible for the apparition of a ''growth edge''. SEM imaging shows that this ''growth edge'' is formed along the periphery together with ''cracks'' at the corners of the pixel. The EBIC analysis suggests that an enhancement of the electric field combined with an increased defect density is at the origin of the observed additional leakage current. This phenomenon is localized along the periphery and at the corners of the pixels.

Several approaches for improving the J_{dark} are evaluated, indicating that any solution aiming at removing the passivation is beneficial in terms of J_{dark}. Furthermore, it is demonstrated that the suppression of the n-layer strongly reduces the corner leakage current contribution.

This study leads to the choice of the combined best solution: vertical integration of metal-i-p type diode on top of an unpassivated CMOS chip. With such a TFC image sensor, a record value of J_{dark} = 12 pA/cm^2 is measured on a 40x40 µm^2 pixel (at RT, V = -1 V, after thermal annealing at 180°C for 1h30). This TFC sensor also exhibits high sensitivity (S > 60 V/(µJ/cm^2)) together with low temporal and fixed pattern noise, limited by the underlying readout electronic and not by the a-Si:H diode.

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