INVESTIGATION OF THE 3-LEVEL UNIFIED POWER FLOW CONTROLLER (UPFC)

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Abstract

Flexible AC Transmission Systems (FACTS) are systems based on power electronics using GTO or IGCT semiconductors [1] that allow a better use of the transfer capacities of the transmission lines and permit to satisfy the requirements due to the liberalization of the electrical energy market. The Unified Power Flow Controller (UPFC) is one of the most versatile topologies of the FACTS family. The UPFC can be decomposed in two different power circuits: the parallel one maintaining the network bus voltage by consuming or producing reactive power, and the series one controlling the active and reactive power flow with the insertion of a series voltage in the transmission line. The aim of the present paper is to investigate in details the power quality and the dynamic performance of the 3-level UPFC.

Introduction

The topology of UPFC considered is given in figure 1. A 3-level UPFC is inserted on the HV node N1. The left hand side of the converter is called the shunt compensator. It is connected to the HV node N1 through a transformer TSH, able to produce or consume reactive power and, thus, being able to maintain the voltage on the HV node N1. The shunt compensator is also controlling the DC voltage of the converter.

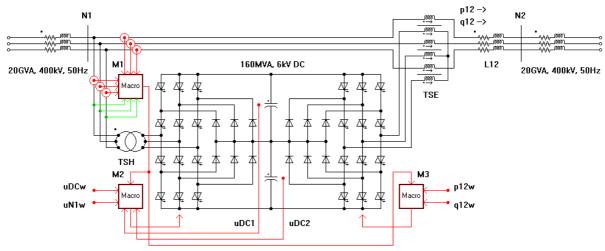


Fig. 1: 3-level UPFC topology

The right hand side of the converter is called the series compensator. It allows inserting a voltage in series with the transmission line L12 and, thus, is able to control the active p12 and reactive q12 power flow between the HV nodes N1 and N2. This series converter is connected to the transmission line L12 through a special transformer TSE with open primary windings.

System modeling

Power system

The whole power system of figure 1 has been implemented using the *SIMSEN* simulation software. This software can take into account the influence of all the semiconductors of the 3-level converter and is therefore able to perform Fourier analysis in order to investigate the power quality of such FACTS devices. In the present example, the series transformer secondary windings are star-connected. A delta-connection can also be selected. It provides a better damping of the zero-sequence currents.

Control system

The basic control of the UPFC has been presented in several papers [2, 3]. The present paper will focus on the extension to 3 levels converter with neutral point clamped diodes. In comparison with the standard 2-level topology [4, 5], a 3-level topology has the inconvenient that not only the DC-link voltage has to be controlled, but also the DC-unbalance. Many solutions have been developed in [6]. Another important point is the modulation method of the VSI. For high power network applications, the switching frequency of the valves has to be kept as low as possible (400-500 Hz), and the THD (Total Harmonic Distortion) of the regulated current as small as possible in order to fulfill the network requirements. An improved PWM control has been implemented. It is the so-called Flat Top Control [6]. The control system has been split in 3 macros M1, M2 and M3.

Macro M1: PLL and currents transforms

Macro M1 is presented in figure 2. This macro provides the voltage and current measurements, including PLL and coordinates transforms.

Macro M1: PLL and currents transforms

ud1f UabN1 y=f(x)UhcN1 Prog UcaN1 uq1f Ths Integr 3->2 **IaSH** idSH v=f(x) IbSH Prog IcSH 3->2 laSE v=f(x)IbSE IcSE

Fig. 2: Control system: Macro M1

The HV node N1 voltages UabN1, UbcN1 and UcaN1 are measured. They are transformed in a d-q frame system rotating with the angular frequency wn of the AC network. The angular position Ths of the rotating frame is obtained by integrating the angular frequency. An additional PLL (Phase Locked Loop) is tuning the input of the integrator in order to maintain to zero the q component uq1f of the transformed node N1 voltage equivalent phasor. This is made by a P-control, due to the fact that a precontrol is already delivering the synchronous angular frequency wn. The shunt currents IaSH, IbSH

and **IcSH** on the primary side of the transformer **TSH**, as well as the series currents **IaSE**, **IbSE** and **IcSE** of the opened windings of transformer **TSE** are also transformed into the rotating d-q frame. From this macro, the following computed values are available in per unit:

ud1f (d component of the voltage on the node N1).

uq1f (q component of the voltage on the node N1, shall be equal to zero).

idSH (d component of the shunt current, primary side of transformer TSH).

iqSH (q component of the shunt current, primary side of transformer TSH).

idSE (d component of the series current, primary open windings of transformer TSE).

iqSE (q component of the series current, primary open windings of transformer TSE).

Macro M2: Shunt and DC control

Macro **M2** is represented in figure 3. This macro contains the shunt compensator control, including the DC link voltage control.

Macro M2: Shunt and DC control

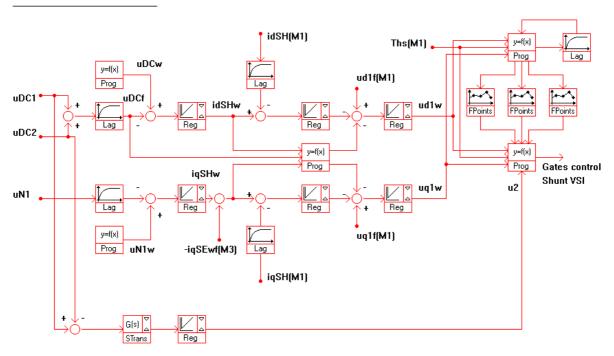


Fig. 3: Control system: Macro M2

The shunt compensator control is also based on the d-q transform, using the rotating frame angular position **Ths** (calculated in macro **M1**).

DC link voltage control

The sum of the two DC link voltages **uDC1** and **uDC2** is low-pass filtered to obtain the value **uDCf**. This value is compared to the reference set value **uDCw** for the DC link voltage. The difference between set value and regulated value is applied at the input of a PI-control. The output of this PI-control corresponds to the current set value **idSHw**. This value corresponds to the active current of the shunt compensator. Usually, this value is very small and is calculated to cover the losses of the shunt converter and transformer. The instantaneous value of the active current **idSH** (calculated in macro **M1**) is delivered through a low-pass filter. The lower part of figure 3 contains the DC voltage unbalance control. This control is responsible for maintaining both DC link voltages **uDC1** and **uDC2** at the same average value. This control is based on the well-known second harmonic injection method. The signal **u2** is added to the reference signals used by the PWM. The DC link voltage unbalance is calculated with the difference between **uDC1** and **uDC2**. As both voltages contain the 3rd harmonic, a special band-pass filter is used, in order to deliver only the DC component.

AC bus voltage control

The voltage uN1 on the node N1 is compared to the voltage reference set value uN1w. The difference between set value and regulated value is applied at the input of a PI-control. The output of this PI-control corresponds to the current set value iqSHw. This value corresponds to the reactive current of the shunt compensator. The instantaneous value of the reactive current iqSH (calculated in macro M1) is delivered through a low-pass filter. To increase the dynamic of the control, an additional signal -iqSEw is added. This signal corresponds to the reactive current set value of the transmission line L12 between the HV nodes N1 and N2. Thus, the reactive power required by the transmission line is delivered by the shunt compensator of the UPFC. The internal circuit of the shunt control is the so-called decoupled current control. This control takes into account the short circuit reactance xsc of the shunt transformer TSH, as well as the instantaneous value of the DC link voltage. This last feature adapts the decoupling terms of the control. The calculated voltages ud1f and uq1f of the node N1 in the d-q rotating frame are also added to the output of the PI-control. The output values ud1w and uq1w are the d and q components of the shunt inverter voltage. They are used as reference signals for the PWM modulation.

PWM modulation

The PWM modulation is the right hand side of figure 3. This PWM command has two special features: Flat Top Control and automatic phase adjustment of reference and carrier signal. These two features reduce the THD of the shunt current. The third harmonic additional signal u3 is calculated in equation 1:

$$u3 = (ua-1) \cdot GT0(ua-1) + (ua+1) \cdot LT0(ua+1)$$

$$+(ub-1) \cdot GT0(ub-1) + (ub+1) \cdot LT0(ub+1)$$

$$+(uc-1) \cdot GT0(uc-1) + (uc+1) \cdot LT0(uc+1)$$

$$(1)$$

with ua, ub and uc the d-q rotating frame inverse transform of the control voltages ud1w and uq1w. The reference signal ua, the two carrier signals tri+ and tri-, the 3rd harmonic additional signal u3 as well as the resulting reference signal uaref with Flat Top Control are represented in figures 4 and 5.

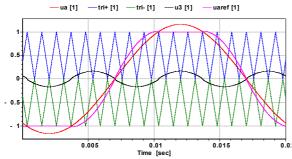


Fig. 4: Reference and carrier signals with Flat Top Control and phase adjustment

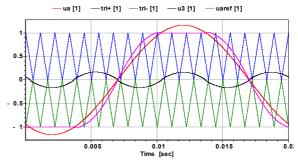


Fig. 5: Reference and carrier signals with Flat Top Control without phase adjustment

One of the improvements with Flat Top Control is the suppression of over-modulation thanks to the limitation of the reference signal to the value of the carrier signals. Another improvement is the disappearance of switching function pulses in the center of each half period. The resulting carrier frequency can be higher as well as the first harmonic of the switching function. In figure 4, the reference and carrier signals are synchronized, in order to generate a symmetrical modulation shape. Figure 5 shows the PWM modulation without phase adjustment. To adjust the phase, an additional angle **dThs** is added to the angle **Ths** of the rotating d-q frame. This additional angle is calculated in equation 2:

$$dThs = ArcTg\left(\frac{uq1w}{ud1w}\right) \tag{2}$$

Note that this corrected angle is only used for the calculation of the carrier signals **tri+** and **tri-**. The phase angle adjustment **dThs** is low-pass filtered to avoid fast changes during transients. This phase adjustment also has an influence on the THD of both shunt and series current of the 3-level converter.

Macro M3: Series compensator control

Macro M3: Series control

Macro **M3** and is represented in figure 6. This macro corresponds to the series compensator control. **Active and reactive power control**

The reference set values **p12** and **q12** of active and reactive power is used to calculate the reference set values **idSEw** and **iqSEw** of the active and reactive currents flowing through the transmission line **L12** taking into account the AC bus voltage. These set values are low-pass filtered, in order to avoid changes too rapid. The instantaneous values **idSE** and **iqSE** (calculated in macro **M1**) of the active and reactive currents are low-pass filtered and compared to the filtered set values. These differences are applied at the input of a PI-control. To improve this control, an additional control is implemented, the so-called decoupled current control. It takes into account the global reactance of the series compensator (short-circuit reactance of series transformer as well as the line reactance) and the instantaneous value of the DC link voltage **uDCf** (calculated in macro **M2**).

PWM modulation

On the right hand side of figure 6, the PWM modulation is working on the same principle as for the shunt compensator. There is also a carrier signal phase adjustment. The output signals **ud2w** and **uq2w** of the current control in the rotating d-q frame are transformed in a 3-phase fixed system using the same rotating frame position angle **Ths** (calculated in macro **M1**).

idSE(M1) y=f(x)Ths(M1) Prog p12w ud2w idSEw y=f(x)**FPoints** Reg Reg Prog Lag uDCf(M2) y=f(x)y=f(x)Prog Gates control q12w Series VSI uq2w y=f(x)Reg Prog iqSE(M1)

Fig. 6: Control system: Macro M3

Simulation

System data

The main system data are:

```
rated apparent power of network
SN
             = 160e6
                       [VA]
UN
             = 400e3
                       [V]
                             rated voltage
                             rated frequency
               50
FΝ
             =
                       [Hz]
SSC1
               2e10
                       [VA]
                             short-circuit power node 1
```

```
U VS1
             = 400e3
                        [V]
                              voltage node 1
SSC2
                        [VA]
                              short-circuit power node 2
                2e10
U VS2
                              voltage node 2
               400e3
                        [V]
L_L12
               1e-1
                        [H]
                              inductance Line 12
R L12
              = 3.0
                        [Ohm] resistance Line 12
;---- UPFC1
SN1 UPFC1
             = 160e6
                        [VA]
                              rated power transformer shunt
UN11 UPFC1
             = 400e3
                        [V]
                              rated voltage primary side shunt
UN12 UPFC1
             = 4000
                        [V]
                              rated voltage secondary side shunt
xcc1_UPFC1
             = 0.15
                        [p.u]
                              short circuit reactance
     UPFC1
                0.005
rcc1
                        [p.u]
                              short circuit resistance
xh1 UPFC1
             = 1000
                        [p.u] main reactance
type1 UPFC1
                        [1]
                              type of magnetic circuit
                        [VA]
SN2 UPFC1
             = 160e6
                              rated power transformer series
UN21_UPFC1
UN22_UPFC1
             =
               16.5e3
                        [V]
                              rated voltage primary side series
                4000
                        [V]
                              rated voltage secondary side series
xcc2 UPFC1
             = 0.15
                        [p.u] short circuit reactance
rcc2 UPFC1
             = 0.005
                        [p.u]
                              short circuit resistance
xh2 \overline{U}PFC1
             = 1000
                              main reactance
                        [p.u]
                               type of magnetic circuit
type2 UPFC1
                1
                        [1]
 UPFC1
             = 4.0
                        [p.u] DC-link capacitance
kths UPFC1
             = 18
                        [1]
                              Nb triangles PWM
\mathtt{TF1}\_\overline{\mathtt{U}}\mathtt{PFC1}
             = 0.010
                              low-pass time constant UDC unbalance
                        [sec]
TF2_UPFC1
TF3_UPFC1
             = 0.003
                        [sec]
                              SE set values time constant
             = 0.0020
                        [sec]
                              SE
                                 currents filter time constant
TF4 UPFC1
             = 0.0020
                        [sec]
                              SH currents filter time constant
UDCw UPFC1
             = 1.08
                        [p.u] DC link voltage set value
```

Steady state

The requested power flow through the transmission line **L12** corresponds to 80% active and 60% reactive power. 60% reactive power is injected through the shunt transformer. The PWM carrier signal frequency is $18 \times 50 \text{ Hz} = 900 \text{ Hz}$. Due to the 3-level topology, this corresponds to a 450 Hz switching frequency for each GTO valve. The DC link voltage has been selected to 1.08% (6110 V). The PWM control shape is working with a 117% modulation. Using the Flat Top Control, this leads to an optimal use of the 3-level Voltage Source Inverter (VSI) on both sides of the converter with a reduced switching frequency (about 250 Hz) for each GTO. Figures 7 to 14 present simulation results.

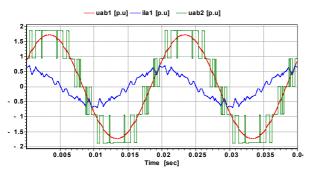


Fig. 7: Shunt transformer: line voltages and phase current (PWM 900 Hz)

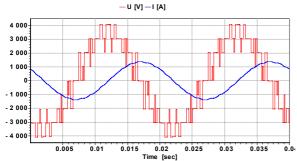


Fig. 9: Series transformer: converter side phase voltage and current (PWM 900 Hz)

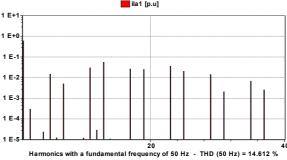


Fig. 8: Shunt transformer: Fourier analysis of phase current (PWM 900 Hz)

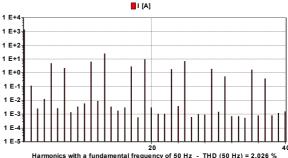


Fig. 10: Series transformer: Fourier analysis of phase current (PWM 900 Hz)

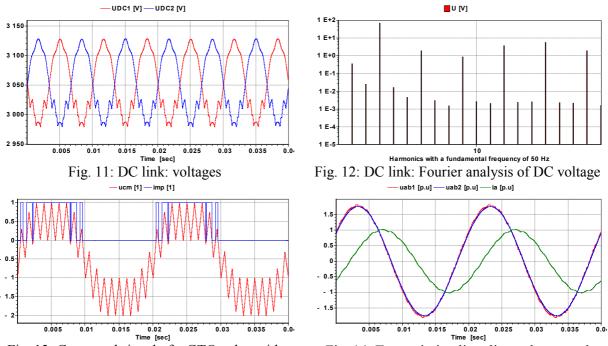
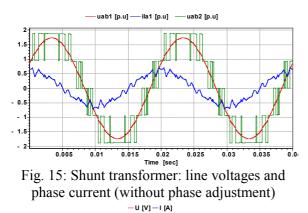


Fig. 13: Command signal of a GTO valve with Flat Top Control

Fig. 14: Transmission line: line voltages and phase current

We can observe that the THD of the transmission line phase current is about 2%. This value could be reduced by increasing the switching frequency of the PWM or the levels number of the converter. As expected, the spectrum of the DC link voltage contains the 3rd harmonic, and the resulting switching frequency of the GTO valve is drastically reduced through the use of Flat Top Control.

To analyze the influence of the carrier signal phase adjustment, an additional simulation has been performed with a DC link voltage set value uDC = 1.08 % and without synchronization control. Results are displayed in figures 15 to 18.



4 000 3 000 2 000 1 000 -1 000 -2 000 -3 000 -4 000 -4 000 -4 000 -5 0.01 0.015 0.02 0.025 0.03 0.035 0.0

Fig. 17: Series transformer: converter side phase voltage and current (without phase adjustment)

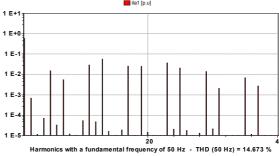


Fig. 16: Shunt transformer: Fourier analysis of phase current (without phase adjustment)

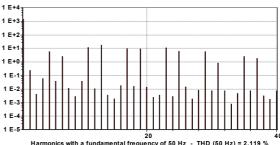
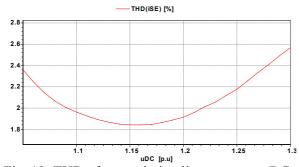


Fig. 18: Series transformer: Fourier analysis of phase current (without phase adjustment)

The carrier signal phase adjustment has only a small influence on the shunt converter of the UPFC (THD = 14.612% with phase adjustment and 14.673% without phase adjustment). This can be explained by the fact that this shunt converter is working only in the d-direction and only has to cover the losses (0.5 %). On the other hand, the series converter is more affected by the phase adjustment (THD = 2.026% with phase adjustment and 2.119% without phase adjustment). The series voltages has both d and q components.

In order to estimate the influence of the DC link voltage value, many simulations have been completed by modifying the DC link voltage set value from 1.05 % to 1.30 %. The results are shown in figures 19 and 20.



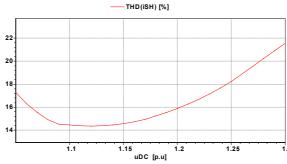


Fig. 19: THD of transmission line current vs DC link voltage

Fig. 20: THD of shunt transformer current vs DC link voltage

The last investigation is to estimate the influence of the switching frequency of the GTO valves. This is performed by increasing the frequency of the PWM carrier signal. In this case, the carrier signal phase adjustment is applied. Figures 21 to 36 show simulation results with a 950 Hz to 1100 Hz PWM carrier signal frequency.

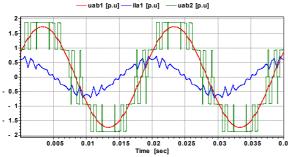


Fig. 21: Shunt transformer: line voltages and phase current (PWM 950 Hz)

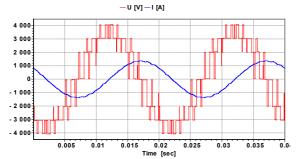


Fig. 23: Series transformer: converter side phase voltage and current (PWM 950Hz)

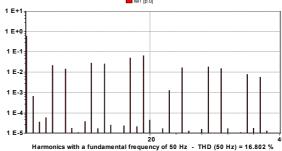


Fig. 22: Shunt transformer: Fourier analysis of phase current (PWM 950 Hz)

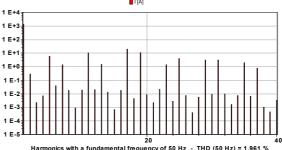


Fig. 24: Series transformer: Fourier analysis of phase current (PWM 950Hz)

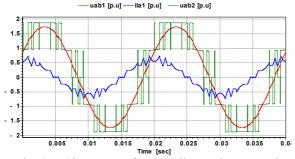


Fig. 25: Shunt transformer: line voltages and phase current (PWM 1000 Hz)

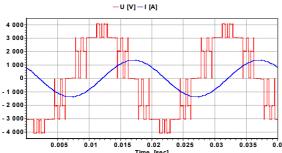


Fig. 27: Series transformer: converter side phase voltage and current (PWM 1000 Hz)

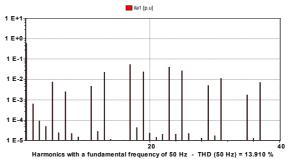


Fig. 26: Shunt transformer: Fourier analysis of phase current (PWM 1000 Hz)

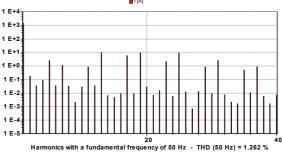


Fig. 28: Series transformer: Fourier analysis of phase current (PWM 1000 Hz)

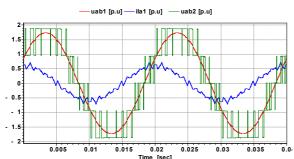


Fig. 29: Shunt transformer: line voltages and phase current (PWM 1050 Hz)

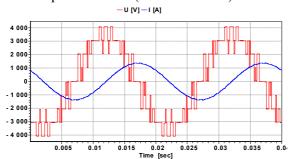


Fig. 31: Series transformer: converter side phase voltage and current (PWM 1050 Hz)

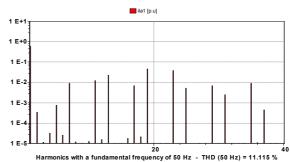


Fig. 30: Shunt transformer: Fourier analysis of phase current (PWM 1050 Hz)

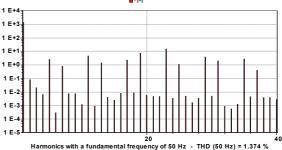
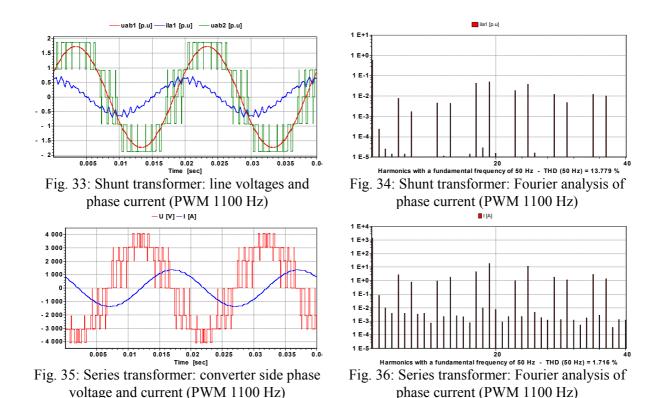


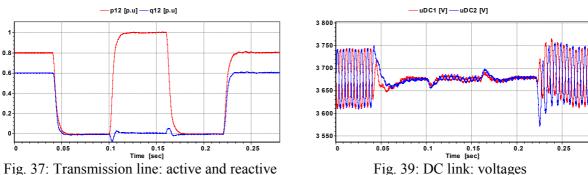
Fig. 32: Series transformer: Fourier analysis of phase current (PWM 1050 Hz)



We can observe that a PWM modulation using a multiple of 3 of the main frequency (18 or 21) presents the best THD results for both shunt and series transformers currents. Higher carrier signal frequencies are not allowed at the present time because of the thermal limit of the GTO or IGCT semiconductors [1].

Transients

If the UPFC is tuned with a high dynamic control, it is able to damp power oscillations in the network [4]. To investigate the dynamic behavior of the UPFC, fast changes of the active and reactive power set values are applied to the control. Figures 37 to 40 show simulation results in transients. From a steady-state operating point with 80% active and 60% reactive power flowing through the transmission line L12, the reference set values for both active and reactive power are reduced to zero after 40 ms. At 100 ms, the reference set value for the active power only is set to 100%. At 160 ms, the set values are reduced to zero again. At 220 ms, the desired operating point is set to 80% active and 60% reactive power again. During all the operating points where power is flowing through the transmission line, we can observe the same apparent power (100%). This leads to the same phase currents amplitude (100%), as shown in figure 38. Figure 39 shows the two DC link voltages and figure 40 shows the voltage on node N1.



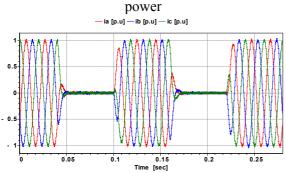


Fig. 38: Transmission line: phase currents

Fig. 40: Node N1: voltage

Taking into account the fact that the UPFC example is based on a 160 MVA device, it is impressive to see the high dynamic of such a FACTS. We can also observe that both objectives of the UPFC are fulfilled: voltage maintainance with the shunt compensator and full control of both active and reactive power with the series compensator.

Conclusion

The paper presents the complete modeling of a 3-level UPFC using the SIMSEN simulation software. The aim of the paper is to focus on the power quality and dynamic performances of a 3-level converter: low THD, reduced switching frequency, additional control of DC-unbalance. The UPFC model has been tested in both cases: steady-state and transient operating modes. The paper also shows the influence of the DC link voltage as well as the PWM carrier signal frequency on the THD of both shunt and series currents. It appears that, for the 3-level topology and a 50 Hz fundamental wave, a 900 Hz or 1050 Hz PWM frequency associated with a Flat Top Control and carrier signal phase adjustment is able to reduce the THD of both shunt and series currents, as well as the switching frequency of the GTOs. Further investigations have to be done in network applications including several UPFCs, for example the 14 nodes IEEE benchmark model [7]. Until now, such a network has only been simulated with simplified UPFC models (fundamental wave).

References

- [1] Horst E. Grüning, Jürgen K. Steinke, 'Design and Manufacturing of Application Specific High Power Converters', EPE 99, Lausanne, Switzerland.
- [2] A. Garcia-Cerrada, P. Garcia-Gonzalez, 'Control System for a UPFC in a Transmission Line', EPE 99, Lausanne, Switzerland.
- [3] I. Papic, P. Zunko, D. Povh, 'Basic Control of Unified Power Flow Controller', IEEE Transactions on Power Systems, Vol. 12, No. 4, November 1997.
- [4] Edvina Uzunovic, Claudio A. Canizares, John Reeve, 'EMTP Studies of UPFC Power Oscillation Damping', Proceedings of the North American Power Symposium (NAPS), San Luis Obispo, CA, October 1999, pp. 405-410.
- [5] Claudio A. Canizares, 'Power Flow and Transient Stability Models of FACTS Controllers for Voltage and Angle Stability Studies, IEEE/PES WM Panel on Modelling, Simulation and Applications of FACTS Controllers in Angle and Voltage Stability Studies, Singapore, Jan. 2000.
- [6] G. Scheuer, H. Stemmler, 'Analysis of a 3-Level-VSI Neutral Point Control for Fundamental Frequency Modulated SVC-Applications', AC and DC Power Transmission, Conference Publication No. 423, IEE, 1996.
- [7] S. Dupuis, M. Crappe, J. Trécat, 'Study of Optimal Location and Control of UPFCs in a standard Power System by Simulation with EUROSTAG', EPE 99, Lausanne, Switzerland.