Pico-Watt Source-Coupled Logic Circuits

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***Abstract*— This article explores the main tradeoffs in design of subthreshold source-couple logic (STSCL) circuits. It is shown analytically that the bias current of each STSCL gate can be reduced to few pico-amperes with a reliable logic operation. Measurements on different digital building blocks are provided to validate the main concepts presented in this paper. Implemented in conventional 0.18μm CMOS technology, the bias current of each STSCL gate can be reduced below 10pA, which corresponds to a power-delay product (PDP) of less than 500aJ.**

I. Introduction

Integrated circuit design techniques using subthreshold MOS devices have been mainly exploited for developing ultra low power systems [1], [2]. Operating with a very low bias current, the value of g_m/I_D in MOS devices achieves its maximum value in subthreshold regime. This means that the MOS integrated circuits exhibit maximum power-speed or power-delay efficiency when the devices are biased in subthreshold regime. These properties have made the design of ultra low power integrated circuits and systems using subthreshold MOS devices very attractive [1].

In [3]-[6] some techniques for implementing ultra low power digital systems using subthreshold devices have been proposed. It is shown in [3] that by proper biasing of CMOS logic gates in subthreshold regime it is possible to minimize the power consumption of the proposed system. To provide the proper operating condition for CMOS gates, supply voltage (V_{DD}) as well as the size of devices should be selected carefully. Speed of operation (f_{op}) and power dissipation (P_{diss}), both are reducing by reducing the supply voltage and it can be shown that there is an optimum V_{DD} value to have the maximum speed-energy efficiency [3].

The tight relationship between the supply voltage and the main specification of the system such as speed and power dissipation, makes this type of digital systems very sensitive to the supply voltage. Therefore, a very careful controlling system for adjusting and stabilizing the supply voltage is required. Source-coupled logic (SCL) circuits (first introduced in [7]) can be considered as an alternative for implementing digital systems with much less sensitivity to the power supply and hence more degrees of freedom for designing the logic cells [8]. Moreover, lower output voltage swing in the SCL gates compared to the CMOS gates provides more efficiency in terms of power-delay product (PDP). As shown in [9], power-delay product of an SCL gate can be lower than its CMOS counterpart by a factor of (V_{DD}/V_{SW}). These properties in addition to their lower sensitivity to the supply and substrate noise and less noise injection to the supply or substrate lines makes this type of circuits very attractive for implementing low power and high performance digital systems [8].

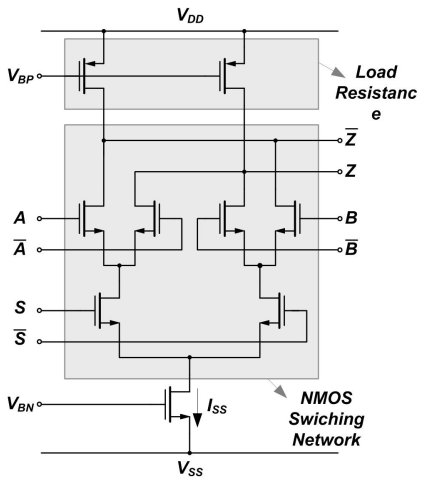

Fig. 1. A two input SCL based MUX. Here, PMOS devices are biased in triode region to realize the load resistances. Output voltage swing can be controlled by V_{BP}.

This article presents some techniques for implementing SCL circuits biased deeply in subthreshold regime to reduce the circuit power consumption. Measurement results show that it is possible to reduce the power consumption of each cell to few pico-watts and still provide stable logic operation. Section II presents a technique for implementing STSCL gates and the main design issues will be discussed. In Section III, experimental results are presented to validate the analytical models.

II. Subthreshold SCL

A. Circuit Topology

In SCL circuits, the logic operation takes place in current domain. A constant tail bias current is steered between two output branched based on the required logic operation. An NMOS switching network is the heart of this operation. The switched current at the output will be converted to voltage with a proper swing by the load resistances. Figure 1 shows

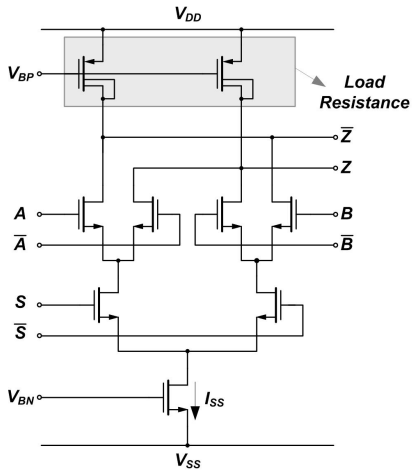

Fig. 2. Subthreshold SCL MUX uses bulk-drain shorted PMOS load devices to implement controllable and high value resistances [6].

an example of a 2-input SCL multiplexer (MUX) circuit. As far as the input voltage swing (V_{SW}) is high enough, by reducing the tail bias current (I_{SS}), NMOS switching network will continue its logic operation in current domain. Therefore, having a large input voltage swing and a bias current higher than the junction leakage current is sufficient to implement successfully subthreshold SCL circuits. Shown in [10], the minimum acceptable input voltage swing for complete switching of the tail bias current by NMOS differential pair is mU_T in which $m \approx 4$, and U_T is the thermodynamic (thermal) voltage ($U_T \approx$26mV in room temperature). Therefore, a load resistance as large as $R_L = mU_T/I_{SS}$ is needed to produce the required voltage swing at the output of each SCL gate. Comparing to the inherent output resistance of a PMOS device (i.e., $r_{sd} = \lambda L/I_{SS}$), and regarding that in a mature technology $\lambda L >> mU_T$ (λL is in the order of few volts, and mU_T=100-400mV), therefore it is not possible to employ the output resistance of a PMOS device for implementing the proposed load device.

To implement compact and high value resistances, the bulk-drain shorted PMOS configuration has been proposed in [6]. Based on this approach, minimum size PMOS devices can be used to implement controllable load resistances. At the following, the behavior of this type load devices will be explored in more details.

B. Behavior of the Load Device

As shown in Fig. 3, bulk-drain connected PMOS device exhibits a wider resistivity range in comparison to the conventional source-bulk connected configuration. Indeed, by increasing V_{SB} in this configuration, absolute threshold voltage value ($|V_{T,P}|$) will be reduced and hence I_{SD} will increase. Using EKV model [11] it is possible to express the I-V characteristics of the device as

$$I_{SD} = I_0 \cdot e^{\frac{V_{BG}-V_{T0}}{n_p U_T}} (e^{\frac{-V_{BS}}{U_T}} - e^{\frac{-V_{BD}}{U_T}}) \qquad (1)$$

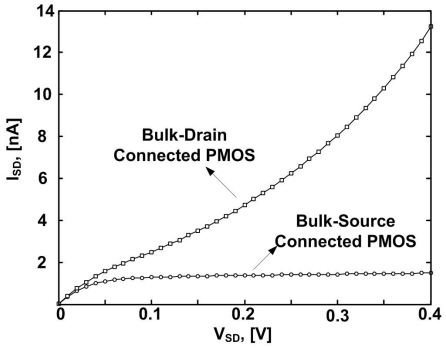

Fig. 3. I-V characteristics of a bulk-drain connected PMOS device in comparison the a bulk-source connected one.

in which $I_0 = 2n_p\mu C_{ox} \cdot \frac{W}{L_{eff}} U_T^2$, and n_p is the subthreshold slope factor of PMOS devices:

$$\frac{1}{n_p} = 1 - \frac{\gamma}{2\sqrt{V_G - V_{T0,P} + (\frac{\gamma}{2} + \sqrt{\Psi_0})^2}}. \qquad (2)$$

Here, γ is the body effect and Ψ_0 is the surface potential of the device. As can be seen in (2), n_p depends on gate voltage of the device and hence tail bias current of the proposed STSCL gate. Since V_{BD}=0, then

$$I_{SD} = I_0 \cdot e^{\frac{V_{DG}-V_{T0}}{n_p U_T}} (e^{\frac{V_{SD}}{U_T}} - 1). \qquad (3)$$

Small signal output resistance of this device also can be calculated as

$$R_{SD} = (\frac{\partial I_{SD}}{\partial V_{SD}})^{-1}$$

$$R_{SD} = (\frac{n_p U_T}{I_{SD}}) \cdot (\frac{e^{V_{SD}/U_T} - 1}{(n_p - 1)e^{V_{SD}/U_T} + 1}). \qquad (4)$$

To obtain a more accurate estimation of the behavior of this device, the effect of parasitic components should be also included in the model. Figure 4(a) illustrates the main parasitic elements associated with this device that affect its I-V characteristics. It is important to include the forward bias diode of the source-bulk junction in calculations, specially in very low power circuits where the tail bias current can be in the order of few pico-ampers. Including the effect of this parasitic diode:

$$I_{SD,tot} = I_{SD} + I_{SBO} \cdot e^{\frac{V_{SD}}{\eta U_T}}. \qquad (5)$$

in which I_{SBO} is the reverse saturation current of source-bulk junction and η stands for the emission coefficient of this device. As illustrated in Fig. 4(b), the expression (5) can predict the I-V behavior of the proposed load device very well. To detect the amount of current of this parasitic diode and hence bias properly the STSCL gate with minimum tail bias current, the bias circuit shown in Fig. 4(c) can be employed.

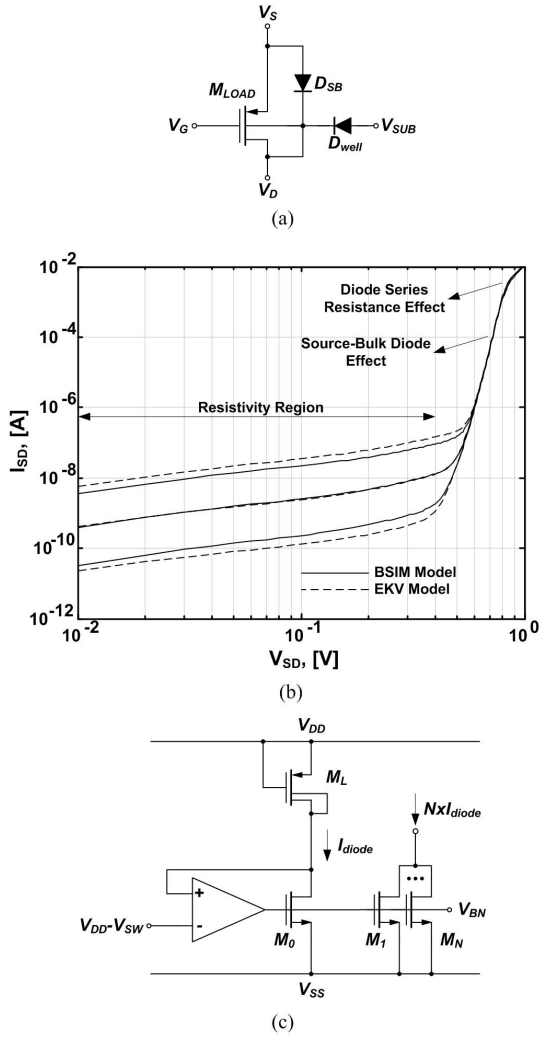

Fig. 4. (a) PMOS load device and its main associated parasitic elements. (b) I-V characteristic of the proposed PMOS load device based on (5). (c) Bias generator circuit to detect the minimum bias current for the proposed STSCL gate.

C. Leakage Current

While in CMOS logic gates, the subthreshold off current of the devices comprises the main part of the circuit leakage current, in STSCL gates it is not the main issue. Indeed, NMOS differential pairs operate well as a switch even for very low bias currents. It is even possible to use low or zero threshold voltage NMOS devices for this purpose. The operation of this part of circuit is limited mainly by the junction leakage current of the NMOS devices. However, these leakage currents are generally negligible in comparison to the forward bias current of the bulk-source junction of the PMOS devices as indicated in Section II.B.

Figure 5 proposes a simple topology for reducing the current injection of the forward biased bulk-source junction of the PMOS load devices. Based on this topology, by increasing the total series resistance of the diode, its bias current can be

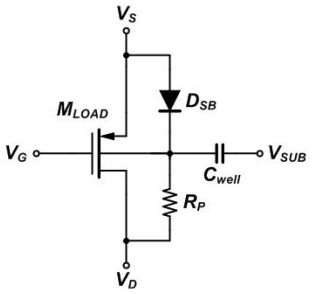

Fig. 5. Reducing the leakage current by increasing the series resistance of the forward biased diodes.

reduced considerably. It can be shown also that employing series resistances as illustrated in Fig. 5 can isolate the parasitic capacitance of the nwell-to-substrate junction (C_{well}) from the output node and hence reduce the total gate propagation delay. Simulations show that this parasitic capacitance is about a few hundred of aF for a minimum size PMOS device. Therefore, this technique can be useful when the load capacitance is not much larger than C_{well}.

D. Compound Structures

Compound SCL gates with merging two or more logic operations in a single gate provides the possibility to reduce the power consumption and improve the speed of operation simultaneously. Figure 6 shows an example in which an AND gate and an XOR gate are merged together to construct the proposed compound logic operation. Using this technique, it is possible to have only one pair of output load devices instead of two and also halve the total current consumption. Assuming that the time constant at the output nodes of each SCL gate is equal to

$$\tau_L = R_L C_L = \frac{V_{SW} C_L}{I_{SS}} \tag{6}$$

then the total equivalent time constant of the circuit of a simple two step SCL gate will be:

$$\tau_{tot,A} \approx 2\frac{V_{SW} C_L}{I_{SS}} \tag{7}$$

On the other side, in Fig. 6, the total time constant of the circuit is

$$\tau_{tot,A} \approx (\frac{V_{SW} C_L}{I_{SS}}) + N(\frac{U_T C_S}{I_{SS}}) \tag{8}$$

in which C_S is the parasitic capacitance seen from the source of each NMOS differential pair. Here, it is assumed that the time constant at the intermediate nodes of a compound SCL gate is $\tau_i = C_S/g_{ms}$ (see Fig. 6) and the total time constant can be calculated by $\tau_{tot} = \tau_L + \sum_{i=1}^{N} \tau_i$ [10]. Comparing (7) and (8) it can be concluded that as far as $NU_T C_S << V_{SW} C_L$, or

$$N << \frac{V_{SW} C_L}{U_T C_S} \tag{9}$$

stacking differential pair stages will not degrade the speed of operation. Simulations show that using the proposed technique

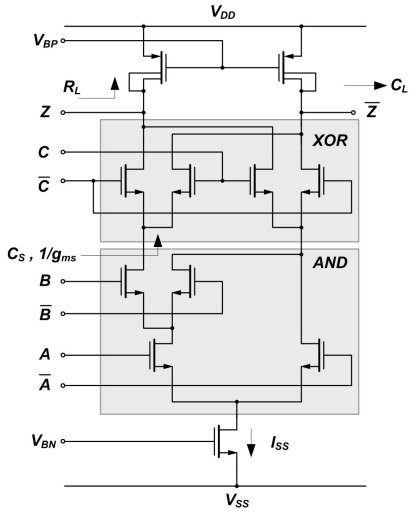

Fig. 6. Compound STSCL gate (AND operation followed by XOR gate).

can reduce the power dissipation of an (8×8) Multiplier by about 40% and at the same time improve the speed of operation.

E. Pipelined STSCL

One possible approach for improving the power-speed performance of the STSCL based circuits is increasing the activity rate by using a simple two-phase pipelining technique. Figure 7 shows one possible approach to implement two-phase latch-based pipelining where the output of each gate is latched during one clock phase, and passed on to the next stage during the other clock phase - effectively reducing the maximum logic depth to two consecutive gates. Instead of using explicit latch stages, such two-phase pipelining can be achieved by increasing and reducing the tail current bias of alternating stages, using the gate terminal of the tail current bias transistor of each stage as the clock input [V_{BN} in Fig. 8]. In this approach, as illustrated in Fig. 8 for example of an STSCL full adder (FA) gate, the current bias of odd stages is reduced to a low (yet non-zero) level to retain (hold) their output while the current bias of even stages is raised to the nominal operating value to enable evaluation. Very simple cross-coupled keeper stages connected to each gate output ensure that the output levels do not degrade significantly during the hold phase. Since the keeper stage is used to maintain the latest state of the output of each gate, it does not need to be very fast. Therefore, the bias current of keeper stage ($I_{SS,L}$) can be chosen as low as 1% of the bias current of the main gate (I_{SS}). This means that the power overhead of the keeper stages is virtually negligible. Meanwhile, since the bias current of half of the gates is almost zero in each clock phase, the overall power consumption of the system will be reduced by a factor of two. In this way, it is expected that PDP of the circuit reduces by a factor of N where N stands for logic depth of the circuit.

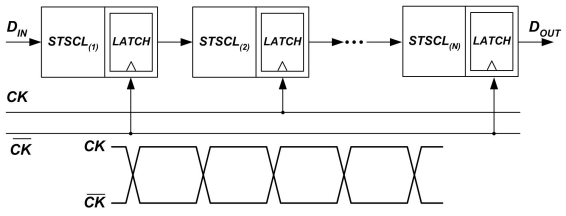

Fig. 7. Pipelining technique for improving the activity rate in STSCL topology.

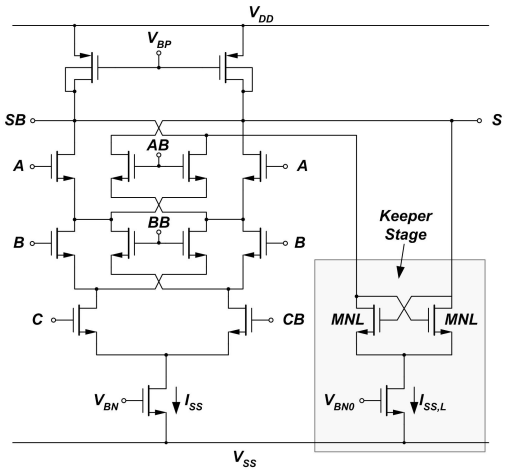

Fig. 8. (a) STSCL full adder and keeper stage. Here, the tail current bias V_{BN} is switched according to CK (or $\overline{CK}$) while V_{BN0} is kept as a constant bias. (b) Simulated output of the pipelined FA chain showing the holding and tracking modes of operation.

III. Experimental Results

A test chip has been fabricated in a conventional 0.18μm CMOS technology to verify the concept of subthreshold SCL circuits. Since minimum size devices have been used for design of STSCL gates, the layout of each cell is very small. Figure 9 shows the layout area of a two input STSCL MUX where the total area of the cell is 6×9 μm^2.

A. Load Device I-V Characteristics

The measured I-V characteristics of the proposed PMOS load device is shown in Fig. 10. As predicted by (5), for $V_{SD} < 0.45V$, the device can be used successfully as a resistance. This voltage headroom is sufficient for implementing STSCL gates where a voltage swing of 150mV to 300mV is required. For higher V_{SD} values (as can be seen in Fig. 10(b)), the current of the forward biased diode will be dominant. In very high bias currents, the series resistance in the path of source-bulk diode limits the exponential I-V characteristics of this diode.

B. Ring Oscillator Test

A ring oscillator using STSCL MUX gates as delay cells has been implemented. In the proposed test chip, it is possible

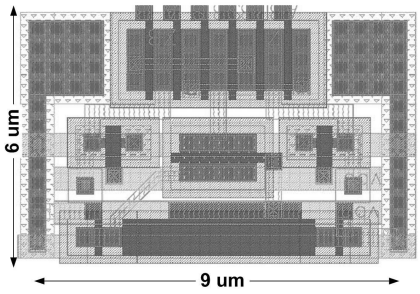

Fig. 9. Layout of STSCL Mux.

to control the tail bias current and also the load capacitance at the intermediate nodes of the ring oscillator.

As illustrated in Fig. 11(a), the oscillation frequency reduces by increasing the load capacitance. Here, a capacitor bank is used to set the load capacitance.

Figure 11(b) shows the oscillation frequency versus tail bias current in two different supply voltages. As can be seen, it is possible to adjust the oscillation frequency over more than four decades. Measurements also show that it is possible to reduce the tail bias current of each cell to I_{SS} ≈2pA with a supply voltage of as low as V_{DD}=400mV. For lower bias currents, oscillation frequency remains almost constant. It is mainly because of leakage current of the current mirrors used to control the tail bias current. This leakage current provides a minimum bias current for each cell and hence the oscillation frequency does not change for lower input bias currents.

Meanwhile, measurements show that the V_{SW} can be reduced to 80mV in the test oscillator. Therefore, for reliable operation V_{SW} >80mV (in room temperature) is feasible.

In these measurements, the minimum load capacitance that can be selected in the capacitor bank is 70fF. In a practical case, the load capacitance can be much smaller and hence operating frequency can be higher correspondingly. Figure 12 shows the measured oscillation frequency for two different types of oscillator: one based on the conventional SCL topology uses triode PMOS load devices (shown in Fig. 1) and the other one based on the proposed topology (Fig. 2). As can be seen, the minimum tail bias current of conventional topology can be reduced not less than 25nA while in the proposed topology, it can be reduced down to few pA. In these two oscillators, there is no capacitor bank and the loading is only due to the interconnect and device parasitic capacitances and therefore the oscillation frequency is much higher than the measurements shown in Fig. 11(b).

Figure 12 also depicts that the power-delay product of the oscillator is almost constant for a very wide range. For V_{DD}=0.4V, PDP of a single gate is approximately 500aJ. Meanwhile, it can be seen that the speed of operation and hence gate delay is independent of the supply voltage. This property is specially desirable in applications where supply voltage can vary considerably.

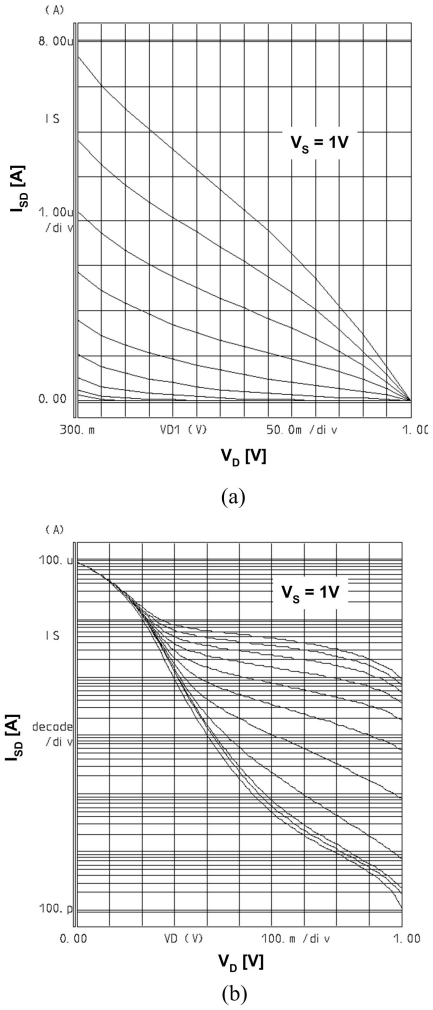

Fig. 10. Measured I-V characteristics of the PMOS load device for different V_{SG} values: (a) linear scale, (b) logarithmic scale.

C. Pipelined Adder Circuit

Figure 13 shows the test chip photomicrograph including two chains of adder stages, one uses simple STSCL adders and the other one uses pipelined STSCL adder gates as shown in Fig. 8.

The measured power-delay product for the two topologies are shown in Fig. 14. Both topologies show a relatively constant PDP over their tuning range. The average PDP for simple and pipelined FA chains are 2.6pJ and 0.18pJ, respectively, which corresponds an improvement factor of about 14. Measurements for pipelined adder chain have been performed for two different bias current of $I_{SS,L}$: $I_{SS,L} = I_{SS}/10$ and $I_{SS,L} = I_{SS}/100$. As can be seen in Fig. 14, the results for two bias currents for the keeper stage are very close. Therefore, it is possible to reduce the bias current of the keeper stage to $I_{SS}/100$ and hence minimize the power overhead of this stage.

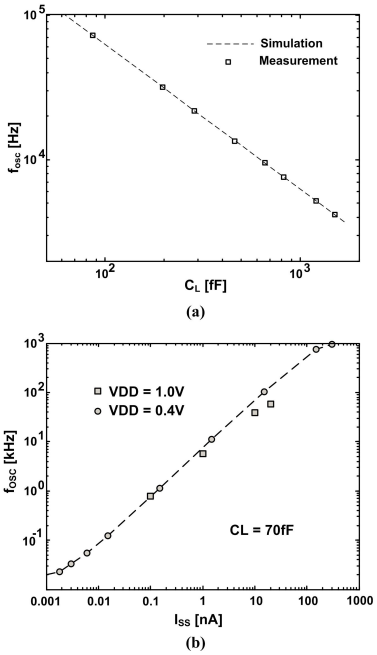

Fig. 11. Measured oscillation frequency of an STSCL-based ring oscillator: (a) for different capacitive load at the output of each delay cell, (b) for different tail bias currents (here C_L is set to 70fF) from the capacitor bank.

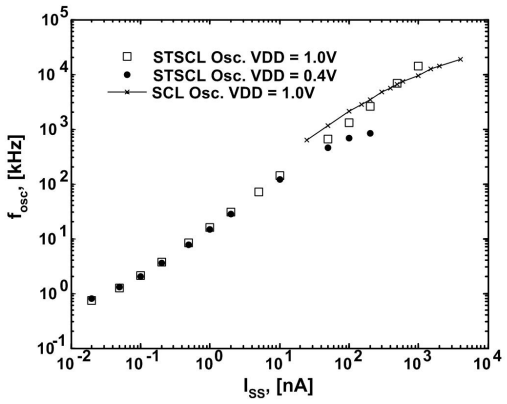

Fig. 12. Measured oscillation frequency of an STSCL oscillator without any load capacitance. Oscillation frequency is shown for V_{DD}=0.4V and 1.0V. The oscillation frequency is compared to a conventional SCL based oscillator where triode PMOS loads have been employed. Here, the load capacitance on each delay cell is limited to the interconnect and device parasitic capacitance.

IV. Conclusion

The main specifications of subthreshold source-couple logic circuits have been analyzed. The I-V behavior of the load device used to implement high value resistances has been analyzed and compared to the measurement results. The main sources of leakage current of the proposed topology have been discussed. Meanwhile, the possibility for using compound SCL gates in order to reduce the power-delay product has been investigated. Measurement results for confirming the analysis and simulation results have been provided. Based on the measurement results, it is possible to reduce the bias current of each cell to few pico-ampers with a supply voltage as low as 400mV.

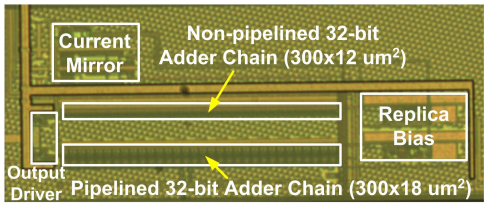

Fig. 13. Test chip photomicrograph.

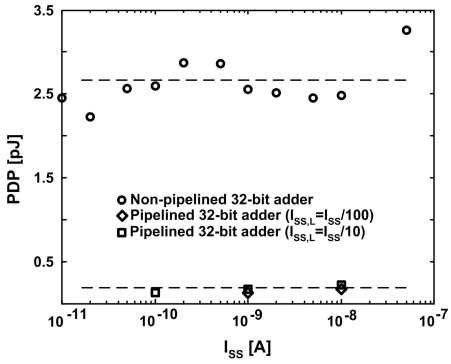

Fig. 14. Measured power-delay product for the two topologies.

References

[1] E. Vittoz, "Weak Inversion for Ultimate Low-Power Logic", in *Low-Power Electronics Design*, Editor C. Piguet, CRC Press, 2005.

[2] E. Vittoz and J. Fellrath "CMOS analog integrated circuits based on weak inversion operation", in *IEEE J. Solid-State Circuits*, vol. 12, no. 3, pp. 224-231, Jun. 1977.

[3] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1778-1786, Sep. 2005.

[4] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," *IEEE Trans. Very Large Scale Integ. (VLSI) Syst.*, vol. 9, no. 1, pp. 90-99, Sep. 2001.

[5] C.H.-I. Kim, H. Soeleman, and K. Roy, "Ultra-low-power DLMS adaptive filter for hearing aid applications," *IEEE Trans. Very Large Scale Integ. (VLSI) Syst.*, vol. 11, no. 6, pp. 1058-1067, Dec. 2003.

[6] A. Tajalli, E. Vittoz, Y. Leblebici, and E. J. Brauer, "Ultra low power subthreshold MOS current mode logic circuits using a novel load device concept," *in Proc. of Eur. Solid-State Cir. Conf. (ESSCIRC)*, Munich, Germany, Sep. 2007, pp. 281-284.

[7] D. W. Murphy, "High speed non-saturating switching circuits using a novel coupling technique," in *ISSCC Dig. Tech. Papers*, pp. 48-49, Feb. 1962.

[8] S. Badel "MOS current-mode logic standard cells for high-speed low-noise applications," *PhD Dissertation*, Ecole Polytechnique Fédérale de Lausanne (EPFL), Switzerland, 2008.

[9] J. M. Musicer and J. Rabaey, "MOS current mode logic for low power, low noise CORDIC computation in mixed-signal environment," *in Proc. of Int. Symp. on Low Power Elect. and Des. (ISLPED)*, pp.102-107, 2000.

[10] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiely & Sons Inc., Fourth Edition, 2000.

[11] C. Enz, F. Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," in *Analog Int. Circ. and Signal Proc. J.*, vol. 8, pp. 83-114, Jun. 1995.