Cross Connected Multilevel Voltage Source Inverter Topologies for Medium Voltage Applications

THÈSE N^{O} 4162 (2008)

PRÉSENTÉE LE 22 AOÛTE 2008

À LA FACULTE SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE D'ÉLECTRONIQUE INDUSTRIELLE
PROGRAMME DOCTORAL EN ENERGIE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

PAR

Toufann CHAUDHURI

ingénieur électricien diplômé EPF
de nationalité suisse et originaire de Lausanne (VD

acceptée sur proposition du jury:

Prof. A. Germond, président du jury
Prof. A. Rufer, directeur de thèse
Dr T. Meynard, rapporteur
Prof. J.-J. Simond, rapporteur
Dr P. Steimer, rapporteur

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE
Suisse
2008

Preface

Looking back at the past 3 years of my professional life, I feel really privileged. After my studies at the Swiss Federal Institute of Technology in Lausanne (EPFL) in 2004, where I specialized in power electronics in the last years, I was given the chance to start a PhD work at the ABB Corporate Research Center in Baden-Dättwil, in collaboration with EPFL. Surrounded by skilled colleagues with a very high level of knowledge in their respective fields of expertise, I progressed quite rapidly, learning from their experiences and help. The work presented here is the result of a 3 years collaboration between the industry and the academical world (2005-2008), during which 2 patents on subjects covered by this thesis were filed.

Firstly I would like to thank prof. Alfred Rufer, from the Industrial Electronics Laboratory (LEI) at EPFL, for having been my PhD supervisor. I would like to express my gratitude for him accepting me as a PhD student, while I was working at the ABB Corporate Research Center, 200km away from his university. Always willing to offer skillful advices and sharing his knowledge, he certainly contributed in a very positive way to the results of this work.

I also would like to express my grateful thanks to Dr. Peter Barbosa who supported me at the Corporate Research Center during the two and half first years of my PhD work. His proposals and ideas gave shape to the topologies presented here, and without his advices the work would certainly have taken a different turn.

Thanks also go to Dr. Peter Steimer, from ABB Industries in Turgi, who also offered a willing support throughout the work. Although his participations remain moderate in terms of quantity, they have always been of very high quality. He definitely has his share of merit in the two patents that were filed.

I would like to thank the President of the Board of Examiners, prof. Alain Germond, and the other members of the Jury, prof. Jean-Jacques Simond, Dr. Thierry Meynard and Dr. Peter Steimer for their participation in the examination of this thesis, and for their helpful comments regarding this dissertation.

I also express my gratitude and thanks to all my ABB Corporate Research colleagues for the great working atmosphere they contributed to create, notably to Dr. Antonio Coccia who became our new group leader at the beginning of year 2008, and who always supported me in my work.

Special thanks go to Christoph Haederli with whom I have had very interesting and motivating discussions on various technical questions. I thank him for the fruitful collaboration on the prototype. I also would like to express my gratitude to Dr. Manfred Winkelnkemper for teaching me how to program the ABB AC800 PEC control system, and for his support in general during his years at the Corporate Research Center.

I equally thank my colleagues of LEI for their everlasting good mood and the pleasant atmosphere they create at the university. I also thank Frederic Mermod for the work he did on the prototype during his master thesis at ABB.

Finally, I would like to express my gratitude to my friends and to my family for their encouragements and the motivation they gave me to finish this work. For sure I would not have been able to come to an end without them and the energy I got from all the social activities I could undertake with them. Special thanks to my beloved girlfriend Mélanie and to my parents.

Toufann Chaudhuri
July 2008

Summary

Multilevel voltage source inverters where first introduced in the early 1980s. Since then, they have been continuously developed, offering a wide new research area in power electronics. The popularity of multilevel solutions come from the advantages that they offer: improved output quality, voltage sharing in high voltage applications, increased power density or reduction of filtering costs.

Two completely new and innovative cross-connected topological families for advanced multilevel voltage source inverters are introduced in this thesis. The motivation for this work stems out from the need to generate multiple output levels while keeping the reliability as high as possible. The offered solutions are able to address the problematic, but of course they do not come without a price: A higher control complexity and more semiconductor blocking voltage capability are necessary in the design of such advanced converters.

The Cross Connected Intermediate Level (CCIL) Voltage Source Inverter is the first of the two new topologies presented here. It is built as a cascade of stages using capacitors which are connected to each other by means of cross connected cell structures. The CCIL can be used in several configurations, like redundant or non-redundant switching state configurations for instance. A graphical model based on the physical properties of the inverter is proposed and an original fuzzy logic controller is designed for the balancing of the capacitor voltages and modulation of the inverter. The control algorithm is implemented and verified in simulations. The results are used to benchmark the topology against standard solutions and the conclusions are used to define what applications could benefit from such a converter structure.

The Common Cross Connected Stage (CCCS) Voltage Source Inverter is the second original contribution of this work in terms of topology. It

is built using the cross connected stage and its capacitor in a common configuration for the three phases of the inverter. Such a design allows to use only one stage per three phases. Because of the intrinsic three phased properties of this topology, a model based on space phasor representation is introduced. With the help of this model, a novel space phasor modulation strategy is derived and proposed. It allows to generate the three phased output voltages while using the available redundancies for balancing of the capacitor voltages. The resulting algorithm is first implemented and tested in simulation, and in a second step a test setup is built and the modulator is coded in VHDL. The simulation and experimental results obtained validate the topology and control concepts. A benchmarking of the CCCS solution is also done to understand what are the benefits and drawbacks of this solution.

Analysis and comparison of the new topologies allow to evaluate in an objective way the contributions brought by this work. It is found that the newly proposed solutions cover an area of multilevel inverters where not so many solutions were available prior to this work: Generation of multiple output levels with reduced number of passive and active components (thus increasing the reliability). The drawback is a higher blocking voltage requirement. Conclusions and case study are proposed to help assess the expected performances and choose the most suitable solutions for given applications.

Keywords: DC-AC voltage source inverter, Multilevel converter, cross connected, phase capacitors, medium voltage, harmonic distortion, power density, topology.

Résumé

Les convertisseurs multiniveaux furent introduit au début des années 1980. Depuis ils ont connu de multiples évolutions, offrant un large domaine de recherche en électronique de puissance. La popularité de ces topologies tient au fait des multiples avantages qu'elles offrent : amélioration de la qualité du signal de sortie, partage des tensions de blockage dans les applications haute tension, augmentation de la densité de puissance ou encore réduction des coûts liés au filtrage.

Deux familles de topologie complètement nouvelles et innoventes pour convertisseurs multiniveaux avancés sont présentées dans cette thèse. La motivation de ce travail vient de la nécessité de générer toujours plus de niveaux tout en gardant une fiabilité aussi élevée que possible. Les solutions qui sont proposées sont capables de répondre au cahier des charges, mais elles ne viennent pas sans un prix à payer : Ces convertisseurs avancés nécessitent une logique de commande plus élaborée et de plus grandes tensions de blocage sur les semiconducteurs.

Le convertisseur de tension "Cross Connected Intermediate Level" (CCIL - niveau intermédiaire connecté en croix) est la permière des deux topologies présentées ici. Il est constitué en cascadant des étages utilisant des capacités connectées entre-elles par une structure topologique en croix. Le convertisseur CCIL peut être utilisé dans différentes configurations, par exemple avec des états de commutation redondants ou non-redondants. Un modèle graphique basé sur les propriétés physiques de l'onduleur est présenté, et une stratégie de commande originale, basée sur la logique floue, est proposée pour l'équilibrage des tensions capacités et la modulation. L'algorithm de réglage et de modulation est implanté et validé en simulation. Les résultats sont utilisés afin de comparer la topologie à d'autres structures plus traditionnelles, et les conclusions sont utilisées afin de définir plus

précisément quelles applications pourraient bénéficier de cette structure de convertisseur.

Le convertisseur de tension “Common Cross Connected Stage” (CCCS - étage commun connecté en croix) est la seconde contribution originale de ce travail en terme de topologie. Il est constitué d'un étage connecté en croix avec sa capacité, et qui est connecté en commun avec les trois phases de l'onduleur. Cette conception permet de n'avoir qu'un étage par trois phases. A cause des propriétés triphasées intrinsèques de la topologie, un modèle basé sur le phaseur spatial est introduit. Avec l'aide de ce modèle, une stratégie de modulation par phaseurs spatiaux novatrice est déduite et proposée. Elle permet de générer les tensions de sortie triphasées tout en utilisant les redondances à disposition pour l'équilibrage des tensions des capacités. L'algorithme résultant est tout d'abords implanté et testé en simulation, puis dans un second temps, un prototype est construit et le modulateur codé en VHDL. Les résultats de simulations et les résultats expérimentaux obtenus permettent de valider la topologie et le concept de réglage. Une évaluation de la topologie CCCS est aussi faite, afin de comprendre quels en sont les avantages et les inconvéniants.

L'analyse et la comparaison de ces nouvelles topologies permettent une évaluation objective de la contribution apportée par ce travail. Il est trouvé que les solutions novatrices proposées permettent de couvrir un domaine de l'électronique de puissance où il existait encore peu de solution : La génération de niveaux multiples avec un nombre restreint de composants passifs et actifs (d'ou une augmentation de la fiabilité). La contrepartie est une augmentation des tensions de blocage des semiconducteurs utilisés. Les conclusions ainsi qu'une étude de cas sont présentés afin d'aider à l'évaluation des performances attendues, et afin de choisir la solution la plus adaptée à chaque application.

Mots-clés : Convertisseur de tension DC-AC, onduleur multiniveaux, cross connected, capacités de phase, moyenne tension, distortion harmonique, densité de puissance, topologie.

Contents

Notations

Abbreviations

$\#L$	# of Levels
$ANPC$	Active Neutral Point Clamped
AC	Alternative Current
$CCCS$	Common Cross Connected Stage
$CCIL$	Cross Connected Intermediate Level
CPU	Central Processing Unit
DC	Direct Current
DPS	Digital Signal Processor
$FPGA$	Field Programmable Grid Array
HV	High Voltage (>10kV)
$HVDC$	High Voltage Direct Current
$IGBT$	Insulated Gate Bipolar Transistor
$IGCT$	Integrated Gate Controlled Thyristor
LV	Low Voltage (<1kV)
$PEBB$	Power Electronic Building Block
MV	Medium Voltage (<10kV)
NPC	Neutral Point Clamped
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter

Roman Symbols

A	Amperes	A
C	Coulomb	$A \cdot s$

E	Energy	J
F	Farads	$\frac{A \cdot s}{V}$
H	Henry	$\frac{V \cdot s}{A}$
J	Joules	$W \cdot s$
L	Levels	$-$
S	Apparent Power	$V \cdot A$
V	Volts	V
VAr	Reactive Power	$V \cdot A$
W	Active Power	$V \cdot A$

Greek Symbols

Ω	Resistance	V/A

CHAPTER 1

Introduction

1.1. A general picture

Since the first introduction of multilevel topologies in the early 1980's, [1], many different solutions and applications have been developed for advanced industrial applications, for instance [2]. The advantages offered by multilevel structures are numerous, notably in terms of harmonic contents and signal quality, costs, modularity, blocking voltage repartition.

This research work was started when the *ABB Corporate Research Center* was working on a hybrid medium voltage prototype for a large windpower energy conversion system, in the range of 5-10MW. The grid interfaced multilevel inverter, based on the ANPC topology, [3], generates 5 level at the output but still requires a filter to be compliant with the most stringent standards. At these power ratings, the output filter is quite massive, and thus a reduction in it's size, or even a complete removal of the filter, offers interesting perspectives in terms of cost reduction and increase in power density. A project was initiated to propose some solutions for improving the signal quality. This means increasing the number of levels generated by the converter, since increasing the switching frequency does not sound reasonable in the MW range.

When this work was initiated there were already a wide variety of multilevel inverter topologies available on the market. It was questionable whether investigating new topologies was justifiable or not. Some elements of answer to this fundamental question can be found with a closer look at

the existing topologies. But before doing so, it should still be mentioned that from a purely academical and technical point of view, it is always interesting to develop new structures and study their properties. On the other hand, from the industrial perspective, it requires more than just novelty to justify a research and development effort on new topologies (although a research center can claim a more academical point of view).

Among the wide variety of existing multilevel inverter topologies, which are listed below, no specific solution seems to really stand out from the others. It does not mean that all the solutions offer the same performances. The reasons for choosing a specific topology are various, starting from intellectual property questions and going to costs, and more generally speaking, considering how given solutions perform depending on the application and the context. Because of their different intrinsic characteristics, some topologies can be very well adapted in some cases and totally unsuitable in some others. Therefore the optimal solution is often strongly dependent on a case to case analysis.

Another aspect that can be considered is the individual assessment of the topologies, and more specifically regarding their characteristics. The important criteria are not the same for everyone, for instance having a minimal stored energy or having the lowest number of semiconductor devices possible (with their influence on reliability, on conduction losses or on the costs tied to blocking capabilities). This can lead to fundamentally different approaches in design, conception and rating of multilevel solutions.

1.2. Structure of the work

In the following sections of this introductory chapter, a small overview of the state of the art in multilevel conversion is presented. A non exhaustive, but containing the main candidates for MV applications, list of existing topologies for 5L inverters is briefly reviewed. Electrical characteristics and control strategies are discussed to situate the background technical context to the reader.

Since the topologies are evaluated, the mains characteristics, advantages and disadvantages, are discussed. Lot of work has been done to propose specific solutions and workarounds for these topologies, but they are not discussed or considered in here. The comparison can seem rough, but it must be kept in mind that only the general behavior and trend of these topologies are of interest. As it was previously mentioned, the rating depends on more criteria than just factual analysis of the characteristics.

Chapter 2 then introduces the Cross Connected Intermediate Level (CCIL) Voltage Source Inverter. This is the first of the two new and orig-

inal multilevel topologies proposed in this work. It is studied in details theoretically and in simulation. The topology is then benchmarked such as to assess its main characteristics compared to the existing solutions.

Chapter 3 introduces the Common Cross Connected Stage (CCCS). This second topological proposal certainly presents a high interest from the novelty and the technical point of view. This topology is also validated experimentally in a test setup.

For each of the aforementioned topologies, the structure of the study is the same. The main topological and electrical characteristics are analyzed, a model is proposed, and a modulation and control algorithm is defined based on the model. The concepts and topologies are then simulated to verify if the proposed solutions are valid, and then they are benchmarked against some traditional multilevel topologies to assess the difference in performances.

1.3. State of the art

1.3.1. NPC

Electrical characteristics

The NPC (Neutral Point Clamped) inverter, Figure 1.1, introduced in the early 80's by Baker, [4], and by Nabae et al., [1], [5], is composed of 2 DC-link capacitors (common for the three phases), 2 active switches (IGBTs) and 2 diodes per level and per phase. Increasing the number of generated levels is problematic from two point of views. The number of required diodes can quickly become prohibitive and the balancing the the DC-link middle points is not possible at high modulation indexes.

Modulation and Control

The DC-link balancing problem is well known and a certain number of solutions are already proposed, like [6], [7]. The modulation index limit is situated in the range of $m = 0.5 - 0.6$ depending on the modulation strategies, at active power generation. With higher modulation indexes it is not possible to balance the middle points anymore unless an active front end is used to balance the DC-links in a back to back configuration, or a specific external circuit is used. For those reasons, this topology is not really adapted for generation of many levels.

For reactive power however, the topology can be interesting since the balancing problems can be addressed, [8], and the maximum modulation index can be reached.

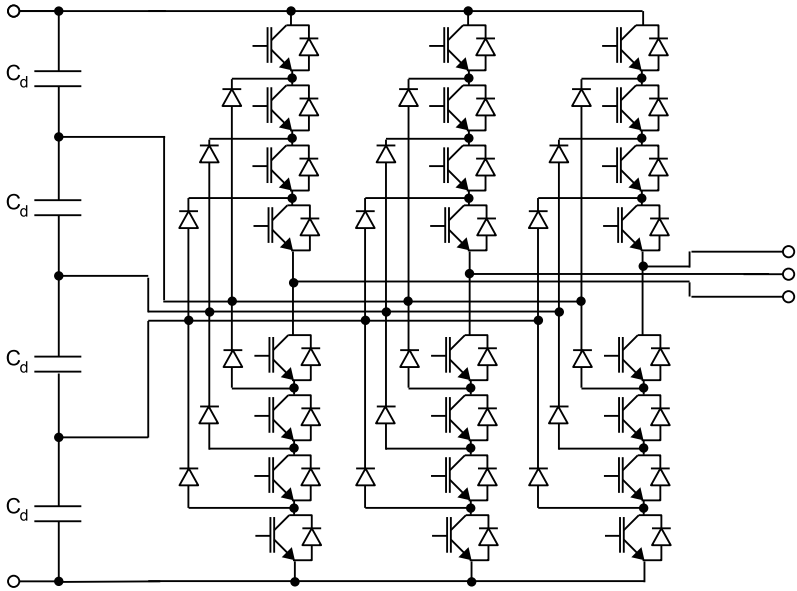


Figure 1.1.: *3 phase 5L NPC inverter*

1.3.2. Cascaded H-Bridge

Electrical characteristics

The 5L Cascaded H-Bridge inverter, [9], shown on Figure 1.2, is composed of series connection of H-Bridges. It requires 4 active switches and one capacitor per phase and per level. The major drawback of this topology is the necessity to supply the capacitors or store a lot of energy into them, as they cannot be balanced easily during operation (at active power). For the generation of many output levels, this can results in a large transformer with multiple secondaries and/or really large capacitive energy.

Modulation and Control

Common mode regulation strategies can be used for balancing of the capacitors during operation. The advantage is that the energy can be reduced since it is not necessary to wait one whole period, but the modulation index is then limited. Various strategies are already proposed, but they are not discussed here (see for instance [10]).

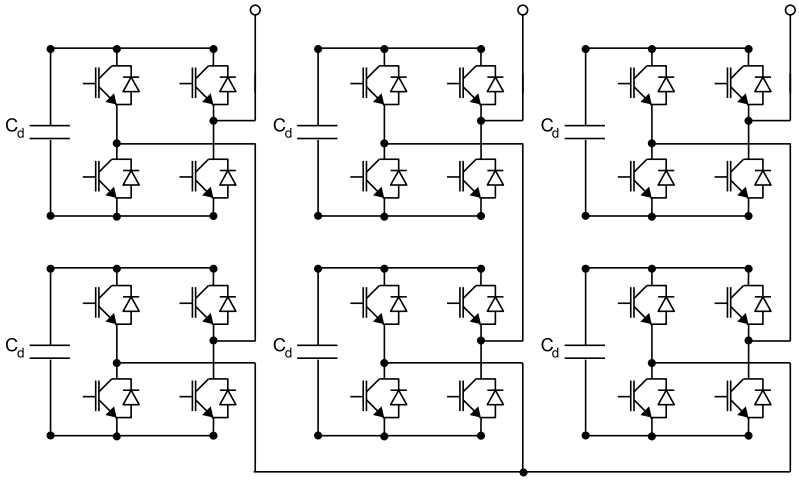


Figure 1.2.: *3 phase 5L cascaded H-Bridge inverter*

1.3.3. Imbricated cells (flying capacitor)

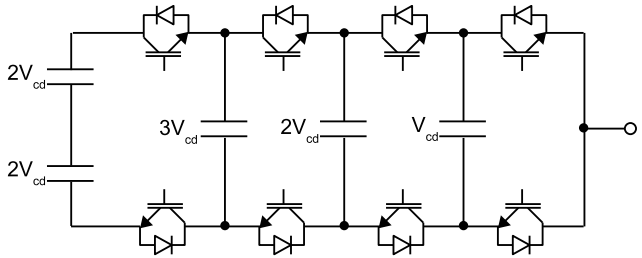


Figure 1.3.: *Single phase 5L flying capacitor inverter*

Electrical characteristics

The flying capacitor topology, introduced in 1992 by T.Meynard and H.Foch, [11], [12], [13], and shown on Figure 1.3, is a very interesting structure which minimizes the sum of the blocking voltage of every switches of the circuit (i.e. the total amount of silicon installed). It requires 2 switches

and 1 capacitor per phase and per level. The capacitor voltages are fractions from $\frac{N}{N}$ to $\frac{1}{N}$. There is no need to supply them since they can be balanced during operation for any power factor and modulation index. Every switch needs to block only the basic voltage step. The drawbacks of this topology are that total stored energy can become quite large, especially when the switching frequency cannot be increased (typically for MV or HV applications), and that there is a high number of components.

Modulation and Control

The control of the flying capacitor topology is not an issue with modern control hardware. Many papers treat about voltage balancing strategies, like [14] for instance.

1.3.4. SMC

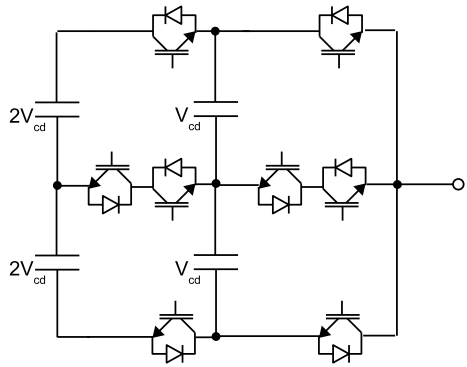


Figure 1.4.: *Single phase 5L SMC inverter*

Electrical characteristics

The SMC (Stacked Multi Cell) inverter, [15], Figure 1.4, is a generalization of the flying capacitor topology. It requires per phase for each extra level 2 capacitors and 4 active switches (2 at each end and 2 in anti-series in the middle). Similarly to the flying capacitor topology, the SMC also allows balancing of the capacitors within the topology and additionally also allows to control the neutral points of the DC-link. The advantage with the SMC is that the DC-link can be split over several capacitors. But the

number of switching elements is no longer optimum compared to the flying capacitor solution.

Modulation and Control

The modulation strategy to balance the capacitors is not extremely complicated and can be handled by modern DSP control systems, like the flying capacitor topology. Natural balancing schemes are also available, [16].

1.3.5. Other topologies

Aside the topologies presented previously, there is also a couple of other multilevel topologies which exist. The ANPC topology is a modification of the NPC structure offering an improvement from the point of view of the loss balancing within the semiconductor devices, [17]. It is discussed in greater details in §1.3.7.

The generalized ANPC topology (Figure 1.5-top), [3], is an extension of the ANPC structure, which allows a good control of the neutral point current, but is not optimal from the point of view of the number of components needed and also regarding the stored energy.

The generalized multilevel inverter topology by F.Z.Peng, [18], shown on Figure 1.5-bottom, is another kind of multilevel topology. What strikes with this topology is the very large number of active and passive components. It is quite likely not suitable for MV and HV applications. The topology was initially designed for LV applications.

The M2LC is a modular multilevel topology, [19], Figure 1.6. This topology uses 2 unipolar strings per phase to generate a multilevel output. It is possible, with this topology, to balance the capacitors more often then just once in a grid period which helps reducing the stored energy. The large number of components and the unipolar string approach are well suited for HV applications. The advantages are not so clear regarding application of the topology to MV converters.

1.3.6. Hybrid topologies

Hybrid topologies, [20], [21] or [22], represent a very large family. They are resulting from the combination of several type of topologies. Theoretically speaking, the number of possible combinations, thus the number of different topologies, is extremely large. The combinations can be on a phase level, or on a converter level, with different phase configurations resulting in composite multilevel topologies.

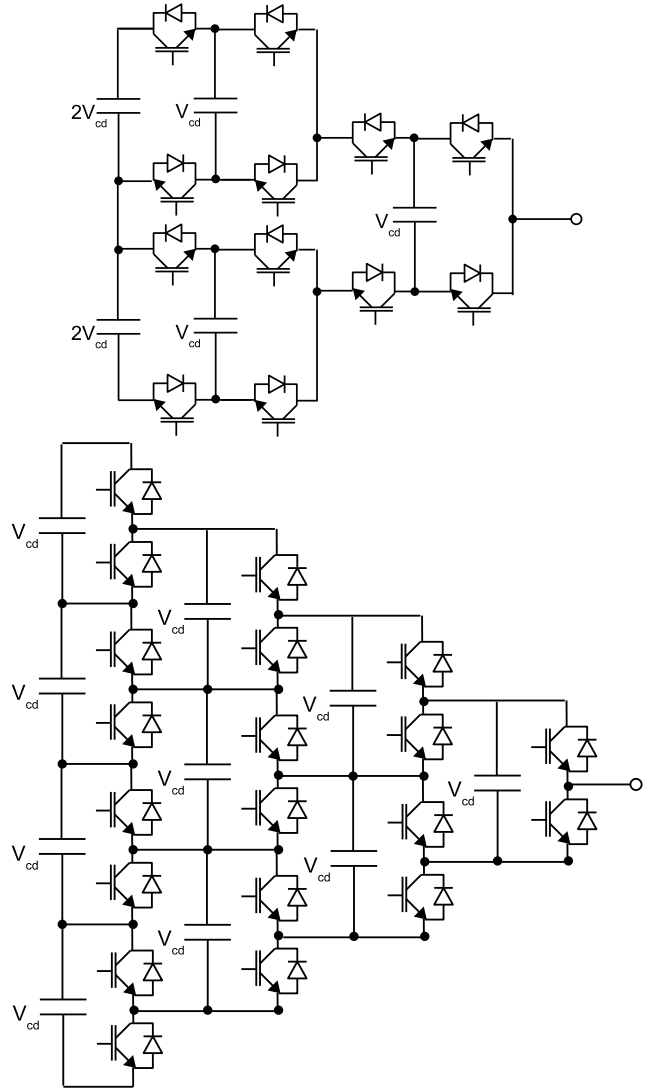


Figure 1.5.: *Top: Single phase 5L generalized ANPC inverter. Bottom: Single phase 5L generalized multilevel inverter topology by F.Z.Peng*

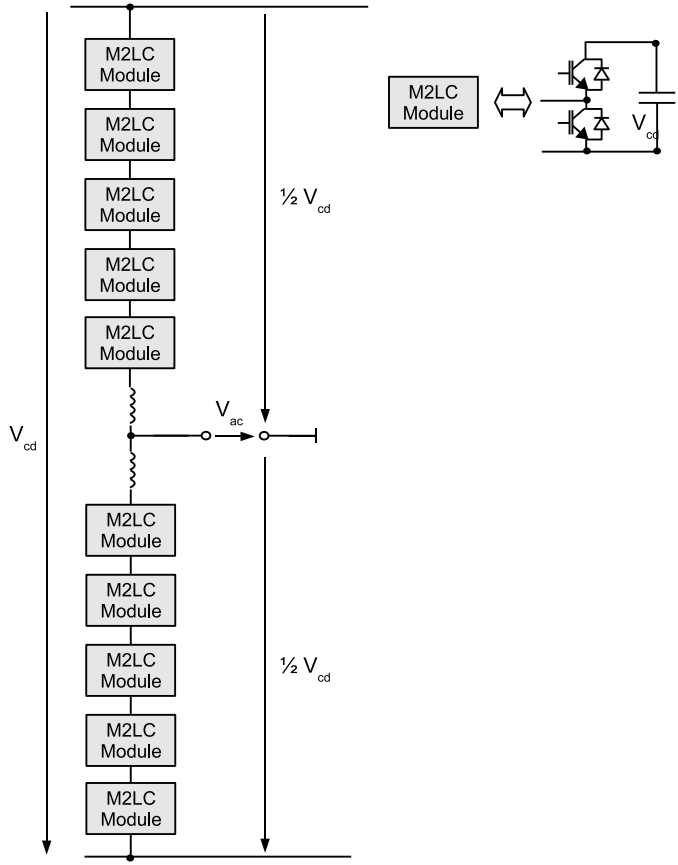


Figure 1.6.: *Single phase 5L M2LC inverter topology*

It is hard to assess the hybrid topologies in general, because of their diversity. It would be required to draw general characteristics resulting from all the possible different combinations of basic cells, and then extract the main characteristics for a comparison.

The 5L ANPC topology, which is the main topology of concern in this work, and which is introduced in §1.3.7, is in fact a hybrid topology. It is the combination of an ANPC and one flying capacitor stage.

1.3.7. The 5L ANPC topology

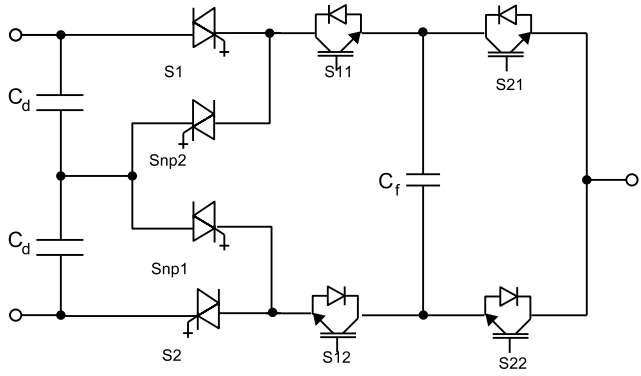


Figure 1.7.: *The single phase 5 level ANPC voltage source inverter*

The base topology considered in this work is the 5 level ANPC voltage source inverter, [17], [23], shown on Figure 1.7. This multilevel topology is suitable for many LV and MV applications. In the initial project from which this work was initiated, the topology was studied for a large windpower system. Investigation were being done about the hybrid IGCT/IGBT nature of the solution, [24], which is the reason why it is drawn here with both, IGBTs and IGCTs.

The topology is used in a back to back configuration for a 5-10MVA windpower generator and offers low enough harmonic distortion to comply with the IEEE standards (IEE 519) in filterless grid connection.

However complying with the very strict German energy standards defined by VDEW, [25], requires an output filter. In this power range, the LC filter is considerable in terms of size, weight and cost. The main target is therefore to upgrade the topology so as to generate a sufficient output quality to comply with VDEW standards, without needing an output filter.

The main characteristics of the 5L ANPC are a reduced number of components, especially passive, which result in a higher power density and a higher reliability. The balancing of the capacitors can be done by means of redundant switching states, and for that reason, the modulation of the inverter is simplified.

1.4. Motivation of the work orientation

From the characteristics of the topologies presented previously, some general trends can be drawn. The main topological criteria are:

1. the number of components (DC-link, capacitors, switches)

2. the total blocking voltage of the converter (which depends on how many switches and what voltage levels are found within the topology)

3. the controllability of the topology (from the point of view of the stabilization of the capacitor voltages of the topology)

These parameters influence the reliability (1.), the efficiency (1. and 2.), the power density (1.), the costs (1., 2. and 3.), the application and the performances (3.), the control complexity (3.) and some other aspects like protection strategy (1. because of stored energy), for instance.

Intuitively, it can already be understood that designing a converter topology which optimizes the 3 aspects is not trivial, and that most likely there will be a trade off between the different aspects. Optimizing one point can result in making another point less good.

A global and detailed analysis has to consider many aspects (for instance, [26]). But since the objective of this work is to provide a solution for the 5L ANPC topology only, the analysis must focus on the main characteristics of that topology first.

The interesting features of the 5L ANPC topology are the high reliability and the high power density. To upgrade this topology means that the main characteristics should be kept. Thus the proposed solution should focus on the point 1., since this characteristic is the key to the main features of the ANPC. And of course, the proposed solution should be compatible with the ANPC topology.

Several approaches can be considered to find solutions for the so far defined problem. For instance working on improvements of existing topologies or orienting the investigations in the direction of new topological developments. To answer this question, and finally give an orientation to the work, a comparison of the various topologies is done. Figure 1.8 roughly positions the topologies against each other with respect to the point 1. It shows how the topologies compare to each other regarding the number of components required versus the number of levels typically produced.

This is of course only one of several aspects characterizing multilevel topologies. But from that comparison, it can be seen that topologies offering a large number of levels with a reduced number of components are lacking. Since this is exactly where the research should focus, none of the

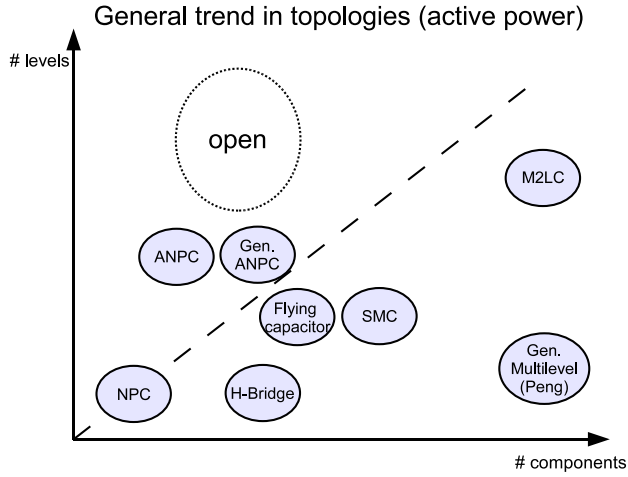


Figure 1.8.: *General trend observed in multilevel topologies regarding the number of components versus the number of generated levels*

existing topologies seem to offer adequate characteristics. Thus, this shows that investigation on new topologies can help to provide solutions for the lacking criteria. The definition of the work is therefore oriented on new multilevel converter topologies, and more specifically on topologies offering a high output resolution with a reduced number of components.

Orienting the research to an area where no solutions currently exist is of course of high technical interest. But the constraints and the limitations that will be found might result in solutions that are not adapted to industrial applications. Finding this out and comparing the solutions is exactly what this work proposes to do.

CHAPTER 2

Introducing the Cross Connected Intermediate Level VSI (CCIL)

2.1. General topology of the CCIL

2.1.1. Cascadable general topology

The Cross Connected Intermediate Level (CCIL) Voltage Source Inverter, [27], is a novel topology presented in Figure 2.1. It is the first original contribution of this thesis. It is based on the ANPC structure and has 2 extra switches in a crossed configuration. It is modular and based on three different stages, referred to as A,B and C. The first stage, A, is an active clamped 3 level inverter. It uses two DC-link capacitors and four switches similarly to the 5 level ANPC.

The second stage, B, is the so-called cross connected intermediate level stage consisting of one phase capacitor C_{f1}, two longitudinal switches, $Si1$ and $Si4$, and two cross connecting switches, $Si2$ and $Si3$. This stage can be cascaded or stacked in a theoretically unrestricted way. On Figure 2.1, B' is cascaded to B.

Finally the output stage consists of two unidirectional switches connected to the phase output. Similar stage can be identified in the 5 level design.

Upgrading from the 5L ANPC topology is quite straight forward and it is seen later that the 5L ANPC is, in some way, a particular case of the CCIL general topological family.

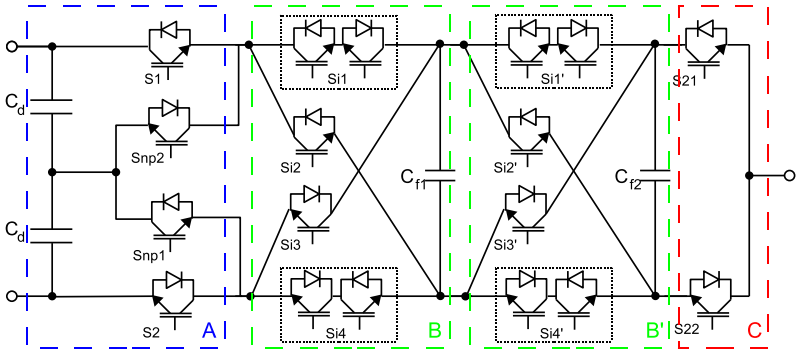


Figure 2.1.: *General view of the Cross Connected Intermediate Level Voltage Source Inverter*

The specificity of the CCIL topology is that it allows to add or to subtract, in each possible way, the voltages found on either of its input terminals, with the voltage of its capacitor. This allows to theoretically obtain up to four different levels on each of the two output terminals: Figure 2.2, 3 and 4 can generate:

$$V_3 \in \begin{cases} V_1 \\ V_1 - U_{C_{f1}} \\ V_2 \\ V_2 - U_{C_{f1}} \end{cases} \quad \text{and} \quad V_4 \in \begin{cases} V_1 \\ V_1 + U_{C_{f1}} \\ V_2 \\ V_2 + U_{C_{f1}} \end{cases}$$

The capacitor voltage level determines how many of the possible output levels are redundant and if the output steps are uniform or not. In a general case, the total amount of paths through the inverter is given by (2.1). n is the number of stages, on Figure 2.1, $n = 2$.

$$P(n) = 16 \cdot 3^{n+1} \tag{2.1}$$

Among all the possible paths, the zero and the upper and lower DC voltages are redundant multiple times. When these redundancies are eliminated, the resulting possible paths are called the *switching states*:

$$S(n) = 3^{n+1} \tag{2.2}$$

Generally speaking any voltage level can be admitted on the capacitors. However for uniform output voltage steps only fractions of 2 and 3 of the

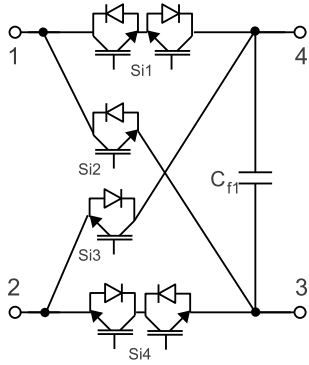


Figure 2.2.: *Dipole representation of the Cross Connected Intermediate Level stage*

DC-link should be considered, [21], such as : $V_{C_{f1}} = \frac{V_{C_d}}{3}$, $V_{C_{f2}} = \frac{V_{C_d}}{9}$, etc, or $V_{C_{f1}} = \frac{V_{C_d}}{2}$, $V_{C_{f2}} = \frac{V_{C_d}}{4}$, etc.

When the phase capacitor voltages are chosen as fractions of 2 of the DC-link voltage, a so called *redundant (switching) state* voltage source inverter is obtained. When fractions of 3 are used, a *non-redundant (switching) state* inverter results. It is also possible to mix fractions of 2 and of 3: the result is an uniform output step, semi-redundant state, voltage source inverter. These differences are discussed in a more detailed manner in the following §2.1.2.

Table 2.1 summarizes all the different output states that can be generated with the topology of Figure 2.1. There are 27 possibilities :

Table 2.1.: *All the different output combinations which can be generated by the inverter of Figure 2.1*

$\pm(V_{C_d}+V_{C_{f1}}+V_{C_{f2}})$	$\pm(V_{C_d}+V_{C_{f1}}-V_{C_{f2}})$	$\pm(V_{C_d}-V_{C_{f1}}+V'_{C_{f2}})$
$\pm(V_{C_d}+V_{C_{f1}})$	$\pm(V_{C_d}+V_{C_{f2}})$	$\pm(V_{C_d})$
$\pm(V_{C_d}-V_{C_{f1}})$	$\pm(V_{C_d}-V_{C_{f2}})$	$\pm(V_{C_d}-V_{C_{f1}}-V_{C_{f2}})$
$\pm(V_{C_{f1}})$	$\pm(V_{C_{f1}}-V_{C_{f2}})$	$\pm(V_{C_{f2}})$
$\pm(V_{C_{f1}}+V_{C_{f2}})$	0	

The topology always offers the possibility to boost the output voltage. The cross switches allow to add up the phase capacitors and DC-link volt-

ages. This characteristic has various influences on blocking voltages and controllability that are discussed in details later on.

2.1.2. Redundant and non-redundant states

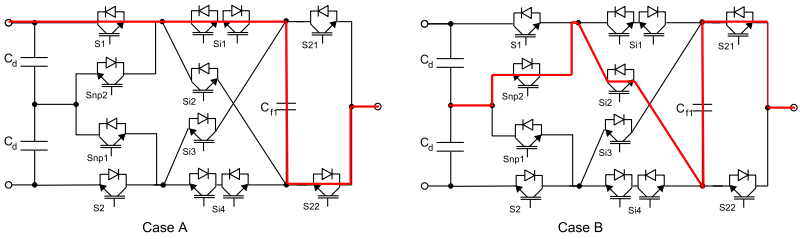


Figure 2.3.: *Redundant and non-redundant states depend on the voltage ratios between the capacitors of the DC-link and of the phase*

As mentioned this characteristic depends on the chosen phase capacitor voltage ratios. Only the cases where voltage ratios are either 2 or 3 are considered (uniform voltage steps).

The general CCIL topology contains one to several phase capacitors depending on how many stages are cascaded. These capacitors are not supplied by any external power sources (to avoid the problem of the cascaded H-Bridge topologies, see §1.3.2). Therefore the balancing of the capacitor voltages has to be handled by the modulator. The redundant or non-redundant characteristic has a major influence on the balancing strategy.

A single stage CCIL, Figure 2.3, illustrates the concept of redundant and non-redundant switching states: The two states, A and B, make use of the phase capacitor to generate a given output voltage. Considering an initial condition with the phase capacitor charged to its nominal voltage, the following properties are derived:

Ratio 2

- If the capacitor voltage is a fraction of 2 of the DC-link voltage (i.e. $V_{C_{f1}} = \frac{V_{C_d}}{2}$), the output voltage level for the two switching states is equal to $\frac{V_{C_d}}{2}$.
- The current flows in a different direction through the capacitor depending on the switching state.

Ratio 3

- If the capacitor voltage is a fraction of 3 of the DC-link voltage (i.e. $V_{C_{f1}} = \frac{V_{C_d}}{3}$), the output voltage level is different for the two switching states. Case A = $\frac{2 \cdot V_{C_d}}{3}$ and case B = $\frac{V_{C_d}}{3}$.

- The current flows in a different direction through the capacitor depending on the switching state.

A switching state is said to be redundant if it allows to control the direction of the current flowing across one or several capacitors without influencing the output level, for instance in the case of the 5L ANPC, which is a simplified cross connected topology, with voltage ratios equal to 2.

When fractions of 3 are chosen, non-redundant states result. The output level is different for every switching state. This lack of redundancy means that it is not possible to reverse the current direction in a phase capacitor without influencing the output voltage. Thus it is not possible to balance the capacitor without influencing the output.

A tree representation, [28], can be helpful to get different view of the repartition of the levels and the redundancies. The 9L redundant and non redundant topologies are considered and the switching states are represented on Figure 2.4.

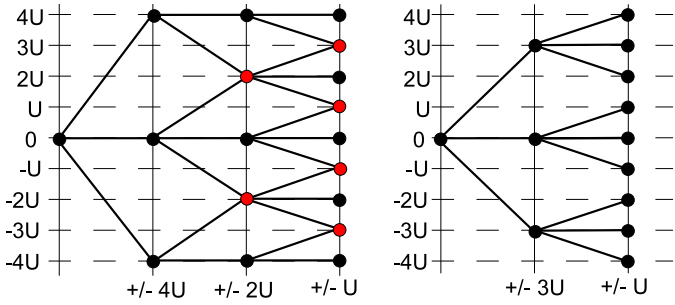


Figure 2.4.: *9L switching states representation, in red are the redundant states. Left: 9L CCIL with redundant switching states. Right: 9L CCIL with non redundant switching states.*

In a topology with a mixed configuration of fractions of two and of three, a mixed behavior results. Figure 2.5 illustrates such a topology. It generates 15 levels without the voltage elevation characteristic. It is a semi-

redundant uniform output step configuration. Some output levels are redundant whereas others are not.

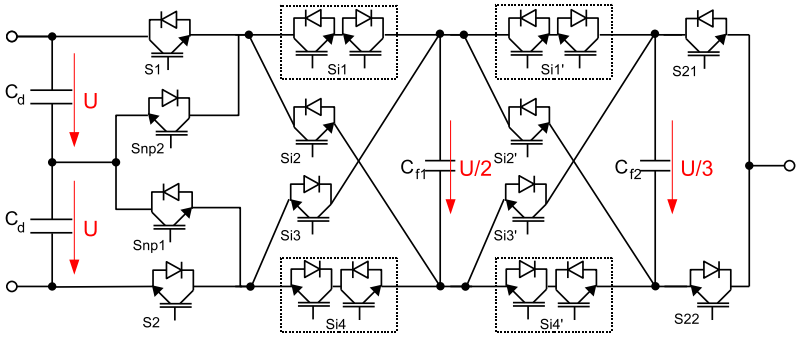


Figure 2.5.: *Topology using a mixed configuration of rations of 2 and 3 - 15 levels without voltage boosting*

The boosting levels are never redundant, whatever the chosen voltage ratio. So a CCIL boosting inverter with voltage levels in fractions of 2 is a semi-redundant topology.

Finally, it must be mentioned that although the term redundancy is used when fractions of 2 in a non-boosting topology are considered, it does not mean that all the capacitors can be controlled independently one from another. This means that it is possible to balance the capacitors, but that not all the possibilities exist. Figure 2.6 shows the redundant states for the level $+3U$. The modulator must therefore be able to prioritize the capacitors for the corrective action to have a positive effect.

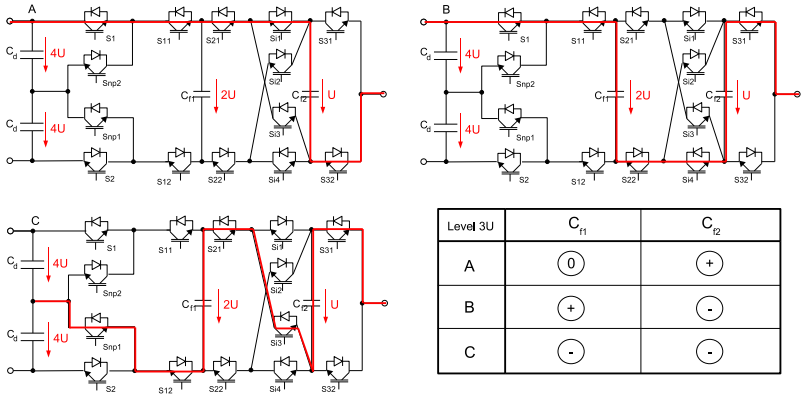
The most deviated capacitor is given a higher priority so that even if the chosen switching state is not optimal for another capacitor, the corrective action is still applied.

2.1.3. 9 level voltage source inverter topologies

Introductory word

The CCIL topology introduced in the previous section can be used to build multiple output level voltage source inverters. In the present section 3 different ways of building a 9 level inverter are presented.

9L are sufficient to ensure compliant operation with the standards in filterless operation.



Level 3U	C_{f1}	C_{f2}
A	0	+
B	+	-
C	-	-

Figure 2.6.: *The redundant states of the 9L double capacitor CCIL configuration*

Two capacitors 9 level voltage source inverter

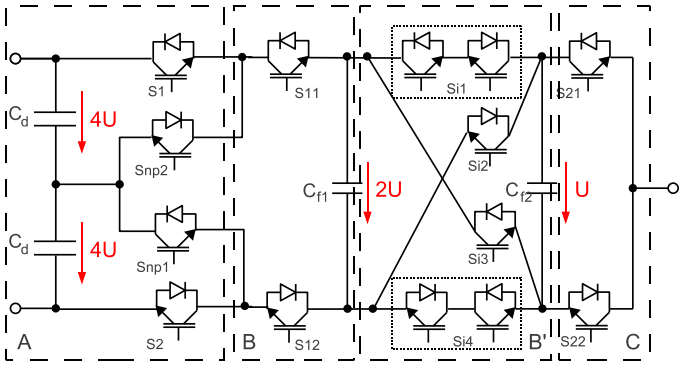


Figure 2.7.: *Double capacitor 9 level CCIL voltage source inverter*

Figure 2.7 shows the proposed topology for a non-boosting 9 level inverter with 2 phase capacitors. The voltage values are respectively $2U$ and U. This is a redundant switching state topology (see §2.1.2). The modulation algorithm is simplified and is summarized to choosing the proper switching state among the possible redundant states.

The topology uses one CCIL stage B' and one "standard" stage B ("standard" meaning similar to the 5L ANPC stage). The simplification of the cross switches in the first stage B is possible with non-boosting topologies. Because of the two phase capacitors, the stored energy in the converter is higher than in the single capacitor version.

Table 2.2 summarizes the mains characteristics of the double capacitor 9 level inverter topology.

Table 2.2.: *Characteristics of the 2 capacitor 9 level voltage source inverter*

Output voltage levels	$4U, 3U, 2U, U, 0, -U, -2U, -3U, -4U$
Characteristics of switches	- 4 switches $4U$ (*S1, Snp2, Snp1, S2*) - 4 switches $2U$ (*S11, Si1, Si4, S12*) - 2 switches $3U$ (*Si2, Si3*) - 6 switches U (*Si1, S21, Si4, S22*)
Stored energy	2^{nd} capacitor 25% of energy stored in 1^{st}.
Control of capacitor voltage	Appropriate choice of switching state.

Single capacitor 9 level voltage source inverter

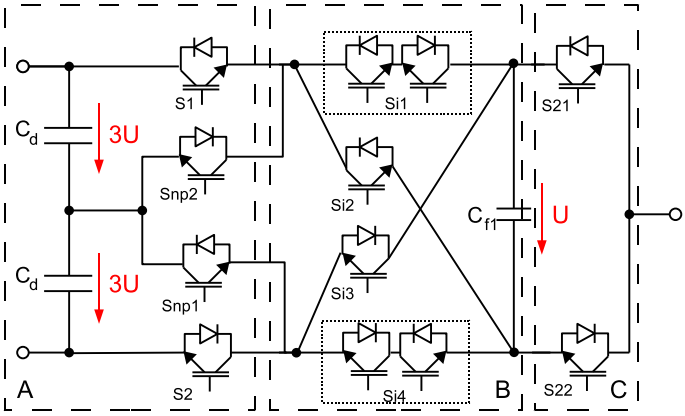


Figure 2.8.: *Single capacitor 9 level CCIL voltage source inverter*

Figure 2.8 shows the topology of a single capacitor 9L CCIL boosting voltage source inverter. The topology contains one CCIL stage B. This

Table 2.3.: *Characteristics of the single capacitor 9 level voltage source inverter*

Output voltage levels	$4U, 3U, 2U, U, 0, -U, -2U, -3U, -4U$ (*voltage elevation*)
Characteristics of switches	- 6 switches $3U$ (*S1, Snp2, Snp1, S2, Si1, Si4*) - 2 switches $4U$ (*Si2, Si3*) - 4 switches U (*S21, S22, Si1, Si4*)
Stored energy	20% (5 times less) of the total energy stored in the 2 capacitors of the previous 9 level configuration.
Control of capacitor voltage	Using a common mode control strategy.

topology is more compact then the previous one, but stabilizing the capacitor voltage (without use of an external circuit) is more difficult because of non-redundant switching states. A strategy using common mode is developed and presented in §2.3.2.

This topology is optimal in the sense of the number of capacitors used versus the number of levels generated.

The boosting characteristic can appear as a drawback for several reasons. First in terms of required blocking voltage and secondly from the point of view of capacitor voltage regulation. On the other hand, the voltage boosting can result in a lower DC-link voltage, which in turn leads to lower blocking voltage requirements. It does not mean that the total blocking voltage is at the same level as, for instance, the double capacitor 9L CCIL. Assessment of these aspects is done in §2.6.

From the point of view of control, it is shown that on non redundant topologies, the boosting characteristic is actually helping in stabilizing the system. This aspect is explained in §2.5.3.

Overall this topology offers an interesting study subject and it is the first retained topology. It analyzed in detail in the next sections of this chapter.

Two capacitors 9 level stacked CCIL

Figure 2.9 shows another proposed topology for a 9 level VSI using a stacked structure. The benefit of this topology is not obvious at first sight. The reason it is presented here is to illustrate how the CCIL basic building block can be stacked up to construct a different type of cross connected inverter topology. Notice that in this case the input stage A is no longer a NPC structure.

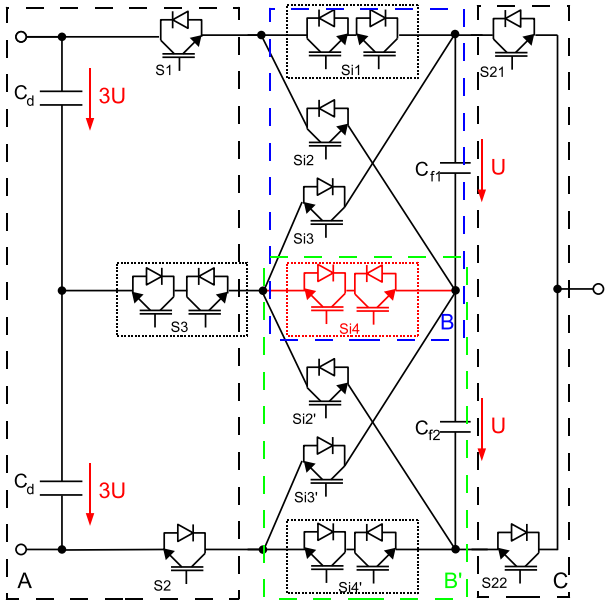


Figure 2.9.: *Double capacitor stacked 9L CCIL voltage source inverter*

This is a boosting semi-redundant topology, so the behavior, from an electrical point of view, is a mixture of the two previous topologies. Some states can be stabilized using redundant states, while others probably require an appropriate control and modulation algorithm.

The bidirectional switch *Si4* is not mandatory for the system to work, but offers however a supplementary redundancy in the states used to generate the output levels $+U$ and $-U$. This topology is not studied further in this work.

2.1.4. Pure CCIL topology

Besides being used in a hybrid configuration associated to an existing multilevel topology, the CCIL PEBB can also be used by itself. It can be cascaded in series or in parallel, Figure 2.10. The properties are not discussed or studied here, since the interest is to use the CCIL with the ANPC topology. But for the sake of completeness, the possibility is mentioned.

In this configuration, the topology offers the possibility to boost the voltage, and there are some redundancies for the stabilization of the capacitor voltages. The detailed characteristics depends on what voltage ratios are retained. It is also not clear if this solution has any advantages over existing solutions such as the flying capacitor or the SMC.

2.2. Characterization of the CCIL VSI

2.2.1. From boosting to non boosting

The CCIL topology can have multiple forms. The redundant or non redundant nature is coming from the choice of the voltage ratios, as explained in §2.1.2.

On the other hand, the boosting and non-boosting behavior is only defined by what are the allowable switching states for the converter. If all the switching states leading to an output voltage higher than the DC-link voltage are forbidden, then logically a non-boosting topology results.

From the electrical point of view, the boosting requires from the switches to be able to block larger voltages, and voltage variations in both directions. This means that boosting topologies require, generally speaking, extra blocking capability compared to non-boosting topologies.

From the topological point of view, designed a non-boosting CCIL inverter allows to get ride of the first cross connection. When this connection is removed, it is never possible for the voltage to add up to a higher value than the DC-link voltage. So from this point of view as well, the total blocking voltage is reduced. Additionally, the number of switches is also a little bit reduced.

2.2.2. General equations

Boosting capability and voltage ratios are the 2 parameters that determine how many levels can be generated by a given topology. The present section gives some analytical equations relating the main characteristics of the inverter to the number of stages, n, and the voltage ratios (for definition of redundant, non-redundant and semi-redundant, see §2.1.2).

Table 2.4 gives the relationship between the number of levels produced, $L(n)$, and the cascade of n stages of the CCIL basic building block.

The total number individual switches, $T(n)$, needed par phase, in function of the number of cascaded stages, n, is given by the set of equations of Table 2.5. This value $T(n)$ says how many individual switching positions are necessary, independently from their blocking voltage (and if the switch should have a 4 quadrant operation characteristic or not). Of course, in

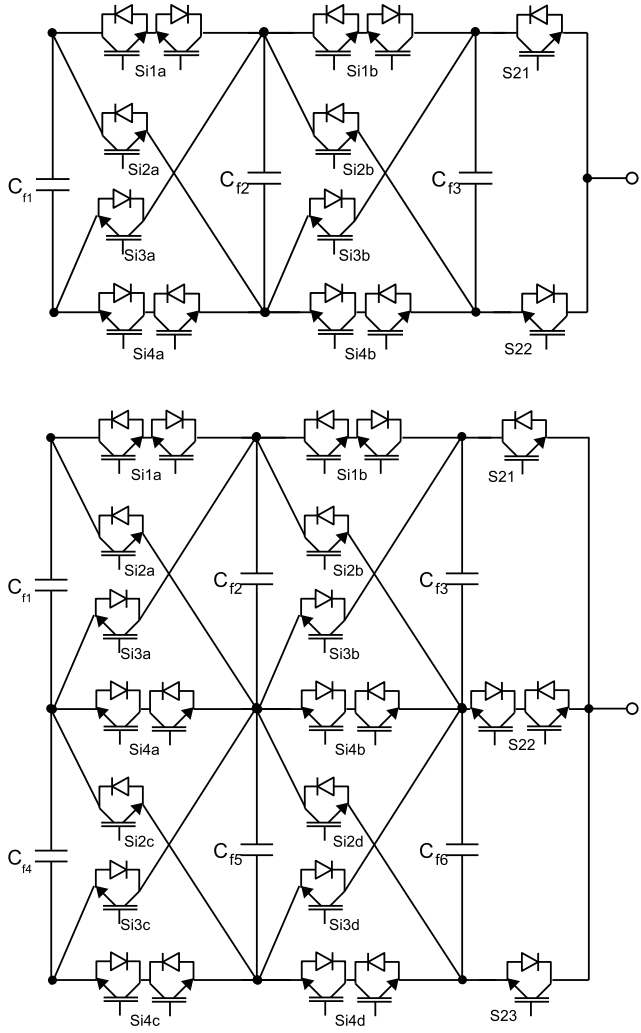


Figure 2.10.: *Stand alone CCIL topology*

Table 2.4.: *Number of output levels as function of stages n and inverter parameters*

Non Redundant boosting	$L(n) = S(n) = 3^{n+1}$
Non Redundant non- boosting	$L(n) = 2 \cdot 3^n + 1$
Semi Redundant boosting	$L(n) = 2^{n+2} - 1$
Redundant non-boosting	$L(n) = 2^{n+1} + 1$

reality depending on the required blocking voltage, the equivalent switch might require a serial connection of two or more switches. But this is not considered here.

Table 2.5.: *Number of individual switches as function of stages n and inverter parameters*

Boosting	$T(n) = 6 + 4 \cdot k$
Non-boosting	$T(n) = 8 + 4 \cdot (k - 1)$

Intuitively, it is already possible to predict that boosting requires more blocking capability compared to non-boosting. This implies larger switches (or series connection of smaller ones if larger switches are not available). The normalized (to half DC-link voltage) total blocking voltage, $B(n)$, for n cascaded CCIL stages is given by the equations of Table 2.6.

Table 2.6.: *Normalized (to DC-link) total blocking voltage required for cascade of n stages*

Non Redundant boosting	$B(n) = 4 + \frac{2}{3^n} + \sum_{k=1}^{n} \frac{2}{3^{k-1}} + \frac{4}{3^k}$
Non Redundant non-boosting	$B(n) = 5 + \frac{2}{3^n} + \sum_{k=2}^{n} \frac{2}{3^{k-1}} + \frac{4}{3^k}$
Semi Redundant boosting	$B(n) = 4 + \frac{2}{2^n} + \sum_{k=1}^{n} \frac{2}{2^{k-1}} + \frac{4}{2^k}$
Redundant non-boosting	$B(n) = 5 + \frac{2}{2^n} + \sum_{k=2}^{n} \frac{2}{2^{k-1}} + \frac{4}{2^k}$

2.2.3. Blocking voltage optimization

It is possible to optimize the total blocking voltage of the CCIL converter topologies by sharing some switches across 2 switching positions. Analyzing the different topologies drawn with series connection of elementary blocking voltage devices is helpful to point out a certain number of redundant switches.

The single capacitor 9 level topology (Figure 2.8) is represented on Figure 2.11-top, using only elementary blocking voltage switches. By elementary blockage voltage, it is meant the voltage of the smallest step U.

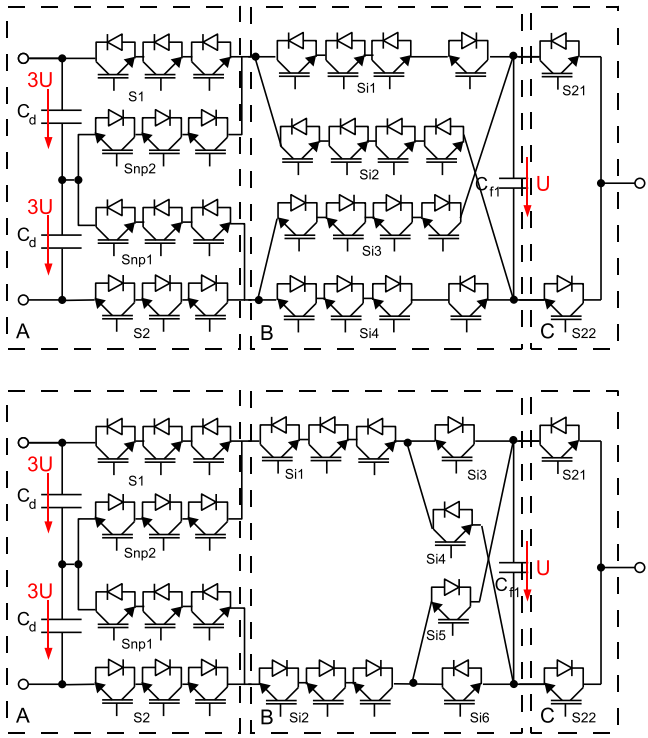


Figure 2.11.: *Top: Single capacitor 9 level CCIL designed with elementary switching devices. Bottom: Optimal design of the 9 CCIL*

It is found that there is a redundancy of switches within the switching position *Si1* and *Si2*, respectively between *Si3* and *Si4*. A redesign of

the circuit taking into account these redundancies leads to the topology of Figure 2.11-bottom.

This means that the total blocking voltage of the CCIL converter can be reduced by $\sum_{k=1}^{n} \frac{3}{3^{k-1}}$ and $\sum_{k=1}^{n} \frac{3}{2^{k-1}}$ for the non-redundant, respectively redundant design. This optimization is already taken into account in the equations of Table 2.6.

2.2.4. 5 level ANPC as a part of the CCIL family

The 5 level ANPC inverter can be seen as a topology belonging to the general CCIL topological family. The particularities of the 5L are redundant and non-boosting behavior. From the previously defined design rules, the topology can be drawn as a one stage non boosting redundant CCIL. The equivalence is shown on Figure 2.12.

In non-boosting topologies, the first set of cross switches can be omitted, as explained in §2.2.1. The simplification of the cross switches leads to the simplification of the anti-series switches. Thus, the 5L ANPC topology is then found.

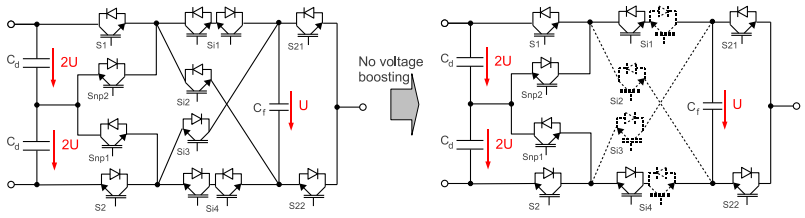


Figure 2.12.: *The 5L ANPC inverter is a one stage non-boosting and redundant CCIL inverter*

2.3. 7 or 9 level CCIL

2.3.1. Retained topology

Figure 2.13 shows the retained topology which was already introduced in the previous sections. The circuit is a 9L single stage boosting (or a 7L non-boosting) non redundant CCIL VSI. Stabilization of the capacitor voltage cannot be done through redundant switching states. A stabilization strategy, based on [29], using common mode is proposed and introduced.

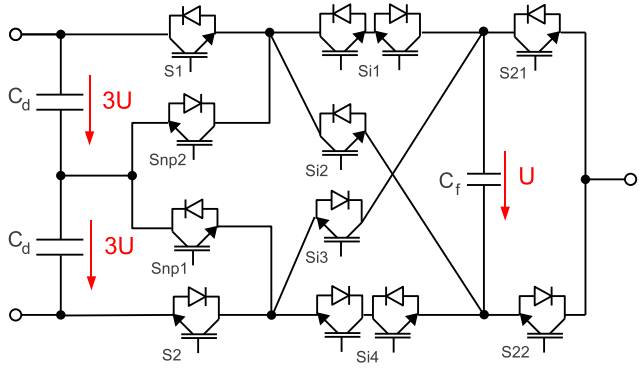


Figure 2.13.: *The retained 9L CCIL voltage source inverter*

The major drawbacks of this method are analyzed and a new stabilization strategy is then proposed.

Because of the blocking voltage characteristics, the 9L inverter can be restrained to a 7L, by renouncing to the boosting behavior. As it has however no incidence on the general analysis of the topology, no restrain to 7 level is done at this point. Moreover, as far as the controllability of the capacitor voltage is concerned, it is shown later that the behavior of the system is performing less well with 7L compared to 9L.

The inverter topology contains one flying capacitor and one DC-link (plus and minus) allowing 9 different output levels to be generated. To each of these output levels is associated only one switching state V0 to V9. V1', V3', V4', V5', V6' and V8', are redundant switching states in the sense that they allow to generate the same levels but not from the point of view of capacitor balancing. These states could be used for loss power balancing and thus optimize the dissipation and cooling of the inverter.

Figure 2.14 shows all the possible switching states and the associated output level for the 9L inverter. To each output level there is a defined action on the capacitor, charge ($\oplus$), discharge ($\ominus$) or do noting to it (0). Table 2.7 summarizes this behavior.

2.3.2. Common mode balancing strategy

Definition of voltages The following voltages are defined, Figure 2.15: V_{12}, V_{23} and V_{31} are line to line voltages. V_1, V_2 and V_3 are line voltages. V_{10}, V_{20} and V_{30} are pole voltages.

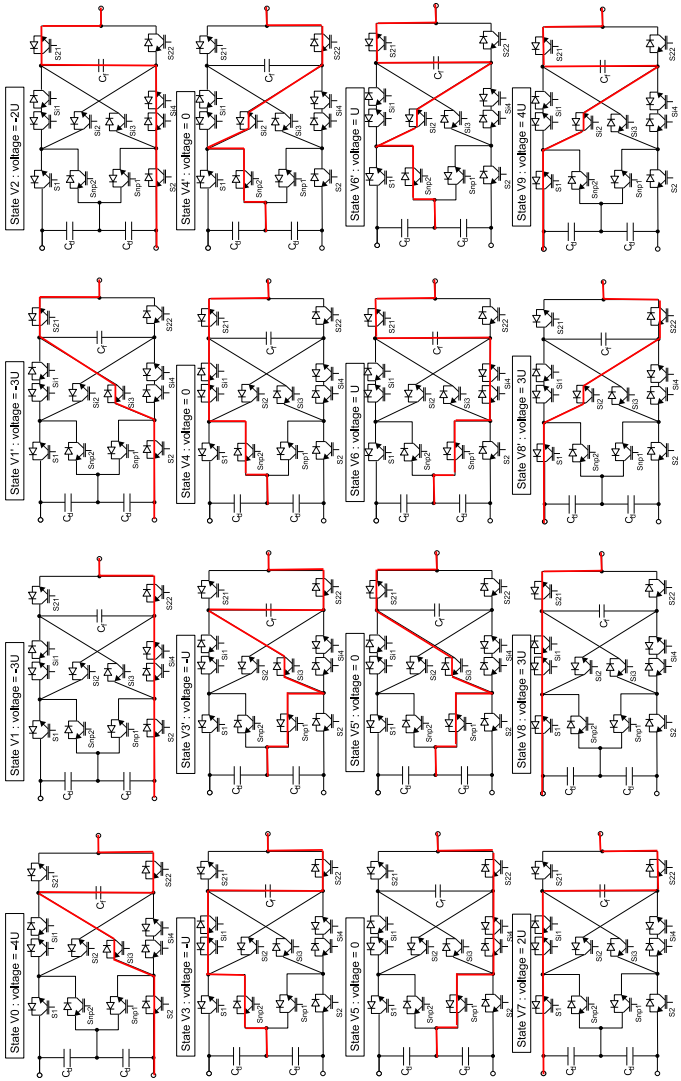


Figure 2.14.: *All the possible output states for the 9L CCIL voltage source inverter*

Table 2.7.: *Switching states of the 9L CCIL voltage source inverter*

Phase Voltage	switching state										Effect on C_f		switching vector
	S1	Snp2	Snp1	S2	Si1	Si2	Si3	Si4	S21	S22	$i > 0$	$i < 0$	
$-4U$	0	1	0	1	0	0	1	0	0	1	$\ominus$	$\oplus$	V0
$-3U$	0	1	0	1	0	0	0	1	0	1	0	0	V1
$-3U$	0	1	0	1	0	0	1	0	1	0	0	0	V1'
$-2U$	0	1	0	1	0	0	0	1	1	0	$\oplus$	$\ominus$	V2
$-U$	0	1	0	1	1	0	0	0	0	1	$\ominus$	$\oplus$	V3
$-U$	1	0	1	0	0	0	1	0	0	1	$\ominus$	$\oplus$	V3'
0	0	1	0	1	1	0	0	0	1	0	0	0	V4
0	0	1	0	1	0	1	0	0	0	1	0	0	V4'
0	1	0	1	0	0	0	0	1	0	1	0	0	V5
0	1	0	1	0	0	0	1	0	1	0	0	0	V5'
U	1	0	1	0	1	0	0	0	1	0	$\ominus$	$\oplus$	V6
U	0	1	0	1	0	1	0	0	1	0	$\ominus$	$\oplus$	V6'
$2U$	1	0	1	0	1	0	0	0	0	1	$\oplus$	$\ominus$	V7
$3U$	1	0	1	0	1	0	0	0	1	0	0	0	V8
$3U$	1	0	1	0	0	1	0	0	0	1	0	0	V8'
$4U$	1	0	1	0	0	1	0	0	1	0	$\ominus$	$\oplus$	V9

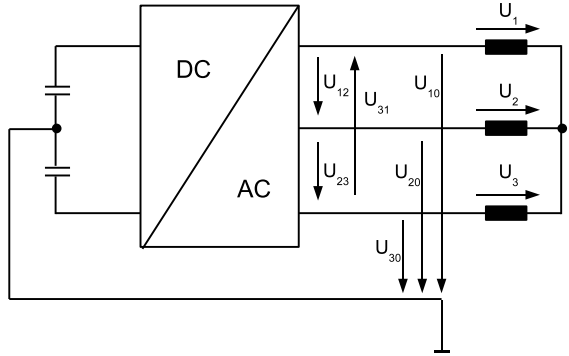


Figure 2.15.: *Definition of voltages for a 3 phased inverter with non connected neutral point*

Basic principle A direct conclusion drawn from Table 2.7 is that when a given sequence is applied, say a PWM sinusoidal reference signal, no control of the phase capacitor voltage is possible. It cannot be said that there is a natural balancing of the capacitor's voltage over a certain period, although this can happen for some modulation indexes and some power factors ($\cos\varphi$).

The only available action is influencing the output voltage (i.e. the reference signal) such that the required level has a corrective action over the voltage of the capacitor. This means distorted pole voltages. This is the idea behind the common mode control strategy. If the output voltages can be modified in such a way that the capacitors are balanced and that the line to line voltage remains undistorted, then the common mode component is acting as a stabilizing factor.

The principle of operation with common mode is illustrated in Figure 2.13. It can already be seen that there is a certain number of limiting factors:

- If one (or several) phase voltages are too close to the upper or lower bounds (high modulation index), the common mode voltage margin is too small to balance the capacitors. In order words, the degree of freedom for the corrective action becomes smaller as the modulation index rises.

- Correction of one phase capacitor can have the opposite action on another phase capacitor. It might therefore be necessary to assess

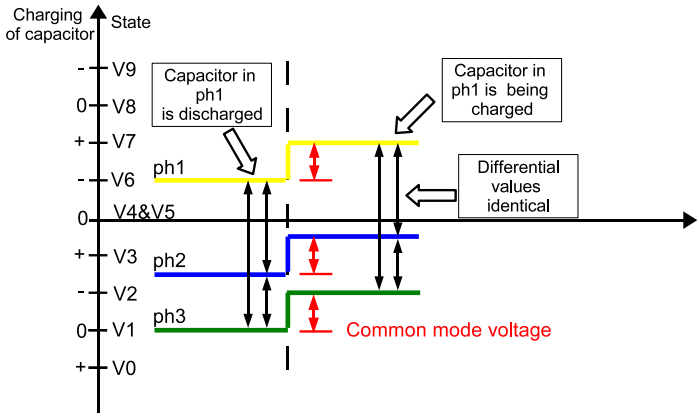


Figure 2.16.: *Principle of the common mode action on the capacitor charge*

if correcting one capacitor does not lead to the opposite action on another capacitor such that the system becomes unstable.

The common mode control of the phase capacitor voltages is straight forward to understand, but to define an appropriate control scheme is not immediate or trivial. The main focus of this section, and the next ones, is to provide some methods to help understanding the system dynamics and define a control algorithm.

Regulation diagram Figure 2.17 shows the proposed common mode regulation diagram. The common mode component is calculated by the common mode regulator, based on the three phase capacitor voltage deviation values, and added to the three reference signals.

Since the reference signals represent the pole voltage of the converter, the common mode value can be seen on that voltage. But because the neutral point of the converter is not connected, the line to line and line voltages will remain undistorted.

Stabilization through common mode harmonic components

Common mode harmonic The strategy is inspired by the PhD work of Martin Veenstra ([29], [30]). The idea is to modify the shape of the pole voltage (by modifying the shape of the reference signal) with the help of

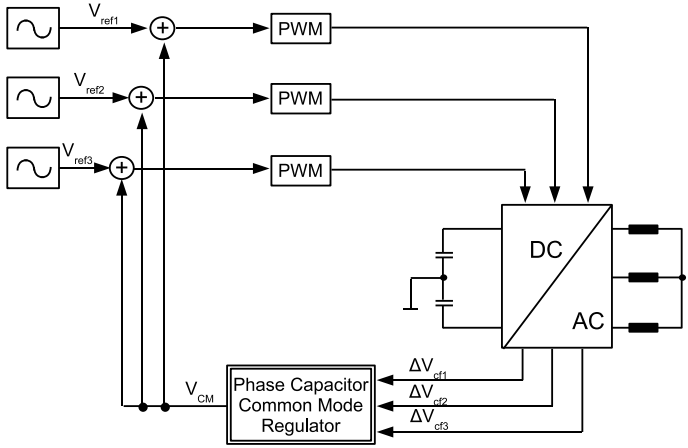


Figure 2.17.: *Structural diagram of the common mode regulation strategy*

a harmonic component common on the three phases so as to stabilize the phase capacitor voltages. The harmonic component is a sinusoidal wave with a frequency set as a multiple of the fundamental frequency.

The reference signal has a non sinusoidal shape in the following examples, because the third harmonic modulation strategy is used to be able to increase the maximum modulation index by 15%. Also, the harmonics of rank 3 and multiple are not directly considered here, since they already have been the object of the previous study by M.Veenstra in [29]. Instead a construction based on other harmonic ranks is used, to verify if this apporach allows to get some different understanding of the control problem.

Figure 2.18 shows the result, $\mathrm{Ref}_{\mathrm{ph}n} + \mathrm{CM}_{\mathrm{harmonic}}$ of the application of a 5^{th} harmonic component, $\mathrm{CM}_{\mathrm{harmonic}}$, on the three reference signals, $\mathrm{Ref}_{\mathrm{ph}n}$. It is noticeable that the resulting signals are non-symmetrical.

The problem with non-symmetrical waveforms is that the influence of the common mode on the capacitors will be different on the three phases. Thus, it becomes more complicated to control the system because this dissymmetry.

Only 3^{rd} order common mode harmonic components, and multiples, provide a symmetrical signal on the 3 phases after addition with the reference signals, [29]. To overcome this limit, an artificial common mode harmonic signal is built. The idea is to use portions of 3 phases shifted harmonic common mode signals.

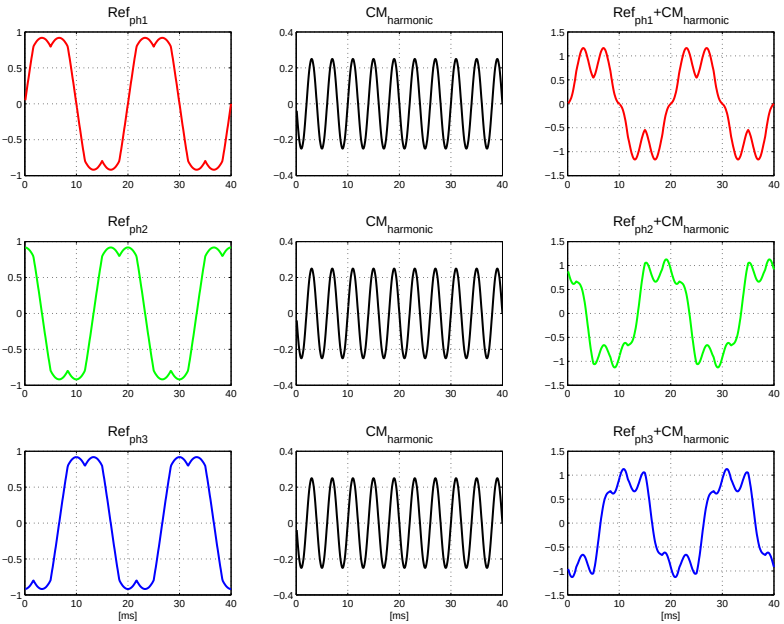


Figure 2.18.: *Left: standard reference signals. Center:* 5^{th} *order harmonic common mode signal. Right: resulting reference signal*

Depending on the phase of the common mode harmonic signal, one of the resulting reference signals, $\mathrm{Ref}_{\mathrm{ph}n} + \mathrm{CM}_{\mathrm{harmonic}}$, is symmetrical, for instance the phase 1 of Figure 2.18. Thus, by changing the phase of the harmonic signal several times per period, it is possible to symmetries the three resulting reference signals.

The common mode signal, which is the sum of a short sequence of the given phase shifted harmonic signal is constructed, Figure 2.19. Symmetric signals are obtained on the 3 reference signals, as illustrated on Figure 2.20.

Having a symmetrical signal on the 3 phases allows to simplify the control algorithm. When one phase is balanced then the 2 others are as well balanced, if the 3 phased system is perfectly symmetrical.

Using this method, it is possible to add up several common mode harmonic components of different frequencies, different phases and different amplitudes. Each combination of common mode harmonics has a different effect on the balancing of the phase capacitors. But to define which is the

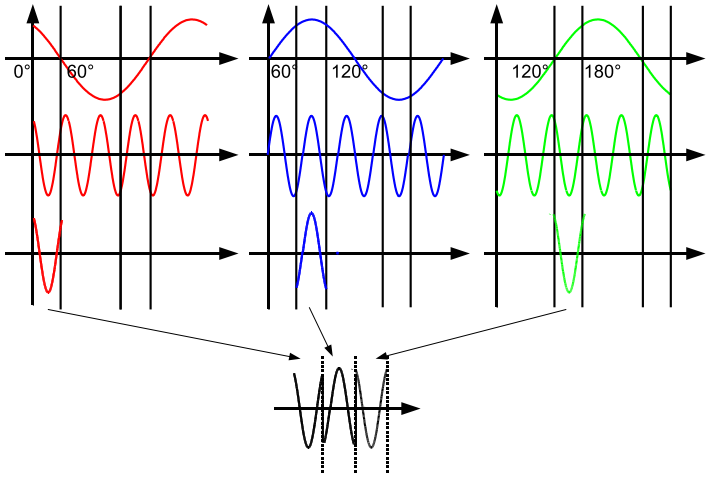


Figure 2.19.: *Construction of common mode harmonic for symmetrical reference signals*

optimal sequence is not trivial, as there is theoretically an infinite number of combinations possible.

The mathematical representation of the resulting signal is given as:

$$\begin{aligned} U(t, \vec{\Theta}, \vec{k}, \vec{A}) \quad = \quad & A_1 \sin(2 \cdot \pi \cdot f_r \cdot k_1 + \Theta_1 + \phi) + ... \\ & + A_n \sin(2 \cdot \pi \cdot f_r \cdot k_n + \Theta_n + \phi) \end{aligned} \tag{2.3}$$

with

- $\vec{\Theta}$ Starting angular position (phase) of the n common mode harmonic signals
- $\vec{A}$ Amplitudes of the n common mode harmonic signals
- $\vec{k}$ Frequency factor of the n common mode harmonic signals
- ϕ phase shift $\in [0; \frac{2\pi}{3}; \frac{4\pi}{3}]$

Third harmonic modulation It is common, in three phased inverters, to use third harmonic modulation signals (see Figure 2.18 or 2.20). This method provides a similar modulation pattern as given by vector modulation, and thus allows to reach modulation indexes up to 1.15.

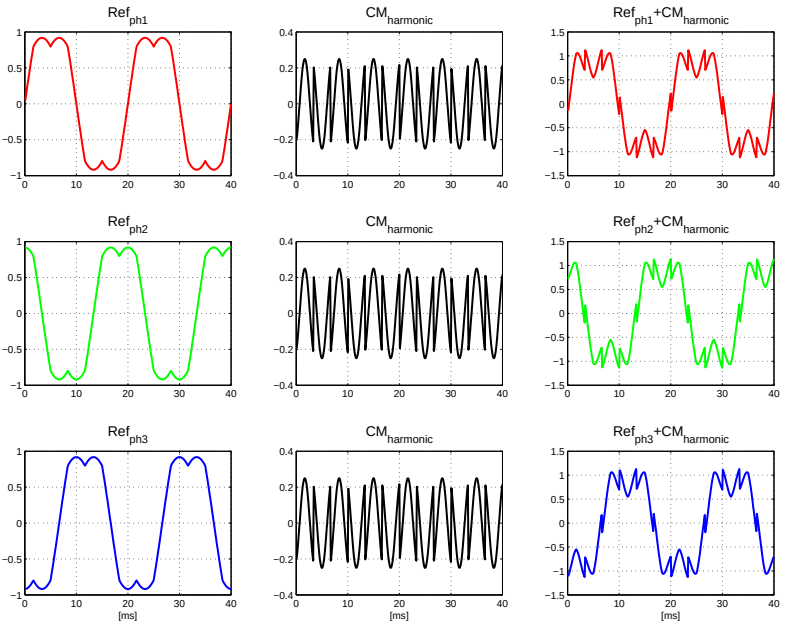


Figure 2.20.: *Left: standard reference signals. Center: 5^{th} order symmetrically constructed harmonic common mode signal. Right: resulting reference signal*

Third harmonic modulation is in fact a common mode pattern. Looking at the way the signal is constructed (equation (2.4)), it is seen that the same given time dependent value is added to the three references. This time varying signal is therefore, by definition, a common mode signal.

$$u_{3^{rd}} = \begin{cases} |u_1| & if \quad |u_1| < |u_2| \text{ and } |u_1| < |u_3| \\ |u_2| & if \quad |u_2| < |u_1| \text{ and } |u_2| < |u_3| \\ |u_3| & if \quad |u_3| < |u_1| \text{ and } |u_3| < |u_2| \end{cases} \tag{2.4}$$

$$u_1^{3^{rd}} = u_1 + \frac{u_{3^{rd}}}{2} \tag{2.5}$$

$$u_2^{3^{rd}} = u_2 + \frac{u_{3^{rd}}}{2} \tag{2.6}$$

$$u_3^{3^{rd}} = u_3 + \frac{u_{3^{rd}}}{2} \tag{2.7}$$

Phase of the current The phase of the current has in important influence on the phase capacitor voltage control. As shown on Figure 2.21, the instantaneous value of the current (which depends on its phase and amplitude) has a significant influence on the charge and discharge of the capacitor. This means that one given pattern will only work for one given power factor.

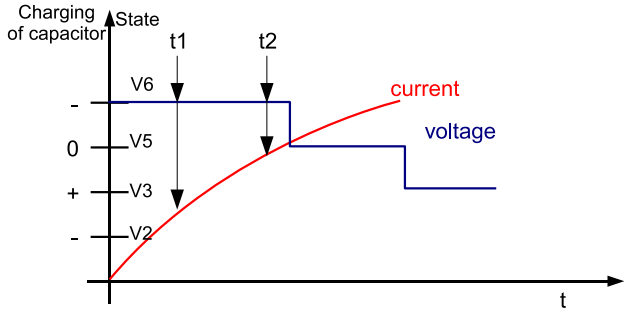


Figure 2.21.: *Influence of the phase of the current on the flying capacitor ripple - the amplitude of the current varies with the time, so a given voltage pattern will not influence the capacitor voltage the same way with different* $\cos\varphi$

Effects of the common mode harmonic parameters variation Before designing a "common mode harmonic" controller adjusted in frequency, phase and amplitude, it is necessary to verify the controllability of the system with a common mode regulator. The analytical expression of the system being non-linear and rather complex, a variation of the parameters (amplitude, phase, frequency) in simulation is used to determine if the system can or not be controlled in such a way.

Each parameter is varied in turn, while the 2 others are kept constant, and the controlled variables are observed. These simulations are done with Matlab, using the PLECS Toolbox. The results are presented on the graphs (amplitude - Figure 2.22, frequency and phase - Figure 2.23) and show the evolution of the capacitor voltage during 2 grid periods. The initial condition is the capacitor voltage loaded at its nominal value.

As it can be noticed from the simulation results, some set of parameters charge while others discharge the capacitor (regions in red or in blue respectively, other colors are intermediate states). From these results, it can

be concluded that, by varying the parameters adequately, it is possible to control the phase capacitor voltage.

Since, in a symmetrical 3 phased system, all three capacitors are stabilized by the same common mode scheme, finding the correct sequence can ensure proper stabilization. Optimally determining these parameters (frequency, amplitude and phase) is the object of the next section.

$$U_{common\ mode} = f(\vec{A}, \vec{k}, \vec{\theta}) \tag{2.8}$$

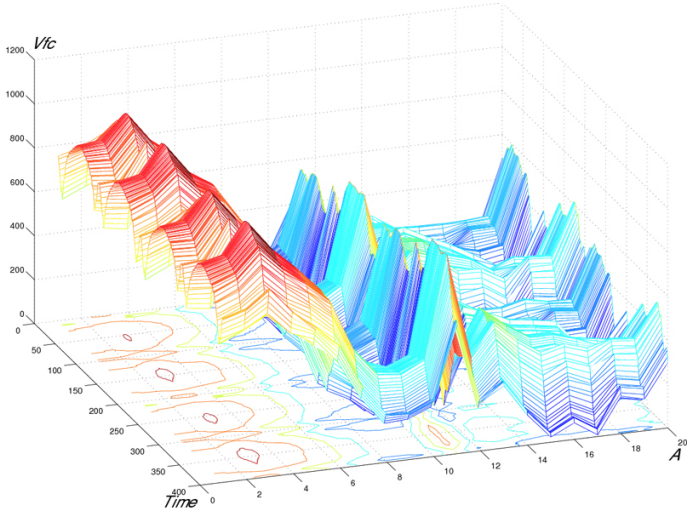


Figure 2.22.: *Amplitude variation of a 5th order harmonic common mode value - red means over-charged, blue discharged*

2.3.3. Mathematical model

Electrical equations

A model for the 9L inverter is derived from the system equations. It is necessary for the controller to have the most accurate possible representation of the reality while still maintain the complexity level in a reasonable range as it should be solved on-line.

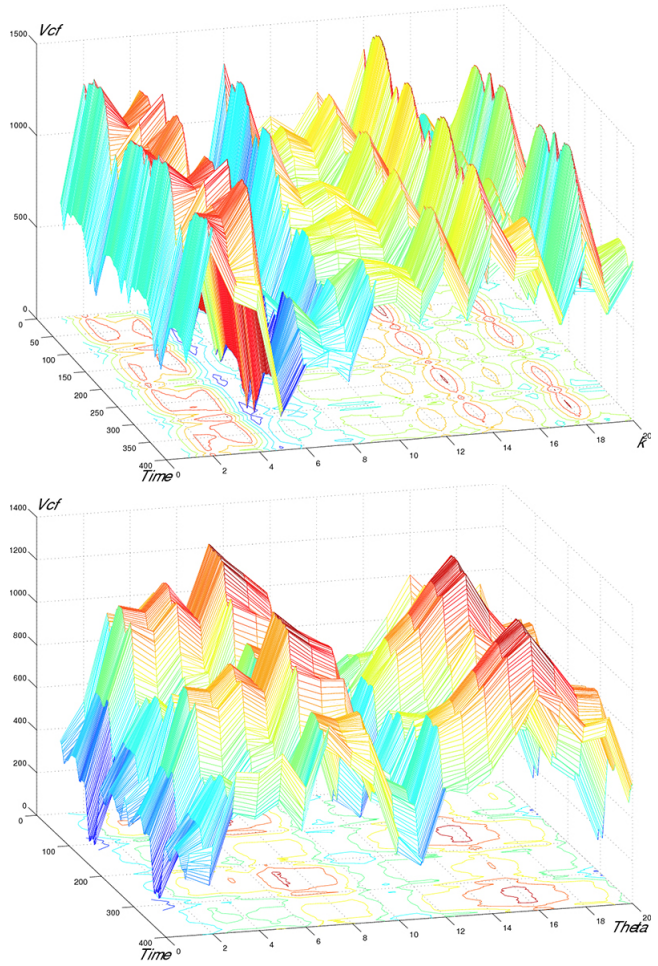


Figure 2.23.: *Top: Frequency variation of common mode value with a phase angle of* π*. The order* k *varies from 2 to 40. Bottom: Phase variation of a 5th order common mode signal. The phase* Θ *varies from* $0 - 2\pi$ *- red means over-charged, blue discharged*

One straight forward way to model the system is to start with the electrical equations of the system. Considering as hypothesis a perfectly sinusoidal current at the output, no parasitic elements and an infinite switching frequency, the electrical equation of the capacitor can be derived:

$$U_{fc}(t) = \frac{1}{C_f} \int i_{fc}(t)dt + U_{fc0} \tag{2.9}$$

The current flowing through the capacitor depends on the output current magnitude (considered as an ideal sine source) and the switching function, which describes how the capacitor is connected from the DC-link to the output. The switching function f_{sw} is:

$$f_{sw}(z) = \quad r_{i-1} \cdot S_{i-1} + (1 - r_{i-1}) \cdot S_i \tag{2.10}$$

with

$$\begin{array}{c} {\scriptstyle U_{i-1} \leq z \leq U_i} \\ r_{i-1} = \dfrac{z - U_i}{U_i - U_{i-1}} \\ {\scriptstyle S_i = sign(i_{fc})|U_i} \end{array}$$

The eq.(2.10) describes the relationship between the input reference and the resulting PWM signal. The PWM is defined by the ratio of the two adjacent levels composing the output signal. For each output level U_i, a current direction S_i is applied with the rate r_i. The S_i's are defined by the structure of the topology (see Table 2.7). The result of the switching function is a value $\in [-1; 1]$ which gives an approximation over one switching period of the direction of the current across the phase capacitor.

If (2.10) is replaced in (2.9) and with a few steps, the following state equation representing the model of the system is obtained:

$$x(t) \quad = \quad \frac{1}{C_f} \cdot \int W_1(t, \varphi) \cdot f_{sw}(U(t, \vec{\Theta}, \vec{k}, \vec{A}) + W_2(t))dt + x_0 \tag{2.11}$$

with

	$x(t)$	: flying cap voltage
$x_0 =$	$V_{fc}(0)$	: flying cap at t=0
$W_1(t, \varphi) =$	$i_{out} \cdot \sin(2 \cdot \pi \cdot f_r \cdot t + \varphi)$	: output current
$W_2(t) =$	$m \cdot \sin(2 \cdot \pi \cdot f_r \cdot t) + H_3(t)$	: modulation signal H_3: 3^{rd} harmonic
$U(t, \vec{\Theta}, \vec{k}, \vec{A}) =$	$A_1 \sin(2 \cdot \pi \cdot f_r \cdot k_1 + \Theta_1 + \Delta\phi) + ...$ $+A_n \sin(2 \cdot \pi \cdot f_r \cdot k_n + \Theta_n + \Delta\phi)$	U : common mode $\vec{\Theta}, \vec{k}, \vec{A}$ are vectors with several common mode harmonic components

$$\vec{\Theta} = \begin{bmatrix} \Theta_1 \\ \Theta_2 \\ ... \\ \Theta_n \end{bmatrix} \quad \vec{k} = \begin{bmatrix} k_1 \\ k_2 \\ ... \\ k_n \end{bmatrix} \quad \vec{A} = \begin{bmatrix} A_1 \\ A_2 \\ ... \\ A_n \end{bmatrix}$$

The state equation (2.11) is a non linear function of the common mode harmonic components and the flying capacitor voltage, considering grid current and the modulation signal as disturbances.

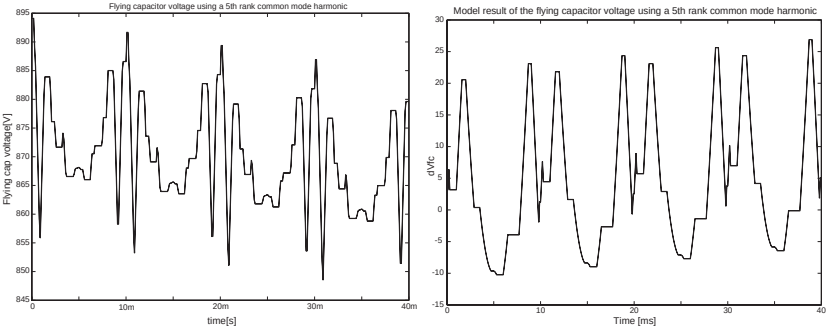


Figure 2.24.: *Flying capacitor voltage using a 5th order stabilization common mode signal. Left, simulation, and right, mathematical model results.*

Comparison between the model and simulation results show that the correlation is not very good although the allure is similar. Divergence over the time can be typically corrected closed loop correction of the state variables.

Conclusions

It can firstly be noted that the model presented here, even though it is a much simplified representation of the reality, is already quite complex and non-linear. The discrete characteristic of the switching events is made continuous by a mean value approximation in order to avoid having a discrete time hybrid system (which would lead to a mixed logical dynamical model and therefore complex algebraic calculations) but still the equations remain highly non-linear. The results of the model show a correlation with reality (in this case simulations) but the performance is not so good.

But more importantly, this modeling does not allow a direct understanding of the influence of the parameters on the system dynamics. For this

reason mainly, a different approach to the modeling of the system was undertaken. The aim is to try to reveal the influence of adding some harmonics, or changing the power factor, on the stabilization of the capacitors of the CCIL topology.

2.3.4. A graphical model

Background motivation

The idea is to find a new model which allows a general understanding of the system's dynamics, for any power factor or modulation index. In his PhD work, Martin Veenstra presents a set of graphs showing the charging and discharging regions in function of the modulation index and the power factor. The target here is to obtain one single representation valid for all modulation indexes and power factor.

The expected representation is obtained inspired by the work done by Christoph Haederli, on the representation of the neutral point current, for his PhD work.

Common mode representation

Methodology The representation is built in two phases. First the current is considered. Since the capacitor voltage is exclusively controlled by the current, it is necessary to find the graphical adequate representation for the current flowing through the capacitor.

The second phase concerns the output voltage. Since the modulation must ensure that the output remain undistorted, the maximum allowable common mode regions have to be drawn such that they are never exceeded. The control variable is the common mode voltage, so it must be drawn in a proper way as well.

First step - the current The current is considered as perfectly sinusoidal and of constant amplitude. The influence of these hypothesizes are discussed later. Thus, in space phasor representation, the current moves around a circle of constant amplitude and with a constant speed, Figure 2.25B.

Instantaneously, the sign of the current flowing across the the capacitor depends on the converter's switching state and is described by the switching function, eq.(2.11). The amplitude of the current is given by the instantaneous current magnitude.

Because the current amplitude varies like a sinus with a fixed frequency, the current across the capacitor, for one switching state, behaves like a

sinus as well. A maximum current will become a minimum current after half a period. At each levels, the current amplitude is plotted, and between the levels, a linear extrapolation is done, Figure 2.25A.

The global picture coming out of Figure 2.25 is that, as the red phasor moves to the blue one, the red pattern turns into the blue one.

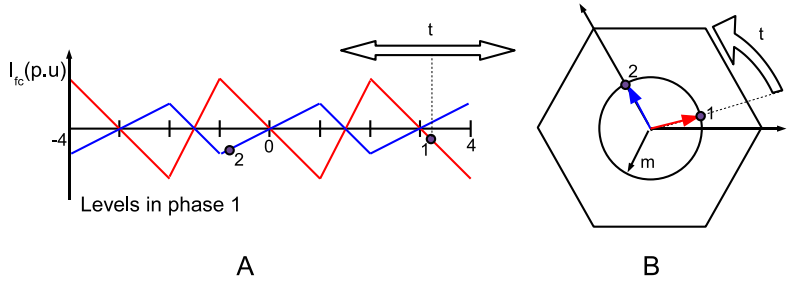


Figure 2.25.: *Common mode general representation - step 1*

The output voltage is now also considered. Assuming that the current and voltage are in phase, the voltage is also represented by the points (1) and (2), Figure 2.25B. The voltage is generated by the choice of the appropriate level at the output. Assuming that the voltage of point (1) corresponds to a positive amplitude between 3 and 4, the point (1) is represented on the red current pattern, Figure 2.25A.

Since the voltage is also sinusoidal, the point (1) moves to the point (2). At the same time, the current pattern moves from the red to the blue. This gives an image of the current amplitudes the phase capacitor sees, and is precisely what is looked for.

Second step - the common mode The dashed red area on Figure 2.26 represents the maximum allowed common mode amplitude on the upper and lower side in function of time. The size of the common mode area is a function of m and of time. The common mode which can be applied is not the same everywhere during one period. There is also a anti-symmetry on the common mode area between the positive and negative side.

Final step The two representations of Figure 2.25 and 2.26 are combined into a single Figure 2.27.

The background pattern of the figure is the capacitor current amplitude pattern defined by the current amplitude and the switching states. The

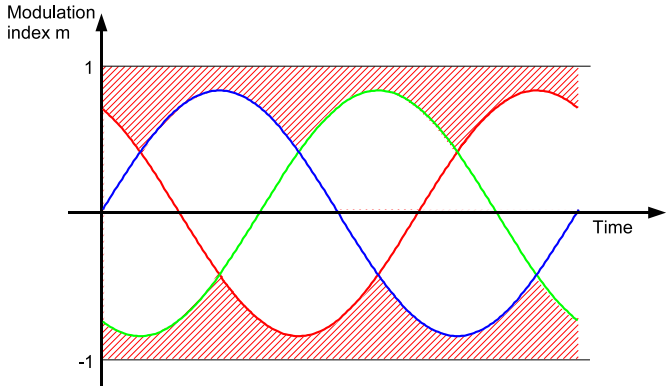


Figure 2.26.: *Common mode general representation - step 2*

pink regions are positive current densities regions and the blue negative current density regions.

The levels are indicated on the Y-axis. For a given level, i.e. on a horizontal line, the current density follows a sinusoidal variation which amplitude depends on the switching state.

The influence of a different power factor $\cos\varphi$ (i.e. a phase shifting of the current with respect to the voltage) is translated by a shift of the background pattern toward the left or the right, with no change in the structure. In fact, the structure depends only on the topology of the converter (see Table 2.7).

The black sine curve is the reference signal. The common mode region is represented here by the darker area around the voltage reference. If the reference plus the common mode stabilization value remain in this area, the phase to phase voltages are never distorted.

Capacitor voltage ripple analysis

With the new graphical model, it is possible to analyze the common mode harmonic strategy of §2.3.2, and explain and reproduce the resulting waveform of the flying capacitor voltage observed in simulation. The voltage trajectory is plotted in the model, and the capacitor ripple is analyzed, Figure 2.28. The trajectory crosses two main areas denoted as 1 and 2.

1. In this region, the voltage trajectory crosses regions where the capacitor is loaded with high charging and discharging current densities in

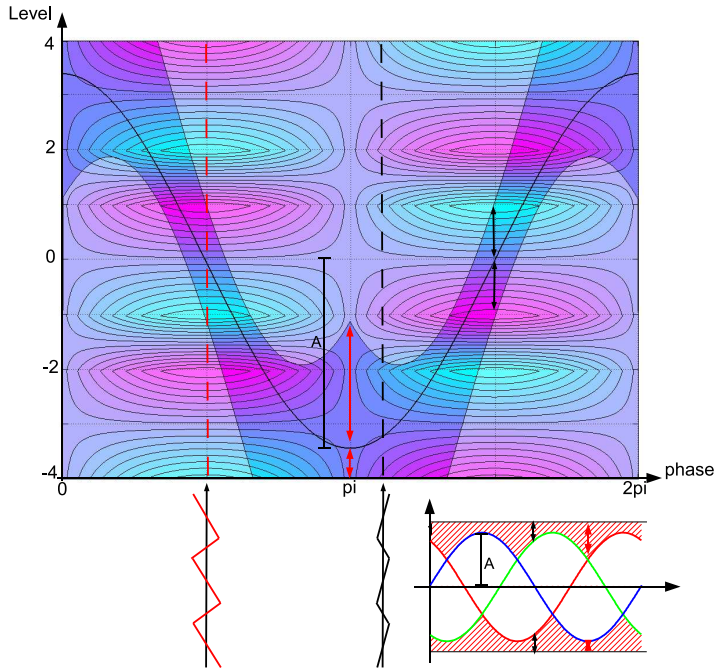


Figure 2.27.: *New general common mode representation*

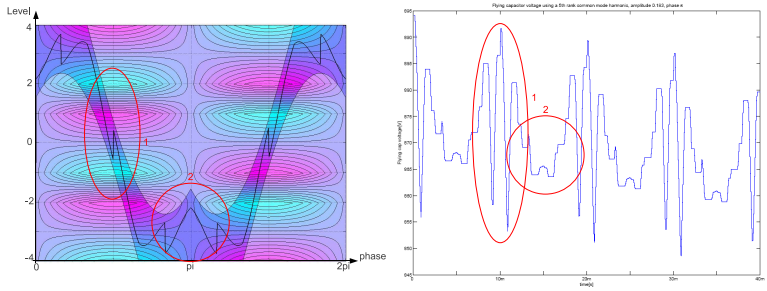


Figure 2.28.: *Flying capacitor ripple analysis*

a short period of time. The natural consequence is a high frequency and high amplitude ripple on the flying capacitor.

2. In this region the trajectory crosses a much "flatter" region. This results in the low frequency ripple that is observed from simulation results.

Graphical model

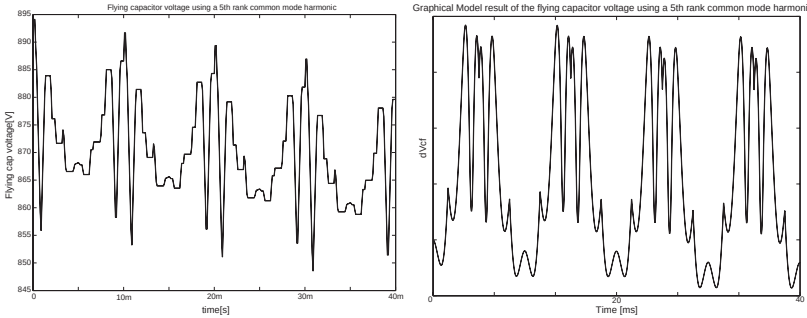


Figure 2.29.: *Flying capacitor voltage using a 5th order stabilization common mode signal. Left, simulation, and right, graphical model results.*

Not only can the representation be used to analyze the capacitor ripple, it can also be used as a model. Integration of the background on the trajectory described by the curve on Figure 2.28 gives the waveform of the flying capacitor voltage (Figure 2.29). When compared with the simulation results (Figure 2.24) it is seen that the curves are pretty similar, even though the discontinuous behavior is not modeled in the graphical representation.

Limitations and use

The developed model is very convenient for implementation. It is basically a 2 dimensional lookup table giving the relative amplitude of the current in the phase capacitor as a function of the relative output voltage amplitude and the time. Very low calculation power is required, and the model is valid for any operating points and power factor.

There are two main limitations that must be taken into account regarding the graphical model of the CCIL phase capacitor. It should not be forgotten

that the representation results from a simplification of the real life behavior of the system.

First, the currents are always considered sinusoidal. If this should not be the case, the representation can be modified adequately. But in the case the representation is used like a model of the system, and stored in a lookup table, it cannot be modified on-line. In that case, the model would no longer be valid.

Secondly, the switched behavior is not modeled. Linear extrapolation is done between the levels to get a piecewise linear switching function. If the switching frequency is too low compared to the capacitor voltage inertia, then the model is also not longer valid.

Conclusions

With the new representation method developed in this section, several interesting results are obtained. Physical understanding of the influence of the common mode on the flying capacitor voltage ripple is achieved. This representation, helps to explain and even reproduce the capacitor ripple waveform as well, if not better, then the previously developed mathematical model, §2.3.2.

It is a powerful tool to qualitatively predict what is the influence of given control signals, and can therefore be used as a simple model of the system (in the form of a lookup table for instance) for implementation of a capacitor voltage regulation algorithm.

2.3.5. Blocking voltage requirements

Hybrid topology

Until here, the topologies were always drawn with full IGBT configuration. It is however reminded that the initial topology is the 5L hybrid ANPC configuration. Hybrid in the sense that the switches are of mixed type, IGBT and IGCT, according to their respective voltage stress in the circuit.

In this section a small analysis of the blocking voltages is done, in order to give an idea about the requirements in terms of components for the CCIL and the influence of the voltage boosting over this aspect.

The IGCT stage of the 5L requires 3.2kV DC blocking voltage capability. It is a low switching frequency stage (fundamental switching frequency) which makes use of IGCTs interesting in terms of conduction losses.

The 4 IGBTs require 1.6kV of DC blocking voltage capability. One criteria for measuring the characteristics of the inverters, and which is used later

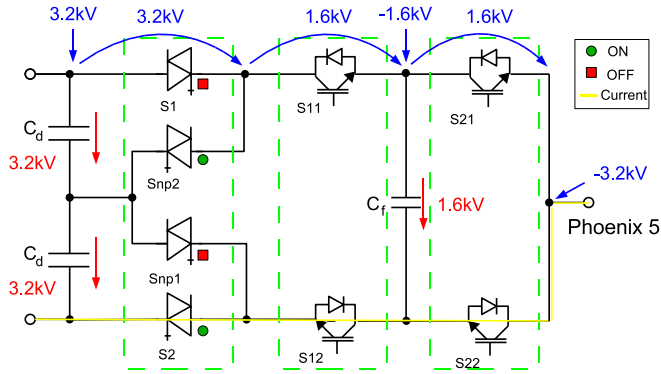


Figure 2.30.: *5L ANPC - blocking voltage requirements*

on for the comparison of the topologies, is the total installed blocking voltage. It is the sum of the blocking voltage of every individual switch within the circuit. This figure gives an image of the amount of silicon installed and reflects to some extent the costs and the losses induced by the circuit. For the ANPC converter, the overall total blocking voltage requirement is 19.2kV.

9 level and 7 level CCIL single capacitor

Until now, nothing has been discussed about the switching frequency of the high voltage stage in the boosting CCIL configurations. Because of the common mode control algorithm, it is possible that the high voltage stage must switch with a higher switching frequency than the fundamental.

For that reason, the switches are drawn using all IGBT configuration.

The total blocking voltage for the 9L single capacitor CCIL is 19.2kV as well. The boosting capability implies that the DC-link voltage can be reduced.

The 7L CCIL single capacitor topology is in fact the 5L ANPC with a different voltage ratio on the capacitor. The total blocking voltage of the converter is in this case also 19.2kV.

It should be kept in mind that the 7L and 9L CCIL topologies cannot achieve maximum modulation index at active power. In other words this means that a higher DC-link voltage would be required on the 7L and 9L inverters in order to get the same output power, thus a higher total blocking voltage with respect to the output power.

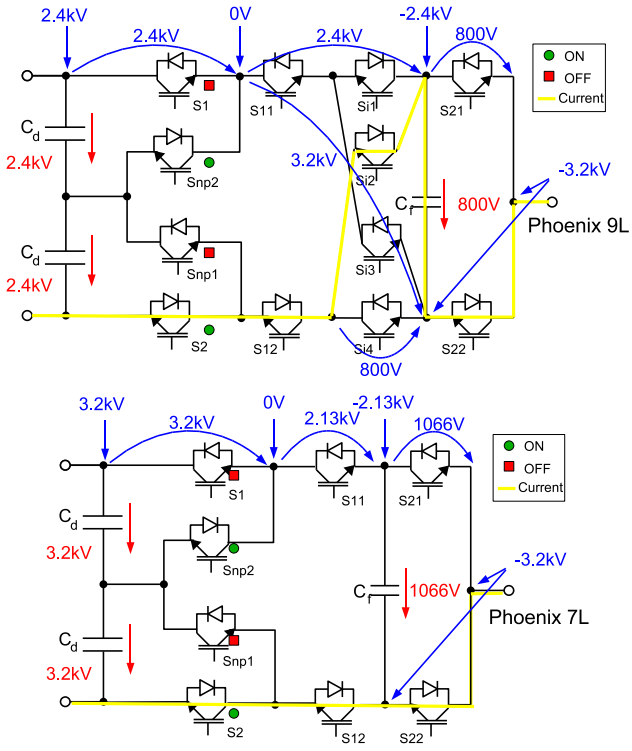


Figure 2.31.: *9L (top) and 7L (bottom) - blocking voltage requirements*

As the maximum modulation index with the proposed strategy is known, it is possible to define how much more blocking voltage is necessary. This amount is not an absolute value, since optimizing the control can allow to reach higher modulation indexes and thus, reduce the total blocking voltage.

The modulation index limit observed in simulations for the 9L CCIL around $m = 0.9$. This means that to reach the same output power then an inverter with a modulation index of $m = 1.15$, the DC-link must be increased by approximately 20%. Thus the total blocking voltage rises from 19.2kV to 24kV.

9L double capacitor CCIL

Just as an additional information, the blocking voltage of the 9L double capacitor is also given here. Since the topology has redundant states, it can be drawn using IGCTs. Fundamental switching of the high voltage stage can be ensured. The total blocking voltage is 24kV.

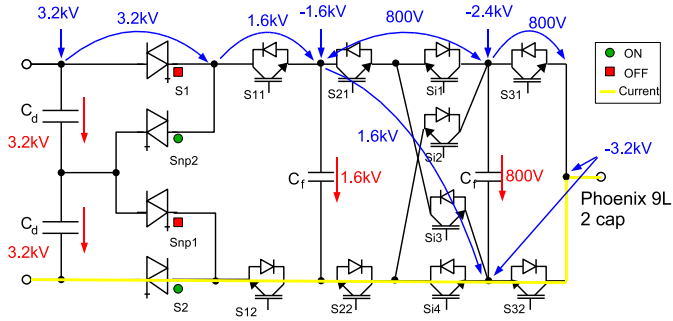


Figure 2.32.: *9L double capacitor CCIL - blocking voltage requirements*

2.4. Modulation algorithm

2.4.1. Model predictive control

Principle

Model predictive control becoming more and more common in industry, [31]. It is quite commonly used since the 1980s in complex but slow systems, like petrochemical plants, but can be traced back to the 1960s, Kalman et al., [32], [33]. With the increasing computational power, this control strategy is becoming applicable in a larger variety of systems. The concept is relatively simple in theory, but applying it to a non-linear system with n-degrees of freedom is however not so trivial.

MPC is discussed here because the graphical model offers interesting perspectives regarding the prediction of the capacitor voltage variations, and that thus, it might be possible to optimize the ripple with the help of this powerful control theory.

As demonstrated by the open loop multi-parametric simulation results (§2.3.2), the control of the flying capacitor voltages by common mode harmonics is possible. However the influence of the control parameters on the

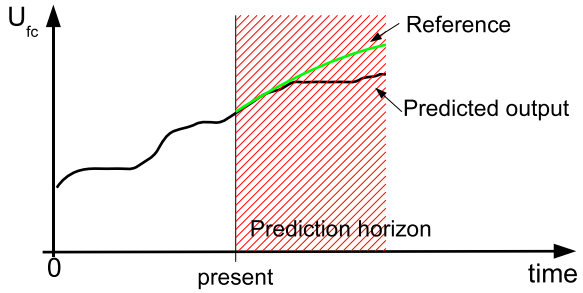


Figure 2.33.: *Model predictive control strategy - minimize the trajectory error on a given horizon*

capacitor voltage is highly non-linear. One possible way to control this system is to use model predictive control. The outputs can be predicted for various input parameter combinations and the best solution retained.

MPC schemes, Figure 2.33, [34], [35], are based on measurement (and/or estimation) of the converter state (currents, voltages) at current time and a model of the system. The evolution of the controlled variables is predicted for various inputs and tuned until the predicted output error is minimized over a so called prediction horizon.

In the present case, finding the optimal control sequence requires minimizing a linear or quadratic optimization problem, subject to non-linear constraints (the model of the system), with n-degrees of freedom. The number of variables in the optimization problem, n, is the control horizon size multiplied by the number of parameters to optimize. This means that the control equation to be solved is rather complex, and stability issues are non-trivial to answer.

Formulation of the control problem

This section reminds the basic principles of model predictive control. Because of computational constraints, the cost functions are most of the time chosen as quadratic, unless the problem explicitly would require a linear cost function. In the case of the CCIL topology, and for minimizing capacitor voltage deviations, quadratic cost functions ought to be well suited.

In general, for linear systems, the state equations can be written as:

$$\dot{\vec{x}} = A\vec{x} + B\vec{u} \tag{2.12}$$

$$\vec{y} = C\vec{x} + D\vec{u} \tag{2.13}$$

The optimization problem reads :

$$\min_{u(t,t+T)} J \tag{2.14}$$

with

$$J = \underbrace{\frac{1}{2}\int_{t}^{t+T} x(\tau)^T Q x(\tau) + u(\tau)^T R u(\tau) d\tau}_{\text{quadratic cost}} + \underbrace{\frac{1}{2} x(t+T)^T P x(t+T)}_{\text{terminal set}} \tag{2.15}$$

Assuming it is possible to solve the optimization problem J, under the constraints given by the system's state equations, a control sequence $u^*([t, t+T])$ is obtained. This sequence is the optimal solution of the control problem. If the system is ideal (no disturbances, perfect model), the sequence can be applied and the output will perfectly match the reference, with a minimum cost, after time T (prediction horizon).

In reality, the sequence cannot be applied from the beginning till the end, since an ideal system does not exist. A closed loop version of the MPC is then used. It is called receding horizon MPC and it introduces a feedback in the controller, [36]. Only the first sample of the calculated sequence is applied to the output. At the next step, a new optimal control sequence $u^*([t+1, t+1+T])$ is calculated, of which only the first step is applied, etc.

The quadratic cost function J is the Lyapunov candidate function for assessing the stability of the system. It can be demonstrated that with infinity time prediction horizon, and convex constraints, the quadratic cost function is a strictly decreasing energy function. Thus, there exists one and only one solution to the optimization problem. The problem is then always feasible and the controller is stable.

For non infinity time prediction horizon, which is the case in real life, an additional term is necessary to ensure stability. This term covers the time from the end of the prediction horizon up to the infinity, and is called the terminal set.

To summarize, the terminal set is required because receding horizon MPC is only a suboptimal solution to the optimization problem. Stability can only be demonstrated for infinity time prediction horizon, so the terminal set must cover the part of the cost function from time $N+1$ to infinity.

Equation (2.15) contains 2 terms. The first expression (inside the integral) is the quadratic cost function to minimize (error on the states of the predicted output). Matrices Q and R give relative weights to the states and the inputs, and can be used, if necessary, to tune the optimization. The other term of the cost function is the terminal set. There are several ways to determine this terminal set, who lead to various MPC strategies.

It is also fundamental to define how the problem should be solved. If it is possible to decompose the system in piecewise affine subsystems, linear MPC can be applied locally.

Explicit MPC strategies (off-line MPC) can also be interesting since they implicitly define linear regions. The controller gains are then implemented in a look-up table, in function of the region where the system is, defined by states, the correct gains can be retrieved from the table.

Applying MPC to the CCIL inverter

The main difficulty in applying MPC to control the capacitors of a CCIL inverter is to define the system's equations. They must be defined mathematically. Preferably, they should be linear, and it is indispensable that are convex. The problem can then be formulated, and ideally, the stability can be assessed.

The optimization problem must then be solved. Here also, solving the quadratic control problem is most likely non-trivial.

At this stage of the work, one of the main interest is to assess whether the topology actually can be stabilized with the proposed model, and what are the expected performances. For that reason, spending a lot of time on developing a MPC scheme for this topology is not desirable.

Conclusions

MPC is a powerful control strategy, but has several drawbacks: the formulation of the problem and the stability of the controller are important and hard to solve, and would need some time.

It is important to remind that at this stage, the principle target of the work is to demonstrate the feasibility of the stabilization concept, in order to assess the performances provided by the CCIL topology. Future work can include advanced control schemes to get higher performances out of the system, but at this stage, functionality is the main aspect to be demonstrated.

This is the reason which motivated a different approach of the control problem. A more direct method was retained, which certainly gives less good overall performances than a carefully defined MPC scheme but which is, on the other hand, more straightforward to implement.

2.4.2. Fuzzy logic control

Motivation

Use of fuzzy logic control in multilevel inverters is not new, [37]. It is usually motivated by control of complex non linear systems for which a good base of knowledge is available and can be exploited. The basic idea of the control scheme is to use the graphical model to get information about the system's dynamics and evolution.

The graphical model of section §2.3.4 easily gives a qualitative information about the behavior of the system (it is of course also possible to get quantitative information out of the model if necessary). The common mode harmonic approach is dropped and a strategy focusing on the correction of the deviation of the capacitors one at a time is chosen. This results in a high frequency common mode pattern which corrects the capacitors the most deviate in priority.

Since a simple, yet robust, algorithm is desired to mainly demonstrate the feasibility of the balancing on the CCIL topology, fuzzy logic controller is well suited. The information given by the graphical model can be directly used and systematical development of the regulator makes the implementation easy.

The development and implementation of a fuzzy logic controller for the CCIL topology, which allows balancing of the phase capacitors of the circuit, with the help of a graphical model, is one the the original contributions of this thesis. The structural diagram of the regulator is already presented on Figure 2.17.

Fuzzy logic - Basics

In this subsection a short reminder of the basics of the fuzzy logic control is given.

Figure 2.34 shows the structure of a fuzzy logic controller. The first step is the fuzzification of the input value. The result is a fuzzy vector which contains as many fuzzy variables as there are of membership functions (the input fuzzy sets characterize the input, for instance, moderately charged, strongly discharged, etc). The fuzzy variable indicates the degree of belong of the input value to the membership functions (or fuzzy sets). In the example of Figure 2.34, a is the degree of belonging of x to the fuzzy set A, and b of x to B.

Once the fuzzy input vector is known, the fuzzy output vector is constructed by means of the fuzzy inference and the fuzzy output sets. The inference is a rule which describes how the degrees of belonging to the input fuzzy sets apply to the output fuzzy sets (the output fuzzy set describe the

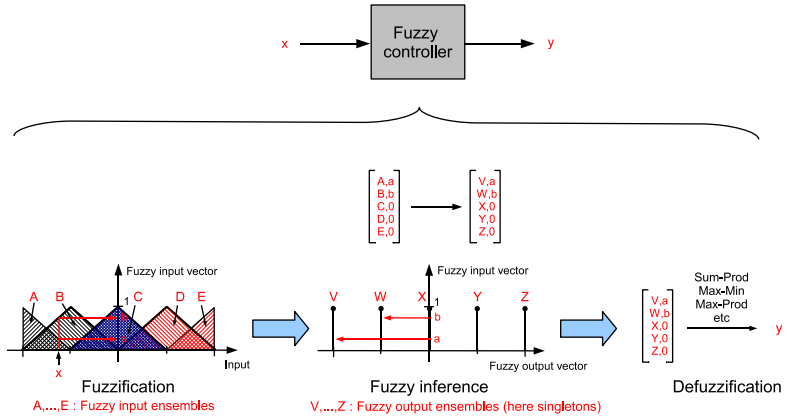


Figure 2.34.: *The 3 main steps of fuzzy logic control: fuzzification, fuzzy inference and defuzzification.*

set of actions to be taken, for instance moderately discharge, or strongly charge). On Figure 2.34, the degree of belonging to A is directly related to the output singleton V, B to W, etc. With this, the output fuzzy vector is constructed.

The last step is transforming the output fuzzy vector into a numerical value which is the output value of the controller. This can be done in several manners among which the sum-prod, max-min, or max-prod methods. For instance, the sum-prod method consists in multiplying the degree of belonging to the set and summing all these products. For example:

$$y = V \cdot a + W \cdot b + X \cdot 0 + Y \cdot 0 + Z \cdot 0$$

CCIL 9 level - Input fuzzy set

The first step is the fuzzification of the flying capacitor voltage. Five input fuzzy sets are chosen, as shown on Figure 2.35. The values of x_1 to x_5 are constants. The maximum instantaneous current amplitude, applied during one switching period on the phase capacitor of known value, determines the largest voltage difference which can be corrected in one cycle. Thus it determines what the boundaries of the fuzzy sets are (x_1 and x_5). The other points are linearly extrapolated in between.

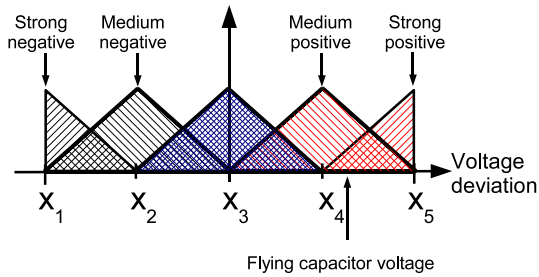


Figure 2.35.: *Fuzzy input set*

For example, with a moderately over charged capacitor, the fuzzy input vector could look like:

$$V_{fc} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ 4/5 \\ 1/5 \end{bmatrix}$$

CCIL 9 level - Output fuzzy set

The output fuzzy sets are dynamic in this application. A new output fuzzy set is defined at every clock cycle, based on the pattern given by the graphical model over a certain prediction horizon.

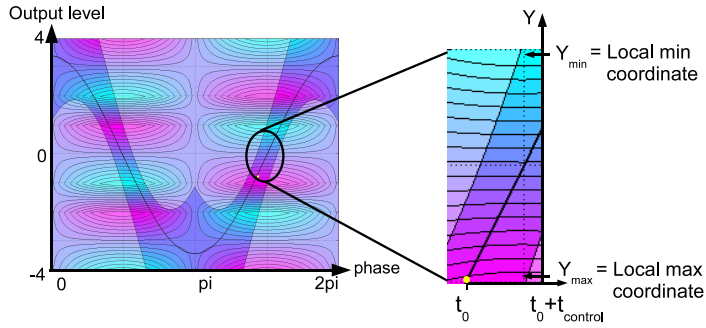


Figure 2.36.: *Pattern over the control horizon* $t_{control}$.

Figure 2.36 shows a point at a given time (yellow spot). It follows a sine reference signal on which a common mode value will be applied to stabilize the capacitor.

Onwards from the yellow point stretches the control horizon $t_{control}$. This is actually the time during which the calculated common mode sequence is applied (i.e. it can be equal to the the switching period or longer). An optimal solution as far as control is concerned is to choose $t_{control} = t_{switching}$.

A first analysis of the pattern in the region defined by the control horizon is needed to find a local maximum and a minimum (red and blue areas). In some cases, with very low modulation indexes, there could be several maximums and minimums in which case adjacent maximum and minimum should be chosen.

The coordinates[1] of the max and the min (y_{max} and y_{min}) are used to determine the fuzzy output set. It is important that the search for the max and the min is done two dimensionally, over the area defined by the control horizon without taking into account, at this point, the common mode limits.

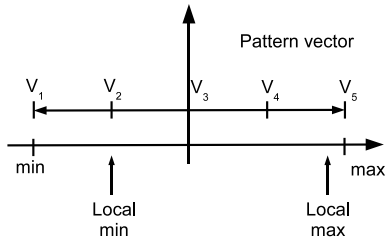


Figure 2.37.: *Position of the local maximum and minimum compared with the absolute ones*

The output set contains the coordinates of the points with the strongest charge respectively discharge available on the prediction horizon. The other points are defined by liner extrapolation. Figure 2.37 illustrates this procedure. The local minimum is always "smaller" or equal (in absolute values) to the absolute minimum (the point over all the operation area where the discharge is the strongest). In the given example, the strongest discharge cannot be applied on the capacitor. Similarly for the maximum. The output fuzzy set is defined as:

[1] The background pattern is built as a lookup table which is why the term coordinates is used

$$V_{pattern}(t) = \begin{bmatrix} strong\ discharge\ region(-1) \\ medium\ discharge\ region(-0.5) \\ zero\ influence\ region(0) \\ medium\ charge\ region(0.5) \\ strong\ charge\ region(1) \end{bmatrix} = \begin{bmatrix} y_{min} \\ y_{min} \\ y_3 \\ y_4 \\ y_{max} \end{bmatrix}$$

The values y_3 and y_4 are found by linear interpolation between y_{min} and y_{max}:

$$V_{pattern_n}(t) = \begin{cases} y_{min} & \text{if } \ local\_min < n \\ & n \in \{-1; -0.5; 0; 0.5; 1\} \\ y_{max} & \text{if } \ local\_max > n \\ & n \in \{-1; -0.5; 0; 0.5; 1\} \\ y_{min} - \dfrac{local\_min - n}{\left(\frac{(local\_max - local\_min)}{|y_{max} - y_{min}|}\right)} & \text{else} \\ & n \in \{-1; -0.5; 0; 0.5; 1\} \end{cases}$$

The output fuzzy set indicates the coordinates (i.e. the common mode value) for all the possible corrections of the capacitor voltage at a given point in time. If the necessary correction is not available at the present converter state (i.e. the available horizon) the best choice is going to the least harmful operating point for the capacitor.

Defuzzification

Once the fuzzy output set and the fuzzy input vector are know, the fuzzy output vector is obtained easily by a simple multiplication between the fuzzy input and the inversed pattern vector (output fuzzy set). The inverse is chosen because when the capacitor is charged, the control will try to discharge it, and vice-versa.

In other words, the current status of the flying capacitor (mostly moderately charged) is used to find the needed correction (go mostly to the moderately discharging region). This means mathematically:

$$V'_{pattern} \cdot V_{fc} = \begin{bmatrix} y_{max} \\ y_4 \\ y_3 \\ y_{min} \\ y_{min} \end{bmatrix} \cdot \begin{bmatrix} 0 \\ 0 \\ 0 \\ 4/5 \\ 1/5 \end{bmatrix} \tag{2.16}$$

The result of this operation is an output fuzzy vector containing the coordinates of each type of region weighed by the desired correction factor (in fuzzy logic language, this is called the degree of belonging). The defuzzification is done using a sum-prod algorithm:

$$y_{out} = 0 \cdot y_{max} + 0 \cdot y_4 + 0 \cdot y_3 + 4/5 \cdot y_{min} + 1/5 \cdot y_{min}$$

The result is an output coordinate which corresponds to a point in the control horizon plan. This point is extrapolated to a trajectory (a line) which is the optimized output signal. It needs to be restricted to the allowed common mode region and then it can then be applied to all the phases (Figure 2.38).

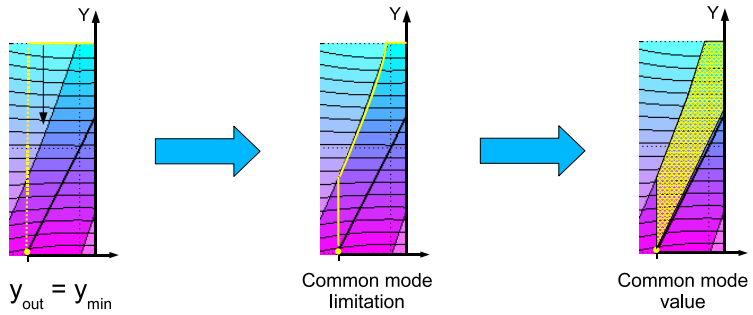


Figure 2.38.: *Once the optimal trajectory has been calculated it must be restrained to the common mode region.*

On Figure 2.39, the result of the fuzzy logic control strategy using the graphical model is shown. It can be seen that the ripple on the flying capacitors is now a random function. The strategy consisting in correcting the most deviated capacitor in absolute value gives good results.

Common mode regulator structure

Putting the various functions, described previously together, yields the final common mode fuzzy regulator. Figure 2.40 shows to structural diagram of the regulator.

Stability analysis

From a strictly theoretical point of view, the stability analysis of the developed fuzzy regulator is not easy to prove. With non-linear systems, asymptotic stability is demonstrated based on the eigenvalues of the system, using the Lyapunovs' methods, [38].

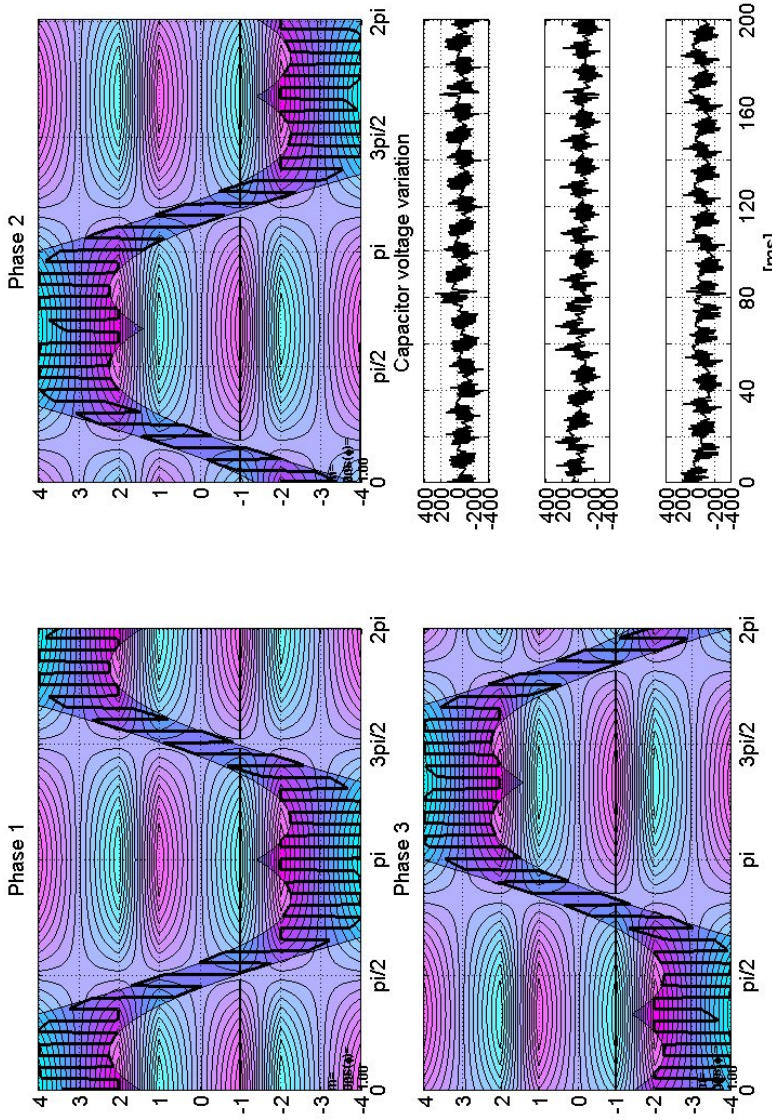


Figure 2.39.: *Waveform obtained with the fuzzy logic controller at a frequency of* $2kHz$, $m = 0.9$, $C_f = 2mF$.

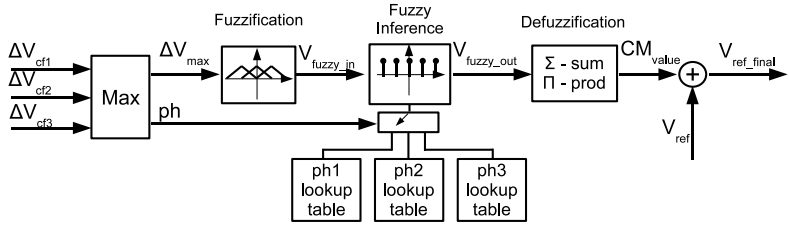


Figure 2.40.: *Common mode fuzzy logic regulator structural diagram*

In this case, the system's equations are not available. Because of high non-linearity, they cannot be derived easily from the graphical model (although it would formally be possible to do so based on model construction rules). So a different approach is proposed to get some idea about stability of the regulator.

The idea is to demonstrate that as time goes to infinity, the system will always tend toward the origin asymptotically. This means that the stability analysis demonstrates that the system will never diverge because of regulator uncertainties under certain operating conditions, and that it is always able to bring the error back to zero as times goes to infinity. From this point of view, some statements can be made.

The system to control is a bunch of capacitors. The dynamics tied to this system are of integral type, unless a short happens between the capacitor and the DC-link. Assuming that the modulation never shorts the capacitor, which is a coherent assumption for demonstration of stability of the fuzzy logic controller which does not look after the modulation, the system can therefore be modeled by some energy function.

The graphical model is closely connected to the physical properties of the system. Because the fuzzy controller rules are based on the inversion of this model, and assuming that the inversion can happen properly (i.e. in other words that the common mode margins are large enough), and because, as demonstrated previously, the controlled variable functions are energy functions, the closed loop equation is somehow a decaying energy function.

So although there is no formal proof of the stability, it can be assumed that the controller is asymptotically stable if the model of the system is correct and the margins are sufficient.

As final word about stability, it can be added that extensive simulation have never shown unstable behavior. It should also be mentioned that formal demonstration of stability is, of course, of high interest on final

solutions. But in this case, the idea is more demonstrating the topology then offering the most efficient control algorithm.

2.4.3. Maximum theoretical modulation index

The maximum theoretical modulation index which can be achieved by the CCIL converter is calculated based on the principles introduced by S.Mariethoz in his PhD work, [21]. The idea is that the maximum power transmitted by the converter is given by fundamental component. The only cells to supply energy to the output are the fed cells, in this case the DC-link.

Thus, the DC-link fundamental waveform is a square waveform of amplitude $3U$. The maximum modulation index is therefore $m_{max=}\frac{3}{\pi} = 0.955$.

2.5. Simulations

2.5.1. Simulation setup

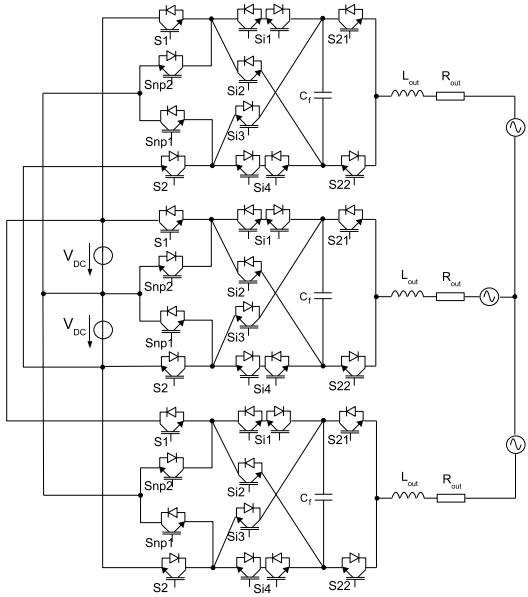


Figure 2.41.: *Simulation setup circuit.*

The fuzzy logic controller is implemented in Matlab Simulink with PLECS for the power electronics part. The simulations show that the control algorithm allows the flying capacitor voltage to be stabilized. The circuit setup for the simulation is configured as a 3 phase symmetrical system, connected to 3 phase shifted voltage sources, to simulate the grid, through an RL load simulating the transformer (Figure 2.41). The phase capacitors $C_f = 2mF$, the output transformer is modeled by an inductance with an impedance X_{out} calculated as 15% of the base impedance, plus a grid short circuit ratio of 20, and R_{out} is 2% of the base impedance (base impedance $Z_b = V_{LL}/(\sqrt{3} \cdot I)$).

2.5.2. 9 level single capacitor CCIL

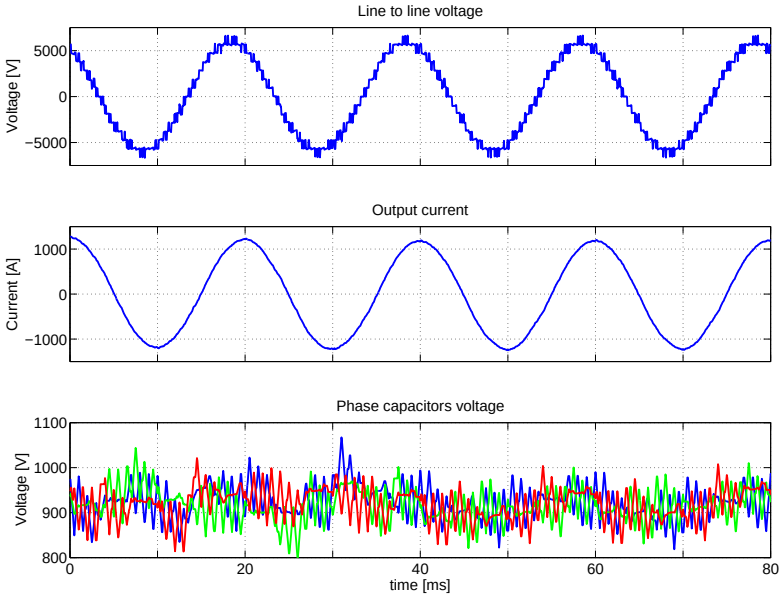


Figure 2.42.: *Simulation waveforms for the 9L CCIL single capacitor, at m=0.9, 2kHz*

The 9 level inverter cannot be stabilized with modulation indexes greater then 0.91 at full active power, while it is possible to stabilize for any modulation index under full reactive power.

The presented simulation waveforms (Figures 2.42) are obtained at $m = 0.9$, $\varphi = 0$, $V_{LL} = 4160V$, $I_{rms} = 900$, $C_f = 2mF$, $f_{sw} = 2kHz$, $V_{DC} = 5.675kV$, $V_{cf} = 946V$.

The voltage ripple amplitude on the phase capacitors is $\pm 150V$. This coincides well with the estimated ripple amplitude given by the graphical model (Figure 2.39) which is also $\pm 150V$.

The capacitor voltage contains some spikes of relatively high amplitude. These can be due to over- or under-corrections of the regulator, or are the result of the correction on another phase capacitor.

The line to line voltage has a good harmonic content (§2.6.3), but there is a low frequency ripple on the output currents. Simulations have shown that with a more stable phase capacitor voltage, these low frequencies are reduced. This indication about the origin shows a correlation between the harmonic content of the capacitors and the output current, while the voltage seems not to be influenced so much by the capacitor ripple.

The control signals are close to expected by the graphical model simulations. The pole voltage can jump more than a step at time, which can lead to increased switching losses (depending on the type of commutation), but is necessary for capacitor stabilization. This is one drawback of the retained stabilization scheme.

2.5.3. 7 level single capacitor CCIL

The control algorithm remains identical for the 7L with only a small change in the pattern structure. Simulation results show that the performance of the 7L is inferior to the 9L, although the output voltage is not boosted. An analysis based on the graphical model is sufficient to understand what happens.

Simulating the 7L regulator with the graphical model gives the results presented on Figure 2.43-top. At the places where the corrective actions are the most efficient (maximum and minimum current amplitudes), the only available actions are to charge or do nothing on the capacitors. At the same positions, with the 9L CCIL topology, all the 3 actions are available on the capacitor. This indicates that the 7L is less controllable then the 9L structure. This explains why the 7L results are inferior to the 9L. This is seen more generally in the benchmarking chapter (§2.6).

Overall, the 7L CCIL can be stabilized for modulation indexes starting from 0.85. For modulation index $m = 0.85$ and a power factor $\cos\varphi = 1$, at 2kHz, the waveforms of Figure 2.43-down are obtained.

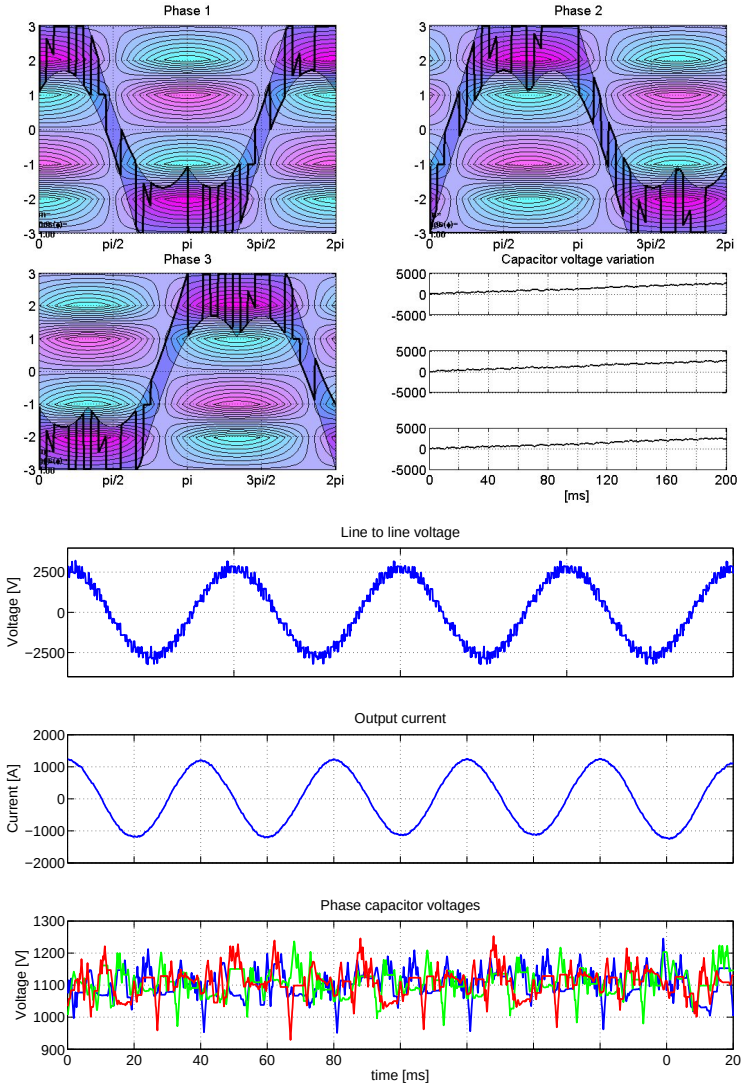


Figure 2.43.: *Top: Graphical model simulation of the 7L inverter - $m = 0.9$, $\varphi = 0$, $f_{sw} = 2kHz$, not stabilizable. Down: Simulation waveforms for the 7L CCIL at 2kHz, m=0.85.*

2.5.4. 9 level double capacitor CCIL

The 9L double capacitor CCIL topology is a redundant state topology. It therefore does not require any specific modulation strategy, from a general point of view. Matlab simulations are also done for this topology, since it is benchmarked later one.

The results shown here are at a modulation index $m = 0.9$, at 2kHz. The capacitors are $C_{f1} = 2mF/1.6kV$ and $C_{f2} = 4mF/800V$. Overall, the capacitor voltages are well stabilized. The ripples are $\pm 400V$ and $\pm 200V$ on the phase capacitors 1 and 2 respectively. This value corresponds to the 20% ripple for which the capacitor values are calculated for using the capacitor equation formula : $C = \frac{I_c \cdot \Delta t}{\Delta V_c}$.

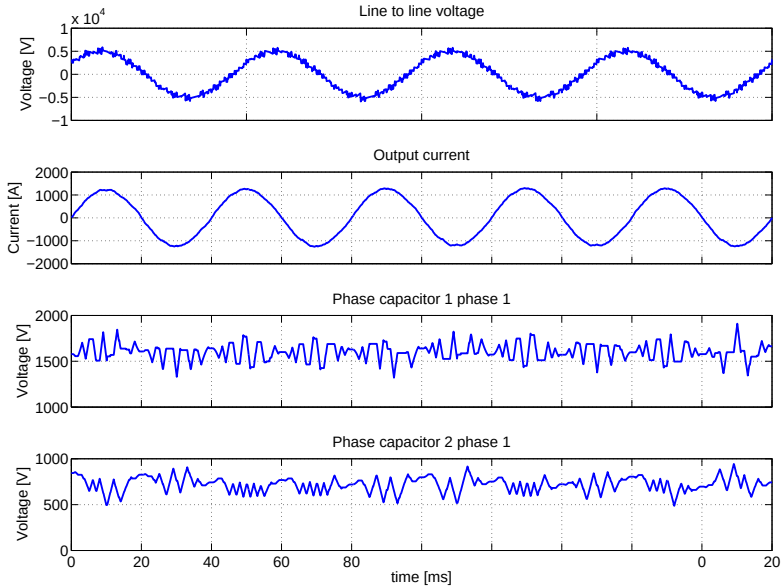


Figure 2.44.: *Simulation results for the double capacitor 9L CCIL, at m=0.9, 2kHz.*

2.5.5. Regulator performances

Regulator-less

Using the graphical model, if a pure sinusoidal waveform is applied, it is observed that the capacitor is balanced after one grid period. This means that theoretically, the 9L single stage CCIL topology does not require the modulator to balance the capacitors (Figure 2.45-top). On the other hand, simulation results show that in reality, at least under certain circumstances, this automatic balancing characteristic is lost, Figure 2.45-down.

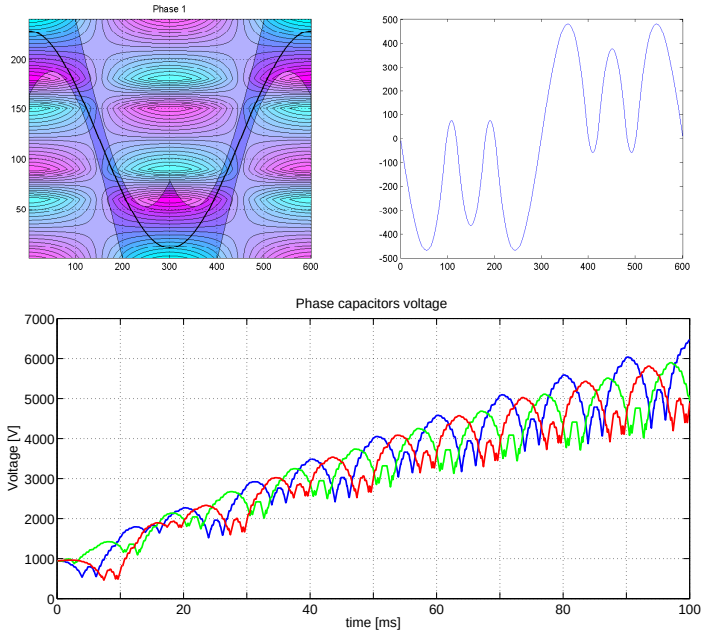


Figure 2.45.: *Top: Graphical model simulation, and down Matlab simulation, of the phase capacitor voltage for an unregulated reference signal - $f_{sw} = 2kHz$, $m = 0.9$, $\varphi = 0$*

The reason why the graphical model gives a different result from what is observed in simulation is because one important assumption of the graphical model is that the output current is sinusoidal. What typically happens, when the output voltages get too distorted due to large capacitor voltage

ripples, is that the output currents are no longer sinusoidal. Thus the model is no longer valid.

If very large capacitors are used, or a very rigid grid, then it is likely that the topology can be self balanced after one grid period.

Smallest theoretical ripple

The smallest ripple achievable, at given modulation index and power factor, is interesting to assess the regulator's performance. Since it is not easy to define a theoretical limit for the modulation index, defining how well the modulator does is not so easy.

For example, at $m = 0.9$ and $C_f = 2mF$, a pattern is tuned "by hand" such as to get the smallest ripple on one phase capacitor (i.e. avoid the strongly charging and discharging regions), regardless of the ripple on the two other phases, Figure 2.46.

The output voltage is tuned for one phase only and it can be made almost equal to 0. But then, on the two other phases, control of the capacitor voltages is lost. This shows that the ripple is strongly depending on the overall balancing of the 3 phases. This helps to give a reference about performances when using the fuzzy logic regulator which ensures equal stabilization on all the capacitors.

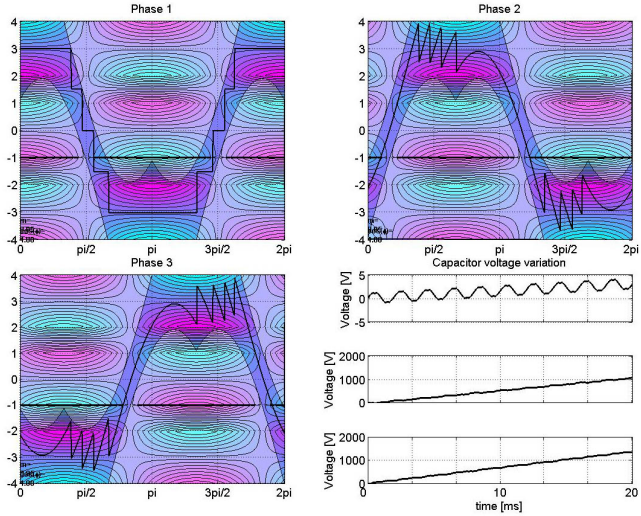


Figure 2.46.: *Tuned pattern for minimum ripple amplitude.*

Hysteresis controller for the 9L CCIL

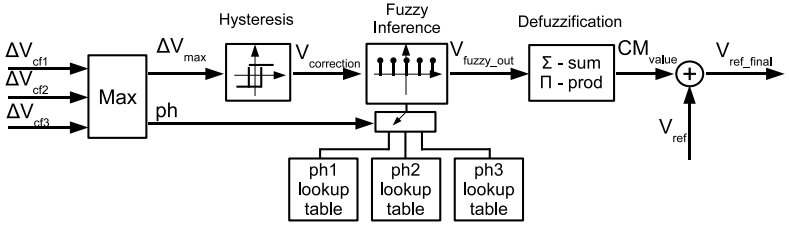


Figure 2.47.: *Common mode hysteresis regulator structural diagram*

The fuzzy logic controller allows to balance the capacitor voltages with a ripple amplitude of $\pm 150V$. A hysteresis controller is implemented to compare performances, Figure 2.47. The strategy of the hysteresis control is very similar to the fuzzy logic control. It is however constraint to only two possible actions: strong or zero correction, depending on the error. This means that the hysteresis controller is a sort of 2 input and output set fuzzy controller, having only the extreme actions. Typically, the $\underline{V}_{\text{correction}}$ vector will have only 2 values, 0 and 1, positioned at the extremes (charge or discharge).

The results are similar in terms of waveform, Figure 2.48, but it happens that the control is locally lost on the capacitors. One possible explanation is that if the capacitor voltage is very close to the hysteresis band, the control applies a strong, since it can't do anything else, correction in the opposite direction. This is likely to generate a deep which must then be corrected, thus influencing also the other capacitors. A sort of self generated transient.

Optimization of the control is likely to solve this problem, but is not the target here.

Overall signal quality is similar to the fuzzy logic control strategy, with a slight advantage to the latter on, because of the spikes that appear with the hysteresis control. Since the hysteresis is only used as a basis for comparison, it is not further developed. By default, the fuzzy control is used for the benchmarking.

2.5.6. Conclusions

The fuzzy logic controller is proposed as one possible solution for stabilization of the phase capacitor voltages. Based on the graphical model of the system, the method is developed and tested in simulation. With the 9L

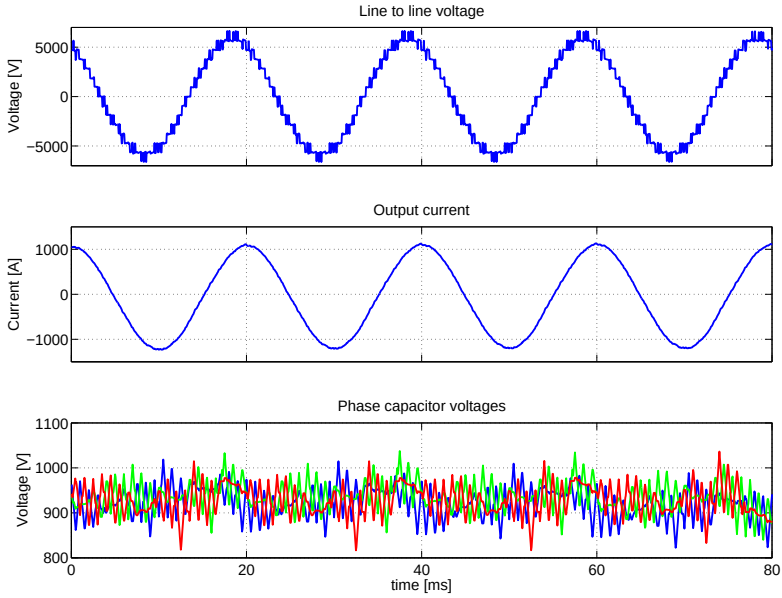


Figure 2.48.: *Simulation waveforms for the 9L CCIL using a hysteresis controller at m=0.9, 2kHz*

single capacitor CCIL topology, the capacitors are balanced up to a modulation index of $m = 0.91$ at full active power. The amplitude of the phase capacitor voltage ripple is close to what is calculated with the graphical model, and also very close to the smallest ripple achieved by hand optimization. This indicates that, with the proposed model, the fuzzy control is well adapted.

The 7L CCIL cannot be balanced for modulation indexes above $m = 0.85$. Analysis and prediction based on the model are able to explain why.

At reactive power, the non-redundant topologies can be stabilized for any modulation indexes. This is not a surprise, and already known in general for non-supplied phase capacitors without redundant states.

The implementation simplicity and low calculation power are extra assets for the fuzzy solution. The question remains whether a MPC based solution could allow to get better results. In fact, MPC will likely not offer higher results regarding control of the phase capacitors, but on the other hand, it allows to take into account other constraints like switching

losses for instance. Thus, the development of an MPC scheme can provide some advantages compared to the fuzzy solution. But the model must be adapted, the problem formalized and the optimization calculated.

At this stage, the results offered by the fuzzy solution are sufficient for moving to the benchmarking of the introduced solution. MPC methods are therefore designated to become a future study subject in a future PhD work.

2.6. Benchmarking

2.6.1. CCIL versus NPC, cascaded H-bridge and flying cap

The equations given in Tables 2.4 to 2.6 of §2.2 characterize the topology in terms of power density and reliability.

The total number of passive components (capacitors) and their voltage ratings define what is the total amount of stored energy, and therefore is a representation of the bulk and the reliability of the inverter. Medium voltage capacitors are space consuming and they account for a large cause in failures.

On the other hand, the number of switches and their blocking capability give an idea about the reliability and the conduction and switching losses in the inverter. Some of these aspects are already discussed in §1.3. The NPC, cascaded H-Bridge and flying capacitor topologies are used as a basis for the comparison, since they are somehow standard in the multilevel topologies.

Number of levels per stage Plotting the number of levels generated versus the number of stages cascaded, Figure 2.49, shows the clear advantage of the CCIL topologies in terms of level generation. The graph shows that in conventional topologies, the progression in the amount of levels generated by the cascade of n stages is linear. Because of the voltage ratios used in the CCIL topologies, the number of levels generated grows exponentially with the stages, denoting that a simple structure offers higher output resolution compared to standard solutions.

It is important to mention that using asymmetric voltage ratios, like for the CCIL, on the other topologies is possible, and would result in similar progressions (exponential) of the number of levels produced by the cascade of stages. But this involves that the principle characteristics in terms of controllability and blocking voltage changes from the usually presented characteristics for these topologies. For this reason, those cases of figure are not considered in the present comparison.

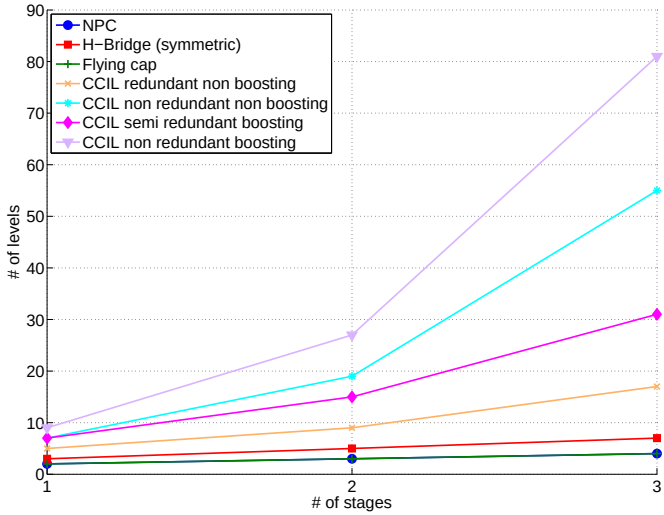


Figure 2.49.: *Number of levels obtained by cascading of stages*

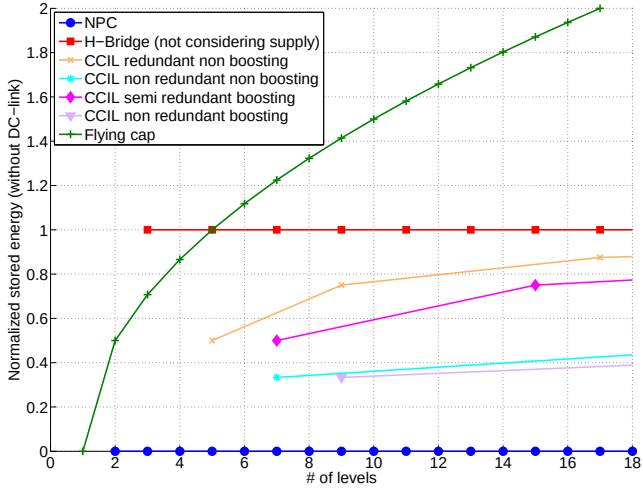


Figure 2.50.: *Amount of energy stored per levels*

Stored energy per level Plotting the amount of stored energy with respect to the number of levels (without counting the DC-link energy with is considered as the same for all the topologies), Figure 2.50, is a representation of the amount of passive components.For details about how the calculation is done for this comparison, refer to Appendix A.1.

This comparison is difficult since the topologies are intrinsically different. The H-bridge configuration likely requires individual power supplies for each of the capacitors or a limited modulation index, which is not shown in the comparison. Similarly, the DC-link of a flying capacitor converter can have a much larger bulk, because it assumes the full voltage by itself, compared to the DC-link of an NPC or CCIL configuration where the voltage is split on several capacitors.

Because the NPC structure is purely DC-link, its energy is minimal. The inherent problems to the topology cannot be seen on this representation, but should be kept in mind (see §1.3.1).

The cascaded H-bridge topology could seem optimal from the point of view of stored energy, however, once again it should be kept in mind that inherently, this topology requires extra power supply or stored energy for proper capacitor stabilization.

The flying capacitor topology requires one extra capacitor per generated level, but with every increasing level, the capacitors see the current for a shorter time ($\frac{T_p}{N}$). The topology can stabilize the capacitors at any operating point, which is not necessarily the case for any of the other topologies. Only the redundant configurations are able to do so, and this is not either shown on the graph.

Even though there are many points to be taken into consideration, the comparison still reflects to some extent that the use of the capacitors is more optimal in the case of the CCIL compared to the other topologies.

Individual switches per level The number of individual switches per levels (independently from their blocking capability), Figure 2.51, gives an idea about the reliability of the inverters. In here, an ideal case is considered, where any blocking voltage would be available. This is of course not the case in reality, but this still gives an indication about the reliability of the converters.

Increasing the number of levels leads to linearly increasing number of switches on standard topologies, which is a direct consequence of the fact that the number of levels grows linearly with cascading of stages. Since the CCIL structure demonstrates saturation behavior, this result is also reflected on the number of individual switches required. Here also, it seems that the CCIL offers some benefits compared to the other solutions.

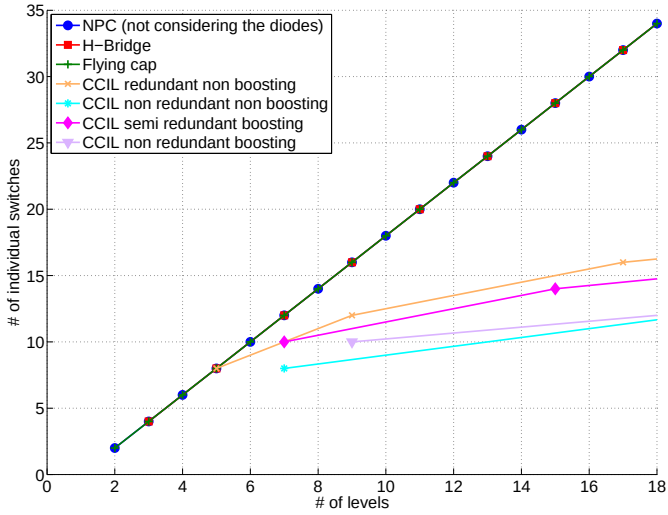


Figure 2.51.: *Number of switches requires per output levels*

Total blocking voltage per level Although the number of individual switches remains low, the total blocking voltage, which is the sum of the blocking voltage of every individual switches, is increased to quite some extent on the CCIL topologies. The ANPC topology already tends to trades off passive components against active switches. The result is fewer switches but of higher blocking capability. The general trend, coming from physics, is that when the number of passive components is decreased, the total blocking voltage is increased.

The most efficient topology in terms of total blocking voltage is the flying capacitor topology (Figure 1.3). It requires a total blocking voltage equal to twice the DC-link voltage value. This topology is situated exactly on the other end of the optimization strategy done here to reduce the number of passive switches. Thus, it offers as advantage a really low blocking voltage requirement.

The NPC seems to compete with the flying capacitor. But it must not be forgotten that the diodes are not considered in this comparison, and that the NPC cannot balance it's DC-link for modulation indexes over the range 0.5 to 0.6.

The CCIL topologies typically require a total blocking voltage equal to 6 to 11 times the DC-link voltage value. In addition to the already pretty high

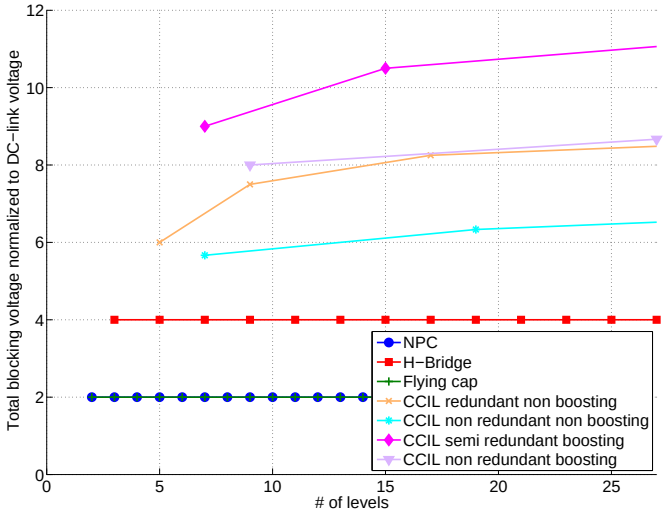


Figure 2.52.: *Total blocking voltage normalized to DC-link voltage per levels*

blocking requirements of the ANPC, the cross connection requires reverse blocking switches and, in boosting mode, higher blocking capability (see §2.3.5).

The comparison is however not so straight forward. It should be remembered that the CCIL can offer boosting capabilities. In this case, even though the total blocking voltage reported to the DC-link is high, since the DC-link can be reduced, the absolute value of the blocking voltage is slightly lower. For instance, with the fuzzy logic control scheme, the DC-link can be reduced by 20%, so the total blocking voltage of an equivalent 9L CCIL is 8 times (see Figure 2.52 for a 9L non redundant boosting CCIL topology) the value of a DC-link voltage reduced by 20%. This means 3 times more blocking voltage compared to the 9L flying capacitor, but 7-8 times less stored energy, and 63% of the number of switches.

2.6.2. CCIL versus hybrid ANPC-H-Bridge

Foremattter

Close to the end of this work, it was found that the CCIL topology offers the same functionalities as the hybrid ANPC-H-Bridge converter (Figure

2.53). This is quite evident, but since the structures differ to some extent, it did not appear that clearly during the study of the CCIL.

Going into more details reveals that in some cases, the hybrid topology is better in terms of blocking voltage, while in other cases, the CCIL is more favorable. But interestingly, besides the fact that the CCIL is a sub-optimal solution regarding switch disposition in some cases, and as a consequence to the fact that the functionalities of the two topologies are the same, the control strategy and the graphical model developed for the CCIL are valid for the hybrid ANPC-H-Bridge topology.

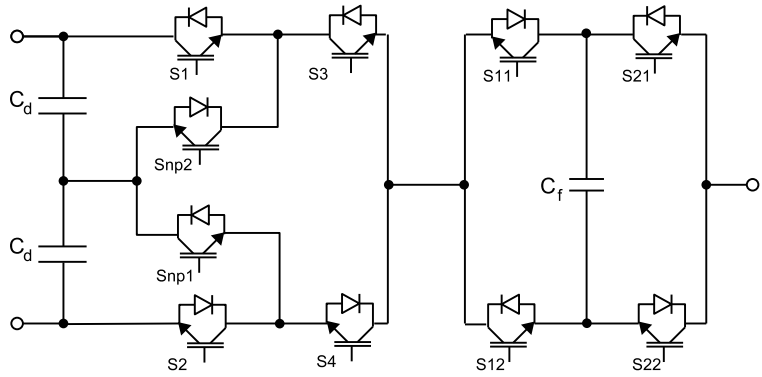


Figure 2.53.: *Hybrid ANPC-H-Bridge converter*

The study of the hybrid topology was already done by M.Veenstra, [29]. The main difference is that M.Veenstra used an MPC approach for the control of the topology, and that in the present case a fuzzy algorithm is used. One of the notable differences is that the proposed algorithm in here does not require any specific startup strategy, contrarily to the MPC based strategy.

Non redundant boosting CCIL

The total blocking voltage in the boosting case, Figure 2.54, of the 9L CCIL topology is $24U$ and for the hybrid converter it is $22U$. Also, the number of individual components is 12 for the CCIL against 10 for the hybrid solution.

In this case, the most interesting topology is the hybrid ANPC-H-Bridge, since its total blocking voltage is a little lower compared to the equivalent CCIL, and so is the number of components.

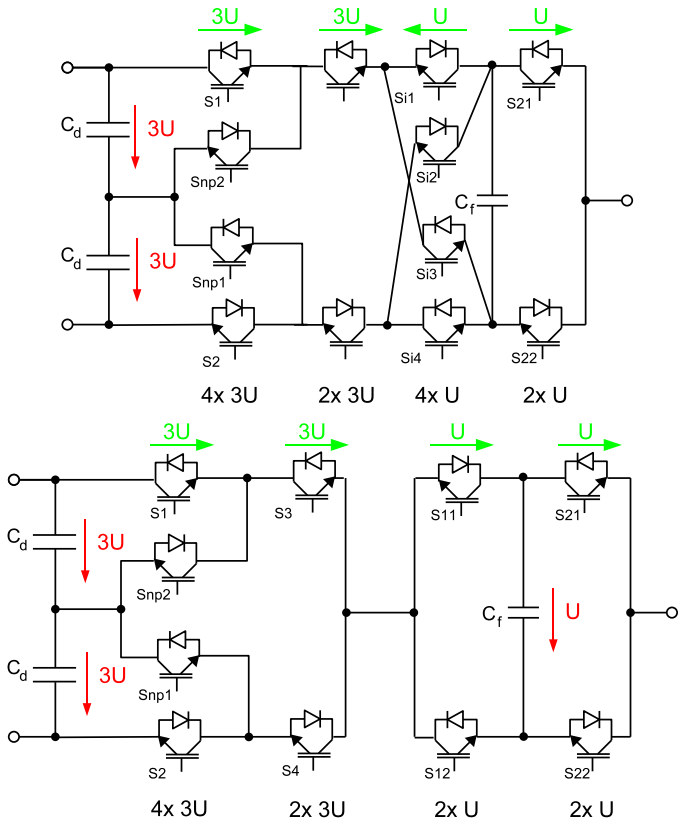


Figure 2.54.: *The 9L boosting CCIL (top) and the 9L boosting hybrid ANPC-H-Bridge (bottom) topologies*

In general, for boosting topologies, the hybrid solution offers lower blocking voltages. The only advantage that can be obtained from the CCIL is that, with more switches, it is possible to share the losses better between the switches, [39], [40]. The significance of this for a given application can only be evaluated in a complex analysis and could be studied in a further work.

Redundant non boosting CCIL

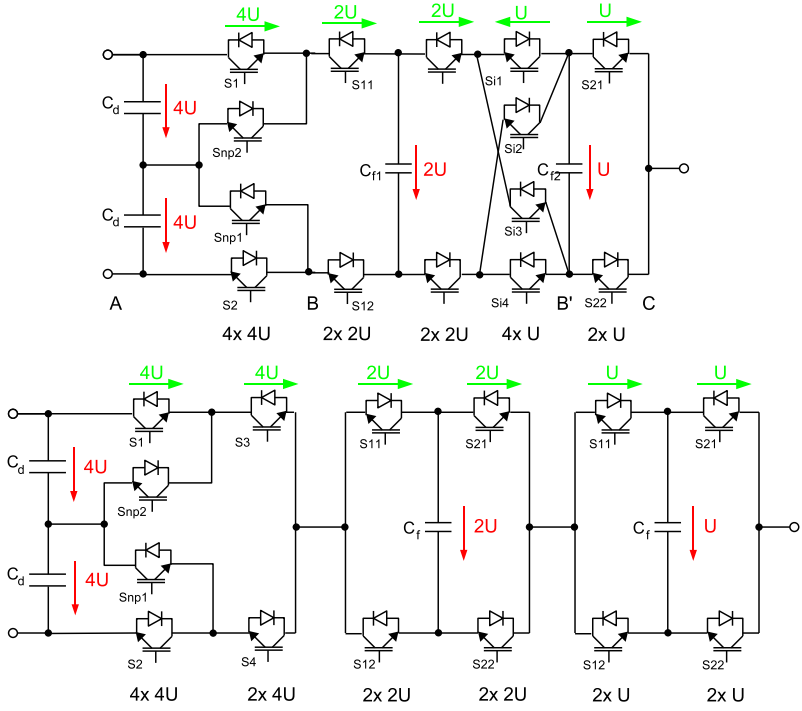


Figure 2.55.: *The 9L redundant CCIL (top) and the 9L hybrid ANPC-H-Bridge (bottom) non boosting topologies*

In the redundant case, Figure 2.55, the total blocking voltage of the 9L CCIL double capacitor topology is $30U$, against $36U$ for the hybrid solution. Both topologies require 14 individual switches.

In this case, the total blocking voltage of the CCIL converter is almost 20% lower than the equivalent hybrid solution. So in the case of redundant configurations, the CCIL is more appropriate than the hybrid inverter.

Conclusion

Since the studied CCIL is based on the ANPC topology, there is a close correlation with the hybrid ANPC-H-Bridge topology. This comparison

shows that, in terms of electrical characteristics, for the boosting case the hybrid solution is better, while in the non boosting case, the CCIL performs better.

From the point of view of the control, both topologies behave exactly in the same way. All the concepts developed for the CCIL apply to the hybrid topology. It is then only the choice of the designer to choose the best suited solution in function of the desired application.

2.6.3. Harmonic distortion

Overview

Demonstration of filterless grid connection requires compliance to the standards. The standards considered in this work are on one hand the German VDEW (Verband der Elektrizitätswirtschaft) standard and on the other the IEEE standards, in terms of current and voltage harmonic contents respectively.

The harmonic content results presented here are obtained from simulation. All simulations are done under Matlab Simulink with the PLECS toolbox for the power electronic circuit simulation. The switching frequency is varied from 1.5 to 5kHz and the power factor is either $\cos\varphi = 1$ or $\cos\varphi = 0$.

The modulation index is set initially to 1.064 which is the nominal modulation index of the 5L ANPC inverter. It is varied down to 0.95, 0.9 and 0.85. This allows the common mode regulator to demonstrate its performances for various modulation indexes. Lower indexes are expected to give better results (see §2.3.2).

Standards

Voltage The voltage standards are given by the IEC61000-2-12 standard, [41] (reported in Table 2.8). They are defined for the 50 first harmonics. The associated THD value is 8%, but this does not necessarily imply that a lower THD value is synonym of compliancy. The distribution of the harmonics across the frequency spectrum is not shown from the THD value alone.

Voltage harmonics beyond order 50 Harmonics beyond order 50 are not taken into account. The reason is that the regulations concerning these high frequency disturbances on the grid are not clearly defined at the moment. Some prescriptions (IEC61000-2-12-Appendix B) suggest that a limit should be given to the harmonics (or interharmonics) between 50th order

Table 2.8.: *IEC61000-2-12 Standards: Compatibility levels for individual harmonic voltages in medium voltage networks (r.m.s. values as percent of r.m.s. value of the fundamental component)*

Odd Harmonics Non-multiple of 3		**Odd Harmonics Multiple of 3**		**Even Harmonics**	
Harmonic order h	**Harmonic voltage %**	**Harmonic order h**	**Harmonic voltage %**	**Harmonic order h**	**Harmonic voltage %**
5	6	3	5	2	2
7	5	9	1 ,5	4	1
11	3,5	15	0,4	6	0,5
13	3	21	0,3	8	0,5
$17 \leq h \leq 49$	$2,27 \cdot (17/h) - 0,27$	$21 < h \leq 45$	0,2	$10 \leq h \leq 50$	$0,25 \cdot (10/h) + 0,25$

and 9kHz at 0.2% of the fundemental. The motivations are acoustic disturbances, resonnance problems or power losses due to circulating currents, to mention only these.

It is to be added that the 9kHz and the 0.2% limitations are highly depending on external parameters which are not clearly defined. Moreover the Matlab simulations with PLECS are not adapted for high frequency analysis, since parasitc effects (like skin effects) are not modeled.

Point of Common Coupling (PCC) Since the inverters are intended to be used in a filterless configuration, the voltage harmonics must be compatible to the standards at the point of common coupling (PCC). In a medium voltage grid configuration, the PCC is situated after the transformer. At the PCC, the voltage and current harmonics should be compliant to the standards. If there are several users on the grid, the sum of the injected harmonics by each of the user should be compliant.

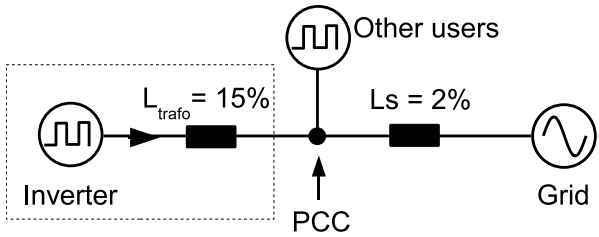


Figure 2.56.: *The converter's output transformer is connected to the PCC, where other users can also be connected*

For that reason, it is not straightforward to establish whether the converter will comply or not, when the actual configuration of the grid is not known. In this case, the transformer has an admitted a short circuit ratio of 15%. Figure 2.56 shows how an actual configuration could look like.

Since the compliance cannot be stated straightforwardly, the output voltage of the converter is compared directly with the standards (Table 2.8). This gives an idea of the range of harmonic distortion which is produced by the converter.

Current The current standards of VDEW[25] are considered in this case. They figure among the most strict standards. They are reported in Table 2.9. As seen, they are valid throughout the spectrum.

Table 2.9.: *VDEW Standards for current harmonic injection in medium voltage networks referred to the short-circuit power*

Order ν, μ (ν odd, μ even)	**Permissible harmonic current** $i_{\nu,\mu\textbf{allowed}}$ in A/MVA	
	10kV network	**20kV network**
5	0.115	0.058
7	0.082	0.041
11	0.052	0.026
13	0.038	0.019
17	0.022	0.011
19	0.018	0.009
23	0.012	0.006
25	0.010	0.005
> 25 or even	$0.06/\nu$	$0.03/\nu$
$\mu < 40$	$0.06/\mu$	$0.03/\mu$
$\mu > 40$	$0.18/\mu$	$0.09/\mu$

THD The THD values are calculated based on the IEC61000-2-12 standards definition:

$$\text{THD} = \sqrt{\sum_{h=2}^{50} \left(\frac{Q_h}{Q_1} \right)^2} \tag{2.17}$$

with

Q	:	current or voltage
Q_1	:	r.m.s. of fundamental
Q_h	:	r.m.s. of harmonic of order h
h	:	harmonic order

Limits of the fuzzy logic common mode regulator

Because the fuzzy control cannot stabilize the topologies for modulation indexes above $m = 0.91$, some operating points will not be achieved on the common mode regulated topologies, depending on the power factor.

But to be systematic, all the considered operating points should be analyzed, even if some topologies give no results.

It must also be remembered that in the present case, the modulation algorithm is designed to validate the control concept and not to offer the highest performances possible, even if the fuzzy control seems to give good results regarding capacitor voltage ripple, and so, indirectly, good results regarding harmonic distortion.

Variations in harmonic content calculations

The harmonic calculation and spectral analysis are highly dependent on the number of samples and the number of periods the signal is simulated on. It is seen that variations in the sampling frequency and/or the number of measured periods can have a significant impact on the spectrum, in the sense that some harmonics start moving around in the spectrum. It can mean that either these harmonics actually do not really exist and are the result of simulation artifacts or that the methodology is important.

Since there is no guideline regarding the way the measurement should be done, it is hard to decide what to do. For this benchmarking, the sampling frequency is always set as 10 times the switching frequency and the the measurements are done over 10 grid periods.

For that reason, the exact numerical values given here can be considered valid for the comparison, since all topologies are benchmarked in the same conditions, but not necessarily true in an absolute way.

Voltage harmonic distortion

Figure 2.57 presents the summary of the findings. Considering each topology separately, the following considerations can be done.

The 5L ANPC topology only starts to be compliant from 3kHz on regarding the THD value. From the spectral analysis, the voltage harmonic contents does in fact comply mostly with a 3kHz switching frequency. At 2kHz, Figure 2.58-top, some harmonics above order 15 are quite largely over the standards.

For 7L CCIL, THD value indicates that the topology is compliant at all the tested switching frequencies. But from spectral analysis, at m=0.85 and 2kHz, Figure 2.58-bottom, the generated waveform is no fully compliant

The 9L CCIL is definitely compliant at all the considered switching frequencies. Figure 2.59-top shows the situation at m=0.9, 2kHz. It is very clearly seen that the voltage is compliant until the 39th harmonic. At these frequencies it is already questionable whether the phenomenons are modeled properly.

The double capacitor 9L CCIL converter offers good results as well, but these are surprisingly not at the same level as the single capacitor 9L topology. It can be caused by the influence of the double capacitor ripple on the output waveforms. It is also noticeable that the results are worse at 2kHz, maybe caused by some resonant problems. The spectrum of the voltage at m=0.9, 2kHz, Figure 2.59-bottom, shows that the voltage is not compliant from order 33 onwards.

Comparing harmonics at active and reactive power, Figures 2.60, shows that the general trend, for the common mode stabilized CCIL topologies, is a better harmonic content at active power. It can be understood by analyzing the repartition of charging and discharging regions over one grid period (§2.3.4). In the case of reactive power, the maximum, respectively minimum, regions are situated where the $\frac{dv}{dt}$ of the pole voltage is high (around the zero crossing). Theses regions are crossed rapidly, generating high frequency and high amplitude ripple on the capacitor, which degrades the harmonic content.

The 5L topology is a redundant state topology allowing the system to be independent from the power factor. The double capacitor 9L is not 100% redundant (see §2.1.2), which can explain the different results observed between active and reactive power.

Current harmonic distortion

The current harmonic distortions of the 5L ANPC cannot comply with the standards below 4kHz. At these frequencies, the waveforms are mostly

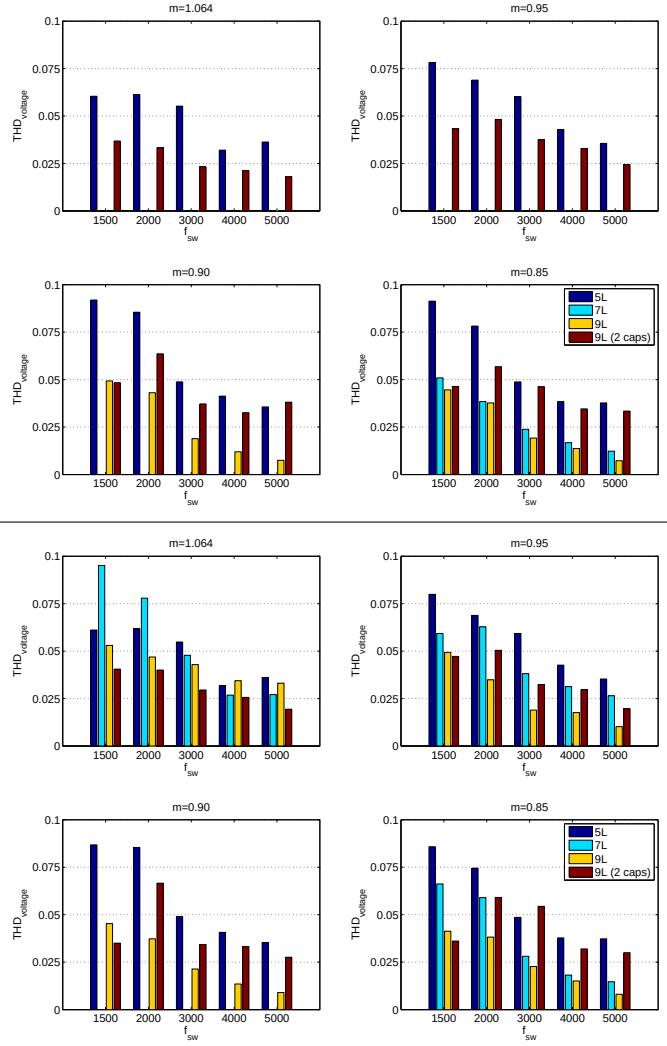
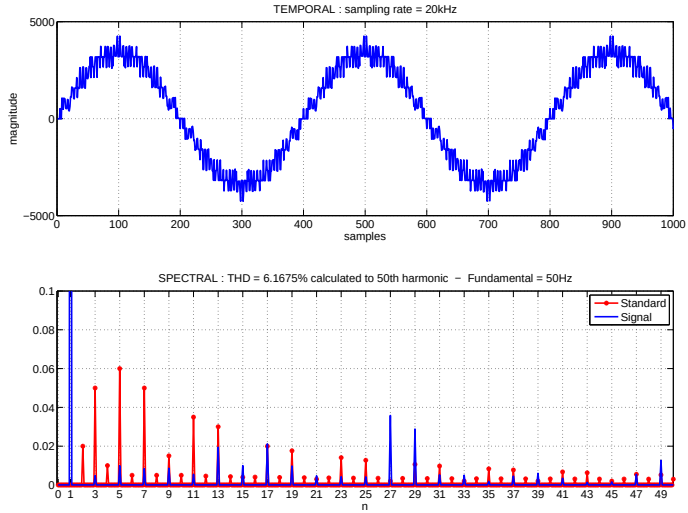


Figure 2.57.: *THD of the line to line voltage. 4 upper:* $\varphi = 0$*, 4 lower:* $\varphi = 90$



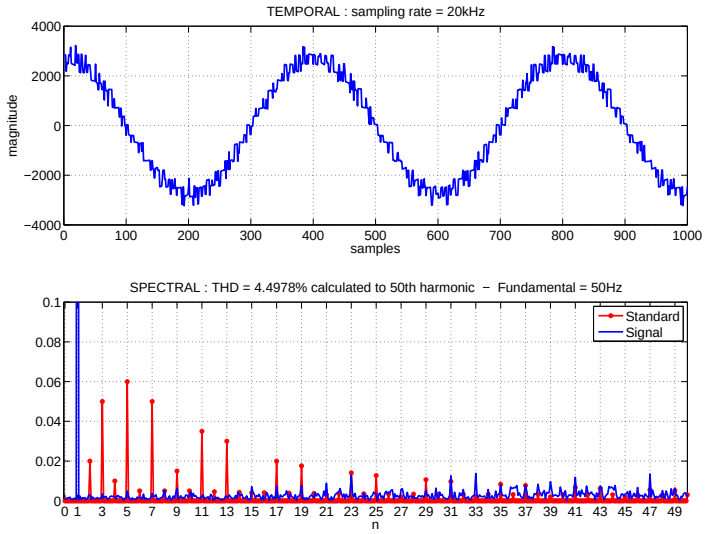


Figure 2.58.: *Voltage THD spectrum for the 5L ANPC (2kHz, $m = 1.064$), top, and the 7L CCIL(2kHz, $m = 0.85$), bottom.*

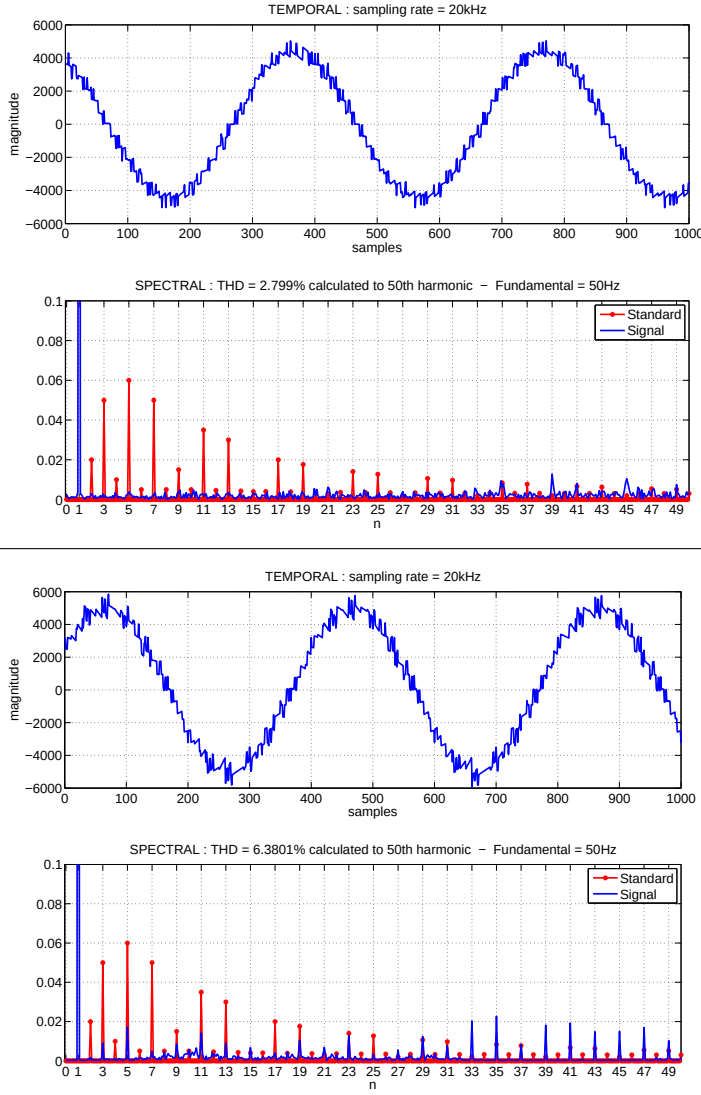


Figure 2.59.: *Voltage THD spectrum for the 9L single capacitor CCIL, top, and the 9L double capacitor CCIL, bottom (both at 2kHz, $m = 0.9$).*

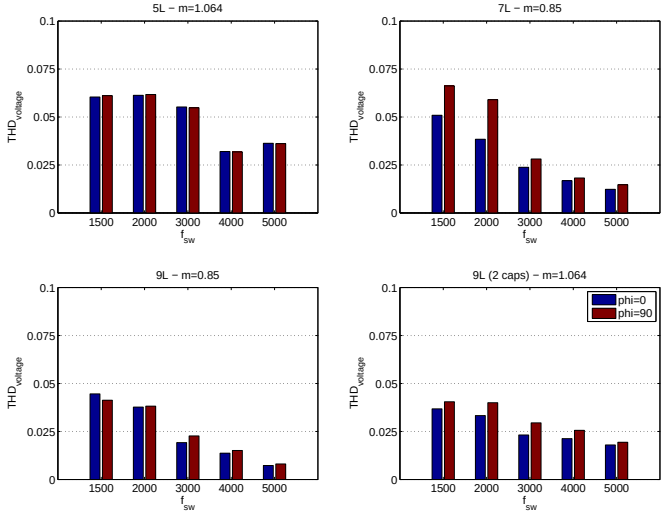


Figure 2.60.: *Voltage THD at one given operating point for each topology,* $\varphi = 0$ *and* 90

compatible, but not strictly. Since the non-compliant harmonics are at higher frequencies, it is likely they are damped.

The 7L CCIL suffers from a large low frequency ripple, Figure 2.62-bottom. It is not really clear where the ripple comes from but this severely impacts the harmonic distortion value. But besides this low frequency, the current is mostly compatible. A large amplitude 27th harmonic can be seen.

The 9L CCIL suffers from the same problem as the 7L regarding the low frequency ripple. It is less marked then in the 7L case, Figure 2.63-top. Increasing of the switching frequency seems to solve the problem. It is possible that a closed loop current control completely eliminates the problem. Besides the low frequency ripple, the current is mostly compatible at all the considered switching frequencies.

The double capacitor 9L CCIL also has a low frequency ripple, Figure 2.63-bottom. The current also presents a quite large quantity of other low frequency harmonics which do not appear on the single capacitor 9L CCIL topology. Increasing the stored energy in the capacitors does not help reduce the harmonic distortion but increasing the switching frequency

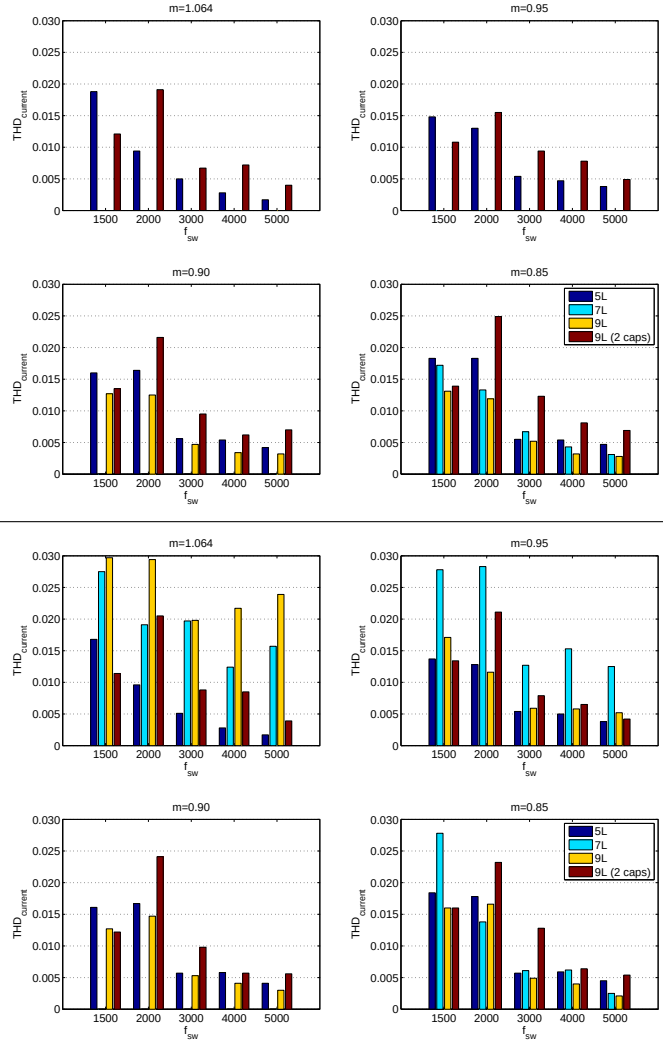


Figure 2.61.: *THD of the output current. 4 upper:* $\varphi = 0$*, 4 lower:* $\varphi = 90$

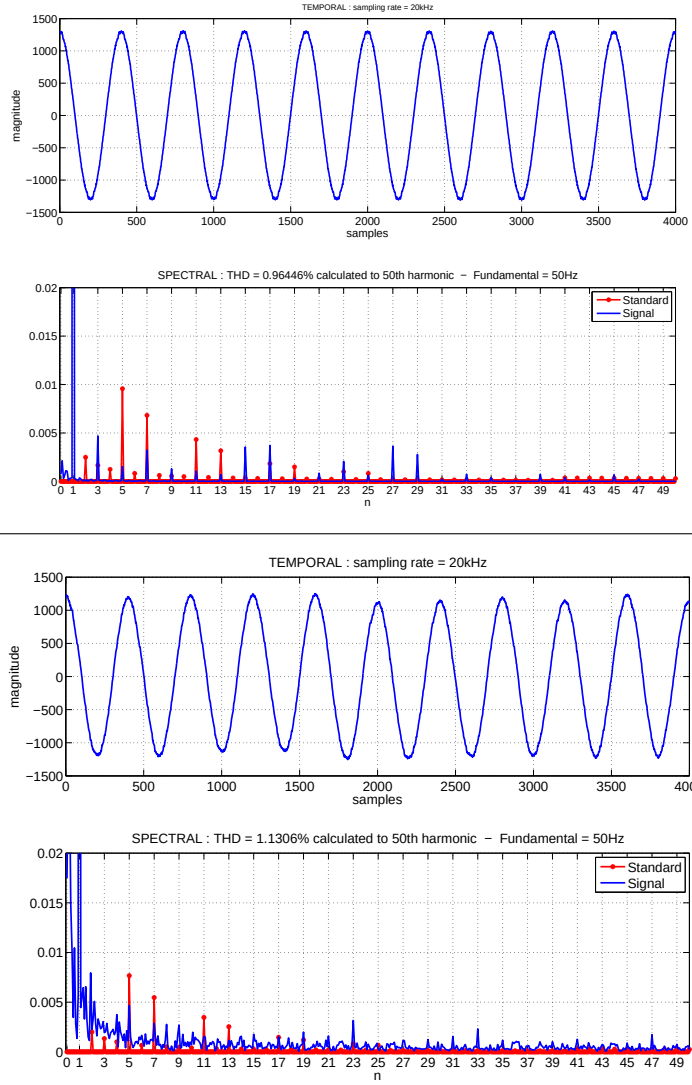


Figure 2.62.: *Current THD spectrum for the 5L ANPC (2kHz, $m = 0.9$), top, and the 7L CCIL (2kHz, $m = 0.85$), bottom.*

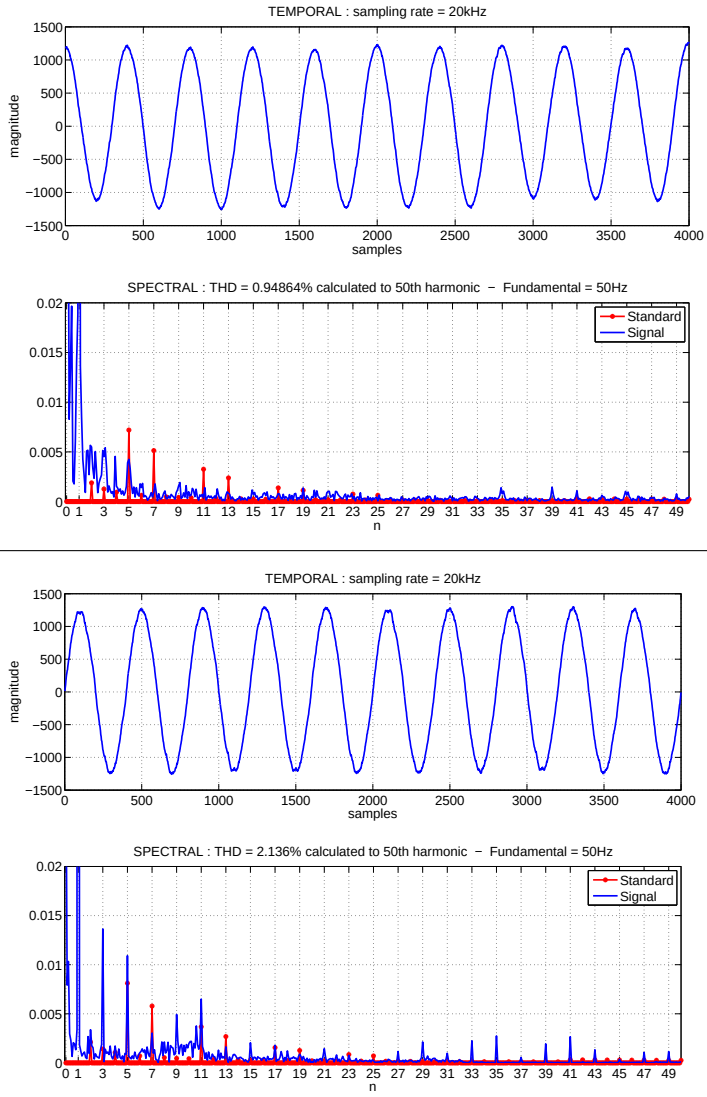


Figure 2.63.: *Current THD spectrum for the 9L single capacitor CCIL, top, and the 9L double capacitor CCIL, bottom (both at 2kHz, $m = 0.9$).*

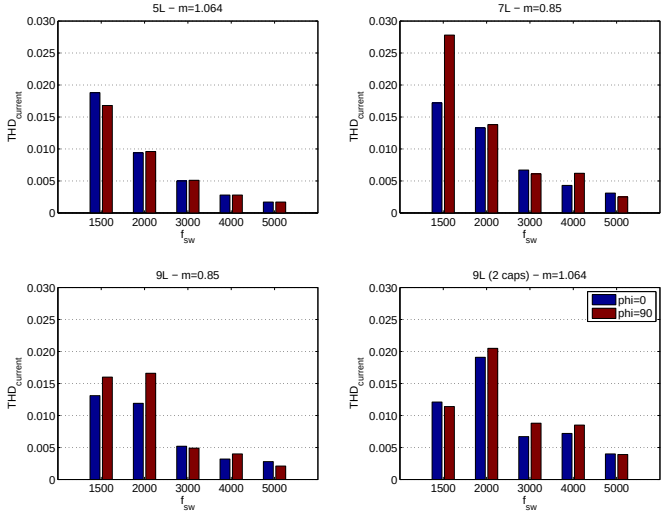


Figure 2.64.: *Current THD at one given operating point for each topology,* $\varphi = 0$ *and* 90

does. The problem could be linked to delays introduced by the control which result in phase errors.

Regarding variations of the harmonic content between active and reactive power generation, Figure 2.64, the same trend as for the voltage can be seen. In general, the harmonic content is better at active power.

Summary of the findings A summary of the previous findings is presented in Table 2.10. It serves as a general overview of the performances offered by the different topologies introduced in this chapter.

Filterless grid connection seems possible with the 9L topologies at switching frequencies around 2kHz, but some optimizations are necessary, especially regarding the current waveforms. Perhaps it is enough to introduce a closed loop current control, but maybe it will also require some optimization of the modulators.

Harmonic distortion conclusions

The results presented in this section are to be taken under the following assumptions: first of all, it should be reminded that they are obtained by means of simulation. It is clear that all the phenomenon are not modeled

Table 2.10.: *Summuray of the various topologies and their conformity to standards*

Topology	Voltage	Current
5L	Above 3kHz	Around 4kHz
7L	Around 2kHz, modulation index is limited to 0.85 at active power	Above 3kHz at m=0.85
9L	Starting at 1.5kHz.	Because of low frequency ripple, starting at 3kHz.
9L 2 caps	Around 2kHz	Because of low frequency ripple, around 4kHz

and reality might differ to some extent. Experience showed that the harmonics calculation is very sensitive to parameters (sampling rate, number of samples) and the results can vary a lot on given harmonics, depending on the parameters. The standards do not mention any specific method for calculation of the harmonics besides the THD formula, so it could be interesting to develop a simulation procedure based on real life measurement methods.

Secondly, concerning the low frequency ripple observed on the currents, it must be as well remembered that the implemented modulator focuses on validating the control concept, rather then optimizing the performances. As mentioned, MPC might offer an alternative to increase the performances, but previous work shows that the design of the MPC can be delicate, [29].

It is hard to rate the topologies adequately, because of the low frequency ripple which introduces lot of distortions in the lower range of the spectrum. However, Table 2.10 summarizes under what conditions the topologies are most likely to allow compliant operations with the standards.

Evidently, more work can be done on the optimization and analysis of the harmonic contents of the CCIL topologies, notable to address the low frequency ripples. Some research directions could focus on phase errors between the output voltages and the grid voltages in open loop control schemes. Small phase errors can result in the sort of phenomenon observed.

2.7. Conclusions

An innovative proposal for a novel multilevel converter topology is done in this chapter. The newly introduced topology offers design solutions for high power density converters. The specific design of the CCIL topology is intended to make full use of voltage ratios which allow an exponential

growth in the number levels produced by cascading the stages. This design procedure is chosen because the target is to obtain a high number of levels with a simple structure containing as few components as possible. Keeping the number of components reduced (active and passive) helps to keep the reliability and power densities high.

Producing many levels with a low number of passive components does not come without a price however, and the main drawback of the CCIL converter topologies is the total blocking voltage which increases by a factor 1.5 to almost 3 compared to more classical topologies. If large blocking voltage components are available, the reliability can be really kept high, but if the ratings are such that series connection of components is necessary, then the solutions must be assessed on a case to case basis.

The conduction losses are, on the other hand, always higher, since the total blocking voltage is higher. This problem is however counter-balanced by boosting capabilities of some CCIL configurations. It is shown, for instance, that the 9L single capacitor boosting CCIL topology only requires 20% extra blocking voltage compared to the 5L ANPC topology to produce the double of the levels.

A graphical model of the system is developed and allows a good understanding of the phenomenons happening in the converter. The capacitor ripple can be estimated with a good precision and various analysis are possible, to explain for instance the origin of the degraded performances of the 7L single capacitor CCIL.

A suitable control algorithm based on fuzzy logic is presented. The control offers sufficient performances regarding the balancing of the capacitor voltages and is suitable for DSP implementation. The maximum modulation index reachable with the proposed control is $m = 0.91$. Theoretically, $m = 0.95$ can be reached. The proposed modulation algorithm is therefore not able to reach the maximum modulation index. Some open questions remain, notably the low frequency ripple on the output currents and the switching frequency of the high voltage stage, but these issues can be solved.

Harmonic analysis shows that the 5L ANPC requires a 4kHz switching frequency to comply with the standards in a filterless grid connected configuration. The 9L boosting CCIL topology can comply already at 1.5kHz regarding voltage harmonic content, and provided the low frequency current ripple can be solved efficiently, it should not require more then 2kHz to be able to comply for currents as well. The principal limitation of the topology concerns the maximum modulation index.

A parallel is found between the CCIL and the hybrid ANPC-H-Bridge topology. In the non boosting cases, the CCIL topology is more efficient then the hybrid topology in terms of components whereas the opposite happens in the voltage boosting case. The model and the control scheme devel-

oped for the CCIL is also valid for the hybrid topology, since the structures are very close and totally similar from the point of view of functionality.

The redundant state CCIL configuration offers the possibility to reach a modulation index $m = 1.15$. The price to pay is a higher number of active and passive components compared to the non-redundant boosting topologies. In this case as well, the low frequency ripple on the current appears, but once again, this issue can be solved and is therefore not a critical aspect.

The efficiency is not addressed. The reason is that the proposed modulator is not optimized regarding the switching frequency of the high voltage stage. The results would then not be valid in the case of an optimized solution. It can still be stated that the conduction losses will increase since they are proportional to the total blocking voltage of the converter. A large amount of silicon implies more resistance on the current paths.

All in all, it can be concluded that the proposed topology offers interesting solutions for increasing the signal quality with a high power density and reliability. There is less stored energy in the converter, fewer switches, no need for an output filter. But the price to pay are higher blocking voltages, thus more conduction losses and more installed silicon. An absolute conclusion cannot be given. The trade-off can clearly be seen between number of components and blocking voltage, and in the end, the choice depends on the wanted characteristics.

CHAPTER 3

Introducing the Common Cross Connected Stage (CCCS)

3.1. Introductory word

The previous chapter introduced as a first contribution of this thesis, a new and original topology containing a cross connected stage. The main characteristics of this topology were the high number of levels generated by a relatively small number of components, increasing the reliability of the converter and reducing the stored energy. But the major drawback is the blocking voltage which leads to increased losses and can have a negative impact on the costs and the reliability.

This chapter introduces as a second original contribution, a new topology which is developed to try to solve the blocking voltage problem. As it is shown, the proposed topology is not able to offer a better result to the total blocking voltage issue, which is tied to physical limits. However, the CCCS topology contains many interesting and unique properties which are of a high technical interest.

It is a very modular solution and a new approach in the domain of multilevel conversion. A detailed analysis of the structure is proposed to show all of its properties.

3.2. General topology of the CCCS

3.2.1. Concept of the Common Cross Connected Stage

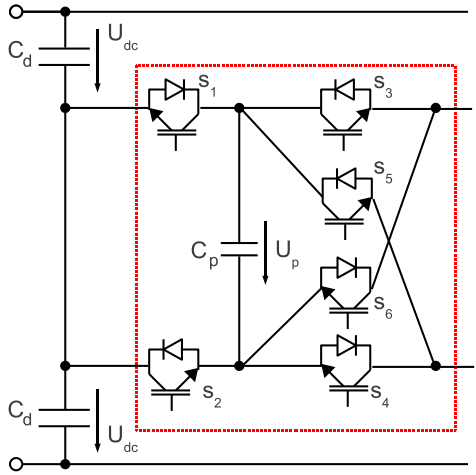


Figure 3.1.: *The Common Cross Connected Stages is connected to the DC-link on one side and to the 3 phases of the inverter on the other.*

The Common Cross Connected Stage (CCCS or C^3S), [42], is composed of 6 IGBTs and 1 capacitor, Figure 3.1. One of the main characteristic of the CCCS PEBB is that it is unique to the three phases of the inverter it is connected to, and allows to boost the number of levels produced. In general, this PEBB can be used on any kind of 3 phased multilevel topology based on a 3 level DC-link (2 capacitors in series).

One example of usage of the C^3S Power Electronic Building Block (PEBB) is connecting it to the 3L ANPC converter, Figure 3.2. The topology then offers 5L at the output with the following possible advantages compared to the 5L ANPC: The switching frequency of the PEBB and the IGBTs might be lower than the 5L ANPC solution and the number of individual components is reduced compared to the known solution, while offering the same amount of output levels. The drawback is the limited modulation index.

The example is not detailed further since the 3L ANPC is not the topology of interest.

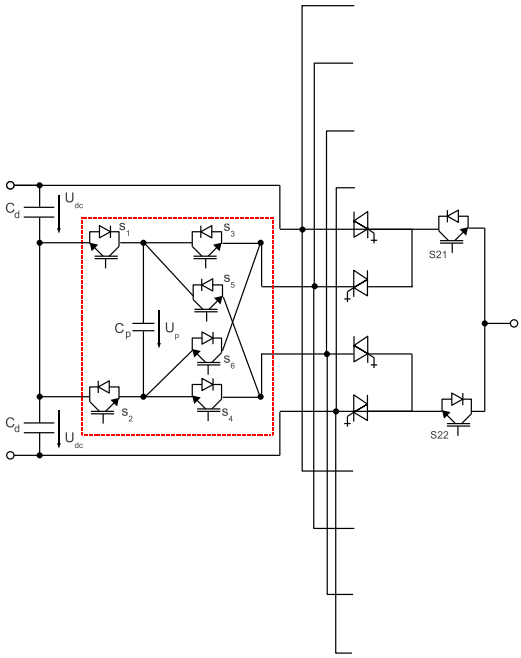


Figure 3.2.: *C^3S PEBB used on a 3 level ANPC inverter*

The CCCS's structure reminds the cross connected structure of the CCIL inverter §2, [27], with the differences that the CCCS is connected in the opposite way (the capacitor being before the cross connection) and, most notably, is common to all phases, and not a multiple of the number of phases, like in the CCIL topology, or any other standard multilevel topologies.

Another difference of the CCCS PEBB, in comparison to the CCIL topology, is that the blocking voltage of the switches of the PEBB are equal the capacitor voltage U_p. This voltage should not be larger then the phase capacitor voltages, as it is shown later, in order to be able to balance the capacitors at active power. Thus the blocking voltage requirements on the PEBB are low.

These characteristics make of the CCCS a cost efficient, modular and reliable improvement for various kind of multilevel topologies, and especially the ANPC topology, which is the topology of interest in this work.

3.2.2. The CCCS on the 5L 3 phase ANPC

Connecting the CCCS to the 5L ANPC converter, [3], yields a 7 or 9 uniform levels multilevel voltage source inverter. It is also possible to generate 11L with almost uniform steps as shown later in §3.3.3.

Whatever the number of levels generated (7, 9 or 11 in this case), the structure does not change, Figure 3.3. The criteria determining the number of levels is the voltage ratio between the DC-link, phase and PEBB capacitor voltages. Thus it is possible to generated various number of levels with an identical topology by changing only the voltages, in the same way as it can be done on standard topologies.

The capacitor balancing is one of the biggest challenge of the CCCS topology. Because of the intrinsic unsymmetrical nature of the PEBB connection-wise (is it connected only to the neutral point and not to the DC-link voltages), fully redundant CCCS topologies do not exist.

Since the PEBB is common to the three phases of the inverter, there is a cross influence between the balancing of the three phase capacitors and the PEBB capacitor. A per phase control is therefore not longer possible. But it is demonstrated that the balancing of all the capacitors of the topology is achievable, under certain conditions, with an appropriate common mode balancing scheme based on a phasor representation.

3.2.3. Cascading the CCCS

Similarly to the CCIL topology, the CCCS can be cascaded as many times as wanted to generate even more output levels. This can have an important influence on the blocking voltages of both, PEBB and phase switching devices, and should be studied case to case depending on the application.

The number of levels generated depends on the voltage ratios and many combinations can be chosen for the PEBB capacitor voltages, and the phase and DC-link voltages. These various combinations do not only lead to various number of levels, the uniformity of the output, the controllability of the converter's capacitors and the blocking voltage requirements of the switches change. For each set of voltage ratios, there is a particular repartition of the space phasors which characterizes the resulting inverter.

Another important aspect is the influence of the cascade on the switching states. Compared to the switching combinations proposed in the next chapters of this section, the cascaded structure has got more constraints, notably on the extended switching states (see §3.3.2).

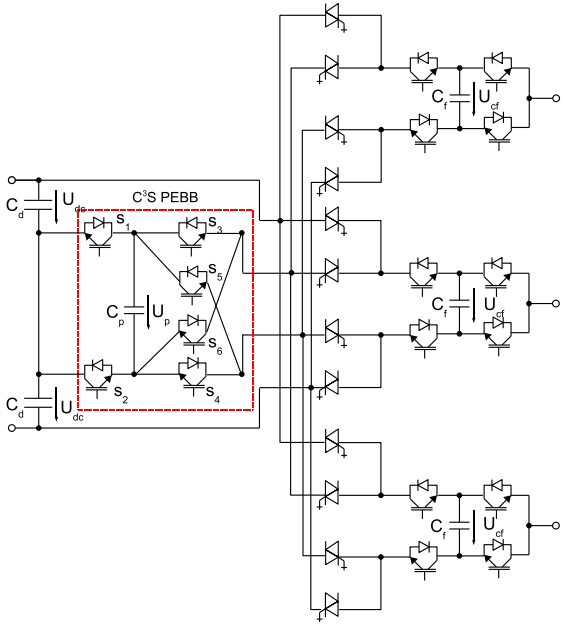


Figure 3.3.: *The CCCS PEBB connected to the 5L ANPC. The topology can generate 7 or 9 uniform output levels*

Figure 3.4 shows the topology of a 2 times cascaded structure. The resulting PEBB remains unique for the 3 phases. The requirement in term of components for the PEBB is 2 capacitors and 10 switches

3.2.4. The CCCS as a 2 level VSI

An alternate way to consider the CCCS topology is to consider it as a 2 level 3 phased voltage source inverter. One phase is connected to the DC-link while the 2 other phases are connected to the middle points of the 3 phase legs of the multilevel ANPC structure.

As such, this perspective opens up another range of possible generalization of the structure. Any kind of three phased 2 level inverter structure could then be considered to replace the CCCS. Similarly, any multilevel 3 phased inverter could also be considered instead of the CCCS PEBB. This would allow to increase further the number of levels generated by the structure, and as such, can be considered as another possible alternative (to the

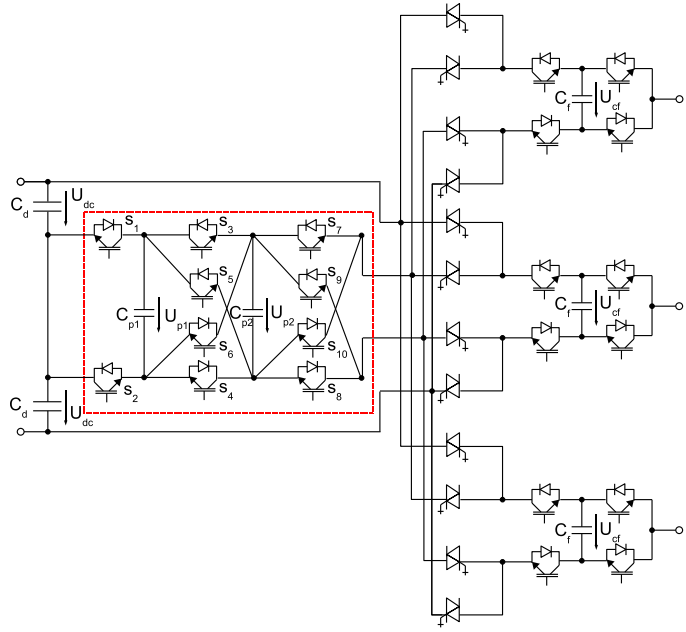


Figure 3.4.: *Cascaded multilevel C^3S topology. The PEBB can be cascaded to generate increased number of output levels*

cascading of the CCCS) to increase the number of levels produced by the structure.

This could be considered as a hybrid common stage approach. It opens up a new horizons to the Common Cross Connected Stage approach proposed here, but is out of the scope of this work. It certainly deserves some further study.

3.2.5. Electrical characteristics

Blocking requirements

Connecting the PEBB, which has got a low blocking voltage requirement to the 5L ANPC converter allows to generate a large number of output levels. But this does not come without a price: some switches within the ANPC part of the topology need to block higher voltages than in the typical 5L case.

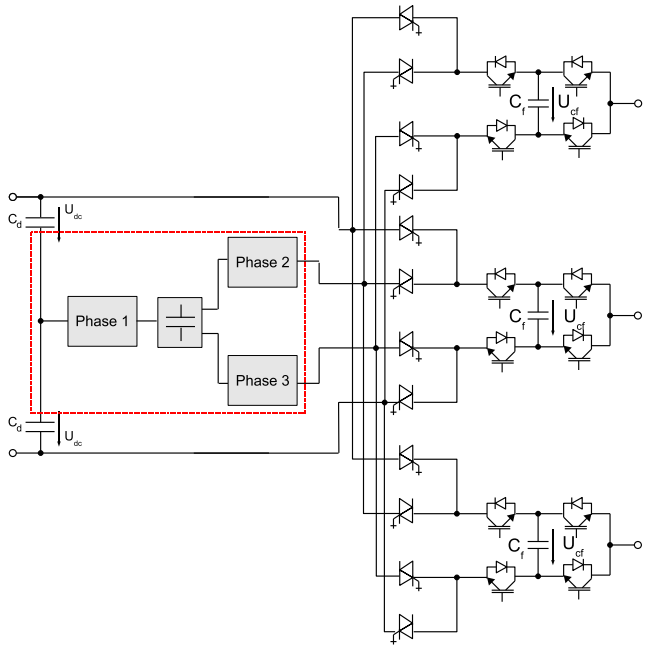


Figure 3.5.: *Generalization of the CCCS to a 2L VSI structure*

All three phases need to be considered when analyzing the blocking characteristics of the switches. The uniqueness of the PEBB implies that all the three phases influence the PEBB simultaneously and in different ways. The currents of the three phases are represented by different colors in a single phase schematic to simplify the representation (Figure 3.6).

Because the PEBB capacitor voltage is connected to the neutral point, the required blocking voltages on the devices $S_1 \dots S_6$ are equal to the C_p capacitor voltage. This can be understood as the connection to the neutral point is always done via S_1 or S_2, and that therefore the voltage U_p can be added or subtracted to that point only.

On the other hand, the IGCT S_{31} in the green phase has to block $U_{DC} + U_p$, because the voltage potential of the neutral point is brought down by the PEBB capacitor voltage. The same happens in the red phase, on the lower IGCT S_{34}. In the blue phase, the PEBB is not used. However, the voltage level on the negative pole of the phase capacitor equals $U_{DC} - U_{cf}$ while the voltage of the neutral point is lower by U_p. The IGCT S_{33} cannot

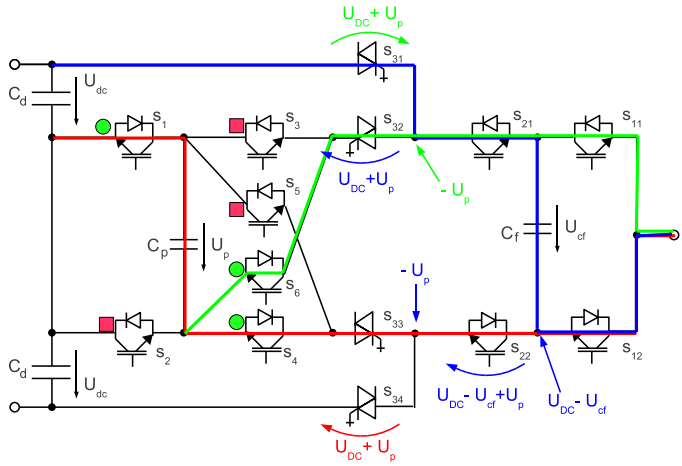


Figure 3.6.: *Blocking voltages requirements for various switching states.*

be used to contribute in the blocking voltage because of it's reverse diode, so the IGBT S_{22} has to block the extra voltage U_p. Of course the same occurs for the other switches not considered in this example. Overall, the blocking voltages of the switches S_{21}, S_{22}, S_{31}, S_{32}, S_{33} and S_{34} have to be increased by U_p. Since the voltage U_p is smaller than U_{DC} and U_{cf}, the increase in the blocking voltages is not dramatic, but still needs to be assessed.

Although the PEBB switches remain typically small, the total blocking voltage of the inverter is still increased. The formal calculation of total blocking voltage, as well as comparison to other topologies, are the object of §3.6.1. As a formatter, it can already be said that the same trend as seen previously with the CCIL occurs here: when passive components are reduced and levels increased, extra blocking voltage is required compared to equivalent topologies with more passives. This results from a physical constraint.

The blocking voltage characteristic of the switches can also depend on the PEBB capacitor supply strategy. This point is addressed separately later in §3.3.5.

Non-symmetrical stray inductances

From the point of view of the implementation, the CCCS PEBB is connected in common to the three phases of the inverter. Therefore, and because in general the three phases are built in parallel, it is likely that the connection line/bus bar from the PEBB to the three phases will be of a different mechanical length.

It results that the stray inductances are not the same from the PEBB to the three phases, and that the rise and fall times are likely to be different from one phase to another. To avoid any problems, it is necessary to make sure that, either the rise times are the same on all the phases, by some sort of mechanical design optimization, or that the rise time is forced to be at least equal to the largest rise time induced by the largest stray inductance (by tuning of gate resistor for instance).

3.3. Characterization of the CCCS VSI

3.3.1. Understanding the PEBB

This first part is intended to give a first physical approach to the functionality of the PEBB and helps to understand the next sections. Then the PEBB switching states section (§3.3.2) presents all the possible combinations of PEBB and phase switching states, and the corresponding output levels. A phasor graphical model (§3.3.3) is then developed, which is later used for the design of the modulator. And finally some general characterizing equations (§3.3.4) are derived and presented for some configurations of the C^3S inverter.

The CCCS capacitor modifies the neutral point voltage of the ANPC in a certain way. This modification influences all the levels that are produced using the neutral point, while the other levels (lower and upper DC-link and their combination with the phase capacitors) are not influenced.

This means that whatever the CCCS switching state is, some levels are never influenced. For all the other levels, the influence depends on the considered phase switching state and how the C^3S PEBB switching state allows to use the capacitor (sign of the contribution).

In addition to this specific behavior of the PEBB, the balancing of all the capacitors within the topology has do be addressed. This is done with the help of the phasor model, but first, the switching states have to be defined.

3.3.2. PEBB switching states

Normal PEBB switching states

There are 6 states the PEBB can take. Each of these states are referred to as PEBB 1 to PEBB 6. They consist in turning on one of the switches connected to the neutral point, and of one of the switches connecting to the input of the ANPC topology. With this strategy only two switches in the PEBB are turned on simultaneously. All possible states are presented on Figure 3.7.

For each CCCS switching state, 6 levels can be produced in combination with the 5L ANPC phase legs. 4 are common to all PEBB states, as the generation of those levels does not require the CCCS (seen on the upper part of the table, Figure 3.7). The other levels depend on the PEBB's switching state. All the levels produced are function of the chosen voltage ratios for the DC-link, the phase and the PEBB capacitors.

The necessary condition for the PEBB capacitor to be balanced is that it's voltage has to be smaller than the voltage of the phase capacitor: $U_p \leq U_{cf}$. When this is verified, the direction of the current across the PEBB is favorable for charging the capacitor, at the PEBB states 3 and 4, phase state 5, while discharging it in the other states (with a $\cos\varphi = 1$), as shown in the table of Figure 3.7.

An example of all the switching states for one given PEBB state is illustrated on Figure 3.8.

In a general consideration, any voltage ratios can be chosen for the capacitor voltages. Because of the interdependence between each phase leg switching state and the PEBB switching state, the uniformity region[1] of a 3 phased system cannot be defined arithmetically for the general case. The phasor representation can however be used to define the uniformity discs for specific cases (according to the definition given in [21]).

There is still a couple of possible choices of the capacitor voltage ratios fulfilling the uniformity step condition. The criteria is that all space phasors must be reachable by at least one combination of switching states. The following Table 3.1 gives the relationship between the the voltage ratios and the number of levels generated.

Notations The capacitor voltage ratios are written as $[U_{DC}; U_{cf}; U_p]$. For instance, [4;2;1] means that the voltage ratio of the DC-link is 4 times the voltage of the PEBB capacitor, and that the phase capacitor is double the PEBB capacitor voltage.

[1] The uniformity region, as defined in [21], corresponds to a specific region in the complex area representing the phasors which can be used to generate an uniform output voltage step

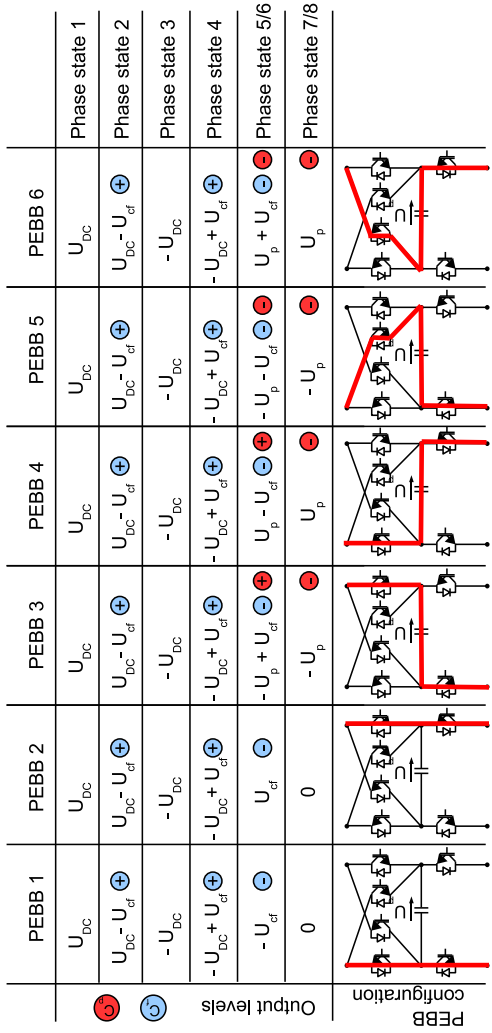


Figure 3.7.: *The 6 normal PEBB switching states and the output levels. Effects on the capacitors (⊕ charging and ⊖ discharging) are given for* $\cos\varphi = 1$.

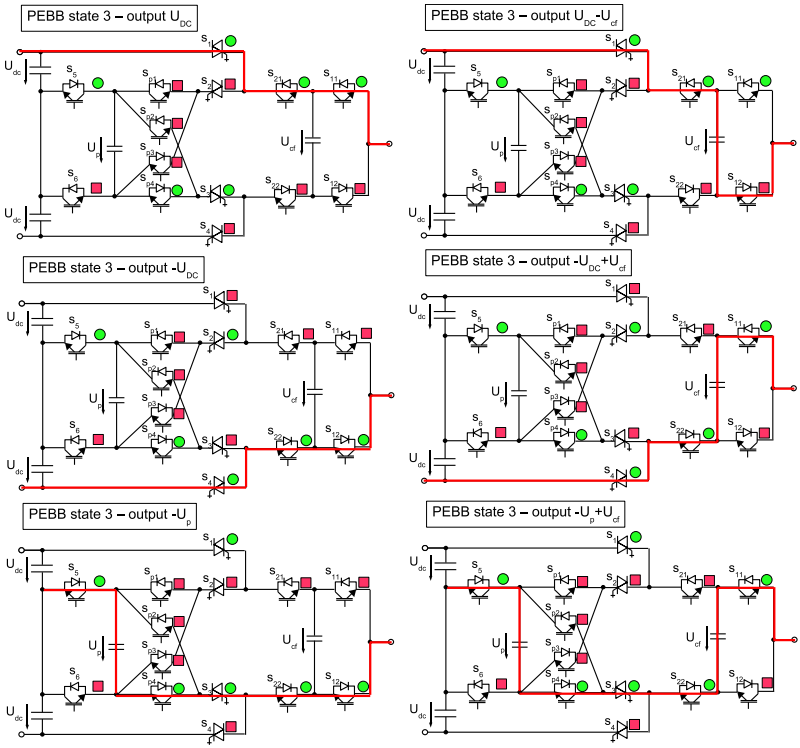


Figure 3.8.: *All the phase switching states for the PEBB switching state 3. Green circle means on, the red square means off.*

Output levels	***Combinations of voltages -*** $[U_{DC}; U_{cf}; U_p]$
7L (uniform output step)	$[3;1;1]$, $[3;2;1]$
9L (uniform output step)	$[4;2;1]$, $[4;3;1]$, $[3;2;2]$
11L (non-uniform output step)	$[5;3;1]$, $[4;3;2]$

Table 3.1.: *Some voltage combinations and the corresponding number of output levels.*

Each PEBB state offers $n_{phasors}$ space phasors, which result from all the combinations of 3 different voltages on each phase plus all combinations of 2 identical voltages and a third one, and plus the combination of all identical voltages on the three phases. Thus:

$$n_{ph} = \quad A_6^3 + 3 \cdot A_6^2 + A_6^1 \quad = 216 \tag{3.1}$$

Since there are 6 PEBB states, there is a total of $6 \cdot n_{ph} = 1296$ space phasors.

From this total number, there are n_{red} redundant space phasors among the PEBB states 1 and 2, 3 and 5, and 4 and 6, due each time to 5 identical voltages in each, such that:

$$n_{red} = \quad A_5^3 + 3 \cdot A_5^2 + A_5^1 \quad = 125 \tag{3.2}$$

Therefore, there are n_Δ different states for each PEBB states 1 to 6:

$$n_\Delta = \quad n_{ph} - n_{red} \quad = 91 \tag{3.3}$$

Thus overall, there are $n_{ph_{tot}}$ total different space phasor which can be generated by this configuration:

$$n_{ph_{tot}} = \quad 6 \cdot n_\Delta + n_{red} \quad = 671 \tag{3.4}$$

This amount is to be compared to the phasors usually generated by traditional inverters. They rank as n^3, with n the number of output levels. Table 3.2 gives the total phasors of classic inverters compared to the total phasors of CCCS topology.

Output levels	***Total states***
Classic 7L	$7^3 = 343$
Classic 9L	$9^3 = 729$
Classic 11L	$11^3 = 1331$
CCCS - 1 stage	671

Table 3.2.: *Total number of states in classical topologies compared to the C^3S topology*

Extended PEBB switching states

A very interesting property of the C^3S PEBB is the possibility to simultaneously turn on more than 2 switches at a time. This is because there are 3 commutation cells within the PEBB. This property allows more levels to be generated with the same PEBB switching state.

An example is given on Figure 3.9, where the blue and red currents are flowing through the CCCS PEBB and then branch out in different phases of the cascaded part of the inverter, although they are drawn on a single phase diagram for reasons of simplified representation. The switches S_5 and S_6 can be turned on at the same time without leading to a short circuit. Similarly the switches S_3 and S_4, S_3 and S_5, and S_4 and S_6 can also be turned on simultaneously, considering that the output phases are not creating short-circuits.

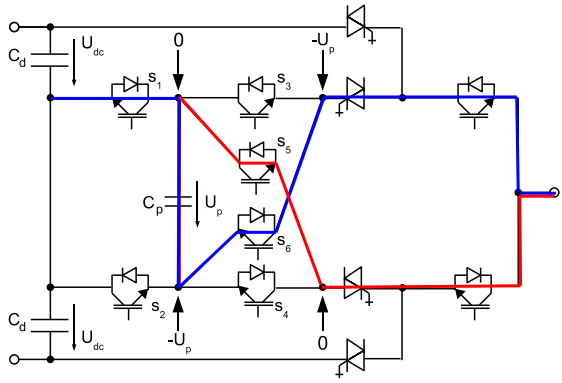


Figure 3.9.: *Simultaneous turn on of several switches of the PEBB. The blue and red paths are flowing across the PEBB and then in different phases.*

There are 8 extended PEBB states referred to as PEBB a to g. The state a can be generated by two different PEBB switching states (which can be used for loss balancing for instance). The different extended PEBB states are shown on the table on Figure 3.10.

The extended PEBB switching states a to e allow more phasors to be generated because the combination of phase states and PEBB states offer now 7 to 8 different levels, instead of the 6 previously obtained. The calculation is done as following:

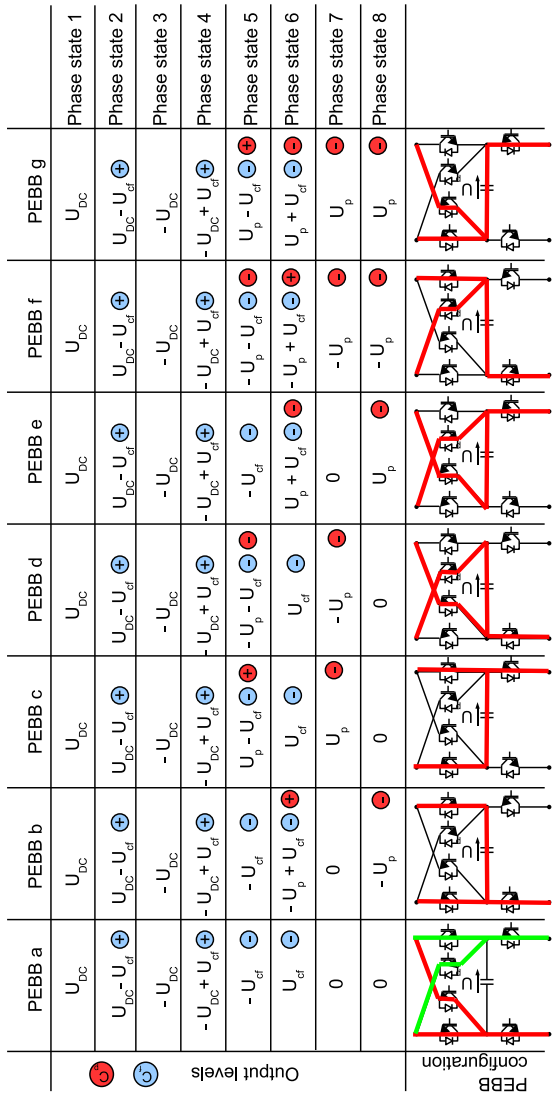


Figure 3.10.: *Extended PEBB switching states and the output levels. Effects on the capacitors (⊕ charging and ⊖ discharging) are given for* $\cos\varphi = 1$.

The total amount of phasors generated by the state a is n_{ph_a}:

$$n_{ph_a} = A_7^3 + 3 \cdot A_7^2 + A_7^1 = 343 \tag{3.5}$$

All PEBB states b to g can generated n_{ph} space phasors, with:

$$n_{ph} = A_8^3 + 3 \cdot A_8^2 + A_8^1 = 512 \tag{3.6}$$

State b can generate n_{ph_b} phasors, which results from n_{ph} total phasors among which n_{red_a} have already been counted in state a. And the same applies for the state c. Thus:

$$n_{red_a} = A_6^3 + 3 \cdot A_6^2 + A_6^1 = 216 \tag{3.7}$$

$$n_{ph_b} = n_{ph} - n_{red_a} = 296 \tag{3.8}$$

$$n_{ph_c} = n_{ph} - n_{red_a} = 296 \tag{3.9}$$

For states d and e can generate respectively n_{ph_d} and n_{ph_e}, which results from n_{ph} total phasors among which $n_{red_{abc}}$ have already been counted in the PEBB states a,b and c:

$$n_{red_{abc}} = A_7^3 + 3 \cdot A_7^2 + A_7^1 = 343 \tag{3.10}$$

$$n_{ph_d} = n_{ph} - n_{red_{abc}} = 169 \tag{3.11}$$

$$n_{ph_e} = n_{ph} - n_{red_{abc}} = 169 \tag{3.12}$$

Finally states f and g, there are 6 possible combinations with each 5 permutations not previously counted, so:

$$n_{ph_f} = 5 \cdot 6 = 30 \tag{3.13}$$

$$n_{ph_g} = 5 \cdot 6 = 30 \tag{3.14}$$

So finally, the total amount of phasors that can be generated, $n_{ph_{tot}}$, is:

$$n_{ph_{tot}} = n_{ph_a} + n_{ph_b} + ... + n_{ph_g} = 1333 \tag{3.15}$$

The total phasors generated by the normal and extended PEBB states, and compared to "standard" multilevel topologies, is presented in the following Table 3.3.

The very high number of phasors generated by the PEBB shows how the C^3S configuration is able to generate so many output levels, even though its structure is relatively simple. Being able to generate many different levels with the same PEBB switching state is the key point to be able to cover the whole space phasor plan, and thus obtain uniform output step inverters.

As it is shown with the phasor model, the extended C^3S switching states allow to generate an uniform 9L output whereas with non extended switching states, only 7L uniform output steps are obtained.

Output levels	*Total states*
Classic 7L	$7^3 = 343$
Classic 9L	$9^3 = 729$
Classic 11L	$11^3 = 1331$
CCCS - 1 stage	671
CCCS - 1 stage with extended switching states	1333

Table 3.3.: *Total number of states in classical topologies compared to the C^3S topology*

3.3.3. Phasor model

General considerations

Throughout this section, a single stage C^3S is studied (Figure 3.3). As shown in the previous section, in a single phase circuit there exist combinations of PEBB and phase switching states which result in various combinations of positive, negative or null currents within the PEBB capacitor C_p and the phase capacitor C_f (Figures 3.7 and 3.10).

In a three phased system, the total combinations of positive, negative and null current in the PEBB and in the three phase capacitors is even higher, as all the possible space phasors potentially lead to a different combination. Being able to model and understand what is the repartition of the charging and discharging phasors for a complete inverter is crucial for modulation and balancing strategies.

Additionally, it is necessary to know what voltage ratios lead to full or partial uniformity regions.

To answer these questions, a graphical phasor model is proposed. It is based on a representation of all the generated phasors and their contributions to the charge of the PEBB and phase capacitors. Different voltage ratios and PEBB switching states (standard or extended) are represented to illustrate the different results that can be obtained.

7, 9 and 11 output levels are studied with only a part of the possible voltage ratios which can be used to generate these levels (Table 3.1). In the case of an application, the choice of a specific voltage ratio and number of output level must consider these 3 main constraints: blocking voltages, ability to balance the capacitors and uniformity region.

In the figures, the circles of different colors and sizes represent the different PEBB switching states. The contribution to the load of the phase

capacitors can be either positive, negative or null and is represented by three colors..

The contribution to the PEBB is more complicated, since 1, 2 or the 3 phases can impose a current through the PEBB, and of these currents, some will or not flow through the PEBB capacitor (in extended PEBB switching state mode). Therefore, the contribution on the PEBB capacitor is marked as a 1,2 or 3 phases, positive or negative contribution. However, it is important to understand that the amplitude of each individual currents will play a role on the final sign of the current through the PEBB (i.e. 1 positive and 1 negative current flowing through the PEBB capacitor does not mean that the contribution is null, it depends on the respective amplitudes). This aspect is treated separately, during the development of the modulation algorithm. For this part, it is assumed that 1 positive and 1 negative current leads to a 0 contribution.

Similarly to the CCIL and any other phase capacitor based multilevel inverter, it is clear that the power factor also has an influence on the charging and discharging states. In this case, the figures are plotted for a power factor $\cos\varphi = 1$.

7 level

Standard PEBB switching strategy - Voltage ratio [3;2;1] The 7L [3;2;1] CCCS VSI can generated all the space phasors, thus producing uniform output steps, Figure 3.11-top.

It can be seen that there is redundancy on the outer phasors, which is unusual. For the C^3S topologies however, this is typical. The redundancies are actually coming from the multiple PEBB switching states which do not influence the levels generated by combinations of voltages using the upper and lower DC-link voltages. So those redundancies do not concern capacitor balancing and in fact they have no influence on the current path.

But they are meaningful in the sense that depending on what levels are needed on the other phases, one or the other PEBB state is necessary and thus, the choice is already imposed by the other phases.

The 3 phase capacitors can be controlled more or less independently one from another, Figure 3.11-bottom. The regions were the phase capacitors are the best controllable are shifted by 120°, in particular the charging and zero action phasors. This implies that when controlling one capacitor some decoupling is likely to happen on the other capacitors, thus not disturbing them too much.

Extended PEBB switching strategy - Voltage ratio [3;2;1] With the extended PEBB switching states, Figure 3.12-top, the phasors also cover the

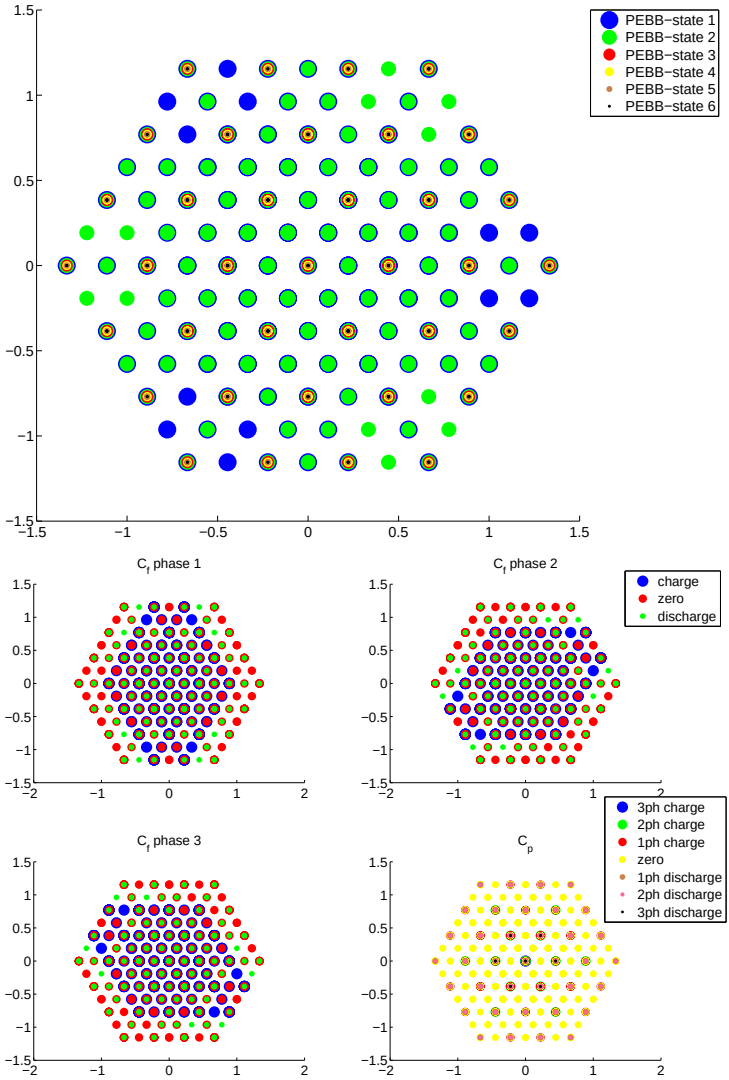


Figure 3.11.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors, for the 7L* $[3; 2; 1]$.

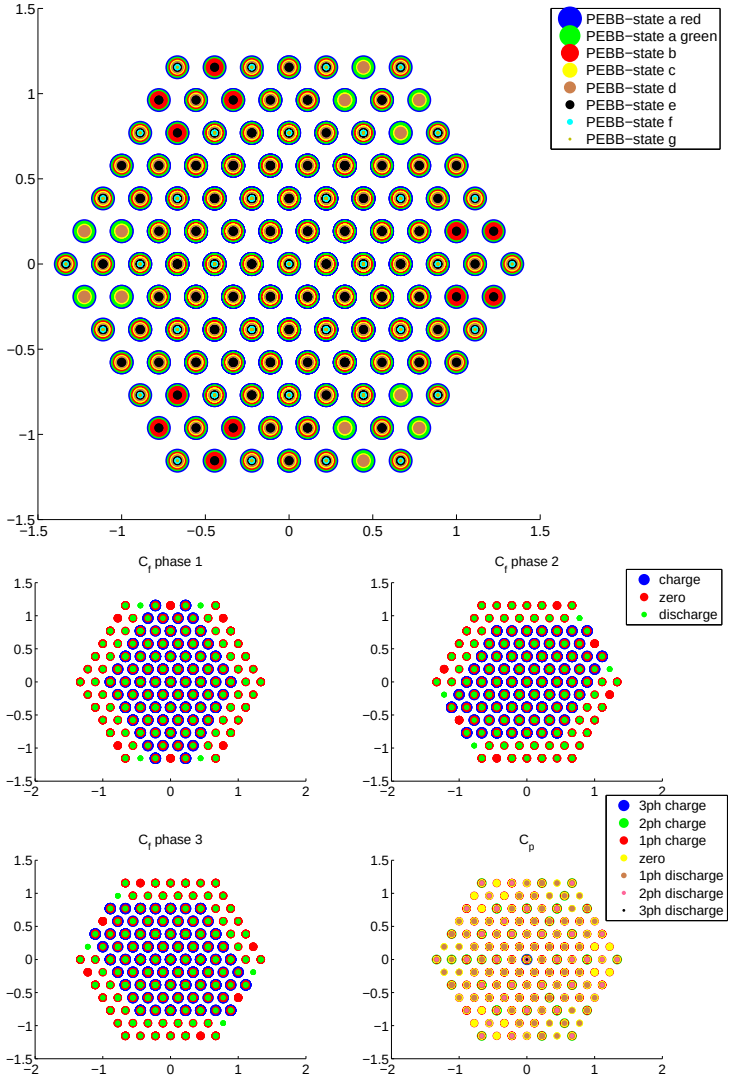


Figure 3.12.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors, for the 7L* $[3; 2; 1]$ *and extended PEBB switching states.*

full space phasor plan. The main difference is a higher redundancy level on each phasor. The repartition of the charging and discharging phasors is strictly identical between normal and extended strategy. It is understandable because the extended switching strategy does not modify the path of the current. It only helps to generate more levels simultaneously with the same PEBB state.

9 level

Standard PEBB switching strategy - Voltage ratio [4;2;1] For the 9L C^3S inverter with non-extended switching states, Figure 3.13-top, there are 12 missing positions in the space phasors plan. These result from the impossibility to impose simultaneously the levels 3 and 0, and the levels ± 3 and ± 1 in sign opposition, when using the standard PEBB switching states.

There is less redundancy at certain points compared to the 7L, which is a natural consequence of the fact that with more levels to be generated, more phasors are required, while the C^3S offers only a fixed number of phasors whatever the number of levels generated (i.e. the chosen voltage ratios).

However controlling the phase and PEBB capacitors still is possible in this case, Figure 3.13-bottom. Decoupling property in the control of the 3 phase capacitors is still present and a ripple of about 6 times the fundamental on the PEBB capacitor is likely to appear, from how the charging and discharging positions are spread out on the space phasor plan. This ripple is by the way observed later on in simulation.

Standard PEBB switching strategy - Voltage ratio [3;2;2] With this voltage ratio for the 9L, all the phasors can be generated, Figure 3.14-top. But, as suggested by the model, at full active power stabilizing the PEBB capacitor is only possible for low modulation indexes, Figure 3.14-bottom.

Additionally, from the analysis of the repartition of the phases, it is shown that only the PEBB states 5 and 6 allow reaching the outermost phasors. When these are used, the PEBB capacitor is only discharged. This further indicates that the topology cannot be stabilized under full active power for large modulation indexes.

From a physical point of view, the indication regarding the stabilization comes from the voltage levels. The subtraction of the PEBB voltage to the phase capacitor voltage, which corresponds to a PEBB capacitor recharging state, equals to 0. This means that for active power, the current amplitude at the PEBB charging state is very small, thus that the influence of the charging state is very small.

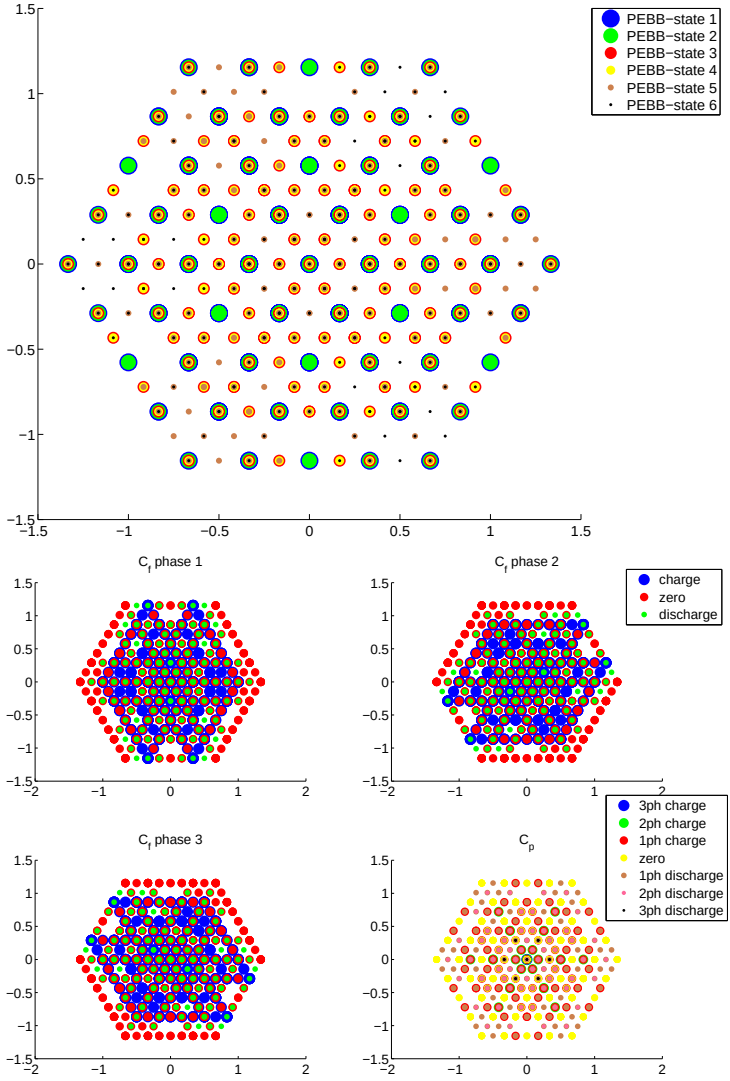


Figure 3.13.: *Top: Repartition of all phasors. Bottom: phase capacitors and the PEBB capacitor charging and discharging phasors, for the 9L* $[4; 2; 1]$.

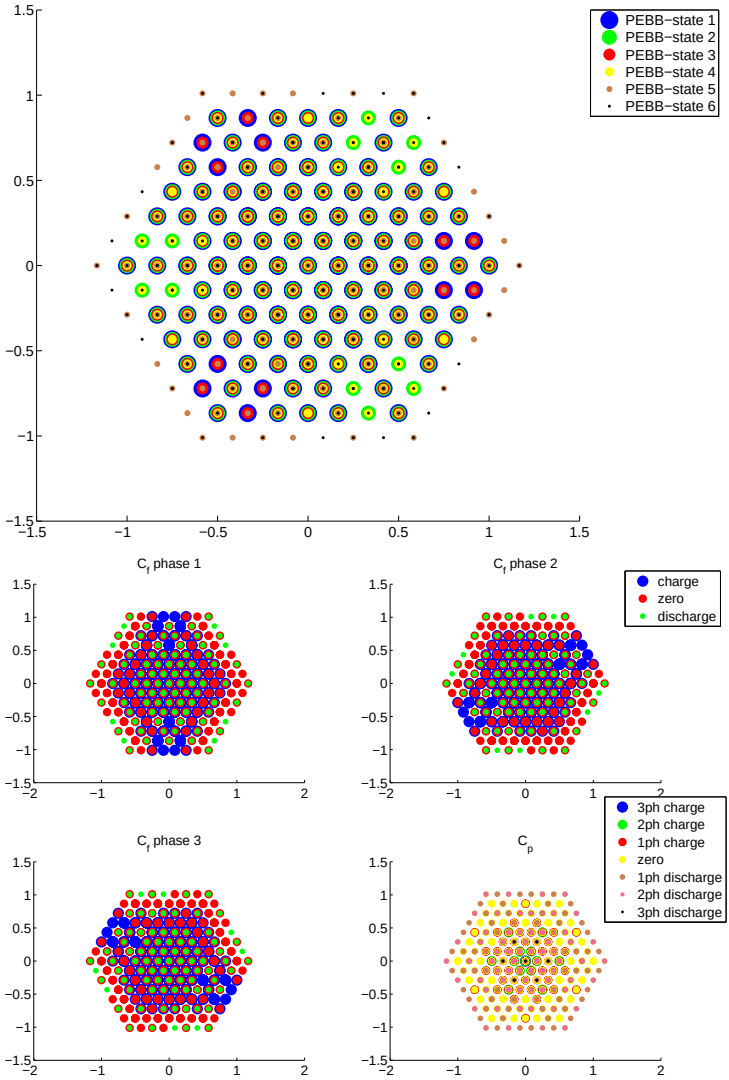


Figure 3.14.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors for the 9L* $[3;2;2]$*.)*

Extended PEBB switching strategy - Voltage ratio [4;2;1] 9L [4;2;1] with the extended PEBB switching states, Figure 3.15-top, can generate all the phasors. The extra redundancies introduced by the extended states allow to generate the previously missing phasors.

In this case as well, the balancing properties, Figure 3.15-bottom, remain identical to the normal switching state case. Therefore, this indicates that the capacitors are likely to be stabilized up to some extent at full active power.

This example illustrates well how the extended PEBB switching states are used to fill the previously missing gaps without requiring any hardware modifications (besides adapting the blocking voltages of the switches).

11 level

Standard PEBB switching strategy - Voltage ratio [5;3;1] For an 11L [5;3;1] C^3S inverter with a standard PEBB switching strategy, Figure 3.16-top, there are many missing positions. It can be understood easily why by comparing the number of generated vectors to those required for an 11L inverter (Table 3.3).

It is also interesting to notice that the repartition of the various capacitors charging and discharging positions remain approximately the same whatever the voltage ratios, Figure 3.16-bottom.

Extended PEBB switching strategy - Voltage ratio [5;3;1] With extended switching states, the 11L [5; 3; 1], Figure 3.17-top, still misses some phasors, although the extended switching strategy allows to fill many gaps. The missing phasors being on the one but last hexagon, they are in the region where the modulation would typically take place, when considering a certain margin, leading to a likely not usable solution.

This means that 11L can be generated at the output, but at some point in time, there are missing steps. This results in a non-uniform output step converter. This choice is interesting from the point of view of the blocking voltages. Because the PEBB capacitor is only 20% of the DC-link voltage and 33% of the phase capacitor voltage, the increase in the blocking voltage of the ANPC part is small.

Extended PEBB switching strategy - Voltage ratio [4;3;2] In the case of the 11L [4;3;2] with extended switching states, Figure 3.18-top, unless maximum modulation index is necessary, all the phasors can be generated. However, the balancing of the capacitors in this inverter is very difficult at unitary power factor. The graphical model suggests, Figure 3.18-bottom,

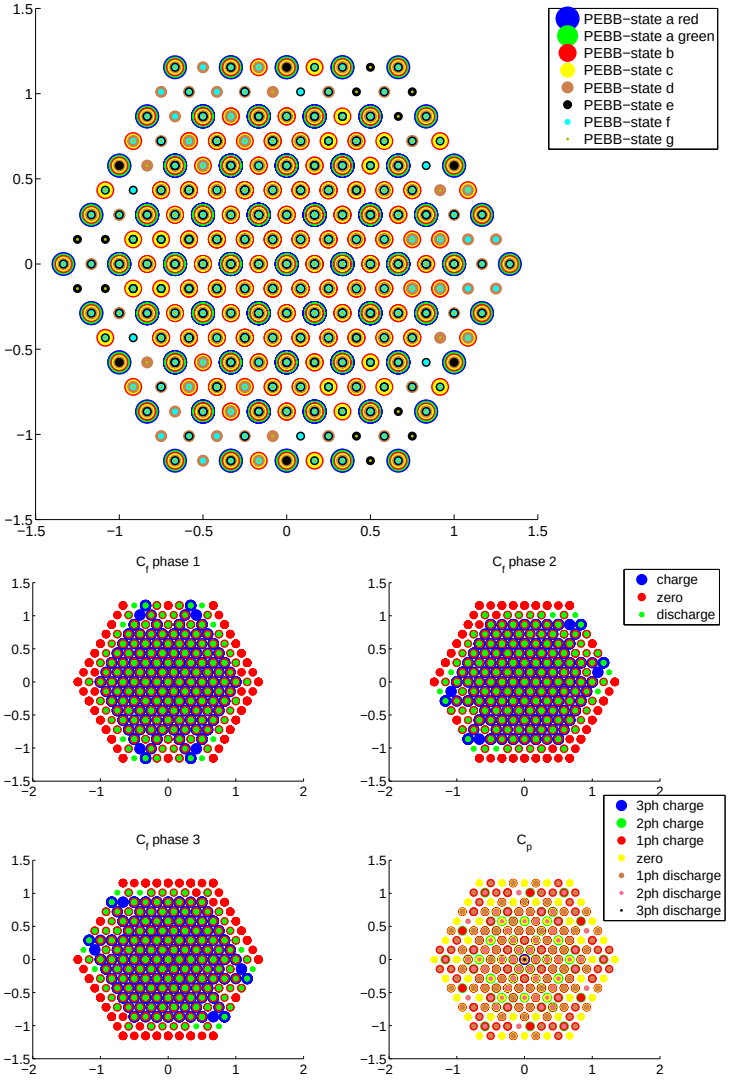


Figure 3.15.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors, for the 9L* $[4; 2; 1]$ *and extended PEBB switching states.*

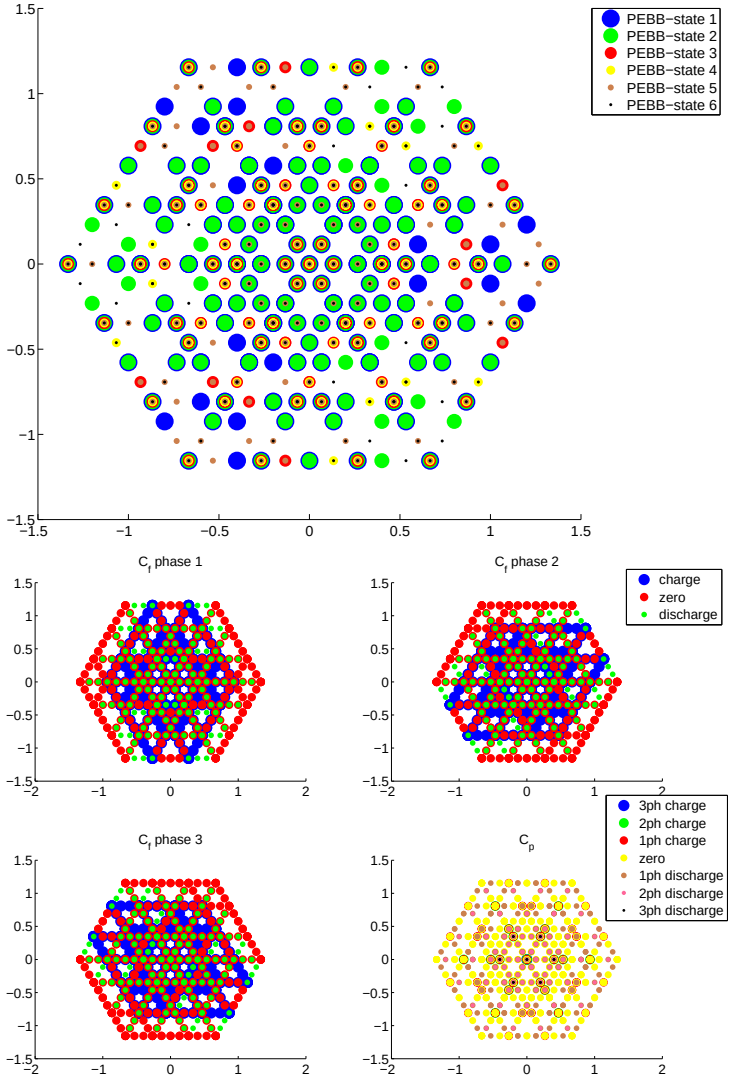


Figure 3.16.: *Up: Repartition of all phasors ; Down: phase and PEBB capacitors charging and discharging phasors, for the 11L with* $[5; 3; 1]$.

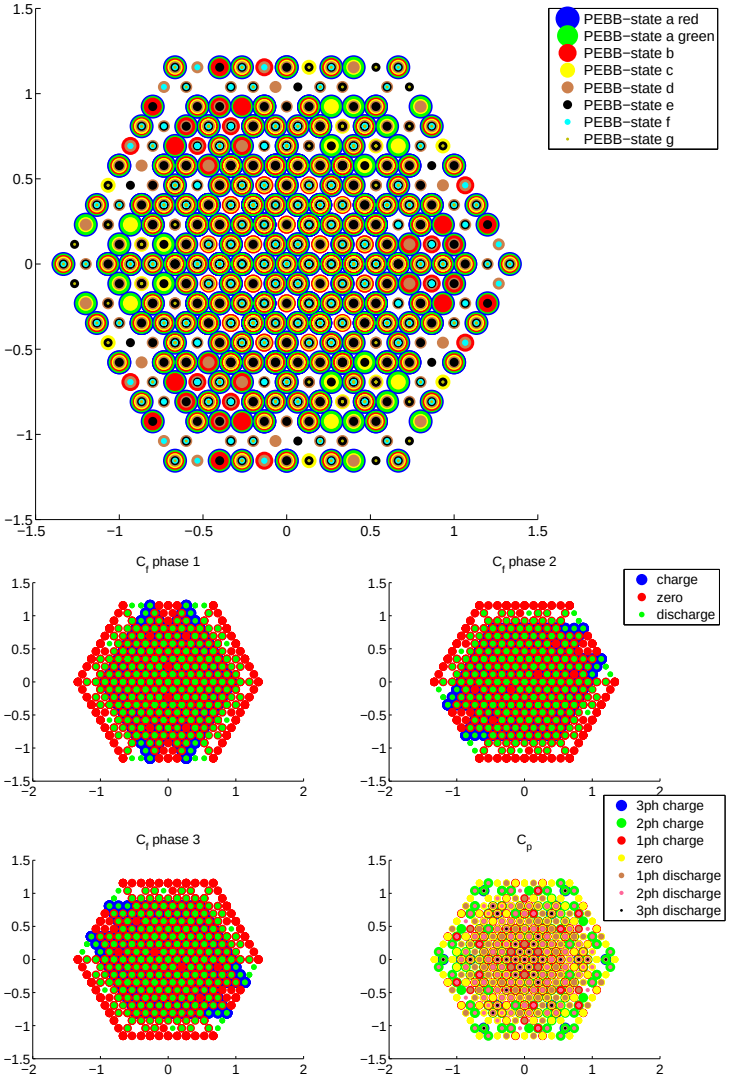


Figure 3.17.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors, for the 11L* $[5;3;1]$ *and extended PEBB switching states.*

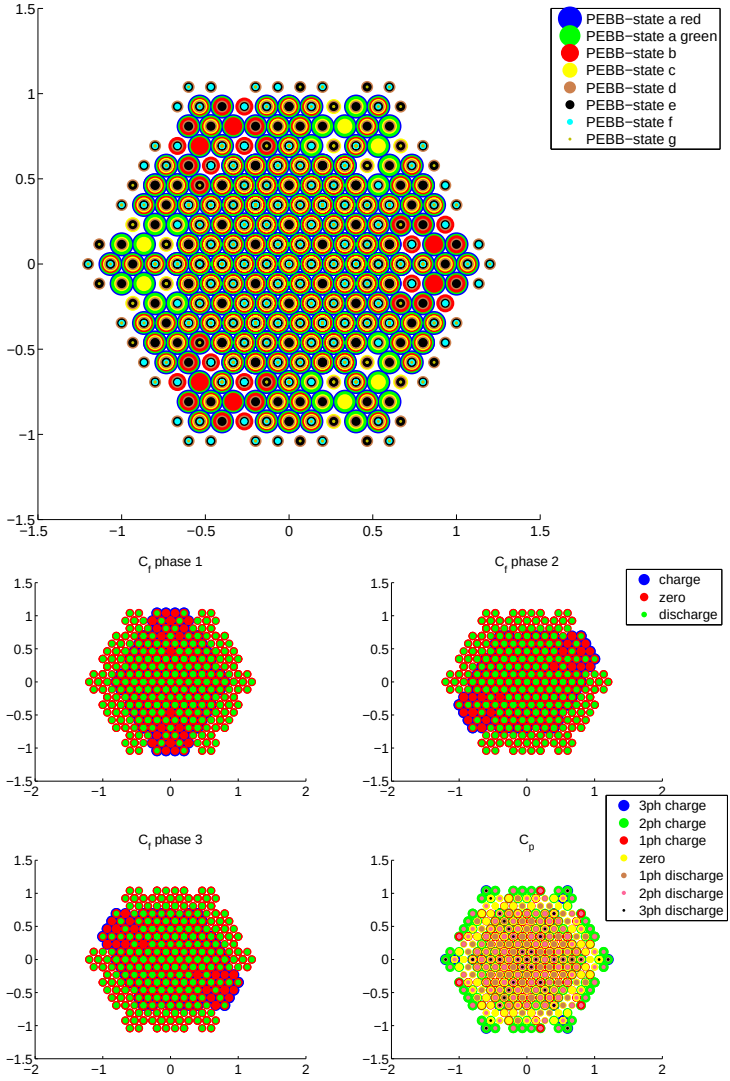


Figure 3.18.: *Top: Repartition of all phasors. Bottom: phase and PEBB capacitors charging and discharging phasors, for the 11L* $[4:3:2]$ *and extended PEBB switching states.*

that there are many positions where only discharging is possible, for phase and PEBB capacitors.

3.3.4. General equations

Because of the multiple combinations and possible voltage ratios (see Table 3.3), it is not possible to give a general equation to predict how many levels are generated per CCCS stage. Additionally, even if there exists many kind of combinations, it should not be forgotten that the main challenge is to balance the capacitors.

However, a general number of levels per stage can be given depending on the main characteristics drawn from Table 3.3. The 2 most interesting voltage ratio series are presented here and the general equations derived.

The first voltage ratio relationship:

$$[k+2; k+1; k; ...; 4; 3; 2; 1] \tag{3.16}$$

where

$$\begin{aligned} V_{Cp1} &= 1 \\ V_{Cp2} &= 2 \\ V_{Cpn} &= k \\ V_{Cf} &= k+1 \\ V_{Cdc} &= k+2 \end{aligned}$$

in which case the number of levels produced by a cascade of n CCCS stages is given by:

$$L(n) = 5 + 2 \cdot n \tag{3.17}$$

The number of individual switches (in average per phase) for n stages is given by:

$$T(n) = 8 + 2 \cdot n \tag{3.18}$$

The normalized (to half DC-link voltage) total blocking voltage for n stages is:

$$B(n) = 6 + 8 \cdot \sum_{k=3}^{n} \frac{1}{k} \tag{3.19}$$

The second voltage ratio relationship:

$$\left[2^{k+1}; 2^k; ...; 16; 8; 4; 2; 1\right] \tag{3.20}$$

where

$$\begin{aligned} V_{Cp1} &= 1 \\ V_{Cp2} &= 2 \\ V_{Cpn} &= 2^{k-1} \\ V_{Cf} &= 2^{k} \\ V_{Cdc} &= 2^{k+1} \end{aligned}$$

in which case the number of levels produced by a cascade of n CCCS stages is given by:

$$L(n) = 5 + 2^{n+1} \tag{3.21}$$

The number of individual switches (in average per phase) for n stages is given by:

$$T(n) = 8 + 2 \cdot n \tag{3.22}$$

The normalized (to half DC-link voltage) total blocking voltage for n stages is:

$$B(n) = 6 + 8 \cdot \sum_{k=3}^{n} \frac{1}{2^k} \tag{3.23}$$

For the 2 voltage ratio series presented here, uniformity can be achieved for any modulation index. But, as it is shown later, because the maximum modulation index at full active power is limited because of capacitor stabilization constraints, it could be interesting to consider topologies with restricted uniformity discs. These are however not discussed here.

It must also be noted that there is no guarantee that the capacitors can be stabilized for n cascaded stages of the CCCS. A case to case study is necessary and the appropriate choice of voltages for the capacitors has to be found, if possible.

3.3.5. Supply of the PEBB capacitor

The problem of the energy in the PEBB capacitor

Analyzing the previous phasor diagrams shows that for many voltage ratios it is difficult to balance the CCCS and/or the phase capacitors.

The tables in Figures 3.7 and 3.10 indicate what is the influence of given levels to the charge of the capacitors. Graphical representation of the same information in temporal form, Figure 3.19, helps to clearly noticed how the power factor influences the charging and discharging states (amplitude and sign).

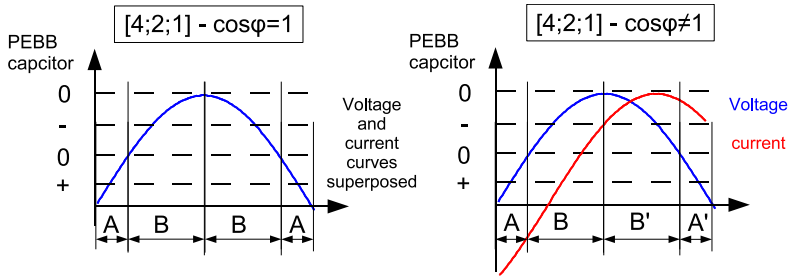


Figure 3.19.: *Influence of the phase of the current on the charge of the capacitor.*

Figure 3.19-left: The capacitor is charged roughly during the time A with the corresponding amplitude shown by the blue curve (where the blue curve is the voltage, but the current is supposed in phase). It is then discharged approximately during the time B and with the corresponding amplitude of the blue curve. On average the energy supplied by the PEBB capacitor to the system is therefore not equal to zero.

Figure 3.19-right: The current and voltage are phase shifted. During time A, the capacitor is discharged with a 0.5 current amplitude (red curve). During B, the capacitor is first charged with a low current, then discharged with a medium amplitude current. During B', the capacitor is discharged with a strong amplitude and finally during A', the capacitor is charged with a strong amplitude.

Therefore, limited modulation index (for common mode stabilization) and/or a partly reactive load help to stabilize the PEBB capacitor voltage. This result is therefore completely similar to the CCIL non redundant phase capacitor multilevel inverter topologies.

Investigating whether it is possible to find a voltage ratio combination, such that the PEBB charging and discharging levels be similar thus allowing to balance the PEBB, is of notable interest. Another idea would be, since the PEBB voltage is relatively low, to supply it by some external circuit.

These off-line optimization issues are addressed in the following subsections.

Adequate choice of the capacitor voltages

Preliminary considerations Several voltage combinations can be used to produce different number of levels (Table 3.1). The possible phasors for some of the proposed combinations are illustrated in the §3.3.3, and show

that the repartition of the charging and discharging phasors for the phase and the PEBB capacitors is somehow similar whatever the ratios.

But besides uniform output steps, different combinations might be considered. For instance a non-uniform output step converter with more steps at the maximums and minimums can be a good choice regarding harmonic distortions.

The choice of the voltage ratios can be motivated also by stabilization considerations. In this subsection the voltage ratios necessary for complete stabilization of the PEBB capacitor are calculated mathematically.

Tune the charging and discharging levels A strategy can be defined graphically based on Figure 3.19: if the discharging level is close to the charging one, then it can be expected that something similar to redundant states is obtained, and that therefore balancing is made easier.

Translated into mathematical terms and with the circuit constraints, the previous condition becomes, referring to the voltage combinations found in the table of Figure 3.10:

$$\begin{aligned} -U_p + U_{cf} + \Delta U &= U_p + U_{cf} \\ \Delta U &= 2U_p \end{aligned} \tag{3.24}$$

The equation (3.24) gives the distance between the levels charging ($-U_p + U_{cf}$) and discharging ($U_p + U_{cf}$) the PEBB capacitor.

From that equation ((3.24)), and in order to make the distance minimal, the basic step is defined as $2U_p$. This leads to the following:

$$\begin{aligned} U_{DC} - U_{cf} &= 2U_p \\ U_{cf} - U_p &= 2U_p \end{aligned} \tag{3.25}$$

and so:

$$\begin{aligned} U_{cf} &= 3U_p \\ U_{DC} &= 5U_p \end{aligned} \tag{3.26}$$

The result of the equation (3.26) is precisely what is set for the 11L $[5; 3; 1]$ inverter, but with the steps size equal to $2U_p$ (i.e. skip one level out of 2). Imposing condition ((3.24)) leads to a 6L converter. It implies loss in resolution and an non-optimal use of the capacitors. The minimum step being $\Delta U = 2U_p$, the distance is relatively large and thus, the balancing is not made much easier.

Skip the strongly discharging level Another solution can be to skip the level which contributes to the strong discharge of the PEBB capacitor. This solution is based on the statement that: the number of levels offered by the topology is high enough to allow skipping some of them.

Skipping the strongly discharging levels means skipping the level situated on the upper side (in absolute value) of the signal (states f and g, Figure 3.10), precisely where it would be nice to have a higher resolution. This level should therefore be replaced by another level, before being suppressed.

$$\begin{aligned} U_{DC} - U_{cf} &= U_p + U_{cf} \\ U_{cf} &= \frac{U_{DC} - U_p}{2} \end{aligned} \tag{3.27}$$

From §3.3.2 the two following relationships are determined:

$$U_{cf} > U_p \tag{3.28}$$

$$U_{DC} > U_{cf} \tag{3.29}$$

By replacing (3.28) in (3.27) the flowing relationship is written:

$$\begin{aligned} U_{cf} &> \frac{U_{DC} - U_{cf}}{2} \\ U_{cf} &> \frac{U_{DC}}{3} \end{aligned} \tag{3.30}$$

Using the equation (3.29) a constraint can be given on the phase capacitor voltage:

$$\frac{U_{DC}}{3} < U_{cf} < U_{DC} \tag{3.31}$$

Finally, using (3.28) in (3.31) the result is:

$$\begin{aligned} \frac{U_{DC}}{3} < U_p &< U_{cf} < U_{DC} \\ 1 < U_p &< U_{cf} < 3 \end{aligned} \tag{3.32}$$

For instance, if $U_p = 1.5$ and $U_{cf} = 2.5$ the fraction $[6; 5; 3]$ is obtained. This results in a non-uniform output step inverter. The levels are:

$$\begin{aligned} U_{DC} &= 6 \\ U_{DC} - U_{cf} &= 1 \\ U_{cf} &= 5 \\ -U_p + U_{cf} &= 2 \\ U_p + U_{cf} &= 8 \\ U_p &= 3 \\ &0 \end{aligned}$$

The level 8 is the skipped level. The levels 2 and 3, respectively $-U_p+U_{cf}$ and U_p, which charge and discharge the PEBB capacitor are subsequent, which has a positive effect on the PEBB capacitor balancing. On the other hand, the levels 5 and 1, respectively $U_{DC}-U_{cf}$ and U_{cf} are really far from each other. These levels are used to balance the phase capacitors.

While the PEBB capacitor charging and discharging levels are tuned, control over the phase capacitors is lost. The non-uniform levels [6; 5; 3; 2; 1; 0] is realistic for an inverter as the missing level 4 is not much used when the modulation index is relatively high. Unfortunately this solution cannot be retained as control of the phase capacitors is lost.

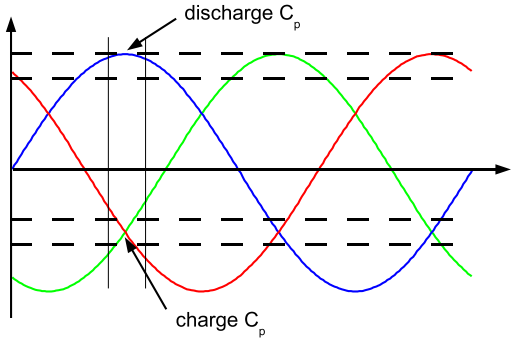


Figure 3.20.: *Using the 3 phase properties to try to compensate strong discharge of the PEBB capacitor.*

Using three phase properties The PEBB capacitor is connected to the three phases of the inverter, which are connected in a Wye configuration. In

this particular configuration, the neutral point is not connected. Therefore, $\sum_{n=1}^{3} i_n = 0$. This implies that while a strong positive current is flowing through one phase of the inverter, the sum of the currents in the two other phases is it's complement to 0, Figure 3.20.

This property can be used to try to tune the different levels by choosing the adequate ratios for the different capacitors, such that in the region where one phase would be strongly discharged the PEBB, the two other phases would contribute in a positive and complementary way. In mathematical terms, the statement that the most discharging level is situated on the end level is:

$$U_p + U_{cf} = N \quad ; \quad N \text{ is the amount of levels} \tag{3.33}$$

The region where it is possible to charge the PEBB capacitor has to be situated at half the full output voltage:

$$\begin{aligned} -U_p + U_{cf} &\geq \frac{U_p + U_{cf}}{2} \\ U_{cf} &\geq 3U_p \end{aligned} \tag{3.34}$$

Combining the equations (3.33) and(3.34) gives:

$$U_{cf} \geq \frac{3}{4}N \tag{3.35}$$

The phase capacitor relationship linking the charging and discharging states is:

$$\begin{aligned} U_{DC} - U_{cf} + \Delta U &= U_{cf} \\ U_{cf} &= \frac{U_{DC} + \Delta U}{2} \end{aligned} \tag{3.36}$$

From (3.36), if ΔU is too large, the levels are too far away from each other and the phase capacitors cannot be controlled. This is the pendant problem to the previous optimization.

An extra condition is given as:

$$U_{DC} \leq N \tag{3.37}$$

Replacing (3.37) in (3.36) results in:

$$U_{cf} \leq \frac{N + \Delta U}{2} \tag{3.38}$$

Equation (3.38) combined with (3.35) gives:

$$\frac{3}{4}N \leq \frac{N + \Delta U}{2}$$
$$\frac{1}{2}N \leq \Delta U \tag{3.39}$$

The final relationship (3.39) indicates that the difference between the levels charging and discharging the phase capacitor is maximum half of the full amount of levels. In other words, the discharging region is at much lower levels than the charging region, and once again, the balancing problem is shifted from the PEBB capacitor to the phase capacitors.

Conclusions No matter how the problem is formulated, the conclusion is always the same. It is not possible to find a voltage ratio such as to balance both, the PEBB and phase capacitors. This is due to physical limitation of the circuit where the contribution of the PEBB cannot be null under full active power with high modulation indexes, simply because the PEBB is connected only to the neutral point, and therefore cannot have any energy inflow from the upper or lower DC-rail.

This problem is similar to the multilevel NPC structures, where a reactive current or a reduced modulation index are necessary to keep the multiple "neutral points" balanced.

Solving the problem of the power supply for the PEBB capacitor has therefore to be done by some other means than simply choosing adequate voltage ratios.

Recharging PEBB commutation

About this strategy The energy needed for the PEBB capacitor can be found either in the DC-link or in the phase capacitors. Because the phase capacitors are far away from the PEBB, and because they are floating, it is not realistic to try to exchange energy between these two capacitors.

Connecting the PEBB capacitor to the DC-link is possible. The resulting switching state is called "recharging PEBB commutation". Commutation to and from this PEBB state is possible, but involves multiple commutations and has high conduction losses. However, this state can still be considered if the application time is short. The most penalizing aspect of this strategy concerns the blocking voltage of the devices.

Switching state The recharging switching state, Figure 3.21, connects the PEBB capacitor to one of the DC-rails and the current flows through the IGCTs, backwards into the PEBB and again forward to the output. During

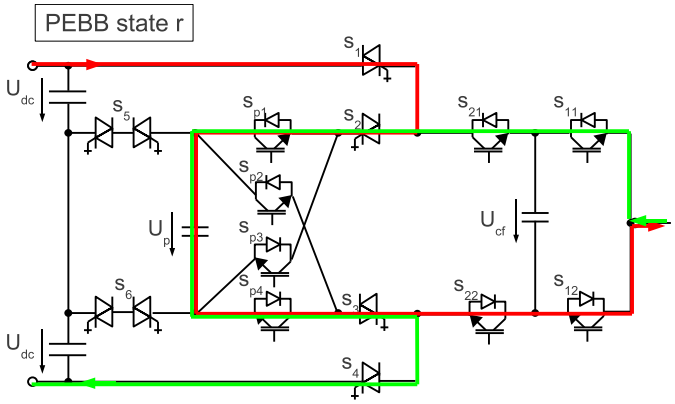


Figure 3.21.: *The recharging PEBB state connects the PEBB capacitor in series with the upper (or lower) DC-link capacitor such as to transfer energy into it.*

this particular PEBB state, it is still possible to generate a certain number of different output levels. They are resumed in the table on Figure 3.22.

4 new levels are introduced with this new PEBB state: $\pm(U_{DC} - U_p)$ and $\pm(U_{DC} - U_p + U_{cf})$. They could be used to refine the output levels, by producing non uniform levels with more resolution at the maximum and minimum of the sinusoidal output waveform, but it must be remembered that this PEBB state involves high conduction and commutation losses and should therefore be used as little as possible.

Blocking voltages The recharging PEBB state requires a high blocking voltages on the inner IGCTs S_{32} and S_{33}, on the IGBTs S_{21} and S_{22}, as well as on the PEBB IGBTs S_1 and S_2 (Figure 3.23). In the recharging PEBB state, the PEBB capacitor is connected to the upper (or lower) DC-rail. Therefore the PEBB IGBTs S_1 and S_2 have to block the DC-link voltage bidirectionally.

This severe limitation makes this solution unrealistic for application at the considered voltage levels.

External power supply

Since the PEBB capacitor voltage is relatively low and because the PEBB is always connected on one side to the neutral point, the voltage insulation

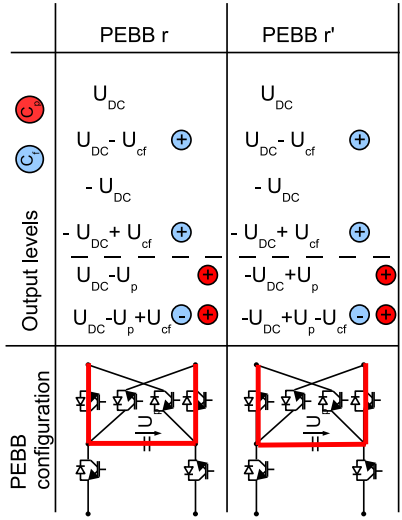


Figure 3.22.: *The 2 PEBB states and the corresponding levels for the recharging PEBB state* ($\cos\varphi = 1$).

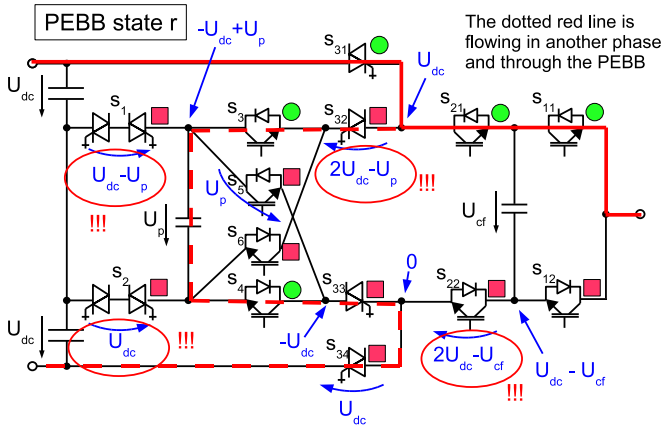


Figure 3.23.: *Blocking characteristic for all the PEBB states and the output level* U_{DC}

of an external power supply can be relatively small. Intuitively, one would say that with an external power supply, the C^3S topology could work at all power factors and with all modulation indexes.

In reality, the problem of the balancing of the phase capacitors must also be addressed. Not only does the PEBB capacitor require balancing, but also the phase capacitors. There are not always redundant states available to balance the phase capacitors.

It is shown later that in some cases of figure, §3.5.1, the PEBB capacitor can be stabilized better than the phase capacitors, due to the 3 phase interactions on the PEBB. In that case, the limiting factor is given by the phase capacitors and not the PEBB capacitor.

The calculation of the required external power supply for the case where the PEBB capacitor would be the limiting factor must then be calculated on the case to case basis. With an efficient balancing strategy and a low capacitor voltage, the external power supply requires an energy equal to a small fraction of the total converter power.

As an indication, the value of the required power supply, for the 9L CCCS of §3.5.1, is a 288kW power supply delivering 360A at 800V. This represents 6% of the total converter power. But in this case, it does not mean that with such a power supply the converter can run at full active power with a modulation index of $m = 1.15$, since the phase capacitors cannot be stabilized either at $m = 1.15$.

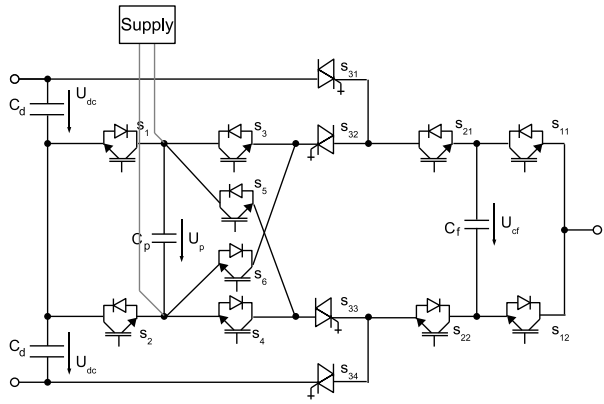


Figure 3.24.: *External supply of the PEBB capacitor*

Reduced number of output levels

The limit imposed on the modulation index concerns the PEBB capacitor voltage balancing. This means that if the modulation index limit is exceeded, the PEBB capacitor cannot be balanced anymore. However, there is a PEBB switching state for which the PEBB capacitor can be disconnected from the current path (state a, see Figure 3.10).

With this switching state, and assuming the correct voltage reference is given for the phase capacitors, the converter can run in the 5L ANPC mode. This means that the capacitors can be stabilized by means of redundant switching states and all modulation indexes are reachable at all power factors.

For instance for disturbance rejection, working for a short time at reduced signal quality might be acceptable, depending on the situation. This allows the C^3S converter to have some extra margin on modulation index for emergency situations, and so, it can be run in normal operation close to the maximum modulation index allowable for the PEBB capacitor balancing.

Topology modification

Instead of adding an external circuit, a direct modification of the topology can be considered. The topology of Figure 3.25 is an alternate solution. On that topology, the PEBB capacitor is directly included in the DC-link. The cross-connection can have interesting properties for stabilization of the capacitor middle points, or, a 4L rectifier could be used. Of course in this solution, the PEBB is also unique, and similar properties as in the CCCS can be found.

But the study of this solution is not considered here as it would require a whole chapter in itself.

Conclusions

The CCCS topology is very interesting regarding certain aspects like number of components, number of levels generated, simplicity of the circuit, upgrade easiness from the 5L ANPC. One drawback is that the capacitors cannot be stabilized for all modulation indexes at active power.

It is shown that the tuning of the levels cannot provide a way to stabilize the capacitors. This means that the designer must choose the voltage ratios based on the blocking voltage characteristics and the number of generated levels. However, there is still no straightforward way to define which voltage ratios lead to controllability on the capacitors and up to what modulation index.

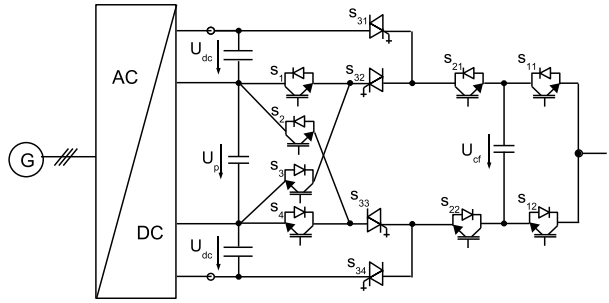


Figure 3.25.: *Proposed topological modification for the C^3S inverter, integrating the capacitor in the DC-link, and using a 4L rectifier for the supply and balancing of the DC capacitors.*

The simulation results show that for the 9L CCCS $[4; 2; 1]$, the maximum modulation index is $m = 0.925$ (see §3.5.2).

The next section focuses on control algorithm definition and simulations. A prototype has been built and the measured results are presented in the next chapter.

3.3.6. Neutral Point Balancing

Until now, nothing is mentioned regarding the neutral point control of the three level DC-link supply. Because of evident analysis complexity of the converter alone, the neutral point balancing is not considered as part of this work. The assumption is therefore made that a balanced 3 level power supply is available.

The unbalance introduced by the modulation might not be too large. In a first approximation, it can be roughly estimated that since the modulator tries to balance the PEBB capacitor voltage, which implies the neutral point current flowing through the capacitor, the average current value should be relatively close to zero. This is however not measured and is not assessed.

3.4. Modulation algorithm

3.4.1. Space vector modulation

The principal target of the modulator is to demonstrate that it is possible to stabilize the 4 capacitors of a 3 phases CCCS multilevel inverter. Getting the highest performances out of the topology is therefore not the main

target. The modulator is developed in the most simple way which can ensure stability of the voltages on the capacitors.

Since the phasor model is available and gives already a good understanding of the system's behavior and dynamics, it is quite straightforward to assume that the most adapted modulation method to apply is the space vector modulation technique, [43], [44]. Additionally, because of the intrinsic 3 phase properties of the C^3S topology, it does not really make sense to try to apply carrier based modulation techniques.

The balancing strategy for the modulation algorithm can be stated as choosing the optimum switching state from the space phasor redundancies, which offer the best stabilization overall, while ensuring a correct three phase modulation of the output.

The redundancies of a phasor in the space phasor plan is equivalent to a common mode shift in a carrier based modulation. Thus the balancing strategy of the CCCS converter is also making use of common mode. It is important to keep this in mind and therefore make sure the neutral point of the Star connection of the load is not connected.

3.4.2. Capacitor stabilization algorithm

General structure

The general structure of the proposed modulation algorithm can be seen on Figure 3.26. The different constitutive blocks are described in more details throughout this subsection.

Implementation specificities are not discussed as they are platform dependent. The first implementation was done in Matlab and then the modulator was coded in VHDL. The two algorithms are therefore completely different from the point of view of the coding, but the structure, presented here, remains the same.

As already mentioned, the modulator is working with space phasors. First, the edges of the triangle (i.e. the three nearest phasors enclosing the reference phasor) are determined, like in standard vector modulation schemes. It is then necessary to define which are the possible combinations of phase and PEBB switching states to generate the 3 required space phasors. In the most general case, there can be up to seven PEBB states possible, and for each PEBB state, there can be several combination of phase states. Each of these combinations can potentially have a different action on the capacitor voltages. Thus there is a lot of combinations to identify and to choose from.

By knowing which are the capacitors to be corrected with the highest priority (usually the most deviated), a score is given to each possibilities.

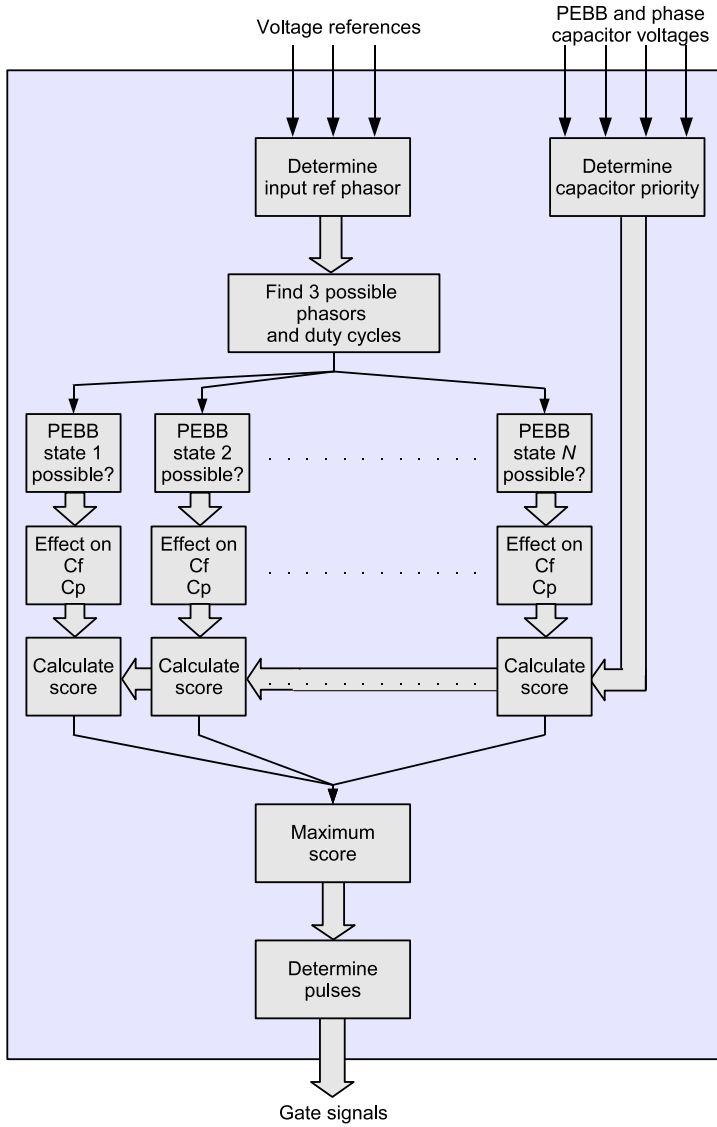


Figure 3.26.: *General structure of the C^3S modulator*

This score also includes other effects like switching losses or penalizing unnecessary IGCT switchings, for instance.

Finally, comparing the best scores for each PEBB states gives a global optimum which is then translated into gate signals to be applied to the converter.

A model predictive control strategy can certainly be of benefit here. The switching frequency of the PEBB and the phases, and the capacitor voltage deviations can be minimized over several switching periods in the future, and because the evolution of the system is known, a pretty accurate prediction can be done. But as already said, the target of the present modulator is to demonstrate the feasibility of the balancing scheme.

Determining the input phasor

The function of this block is to calculate the space phasor corresponding to the voltage reference signals. It consists only of the reference frame transformation. The usual function is used:

$$v = \frac{2}{3} \cdot \begin{bmatrix} 1 \\ -\frac{1}{2} + j \cdot \frac{\sqrt{3}}{2} \\ -\frac{1}{2} - j \cdot \frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} r_1 \\ r_2 \\ r_3 \end{bmatrix} \tag{3.40}$$

Find triangle

This function is part of standard space vector modulation principle. The reference space phasor is approximated by the three closest phasors that create a triangle enclosing the given reference phasor, for instance, see [45].

A fast method to define this triangle using a transformation is described in [46]. A transformation is defined from the space phasor plan (which is orthogonal) to a non-orthogonal reference frame called $'ab'$.

The edges of the triangle in the space phasor plan are non-integers (x_1, x_2, x_3 on Figure 3.27). In the $'ab'$ reference frame the edges become integers, and are easy to calculate since only rounding operations on the transformed space phasor reference are necessary.

The transformation matrix is straightforward to define: The axis x remains identical and is defined as the a axis and the y axis is rotated by 30° counter clockwise to become the b axis. The transformation matrix is therefore defined as:

$$\begin{bmatrix} a \\ b \end{bmatrix} = \begin{bmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} x \\ y \end{bmatrix} \tag{3.41}$$

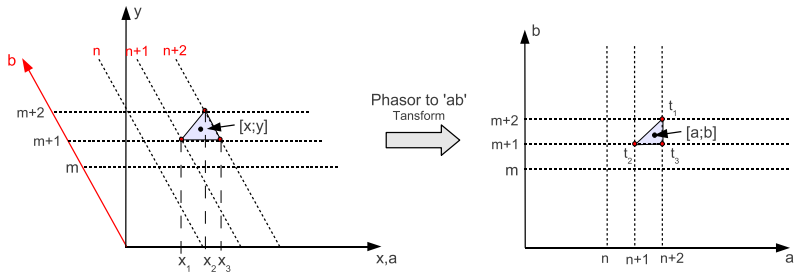


Figure 3.27.: *Transformation from the space phasor plan to the ′ab′ plan*

The diagonally opposed edges of the triangle are calculated by rounding the transformed space phasor reference coordinates to the top (ceiling function $\lceil x \rceil$), respectively to the bottom (floor function $\lfloor x \rfloor$):

$$t_1 = \begin{bmatrix} \lceil a \rceil \\ \lceil b \rceil \end{bmatrix} \text{ and } t_2 = \begin{bmatrix} \lfloor a \rfloor \\ \lfloor b \rfloor \end{bmatrix}$$

Finding the third edge of the triangle depends if the reference point is situated below or above the diagonal. $a - \lfloor a \rfloor$ is the relative height and $b - \lfloor b \rfloor$ is the relative length of the space phasor within the triangle. The diagonal can be then defined simply as:

$$a - \lfloor a \rfloor = b - \lfloor b \rfloor$$

If the difference $(a - \lfloor a \rfloor) - (b - \lfloor b \rfloor)$ is negative, then the reference is situated below the diagonal, and else vice versa. It follows that:

$$(a - \lfloor a \rfloor) - (b - \lfloor b \rfloor) \quad < \quad 0 \Rightarrow t_3 = \begin{bmatrix} \lfloor a \rfloor \\ \lceil b \rceil \end{bmatrix}$$

$$(a - \lfloor a \rfloor) - (b - \lfloor b \rfloor) \quad \geq \quad 0 \Rightarrow t_3 = \begin{bmatrix} \lceil a \rceil \\ \lfloor b \rfloor \end{bmatrix}$$

Duty cycle calculation depends if the reference is above or below the diagonal. They are defined as (see [46]):

$$(a - \lfloor a \rfloor) - (b - \lfloor b \rfloor) \quad < \quad 0 \Rightarrow \begin{cases} t_1 & = & 1 - (\lceil a \rceil - a) \\ t_2 & = & 1 - (b - \lfloor b \rfloor) \\ t_3 & = & 1 - t_1 - t_2 \end{cases}$$

$$(a - \lfloor a \rfloor) - (b - \lfloor b \rfloor) \quad \geq \quad 0 \Rightarrow \begin{cases} t_1 & = & 1 - (\lceil b \rceil - b) \\ t_2 & = & 1 - (a - \lfloor a \rfloor) \\ t_3 & = & 1 - t_1 - t_2 \end{cases}$$

Once the edges of the triangle have been found, they are transformed back to the space phasor plan.

Remark: If the inverter does not allow to generate all space phasors, then a strategy has to be implemented in order to find the next closest phasor, or to use two available phasors to generate a virtual phasor replacing the missing one. These strategies are linked closely to the specific cases and are not discussed here.

Possible PEBB states and effects on C_f and C_p

Several methods can be imagined, but since an a priori knowledge is available, the most straight forward way to implement these functions is to use lookup tables. In these tables, all the possible space phasors are defined. The number of space phasor depends on the number of cascaded Common Cross Connected Stages within the topology. They can be found by calculating all the combinations of levels of a given PEBB state. For one given PEBB state:

$$n_{sp} \quad = \quad (C_3^k + C_2^k + C_1^k) \tag{3.42}$$

where

$$\begin{aligned} n_{sp} &: \text{Number of space phasors} \\ k &: \text{Number of phase states} \end{aligned}$$

For each combination, there is one associated effect on each of the phase capacitors and on the PEBB capacitor. These informations must also be coded in the lookup tables.

The memory contains the essential information concerning the topology to be controlled. All the phasors which can be generated, the corresponding PEBB and phase states, and the actions on the PEBB and phase capacitors are referenced. Getting the information about one phasor and it's effects on the system is then just a matter of finding the correct line to read, in the table.

Figure 3.28 shows the proposed structure for the memory and score calculation. The reference phasor is compared to a list of phasors pre-calculated and stored in a memory. When the reference phasors matches the phasor stored in memory, the a score is calculated using the stored informations about capacitor effects. When the lookup table is fully read, the maximum calculated score is retained and the adequate phase switching state is found, for optimum capacitor balancing.

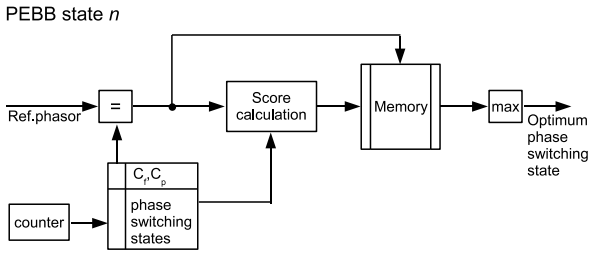


Figure 3.28.: *Proposed memory structure and score calculation*

Determine capacitor priority

This function's role is to associate one priority for correction of the voltages to each one of the 4 capacitors. This priority influences the score in a critical way, and therefore directly modifies which is the best switching state in a given situation.

Basically there are many ways to define the priorities. 2 solutions are discussed here, the second giving better results than the first.

The simplest way to define the capacitor priorities is to give the highest priority to the capacitor with the largest voltage deviation, in absolute value. In this case, the PEBB and the phase capacitors are treated equally. In practice, it can be seen that this solution works, but does not give optimal results. The main reason is because intrinsically, the PEBB capacitor dynamics and controllability are different from the phase capacitors.

The graphical model, §3.3.3, (and the analysis of the switching states §3.3.2) of the circuit shows that the PEBB can only be charged at some give positions in time. This means that usually, the PEBB voltage is more often discharged then charged. It is therefore not wrong to state that when the PEBB can be charged, it should be charged, since it's voltage will always tend to be lower than its reference.

Therefore, the second priority strategy proposed is the following: When the PEBB capacitor's voltage deviation is negative, the PEBB must be charged. But as it cannot be charged that often, the probability that the PEBB capacitor can actually be charged is low. It must then be avoided to discharge it further as the next charging position can potentially be far away in time (up to $\frac{1}{6}$ of the period).

Translated into priority language, it means when the capacitor's voltage is lower than the reference value, give it the highest priority. Else, treat it like the other capacitors.

Calculate score

This function is the heart of the modulator. It defines exactly which PEBB and phase states must be used depending on priority levels and the 3 phasor references. The general concept is based on the following parameters (index $i \in [1;3]$ are the 3 phases and $i = 4$ is the PEBB):

- P_{cap_i} Priority of the capacitor i, 1=high priority
- $C_i(t_{jk})$ Effect on the capacitor i of the phasor j with PEBB state $PEBB_k$
- $C_{i_{ref}}$ Required effect on the capacitor of the phase i
- I_i Current amplitude in phase i
- I_p Sum of the currents through the PEBB capacitor
- sw_i Number of switching required in phase i for new state

Each possible combination of phase and PEBB switching states are analyzed. A score is given to each solution and only the highest score is retained.

$C_i(t_{jk}) = C_{i_{ref}}$ means that the effect of the given switching state is the same as the required effect (i.e. the switching state loads the phase capacitor 3 and the phase capacitor 3 requires to be loaded). On contrary, $C_i(t_{jk}) = -C_{i_{ref}}$ means the effect is exactly opposite and $C_i(t_{jk}) = 0$ means there is not effect on the concerned capacitor. The score S is then defined as follows:

$$\begin{aligned} \text{if} \quad & C_i(t_{jk}) = C_{i_{ref}} \quad \text{then } S = S + \frac{1}{P_{cap_i}} \cdot I_i \\ \text{elseif} \quad & C_i(t_{jk}) = 0 \quad \text{then } S = S + 0 \\ \text{elseif} \quad & C_i(t_{jk}) = -C_{i_{ref}} \quad \text{then } S = S - \frac{1}{P_{cap_i}} \cdot I_i \end{aligned} \tag{3.43}$$

and for the PEBB:

$$\begin{aligned} \text{if} \quad & C_4(t_{jk}) = C_{4_{ref}} \quad \text{then } S = S + \frac{1}{P_{cap_4}} \cdot I_p \\ \text{elseif} \quad & C_4(t_{jk}) = 0 \quad \text{then } S = S + 0 \\ \text{elseif} \quad & C_4(t_{jk}) = -C_{4_{ref}} \quad \text{then } S = S - \frac{1}{P_{cap_4}} \cdot I_p \end{aligned} \tag{3.44}$$

For the switching losses:

$$S \quad = \quad S - K \cdot \sum_{i=1}^{4} sw_i \tag{3.45}$$

K is a factor to parametrize the influence of the switching losses on the score.

From the experience, it can be stated that the most important parameter is the priority weights $\frac{1}{P_{cap_i}}$. Numerically, the capacitor with the highest

priority has the highest value. This however does not necessarily mean that the score will reflect this aspect properly, because the current amplitude also influences the score. The two following situations are presented.

In the first case, a capacitor close to its nominal value is considered. Since its deviation is small, the weight $\frac{1}{P_{cap_i}}$ is low. If a large current is flowing through the capacitor, the score might not reflect well enough that the capacitor will be strongly influenced by the current. Thus it can happen that a switching state where the current is flowing through the capacitor is chosen, when another state could have been chose, avoiding that the current flows through the capacitor.

In the second case, the capacitor with the highest priority is considered. If it is in a phase where the current amplitude is low, it can happen that the final switching state gives more importance to another capacitor because the current is larger in there, and thus the score more influenced by the other capacitor. The is not the required effect, since the score should make sure the best choice is done for the capacitor with the largest deviation. In this case, a capacitor with a lower score is contributing to a larger extent to the score because of it's current amplitude.

From these two examples, the role of the weights in the score appears more clearly. All in all, the priority has the highest importance. It is better to correct properly a capacitor strongly deviated, even if this involves disturbing a capacitor close to its nominal value, then doing the opposite. The trade-off is then clear, the priority must contribute more than the current amplitude. So the score value must be tuned in such a way that even with a lower current amplitude, the concerned capacitor will still contribute significantly to the score.

In practice, the currents are not introduced with exact numerical values. They are given with orders ranking from 1 to 3, the phase with order 3 having the highest current. The current score is then added to the priority (and not multiplied, the reason being that in practice all values are integers and not floats, which would result in wrong score calculations).

The priorities, on the other hand, typically range from 1 to 8, in steps of 2^n. So the capacitor with the highest priority is twice larger than the second capacitor, which is in turn twice larger than the third, etc.

Determine pulses

With the three enclosing phasors calculated, the application time is also defined. But the order of application is not imposed. It is possible here to apply various optimization strategies in order to minimize the THD or possibly eliminate some specific harmonics, [47] or [43].

The best solution from the point of view of global THD value is to reproduce the naturally sampled PWM modulation scheme [48], [49]. The reordering is thus done in the following manner: the longest applied phasor is split into 2 parts. It is applied first for half of it's duration, followed by the second and third phasor in order of application duration. Then, in the last step, the first phasor is once again applied for the second half of the required duration, Figure 3.29.

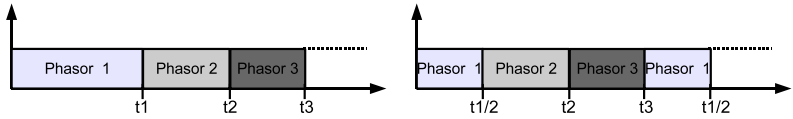


Figure 3.29.: *Space phasor reordering, in function of their application time, to simulate PWM natural sampling*

This strategy is applied in the modulator, but no extensive comparison to other methods is done regarding the optimization obtained by this method regarding the THD.

3.4.3. Reference delay

The low frequency current ripple problem which already occurred on the 9L CCIL topology (see §2.5) also appears with the CCCS topology. A deeper analysis of the problem revealed that the ripple is caused by a wrong estimation of the reference phasor.

It is shown by simulation that increasing the switching frequency reduces the low frequency ripple. Increased switching frequency however does not influence the amplitude of the capacitor voltage ripples and this is also shown by simulation. This leads to conclude that the current ripple is not caused by capacitor voltage ripples.

Increased switching frequency means that the reference phasor is approximated more often, and as a direct consequence, any output error is reduced. In simulation, the calculation delay is 0, since the simulation tool makes sure that all variables are calculated before moving to the next step. But the implementation of the control algorithm is done using a time decoupling block (sample and hold) and a triggered subsystem to simulate the discreet behavior of the system. It is specifically the error introduced by the sample and hold which introduces the delay and the error.

With higher output resolution, 9L in this case, the delay introduced by the control scheme causes an error which is 3 times larger (since the

triangles have a 3 times smaller surface) compared to a 5L output, with a similar delay, Figure 3.30. This means a more precise output requires a faster modulation.

By introducing a phase advance (in feedforward mode) on the reference phasor, which is an open-loop correction of the delay problem, it is possible to reduce the ripple amplitude. Simulation results, with a switching frequency of about 2kHz (50 samples per period for the modulation), show that a phase advance of half the resolution angle already helps to reduce the harmonic distortion of 25%. The improvement is quite noticeable in the lower frequency ranges, Figure 3.31.

A closed loop tracking of the phase (PLL), and estimation and compensation of the delay should solve this problem completely.

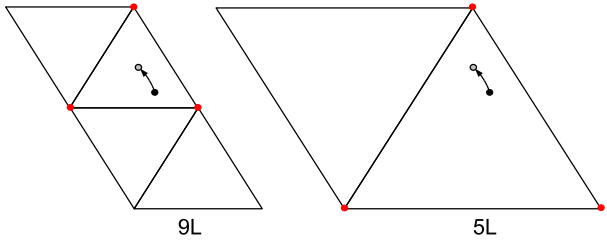


Figure 3.30.: *The delay introduced by the control has more impact with 9L than with 5L*

3.4.4. Short pulse suppression

With high output resolution, it can be interesting to cancel some phasors, when the duty cycles are too small, to avoid unnecessary switchings. In some cases, the error introduced by the approximation of the reference phasor by fewer discrete phasors is relatively small, while the influence on the switching frequency can be interesting.

This solution is interesting with higher output resolution, since there is a higher chance that the reference phasor be close to discrete phasors, as there are more discrete phasors.

Graphically, short pulse suppression is equivalent to defining regions of attraction, Figure 3.32. If the reference phasor falls into the region of attraction defined by the red dashed area, it is approximated to one single discreet phasor. If it falls in the region defined by the black dashed area, it is approximated by two, instead of three, discreet phasors.

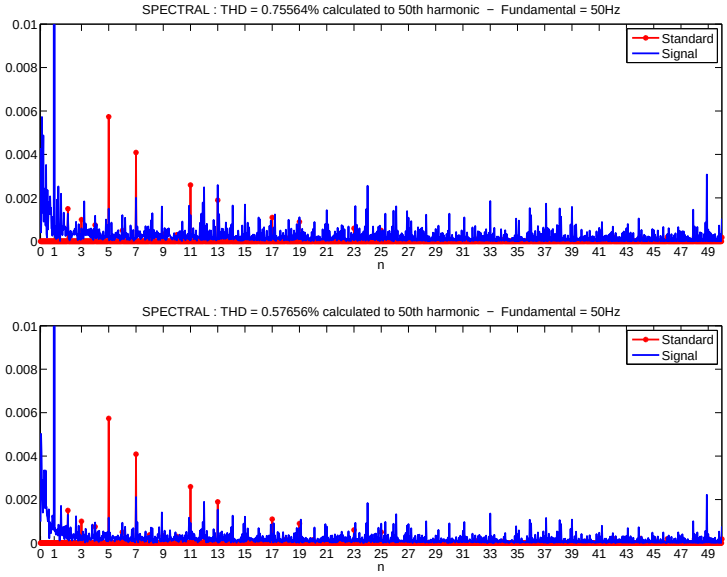


Figure 3.31.: *Top: Harmonic content without angle feedforward. Bottom: Harmonic content with angle feedforward*

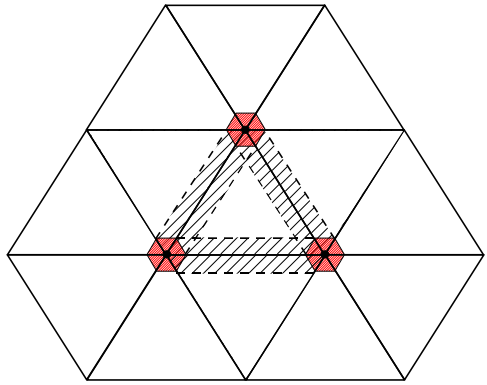


Figure 3.32.: *Short pulse suppression: regions of attraction*

Of course, the larger the regions of attraction are, and the greater the introduced error. The effect of errors on the phasor is discussed in the previous §3.4.3.

Besides reducing the switching frequency, this strategy also influences the harmonic content. The approximation by one or two, instead of three, phasors is somehow similar to controlling turn on and off angles, in steady state operation. Because in steady state, the trajectory is always almost the same, the references are very similar. Thus, the regions of attraction define sort of turn-off and -on angles.

But the impact is not assessed and this topic is not further discussed, since it does not belong to the scope of investigations undertaken here.

3.4.5. Summary

With the generic approach to the modulation algorithm presented here, it is possible to design a modulator for many different CCCS configurations. Up to this point, no a priori conditions are considered regarding any specific CCCS configuration. From the next section on, the implementation of one specific 9L configuration is discussed. The tools developed in the previous and present sections will be used and are therefore verified and validated in simulation.

3.5. 9 level CCCS VSI

3.5.1. Retained topology

Choice of the voltage ratios

The main aspects to be considered for a specific topological choice have already been discussed, and are namely blocking voltage, number of generated levels and controllability of the capacitors. Putting this work back into it's context, the principal target is to design an extension to the 5L ANPC inverter for extra level generation.

From that point of view, keeping the same voltage ratios as on the existing topology (i.e. $V_{cf} = \frac{V_{DC}}{2}$) is an interesting choice because the mechanical design of MV applications is largely (although of course not only) influenced by the size of the passives. Another interesting feature with the PEBB is that, at modulation indexes for which the PEBB capacitor cannot be stabilized, it can be simply bypassed and the converter can operate like a standard 5L, at the same power levels.

Moreover, it is seen with the CCIL converter study, §2.6.3, that 9L are enough to comply with the VDEW and with the IEC61000-2-12 standards.

So for the different reasons presented here, the 9L $[4; 2; 1]$ is retained.

Characteristics

Blocking voltages As discussed in the characterization chapter, §3.2.5, the blocking voltage capabilities of the high voltage cell and those of the first range of the medium voltage cell must be 25%, respectively 50% higher than in the standard ANPC design. The reason is that those switches must block the extra PEBB capacitor voltage.

This can sound as a lot, but it must be reminded that the number of generated levels is doubled and that only one extra passive component is necessary for the 3 phases together, while keeping full compatibility with the 5L operation.

Maximum theoretical modulation index The maximum modulation index achievable such that the PEBB capacitor remains controlled is difficult to estimate. The principal reason is that there is a correlation between the choice of the 3 phase capacitor voltages stabilization, and the PEBB capacitors's stabilization. The two problems cannot be treated separately.

In [21], S.Mariethoz proposes some methods for estimation of the maximum theoretical modulation indexes, but the considerations do not apply here. The reason is that the PEBB capacitor and the phase capacitor contribute to levels lower than the DC-link and that there is a coupling between the 3 phases of the inverter.

An analysis is proposed, based on the graphical representation, in order to understand better what is the behavior of the PEBB and phase capacitor voltages regarding their specific action phasors, and deduce graphically what the maximum modulation index is.

Plotting the average contribution of the phasors on the PEBB capacitor shows what is the average actions available on the PEBB capacitor, Figure 3.33-top. This does not mean that the actions are necessarily spread out in this way. It gives only a global preview. The problem is that the current amplitude in each of the three phases, and the connection to the PEBB cannot be represented in this view.

It is seen that a 6th harmonic ripple is likely to appear on the PEBB capacitor voltages. On the other hand, there are a lot of zero contributions, and quite balanced repartition of the charging and discharging phasors. From this representation, it does not seem that the PEBB capacitor balancing actually does limit the modulation index, and it seems that the ripple amplitude can be quite small.

Doing the same thing for the phase capacitors reveals that, there are much fewer zero contributions, Figure 3.33-bottom and Figure 3.34. Thus

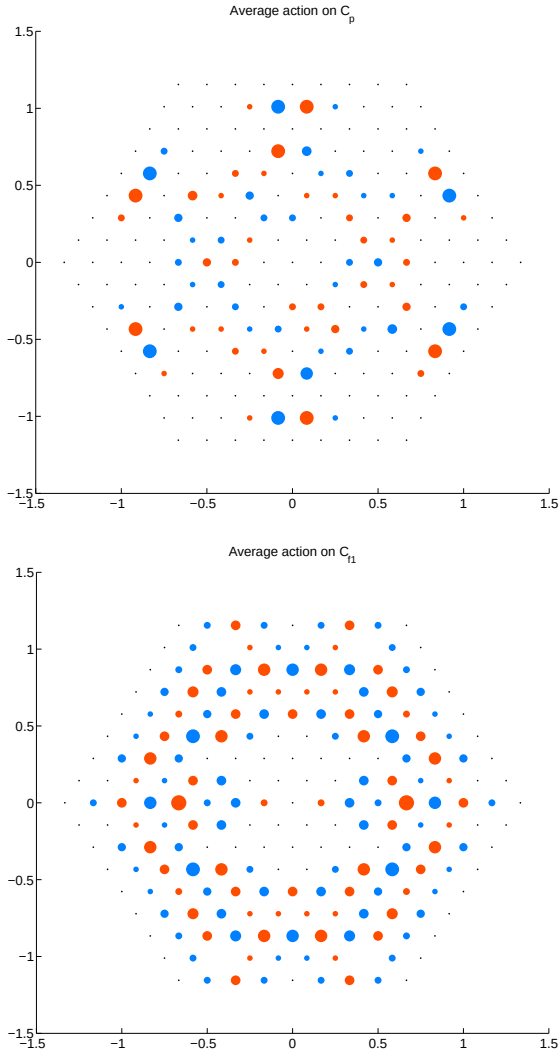


Figure 3.33.: *Average phasors action on the capacitors C_p and C_{f1}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

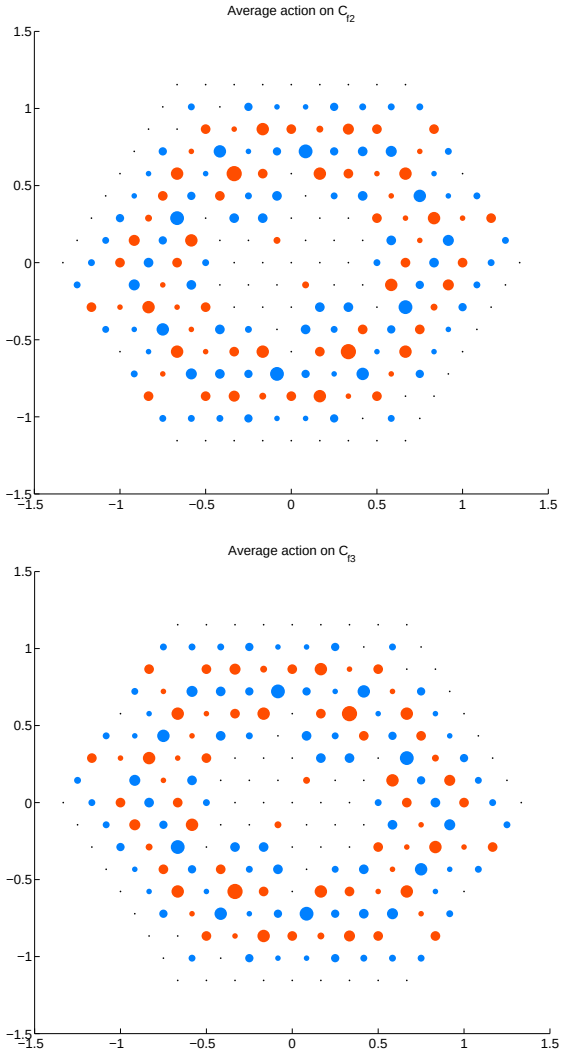


Figure 3.34.: *Average phasor action on the capacitors C_{f2} and C_{f3}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

the capacitor voltages will have a higher frequency ripple. It can also be seen that the phase capacitors definitely cannot be stabilized for large modulation indexes because of the dominant discharging states (blue dots, Figure 3.33-bottom). Therefore, it seems that the constraint is given more by the phase capacitors than the PEBB capacitor, contrarily to what is expected from the previous analysis.

The maximum theoretical modulation index for the phase capacitors is situated somewhere close to the middle of the 7th and the 8th hexagons. The corresponding modulation index can be calculated by a rule of three:

$$m_{max} = \frac{1.15 \cdot 7.5}{9} = 0.958 \tag{3.46}$$

Because it is possible to control the capacitors better every 4th of a period, the ripple is likely to present a 4th harmonic component as well.

Additionally to this, it can be predicted that for modulation indexes around the 6th hexagon, $m_{6th\_hexagon} = 0.77$, the controllability of the phase capacitors is strongly reduced.

3.5.2. 9L CCCS Simulation results

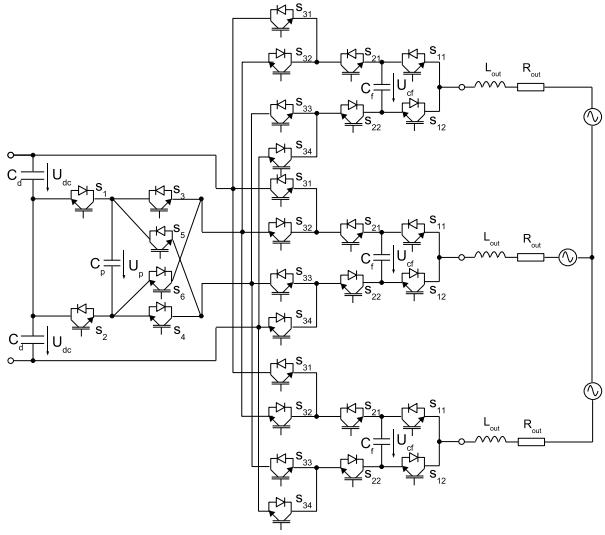


Figure 3.35.: *Simulation setup of the 9L CCCS multilevel inverter*

The previously defined modulation algorithm is applied, to the 9L [4; 2; 1] CCCS inverter topology. The target is to demonstrate the modulator concept and assess the obtainable performances for the retained inverter configuration.

The setup, Figure 3.35, is simulated under Matlab Simulink using the PLECS toolbox. The modulator is implemented in a Matlab M-function. The load is composed of a three phase voltage source system in Star configuration and an inductive output filter (with a small resistance) modeling the transformer. The elements are calculated for a grid short circuit ratio of 20, and the voltages are shifted accordingly to the desired operating point in steady state.

The total DC-link voltage $2 \cdot U_{DC}$ is $6.4kV$. Simulations are run for active power at a modulation index of $m = 0.9$. The corresponding line to line voltage is $3.527kV$. At reactive power, at $m = 1.15$, the line to line voltage is equal to $4.507kV$. The load is computed so that the current is $900A_{rms}$ and the power factor $\cos\varphi = 0$ or $\cos\varphi = 1$. The PEBB capacitor is $6mF/800V$ and the phase capacitors are $2mF/1600V$, according to Table 3.4. The stored energy is the same for the PEBB and the phase capacitors.

Table 3.4.: *CCCS configuration and associated voltage levels*

$[U_{DC}$	$; U_{cf}$	$; U_p]$
4	; 2	; 1
3.2kV	; 1.6kV	; 0.8kV

The vector modulation resolution is 50 reference phasors per period (approximated by 3 phasors each time, see §3.4). The measured switching frequency at the output are reported in Table 3.5.

Table 3.5.: *Measured switching frequencies in simulation*

	Switching frequency		
	S1, S2, S3, S4, S5, S6	S31, S32, S33, S34	S11, S12, S21, S22
Active power	2kHz	50Hz	1.6-1.7kHz
Reactive power	1.7kHz	50Hz	1.2kHz

$1.6-1.7kHz$ for the IGBTs, $50Hz$ for the high voltage IGBTs (or IGCTs) and $2kHz$ for the PEBB IGBTs at active power, and $1.2kHz$, $50Hz$ and

$1.7kHz$ at reactive power respectively. Simulation waveforms are given on Figure 3.36.

At active power the PEBB capacitor voltage contains a 6th harmonic voltage ripple due to the physical repartition of the charging space phasor positions (see §3.5.1). As analyzed, the control of the phase capacitor voltages is what limits the maximum modulation index at full active power. The simulations give a maximum modulation index of $m_{max} = 0.925$. With a higher modulation index, the PEBB capacitor voltage control is lost first, followed by the phase capacitors. This probably due to the modulation strategy which tries to gain back control on the phase capacitors and thus losses the PEBB.

The PEBB capacitor ripple amplitude is around $\pm 50V$, that is 6.25%, and the phase capacitor ripple is $\pm 250V$, which means 15.6%. These values are acceptable, especially because the ripple amplitude does not directly influence the harmonic distortion at the output.

At reactive power in general, the voltage ripple amplitudes are larger and contain typically some second harmonic components. Since the modulation index is really large, the capacitors can be balanced, on average, only every half periods. This can be very clearly seen on the phase capacitor ripples. On the PEBB capacitor the trend is less noticeable however.

The ripple amplitude on the PEBB capacitor is still somewhere around ± 50, while the phase capacitor ripple is now almost $[-250V; +500V]$. A large deep is also noticeable around 80ms. This is caused by the non-predictive regulation scheme which discharges the phase capacitor at some point, without knowing that in the next moments, the capacitor cannot be controlled for some time. This causes a large deep that lasts for about half a period.

THD The voltage THD is 2.6% (Figures 3.37 - up). The harmonic content is completetly compliant with the standards up to the 23rd rank. Beyond this point, there are some harmonics slightly larger than the standards, but it cannot be stated if these really appear in a reality. The is also a large 49th harmonic, but once again, it is not so clear if it will really appear.

The current THD is 0.5% (Figures 3.37 - down). A low frequency ripple is noticeable, but its amplitude is lower than without the reference feed-forward strategy (see §3.4). This indicates that part of the problem (if not all) comes from the phasor approximation error. There is also some harmonic values higher than standards at relatively low frequencies (for

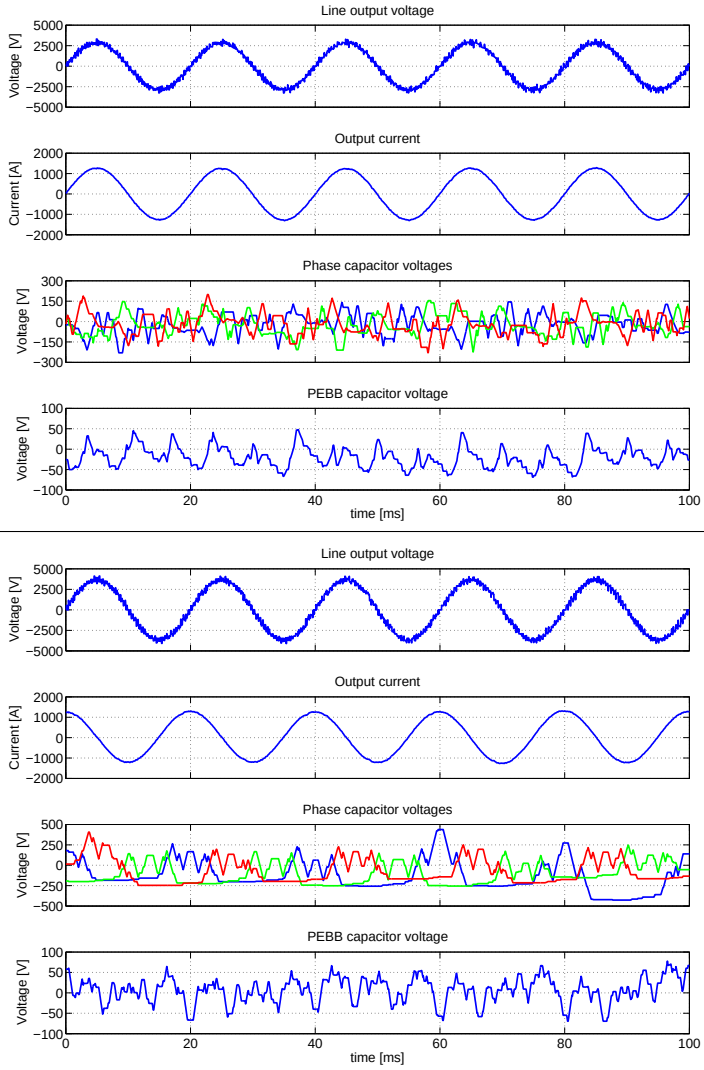


Figure 3.36.: *Simulation results of the line to line output voltage, line output current, phase capacitor voltages, PEBB capacitor voltage. Top:* $m = 0.9$, $\cos\varphi = 1$. *Bottom:* $m = 1.15$, $\cos\varphi = 0$

instance $n = 9, 12$, etc) but these tend to disapear depending on the measurment parameters (number of samples, frequency). It cannot be said if these harmonics are really existing or due to simulation parameters.

3.6. Benchmarking

3.6.1. CCCS versus CCIL, NPC, cascaded H-bridge and flying cap

Comparison

In the §3.3.4 the general equations characterizing the CCCS topology are presented. They are used to benchmark the electrical characteristics of the CCCS against the CCIL and the other standard topologies already discussed previously.

The two CCCS configurations for which the equations were derived in §3.3.4 are configurations with linearly growing voltage ratios, the $[k+2; k+1; k; ...; 3; 2; 1]$ CCCS, and the quadratically growing configuration, the $\left[2^{k+1}; 2^k; ...; 4; 2; 1\right]$ CCCS.

Number of levels per stage In terms of level generation per stages, Figure 3.38 - top, the two CCCS configurations, for which the equations were derived in §3.3.4 , exhibit a completely different behavior. The CCCS $[k+2; k+1; k; ...; 3; 2; 1]$ exhibits a linear progression of the levels per stage, and this is directly linked to the chosen voltage ratios, while the CCCS $\left[2^{k+1}; 2^k; ...; 4; 2; 1\right]$ shows a quadratic progression. Compared to the CCIL topology, the progression is in general less steep.

Stored energy per level The stored energy, Figure 3.38 - bottom, is on the other hand very comparable to the CCIL topologies. If the CCCS is able to compete with the CCIL even though the number of levels produced is in general lower, it is because the CCCS only uses one capacitor per stage and per converter against 3 for the CCIL configuration. The gain in terms of energy, thus in terms of the amount of passive components, is non negligible.

Individual switches per level In terms of number of switches per level, Figure 3.39 - up, the linear progressing CCCS $[k+2; k+1; k; ...; 3; 2; 1]$ still exhibits slightly better performances then standard solutions, ought to the fact that the PEBB is common to the three phases. The CCCS $\left[2^{k+1}; 2^k; ...; 4; 2; 1\right]$ performances fairly, as expected from the previous comparisons, and the performances are in the same range as the CCIL topology.

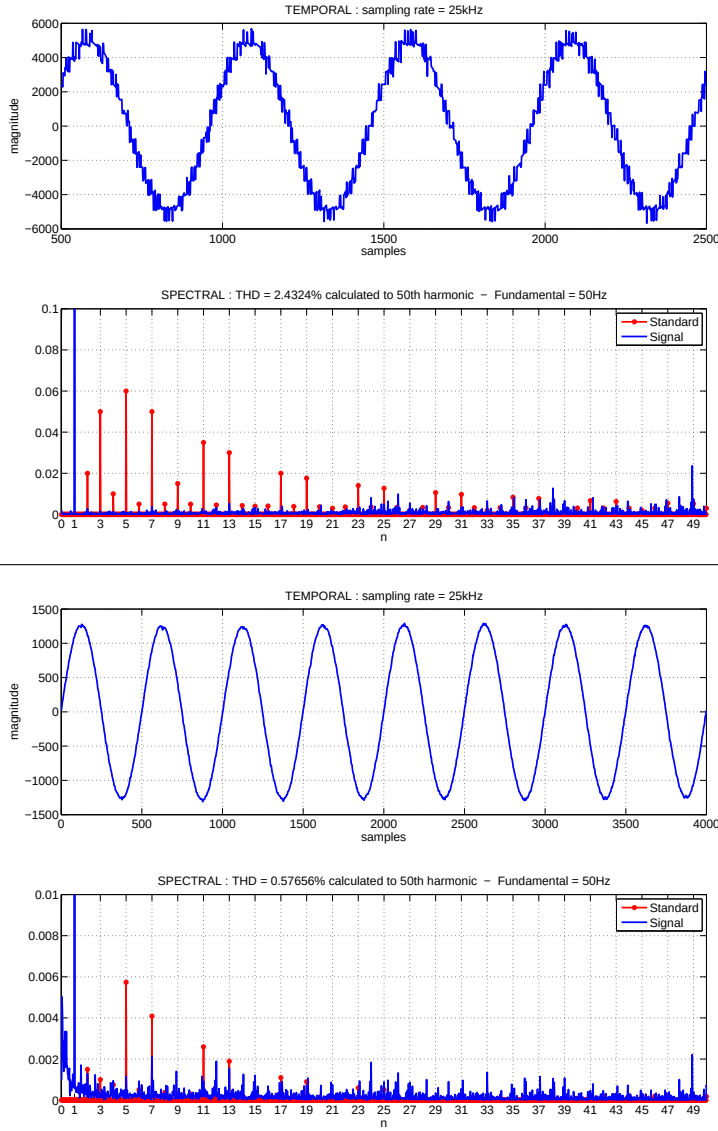


Figure 3.37.: *Top, voltage, and bottom, current harmonic distortion.*

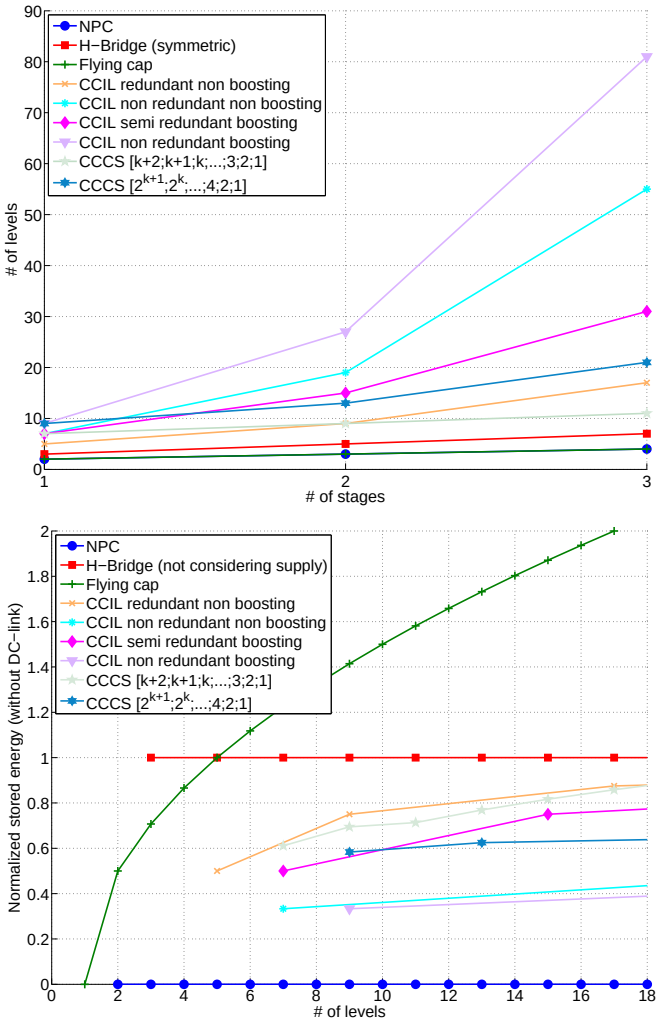


Figure 3.38.: *Top: Number of levels produced by cascaded stages. Bottom: Normalized energy per levels.*

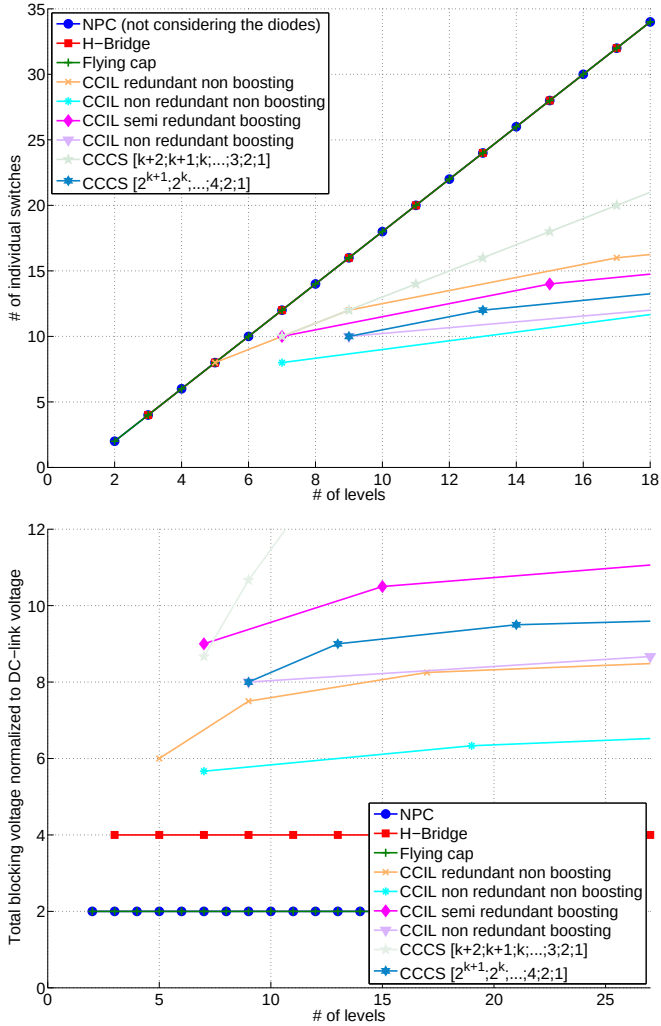


Figure 3.39.: *Top: Number of switches per levels. Down: Total blocking voltage normalized to DC-link voltage per levels.*

Total blocking voltage per level Finally in terms of total blocking voltage normalized to the DC-link voltage, Figure 3.39 - down, the linear CCCS $[k+2; k+1; k; ...; 3; 2; 1]$ is not at all optimal. The progression of the required blocking voltage compared to the produced levels grows drastically. This is a consequence of the fact that there are many switches in the topology influenced by the CCCS PEBB capacitor voltages.

On the other hand, the CCCS $\left[2^{k+1}; 2^{k}; ...; 4; 2; 1\right]$ is still performing slightly better, and is somewhere in the upper range of the CCIL topologies. The total blocking voltage remains pretty high and this is the consequence of the further reduction of the number of passive components. Because the CCCS PEBB is unique for the three phases, it is still able to keep the total blocking voltage somehow under control.

Findings

The CCCS topology positions itself, from the electrical point of view, as solution offering the possibility to further reduce the number of passive components, in the case of several stages cascaded, but at the price of a further increase in total blocking voltage.

Among others, the CCCS [4;2;1] offers some performance increase from the point of view of electrical characteristics, compared to the redundant non boosting 9L double capacitor CCIL topology, but on the other hand, is limited by the maximum modulation index at active power. Compared to the 9L CCIL single capacitor topology (CCIL non redundant boosting), the characteristics are slightly less good, especially because the boosting topology allows a lower DC-link voltage.

On the other hand, it should be taken into account that the CCCS topology allows to fall back to a 5L operation mode with the same power ratings (but of course reduced output signal quality), which is not the case of the 9L CCIL boosting topology.

Finally, the question of stability of the capacitor should be considered as well. With the CCIL configuration, it is possible to build redundant state topologies, which is not the case for the CCCS topology.

3.6.2. Harmonic distortion

Harmonic calculations based on simulation results show that the CCCS clearly offers better signal quality at the output compared to the CCIL topologies with the proposed modulations schemes, Figure 3.40. This is very noticeable on the currents: there is almost no low frequency ripple on the output current compared to the CCIL topologies. At lower switching

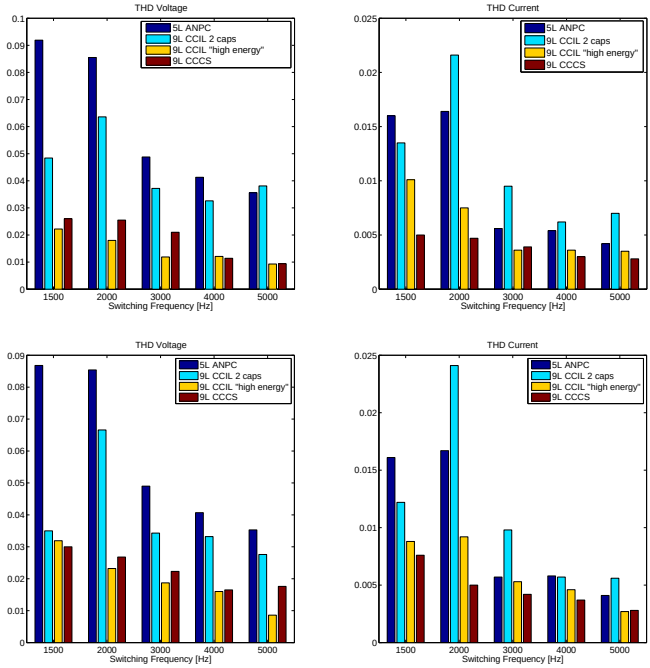


Figure 3.40.: *Voltage and current THD for m=0.9 and* $\cos\varphi = 0$ *(top),* $\cos\varphi = 90$ *(bottom).*

frequencies the CCCS can achieve a similar current signal quality as the CCIL at much higher switching frequencies.

It is questionable whether the influence comes from the control, which is quite different for the two cases, or if the addition of one more capacitor makes the system less sensitive to variations (in comparison with the 9L single capacitor CCIL). Since the PEBB capacitor is used in common by the three phases, it is possible that the coupling introduced by the PEBB capacitor cancels out some harmonics on the line to line voltages.

The maximum modulation index at active power is 0.925 for the CCCS against 0.91 for the CCIL. Another important characteristic of the CCCS is the fundamental switching frequency of the high voltage stage which is currently not guaranteed with the CCIL modulator.

It appears here that the CCCS is able to offer much nicer output waveforms compared to the 9L single capacitor or the 9L double capacitor CCIL. The previous comparison indicated a small advantage from the point of view of electrical characteristics for the CCIL solution, but the present benchmarking, there is a clear advantage for the CCCS.

3.6.3. Efficiency

9L CCCS

The loss calculation is split in three parts: conduction losses $P_{loss_{cond}}$, switching losses $P_{loss_{sw}}$ and reverse recovery losses $P_{loss_{rec}}$. These three powers are defined by the following set of equations for each power semiconductor:

$$P_{loss_{cond}} = V_{on_T} \cdot \overline{I_T} + V_j \cdot \overline{I_d} \quad (3.47)$$

$$P_{loss_{sw}} = (E_{on} + E_{off}) \cdot f_{sw} \quad (3.48)$$

$$P_{loss_{rec}} = E_{rec} \cdot f_{sw} \quad (3.49)$$

$\overline{I_T}$ and $\overline{I_d}$ are respectively the average IGBT (or IGCT) and diode currents. They are determined by means of simulation and reported in Table 3.6.

IGCT stage [50Hz]			**IGBT stage** [1.7kHz]			**PEBB** [2kHz]		
	$\overline{I_T}$ [A]	$\overline{I_d}$ [A]		$\overline{I_T}$ [A]	$\overline{I_d}$ [A]		$\overline{I_T}$ [A]	$\overline{I_d}$ [A]
T_1	286	0	T_5	286	114	T_9	0	286
T_2	115	0	T_6	288	117	T_{10}	0	115
T_3	117	0	T_7	287	114	T_{11}	117	0
T_4	287	0	T_8	289	117	T_{12}	287	0
						T_{14}	287	115
						T_{14}	288	117

Table 3.6.: *Average IGBT, IGCT and diode currents for the 9L C^3S inverter*

Using the data available from the manufacturers datasheets ([50], [51], [52]), it is then possible to determine the switching and conduction losses for each stages of the inverter. The turn-on and turn-off energies are given as functions of the current. It is reminded that the blocking voltages of some switches in the ANPC part are higher, but since no specific components

were retained, the characteristics of the existing components are used, and should roughly offer similar characteristics as possible components.

The values are reported in Table 3.7.

	$P_{loss_{sw}}$ [W]	$P_{loss_{cond}}$ [W]	$P_{loss_{rec}}$ [W]
IGCT stage total losses	320	2774	0
IGBT stage total losses	1224	3638	2312
PEBB stage total losses	480	3351	280

Table 3.7.: *Conduction, switching and reverse recovery losses for IGBT, IGCT and diodes for the 9L C^3S inverter*

The total power of the converter is, at the considered operating point, 5.5$[MVA]$. Summing up the values of Table 3.7 for a complete inverter (3 phases and 1 PEBB), the total loss power $P_{loss} = 34'915[W]$. The efficiency is therefore 99.36% considering only the losses in the semiconductors.

5L ANPC

To give a comparison, the losses of the 5L ANPC topology at 4kHz are calculated. From the benchmarking of the CCIL in the previous chapter, §2.6, it is defined that the 5L ANPC waveform is close to complying to the standards at 4kHz switching frequency.

IGCT stage [50Hz]			**IGBT stage** [4kHz]		
	$\overline{I_T}$ [A]	$\overline{I_d}$ [A]		$\overline{I_T}$ [A]	$\overline{I_d}$ [A]
T_1	288	0	T_5	288	119
T_2	119	0	T_6	285	119
T_3	119	0	T_7	286	118
T_4	285	0	T_8	287	120

Table 3.8.: *Average IGBT, IGCT and diode currents for the 5L ANPC inverter*

The losses are reported in Table 3.9:

The details of the calculation are the same as previously. The total dissipated power is $P_{loss} = 45'288[W]$, resulting in an efficiency of 99.18%.

The global value of the efficiency is not much different between the C^3S and the ANPC, but in reality there is a difference in dissipation of almost 23% or 10kW.

	$P_{loss_{sw}}$ [W]	$P_{loss_{cond}}$ [W]	$P_{loss_{rec}}$ [W]
IGCT stage total losses	320	2780	0
IGBT stage total losses	2880	3655	5440

Table 3.9.: *Conduction, switching and reverse recovery losses for IGBT, IGCT and diodes for the 5L ANPC inverter*

3.6.4. 9L case study

From the previous comparisons, and taking into account the modulation index limitation, it is interesting to see what sort of advantages the CCCS topology really offers compared to existing solutions. In this subsection, a case study is proposed, and a comparison is done between several 9L VSI.

All the main characteristics highlighted previously are taken into account. The considered topologies are the following : a 9L flying capacitor converter, a 9L CCIL double capacitor, a 9L hybrid ANPC-H-Bridge single capacitor (see §2.6.2) and a 9L [4;2;1] C^3S converter.

The comparison assumes identical complete 3 phase converters with the same power ratings, switching frequencies and a 10% capacitor voltage ripple on all the capacitors of the topology. The topologies are tuned to offer the same maximum active output power. The comparison does not consider any eventual increase of the capacitors energy to compensate common mode stabilization issues.

9L flying capacitor The flying capacitor topology is a redundant state topology allowing to balance all the capacitors within the structure. Is allows to reach maximum modulation index whatever the power factor. From the point of view of electrical characteristics, it is situated at the other end of the optimization curve, with the lowest total blocking voltage and the highest stored energy (in a general consideration).

9L SMC The stacked multi-cell topology is a variation of the flying capacitor. By paralleling the stages, it is possible reduce the number of capacitors. Because of increased redundancies, it is also possible to reduce the stored energy, since the current flows during less time in the capacitors. On the other hand, there is an increase in the blocking voltage requirements of the converter.

9L double capacitor CCIL The double capacitor CCIL is a redundant state topology. It also allows to balance all the capacitors at any modulation index and power factor.

9L hybrid ANPC-H-Bridge This topology was found to require a little bit less total blocking voltage and individual components compared to the 9L single capacitor CCIL topology (§2.6.2). Since it is able to boost the voltage, the DC-link can be reduced a little bit for the same output power ratings.

9L [4;2;1] CCCS This is the topology studied in this chapter. Besides the fact that the modulation index is limited for the 9L operation, the topology can offer 5L operation with the same power ratings. For this reason, the topology does not require extra voltage on the DC-link to withstand disturbances.

The results of the comparison are presented in Table 3.10. The smallest stored energy is offered by the hybrid 9L inverter and the SMC. It is about 30% less then the 9L CCCS and as much as 4 times less than the 9L flying capacitor. In general, the cross connected topologies require fewer capacitors (in terms of components) compared to SMC and flying capacitor. So even though the SMC has a similar stored energy then the hybrid topology, it requires more components. The SMC solution actually offers a interesting trade-off between number of components and controllability, in the same way as the redundant and non redundant CCIL.

Regarding the number of individual switches, the 9L hybrid and the 9L CCCS are equal and have basically 20 to 30% less components compared to the other topolgies.

The smallest total blocking voltage is the 9L flying capacitor. It is less then half of any other topologies except the SMC. The 9L CCCS is an average solution offering lower stored energy compared to the other cross connected solutions, reduced number of components, but a higher blocking voltage requirement. The power delivered by the topology is slightly lower, under nominal operating conditions, compared to the 4 other topologies, but for reactive power or disturbance rejection (in 5L mode), the 9L CCCS can deliver the same maximum output power.

The specific aspects of the different topologies do not appear here. For instance, the switching losses of the CCIL and hybrid topologies might be higher than the CCCS, because fundamental switching is not ensured, at the moment, on the high voltage stage.

As well, the C^3S harmonic distortion performances are higher then the 9L CCIL, with the proposed modulation and control algorithms.

	9L Flying cap	9L CCIL 2 caps	9L hybrid 1 cap	9L CCCS	9L SMC
DC-link voltage	1x6400V	2x3200V	2x4000V	2x3200V	2x3200V
Output current	900A	900A	900A	900A	900A
Modulation index at nominal operation	1	1	0.8	0.9	1
Nominal output power	6.1MW	6.1MW	6.1 MW	5.5MW	6.1MW
Maximum modulation index at active power	1.15	1.15	0.91	1.15 (5L)	1.15
Maximum active output power	7MW	7MW	7MW	7MW (5L)	7MW
Maximum modulation index at reactive power	1.15	1.15	1.15	1.15	1.15
Maximum reactive output power	7MVA	7MVA	8.8MVA	7MVA	7MVA
Number of individual switches	48	42	30	30	36
Total blocking voltage	33.6kV	72kV	88kV	73.6kV	38.4kV
Number of capacitors	24	6	3	4	12
Total stored energy in capacitors	35kJ	16.2kJ	9kJ	12.6kJ	9kJ

Table 3.10.: *Comparison of the 9L flying cap, 9L double capacitor CCIL, 9L hybrid ANPC-H-Bridge 9L CCCS and 9L SMC converter topologies characteristics*

3.7. Conclusions

The Common Cross Connected Stage PEBB is a completely new approach to the design of multilevel inverters. The stage is common to the three phases of a multilevel inverter based on a 3 level DC-link. In general, it can be connected to all kind of inverters, but it is studied together with the ANPC topology, since the focus of this work is based on the 5L ANPC topology.

The C^3S allows the converter to which it is associated to generate a large number of output levels. The properties of the topology are studied in details. The aspects covered by the work are the description of the general topology, the electrical characteristics, the modeling, done based on a graphical space phasor representation, and the development of a control and modulation strategy.

A 9L realization of the CCCS topology is proposed, which is well suited for the 5L initial topology. The theoretical limits are defined, based on the model. Then a modulator is implemented in Matlab and tested. The simulation results show that the maximum modulation index reachable at active power in simulation, $m = 0.925$, is close to the theoretical limit of $m = 0.958$ defined with the help of the graphical model.

The modulation index limitation can be overcome by switching the inverter back to a 5L operation. This allows the reach the maximum modulation index and so, cover transients and disturbances when necessary.

Not only does the modulator stabilize the capacitors of the circuit, it also gives higher output signal quality compared to the previously developed CCIL topology. The generated waveforms present excellent harmonic contents, showing that the topology is likely to offer a filterless grid configuration, while complying with the VDEW standards.

Upgrading the 5L ANPC topology is very straightforward. Besides plugging in the CCCS PEBB, it requires on increase in the blocking capability of some switches within the topology. Besides this, the mechanical layout is likely to be significantly simplified, as the 5L ANPC design can be kept almost unmodified. The connection point of the PEBB being close to the DC-link, the design of the converter is likely not to be disturbed by the integration of the PEBB.

Benchmarking and comparison of the CCCS topology to the other existing topologies shows that every solution has its own advantages. It cannot be said that the CCCS is a revolutionary topology overcoming all the problems of the other solutions. It does not either offer a solution for the large blocking voltage requirement of the CCIL. But is does have its own advantages, it is a modular and reliable solution to extend the 5L ANPC topology.

In the specific case of the 9L topologies, the CCCS solution does have some advantages compared to the other solutions, if the target is to obtain a converter with low number of components.

For all the above mentioned reasons, and also because the CCCS PEBB is, from the perspective of power electronics, a very interesting topology, suited for industrial application. It is notably able to answer the initial target of the work which is the development of an upgrade for the 5L ANPC

allowing a filterless grid connection while keeping high reliability and high power density.

CHAPTER 4

CCCS Experimental Setup

4.1. From the PEBB concept to the realization

4.1.1. Existing system

One of the characteristics of the CCCS PEBB is that it is, as it's name tells, a Power Electronics Building Block. It is inherently built as a module which can be plugged in an existing system with only minor modifications. From the point of view of the electrical connections, the implementation of the PEBB on an existing system is very straightforward. On the other hand, actually adapting an existing system, not initially designed to be used with the PEBB, can be tricky, especially when the system is based on PCB design.

In this section it is discussed how the PEBB is adapted to the existing 5L ANPC prototype that is used as a base for the prototyping. This 5L ANPC prototype was built at the ETHZ for 2 PhD works (Leonardo Serpa, ETHZ and Christoph Haederli, LEEI-INP Toulouse) and is actually intended to be used with the ABB AC 800PEC DSP based control system (or any control board able to issue optical gate signals). Because of the rather complex control scheme and because the system was available, the AC 800PEC controller was retained.

Before entering further details and to give a brief overview, the main components to be found on the 5L prototype, represented on Figure 4.1, are the neutral point and DC-link current sensors, the phase capacitors, the IGBTs mounted on the heatsink and the optical interface for the gate

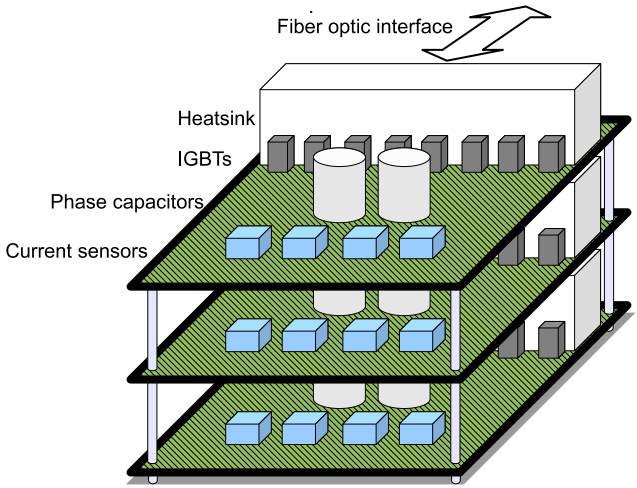


Figure 4.1.: *Overview of the existing 5L ANPC prototype before modification to add the CCCS PEBB*

signals (when controlled by the PEC800). The other components (gate drivers, sensors, supplies) are not discussed here since they do not require any modification.

The interesting aspect of this 5L ANPC prototype is that the current sensors measuring the neutral point currents are situated exactly at the interconnection points where the C^3S PEBB is normally connected (there are 3 sensors measuring the total and per branch neutral point current of each phase), Figure 4.2. As these measurements are not necessary for the C^3S setup, they are removed and the PEBB is connected instead.

The design of the C^3S PEBB PCB, the interconnection and the mechanical layout from the board to the existing converter, the simulation of the switched behavior with regards to the parasitic components due to the unsymmetrical PEBB interconnection to the phases, and the commissioning and testing are part of Frederic Mermod's master thesis [53].

The IGBTs of the existing prototype are $1200V$, $30A$ rated (Ixys) and the phase capacitors are $1mF$. Due to previous design specifications, the gate resistors are 68Ω leading to an almost $1\mu s$ rise time ($0 - 800V$). The slow rise times imply high switching losses and limited switching frequency, but are beneficial in limiting the overvoltages during commutation, due to the stray inductances of the connection to the PEBB (see §3.2.5).

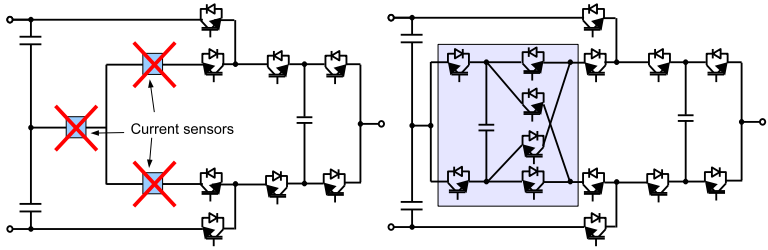


Figure 4.2.: *The neutral point current sensors can be removed to connect the CCCS PEBB*

4.1.2. 9L Common Cross Connected Stage prototype

Design

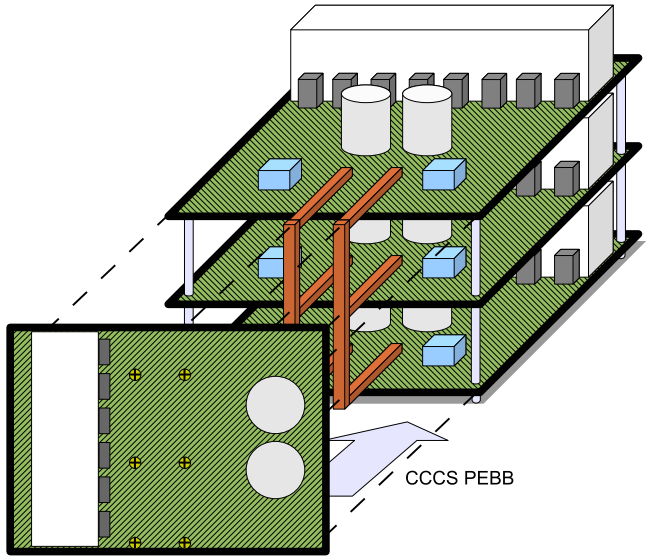


Figure 4.3.: *Overview of the 5L ANPC prototype with the CCCS PEBB connection*

The 9L C^3S prototype is designed as a lateral PCB board which is electrically connected by means of bus bars to the position where the neutral point current sensors were situated, Figure 4.3. One of the design criteria is to minimize the stray inductances of the interconnection of the PEBB to each of the three phases while trying to keep them as symmetrical as possible. Inherently, the PEBB is always closer to one phase than it is to the 2 others.

Besides the layout and mechanical design, the circuit design of the PEBB (choice of IGBTs, gate drivers, etc) is simplified as it is based on the existing prototype schematics.

The PEBB capacitor is $2.4mF$. The switching frequency of the overall system is the same as for the simulations, namely between 1.5 and $2kHz$. The parasitic inductances are estimated with a simple rule of thumb: $L_\sigma = 10nH/cm$.

Simulation

The influence of the switching frequency, the IGBT rise and fall times, and the overall design are assessed in simulation. The simulation is done using Simetrix, which is a PSpice based simulator. The retained IGBT model is not for the exact component but a close model in terms of characteristics was chosen. For more details, see [53].

Simulations are run for varieties of commutations in order to assess the dynamical behavior and the influence of the different stray inductances between the phases and the PEBB. It is seen in simulation, that ought to the commutations speeds, the stray components do not affect the commutations.

Some typical commutation sequences are defined, and the simulated output sequences are compared to the real system's outputs. The comparison between the simulation and the measured outputs are used to verify the prototype.

Figure 4.4 shows, for one switching sequence, the correlation between simulations and prototype results. It is seen that the signals are well correlated, thus validating the hardware implementation of the PEBB.

4.2. Modulator

4.2.1. Control hardware

General overview

As already mentioned, the retained control platform is the ABB AC 800PEC (Power Electronics Controller) DSP based controller [54]. From

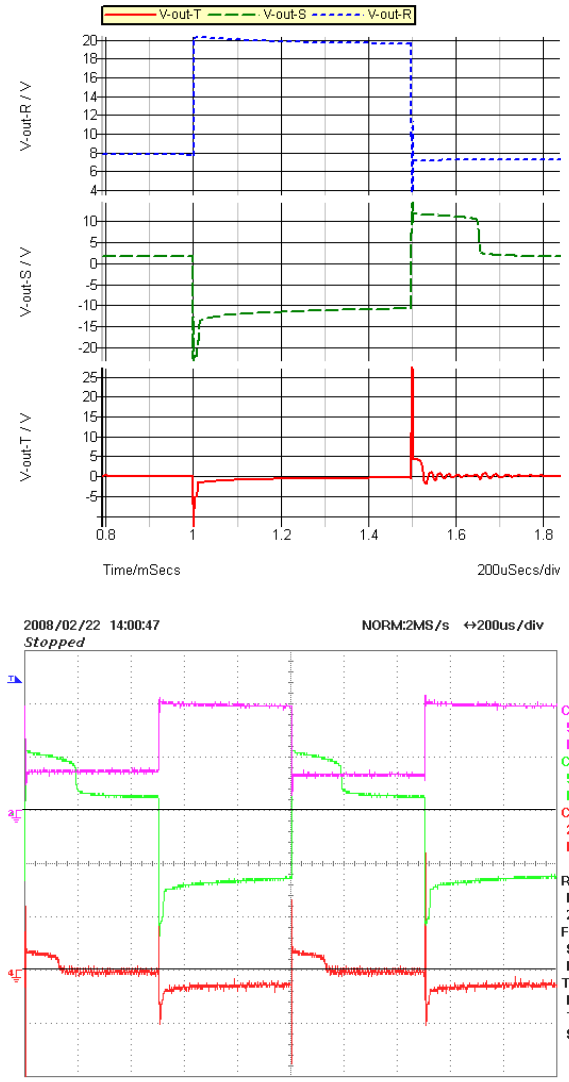


Figure 4.4.: *Complete repetitive commutations of the 3 phases and the PEBB. Simulation results.*

a purely functional point of view, it is an oversized control platform for a low voltage lab prototype. On the other hand, it offers a very flexible and powerful solution for the development of experimental control programs and softwares.

The system is highly modular, as it allows to connect, among others, via a fiber optical interface various measurement interface boards (PECMI boards) for low or high voltage/current sensing.

It is connected to the control PC via an Ethernet connection, from which both, the VHDL and OpCode softwares are downloaded These software layers are discussed in greater details in the coming section. An RS-232 interface is also available for telnet connection and advanced debugging or crash recovery.

Hardware

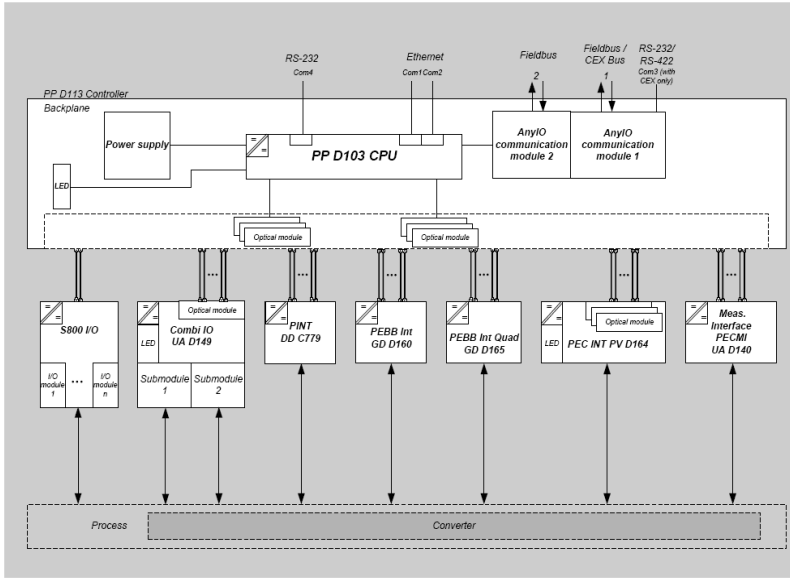


Figure 4.5.: *AC 800PEC: Topology (Source [54])*

The processor module is a IBM PowerPC 750FX running at $400MHz$. It is a 64 bit floating point microprocessor unit with 2x32k byte L1-cache

and 512k byte L2-cache. Besides the main microprocessor, there is a VirtexII FPGA running at $40MHz$. These high-end FPGAs from Xilinx come with dedicated 18x18 byte multipliers and DPRAMs (Dual-Port RAM). The FPGA looks after all the high speed tasks like fault handling, measurements, generation of interrupts for the CPU, optical communication, etc.

The AC 800PEC has up to 6 optical I/O modules for communication with various extension boards, like PECMI boards for measurements, PECINT boards for additional fiber optic links, Combi I/O boards for general purpose inputs/outputs links, etc. These optical links are also used to send the gate signals generated by the modulator.

The general overview of the hardware topology is presented on Figure 4.5. The configuration of the prototype controller included 2 PECMI boards for voltage and current sensing. No additional boards are necessary at this point. The measured values are the 3 phase to phase output voltages, the 3 output currents, the 3 phase capacitor voltages and the PEBB capacitor voltage.

The sampling time for the measurements, including communication between the PECMI and the controller, is $25\mu s$. There is a high-speed communication interface called UltraLink for fast short circuit detection ($< 2\mu s$). The signals are emitted by the PECMI boards. In this case, all the voltages are measured, but sliding mode observers can be applied to reduce the number of sensors necessary, for instance see [55], [56].

Additionally, the gate feedback signals can be read directly from the gate drivers and handled within the FPGA program for IGBT desaturation detection.

Software

As already mentioned, the control software is typically split into 3 levels. The very high speed control tasks ($25ns - 100\mu s$), handled by the FPGA, the fast control tasks ($100\mu s - 5ms$), handled by the microprocessor within a Matlab Simulink program (called OpCode), and a much slower, plant level, control ($> 5ms$).

The C^3S PEBB only requires the very fast and fast control tasks, since the prototype is not included in any sort of plant. The main modulator program (described in §3.4), responsible for output voltage waveform generation and capacitor balancing, is programmed in VHDL and executed in the FPGA. The control part of the program (generation of the space phasors reference, closed loop current control and PLL) are programmed in OpCode. However, the classical control tasks are not necessary for the val-

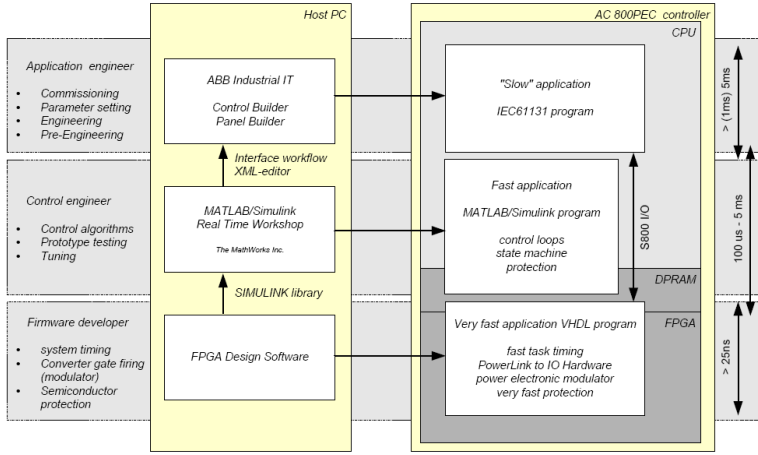


Figure 4.6.: *AC 800PEC: 3 level software block diagram (Source [54])*

idation of the topology. The main focus is given on the VHDL modulator program.

The program running on the FPGA must handle PCI communication to the DSP, interrupt generation, measurements from the PECMI boards, DPRAM, watchdog, clock generation, fast short circuit detection, etc. Most of the basic functionalities are delivered as native with the controller. Besides the FPGA core program, the modulator specific software must be implemented. The whole FPGA program is written in VHDL.

The program running on the DSP is a compiled C-program generated with the Matlab Simulink Realtime Workshop. The OpCode toolbox is used to design the Simulink program for the PEC800. The program is split into 3 different tasks, corresponding each to 3 different execution speeds. The Task A is the fastest task. It is triggered with a maximum speed of $25\mu s$. The task B is then a multiple of the task A and the task C is a multiple of the task B. This allows to split the program into time critical instances which are then executed with different priorities and speeds. In general, the base OpCode program contain regulation and control tasks. For the CCCS prototype, besides the carrier and the corresponding space phasor generation, the OpCode program does not execute any specific algorithm, since there is no current control or grid connection. The control and reference values are sent to the VHDL code from the OpCode layer.

This allows to user to change some critical values during operation, like for instance dead times, reset signals, nominal values, etc.

4.2.2. VHDL modulator program

General code structure

The modulator algorithm is described in details in §3.4. The specific issues linked to the VHDL programing and implementation are not discussed here, but a general overview of the program structure is given, Figure 4.7.

The general state machine is the VHDL instance which triggers all the other instances depending on the system status. The details of the state machine are discussed later in this subsection.

When the state machine is in the "normal running state", the program must execute, in a repetitive manner, the modulation tasks. The main functionality is to provide undistorted output voltages. Additionally, the modulator must make sure the capacitors are balanced.

Since the references are calculated by the OpCode program, the VHDL code must be synchronized with the OpCode, and this is done using the interrupt signals. The OpCode calculation time can be estimated (by some external monitoring program) since converting the three references to phasors is a repetitive task that always takes more or less the same execution time. The interrupt signal is caught by the modulator and used to trigger a counter (ok_to_start signal) which is designed to match the OpCode execution time, plus some margins, Figure 4.8.

Once the counter has underflowed, the synchronization signal (sync_sig) is issued. The switching state calculator instances (one per phasor) read the fresh reference values calculated by the OpCode layer and written in the DPRAM, and calculate the correct gate signals following the specific modulation algorithm for the CCCS inverter (more later).

Because the 3 switching state calculator instances may require different computational times, a trigger is necessary to synchronize the 3 instances with the rest of the VHDL program. When the 3 instances have finished calculating their outputs, the sequence generator is triggered (trigger_seq_gen). The role of the sequence generator is to apply the 3 phasors (i.e. the corresponding gates signals) with the correct given time to the output, following the optimized strategy described in §3.4.2.

The gate signals, issued from the sequence generator at given times and for given durations, are sent to the transition execution instances which are responsible for executing the transition in a proper way and with the correct dead times (more details are also given later).

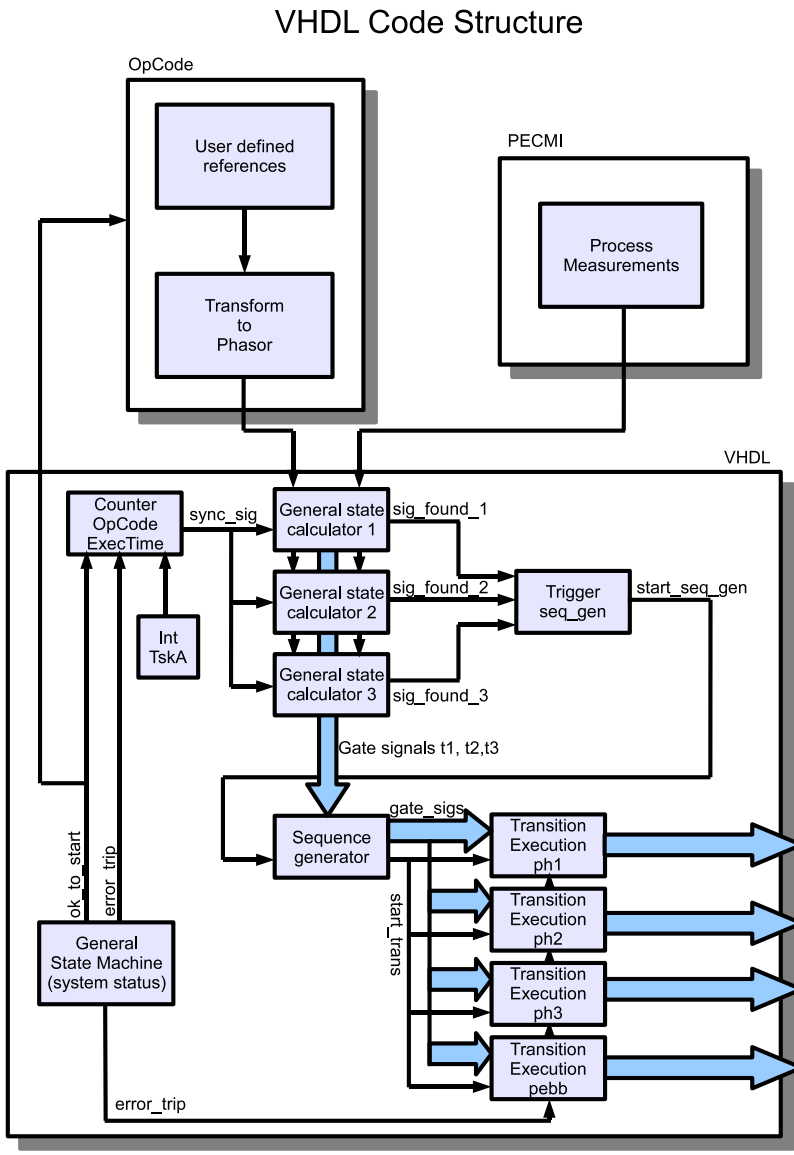


Figure 4.7.: *VHDL general code structure*

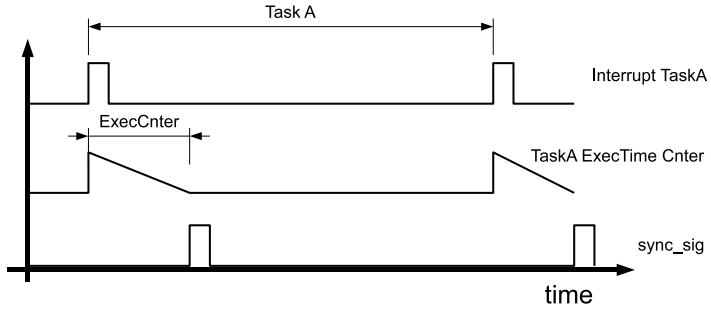


Figure 4.8.: *Timing diagram: OpCode execution time counter*

Finally, it must be noted that the general state machine can generate at any time an error trip signal, which will then result in a turn off of all the switches, whatever the state of the converter is.

General state machine

The general state machine has 7 different states. Just after startup, the state machine is in the initial state. In this state, all gate signals are zero.

The user must then issue a "start preload" command which will drive the state machine into the corresponding state. In the preload state, the modulator turns on the switches such as to connect the PEBB, phase and DC-link capacitors in parallel. Of course they should be discharged before doing so. The DC-link voltage is then ramped up progressively from 0 to the nominal voltage. When the PEBB capacitor reaches its own nominal voltage ($\frac{1}{4}$ of the nominal DC-link voltage), the modulator switches the correct gate signals off so as to disconnect the PEBB capacitor from the rest of the circuit. The same is done for the 3 phase capacitors.

When all the capacitors are loaded to their nominal voltages, the state machine enters the "ready to start" state. It stays there until the order is issued to start up the converter, or until one of the capacitors gets too much discharged.

When the "conv_start" signal is issued, the state machine enters the "normal running state". In this state, the VHDL modulator and the OpCode program are triggered and start immediately calculating the correct output signals.

In the normal running state, 2 things can happen. A fault or a shut down request. In both cases, the appropriate sequence must be applied to

the output. In both cases as well, when the system is fully down (i.e. caps discharged, switches turned off, etc), the state machine can again enter initial state and be ready for a new startup.

In the case of an emergency shutdown, the system cannot be restarted unless the trip error signal is reset. This avoids turning on the system when a failure is still present.

Transition execution

The transition execution instance is responsible for applying the correct transitions and dead times during the switching of one state to the other. The transition happens in several steps. First the outer IGBTs and the PEBB IGBTs are commuted and then, the inner IGBTs (IGCTs in the full scale setup) are commuted. This is in order to avoid transient problems due to the different rise and fall times in case of a hybrid IGBT/IGCT structure. On the prototype, there are only IGBTs, but the transition strategy is kept the same to get a better idea of what will happen on a full scale system. There are 2 dead times and 1 minimum on time defined.

The transition execution structure presented here cannot avoid spikes during the transitions. These are due to partially non controlled freewheeling paths. It can happen that during a transition, the freewheeling current starts to circulate via the upper or lower DC-link, inducing, during the dead time duration, a spike at $\pm U_{DC}$ or some other intermediate level. As an example, a possible commutation from level $+U_p$ to level $-U_p$ at negative current is presented, Figure 4.10.

With the 2 step commutation introduced previously, the outer IGBTs and the PEBB IGBTs are first turned off. During the dead time, the current starts to flow in the upper IGBTs S21 and S31, inducing the level $U_{DC} - U_{cf}$ at the output. This unwanted level is the result of an uncontrolled freewheeling path. After the dead time, the complementary IGBTs are turned on and the inner IGBTs are turned off. During this dead time, the freewheeling path remains unchanged. Finally, once the complementary inner IGBTs are turned on, the correct switching state is achieved and the output level is $-U_p$.

The uncontrolled freewheeling path problem can be partially solved by implementing a more complicated transition execution algorithm. All the transitions should be analyzed for both current signs, and the adequate sequence can then be applied to minimize the effect of the transient levels. But for the sake of simplicity, in here only the basic transition execution instance is implemented, since only the global behavior is of interest for the prototype.

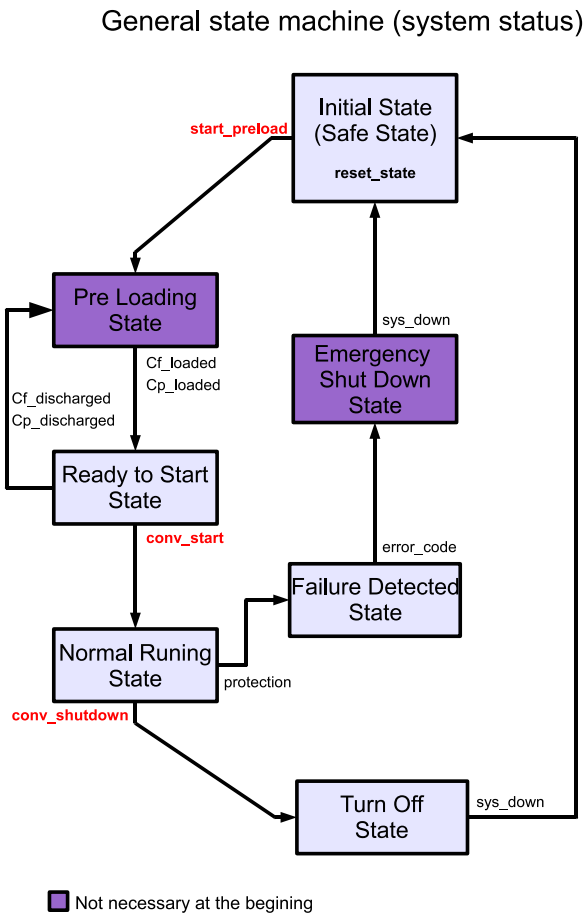


Figure 4.9.: *VHDL code: General state machine. The conditions in red are user issued commands, while the conditions in black are system commands.*

Modulator core VHDL program

Without entering the programing details, some information is given here concerning the general structure of the core code. Information about measured execution time and complexity are also discussed.

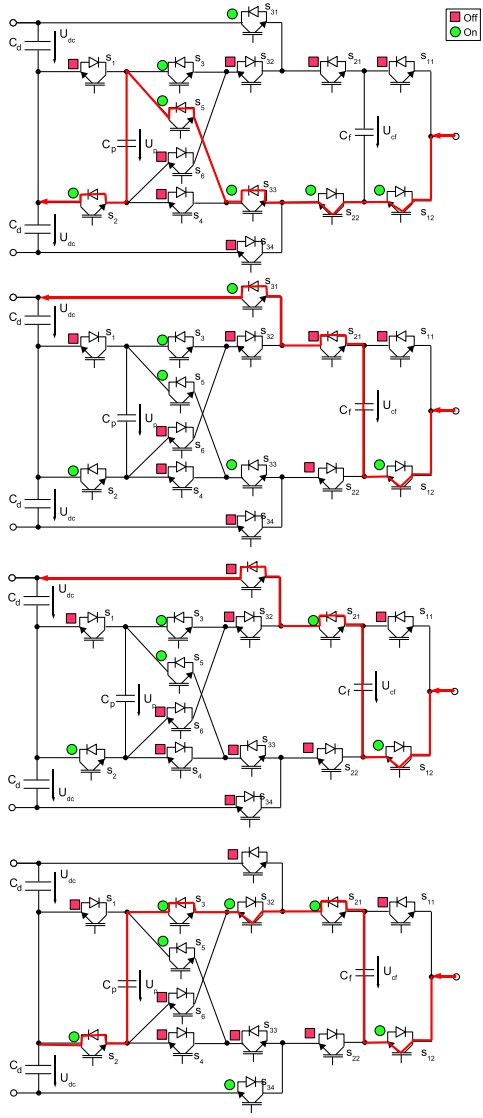


Figure 4.10.: *Example of a commutation, from $+U_p$ to $-U_p$ at negative current, leading to an unwanted transient output level*

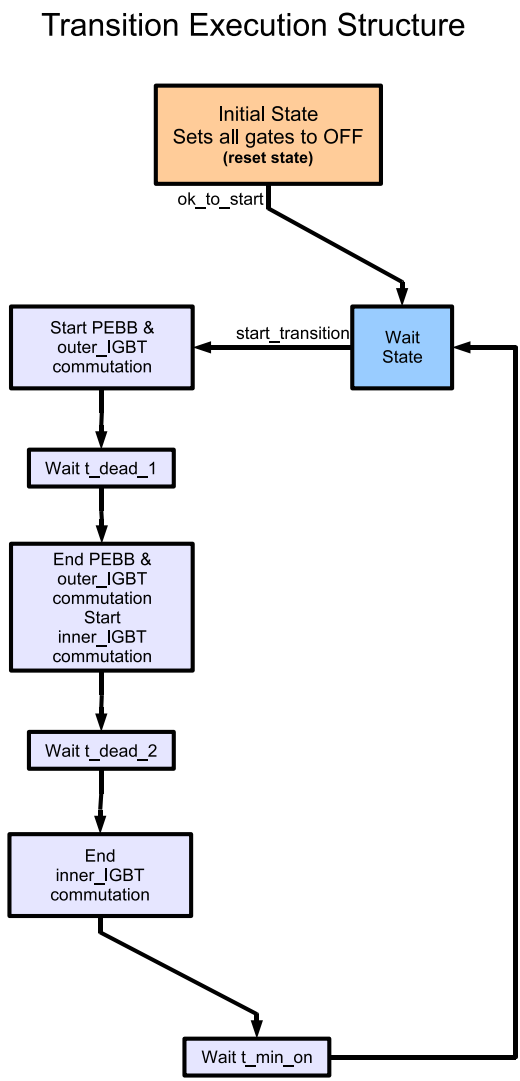


Figure 4.11.: *VHDL code: Transition execution*

The main modulator instance is the biggest VHDL file contained in the FPGA (about 10'000 lines). It is split into 5 different parts executed subsequently and which are briefly discussed here.

First the capacitor priorities are calculated, such as described in §3.4. Then, the reference phasors is searched in a table referencing all possible phasors. This is a large table containing information about the switching states and corresponding output levels, the effects on the capacitors (phase and PEBB) and the possible PEBB states. Because the table must be searched sequentially to look for all the matching phasors, it is split into 6 parts, containing each 120 entries.

When the phasors corresponding to the reference are found in the tables, the informations about the switching states and the effect on the capacitors are stored into 7 stacks, representing each one PEBB state. The next step is then to calculate the optimal score for each PEBB state. This is done by reading all the entries of the stack and calculating the score of the PEBB and phase capacitors (eq.(3.43) and eq.(3.44), §3.4.2). Only the highest score for each PEBB state is kept.

Finally, the highest score among all the PEBB states is chosen and the corresponding switching state for the 3 phases and the PEBB (gate signals) are sent to the output. It should be noted that in this version of the modulator, the switching losses are not included in the score calculation. This can be done in a further revision of the program.

The general structure of the program is represented on Figure 3.26 of §3.4.

The average execution time of the modulator instance is between $7-8\mu s$. The most time consuming part is the sequential search in the lookup tables. It takes one clock cycle for each entry to be read and compared, and there are 120 entries each time. The program could certainly be further optimized on this point, but this is not necessary at this point.

Finally, it can be mentioned that the Xilinx System Generator Toolbox for Matlab Simulink was used to test the modulator. This toolbox allows to implement and simulate a VHDL code within the Simulink environment. It is then possible to simulate the VHDL modulator with a Plecs circuit and a Simulink regulator, which is a very effective way to test the program. The main drawback of this solution is the really slow simulation speed (30min for 20ms, on a Intel Xeon 3.6GHz system with 3Gb RAM memory).

4.2.3. OpCode program

The OpCode layer of the program is responsible for the slower tasks ($25\mu s$ and more). Since the main modulator core is implemented in VHDL, only a small part is coded in OpCode.

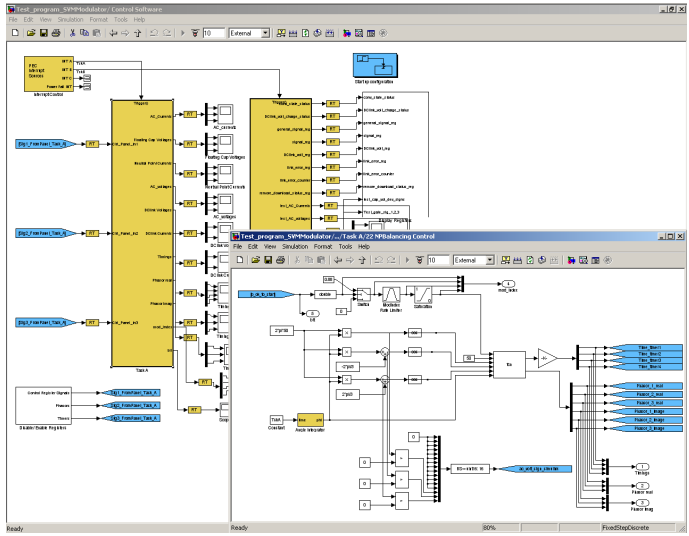


Figure 4.12.: *OpCode program: the main program window and the pre-modulator windows with the embedded m-function*

The 3 phase to phasor transformation of the reference value, and the calculation of the 3 enclosing discrete phasors, is done via an embedded M-function in task A of the OpCode program. It takes roughly $50\mu s$ to execute.

In the case of a grid connection, it would be necessary to add to the OpCode program a PLL and a current controller. But since the first step is the validation of the concept and of the topology, the converter is connected to a passive RL load and not to the grid. Thus control and synchronization with the grid are not necessary.

4.3. Test setup

4.3.1. General setup and protection

The supply of the inverter is done using a series connection of 2 voltage sources, since the neutral point balancing issue is not assessed or discussed (§3.3.6).

The user protection is an essential part of the setup. A bumper button controls the emergency shut down of the setup. When the converter is

shutdown, the button is bumped. In this configuration, the converter is isolated from the supply and all the capacitors are connected to discharge resistors. These resistors are designed to burn the capacitors' energy within a few milliseconds.

In normal running state, the bumper is in open position and the relay is therefore turned on. This connects the DC supply to the setup and the discharge resistors are disconnected. In case of emergency or after normal shutdown, bumping provides an isolation from the source and discharges the capacitors.

Additionally to the bumper, there is an optical control coming from the controller which also allows to emergency shut down the system upon software fault detection.

The load is composed of a 47Ω resistor and a $2.4mH$ inductor. The inductor is used only to filter the current which else would be an image of the voltage. The load resistor is chosen as a function of the DC-link voltage and the power capabilities of the voltage sources. In this case, a 5A limitation of the voltage sources drove the choice of the resistors.

4.3.2. Measurement results

Waveforms

This section presents the main results obtained from the prototype. The DC-link voltage is 48V per capacitor (96V total DC-link voltage). The phase capacitor voltages are 24V and the PEBB capacitor voltage is 12V. The output current is 4A. The most limiting factor preventing to push up the voltage and current of the setup were the available voltage sources in the lab.

Figure 4.14 shows for one grid period, in purple the line to line voltage between the phases 1 and 2, in green the output current of the phase 1, in blue the phase capacitor voltage of the phase 1 and in red the PEBB capacitor voltage, for a modulation index of $m = 0.88$. The multilevel pattern of the voltage can be clearly seen, and the current waveforms presents a descent ripple (which is of course depending on the load inductor). From this figure it is however not so very clearly seen how the phase and PEBB capacitor balancing is performing.

The spikes appearing on the line to line voltage are due to freewheeling paths connecting the output to some intermediate levels during the commutation dead times. The phenomenon is explained in details in §4.2.2.

Figure 4.15 shows additionally the pole voltage. The 9 levels can be identified, but the capacitor ripples make them harder to identify.

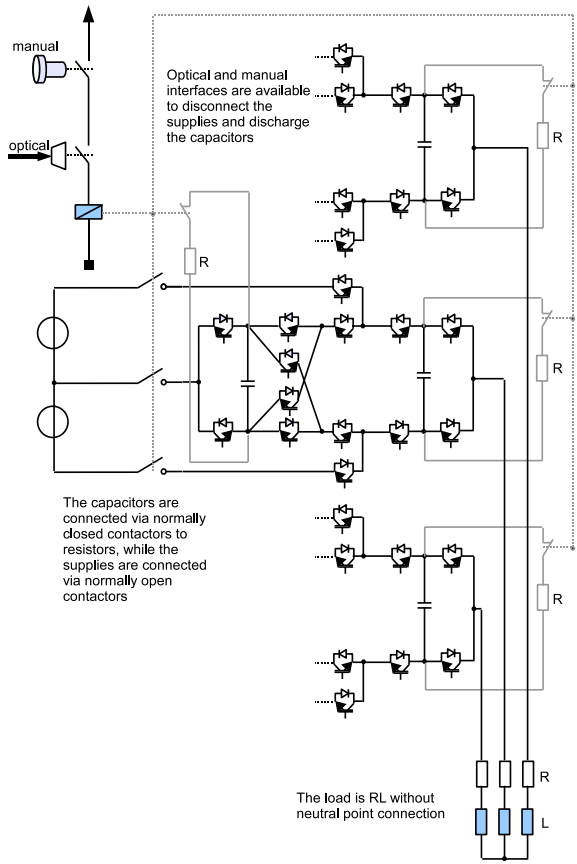


Figure 4.13.: *Test setup: protection, supply and load*

A longer capture of the same values is shown on Figure 4.16. The capacitor voltage ripples are more clearly visible. It can be seen that the PEBB capacitor voltage ripple is very small, and that the phase voltge capacitor ripple contains a $2f$ component.

Figure 4.17 shows what is the result with a modulation index of $m = 1.05$. The PEBB capacitor voltage is 0 since it cannot be controlled anymore at this modulation index. The phase capacitor voltage cannot be kept at it's nominal value of 24V, but stabilizes somewhere around 12V. With an

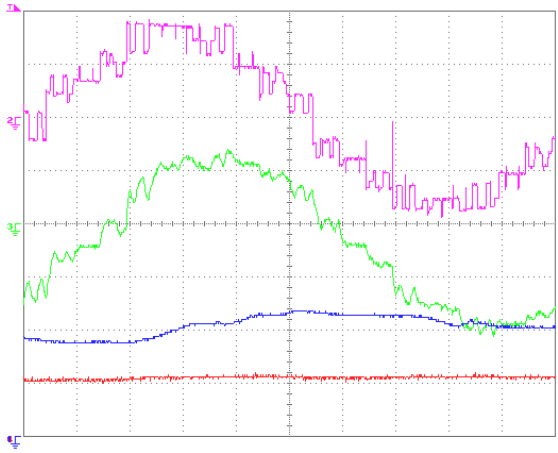


Figure 4.14.: *X-axis: time [2ms/div]. Y-axis: 1-Blue: Phase 1 capacitor voltage [10V/div]. 2-Purple: Line to line voltage [40V/div]. 3-Green: Output current phase 1[4A/div]. 4-Red: PEBB capacitor voltage [10V/div].*

appropriate modulation scheme the inverter would have been able to run in a 5L mode.

The control strategy, for going from a 9L to a 5L mode for increased modulation index operation, requires to be able to bring back the PEBB capacitor voltage from 0 to its nominal value during operation.

Figure 4.18 shows the behavior of the system at startup with discharged capacitors: The modulation index is ramped up to $m = 0.88$. It can be seen that the phase capacitors are brought to their nominal value within roughly $60ms$, and that the PEBB capacitor requires $300ms$.

The capacitor voltages rise time is shorter for lower modulation indexes. This is however a sufficient indication that even during operation at high modulation indexes, with a discharged PEBB capacitor, it is possible to resume nominal 9L operation when the modulation index is brought back to a range where the PEBB capacitor can be stabilized.

The two last Figures 4.19 and 4.20 show the capacitor ripple alone. This illustrates that the three phase capacitors and the PEBB are well balanced, and that there is a 120° symmetry between the three phase capacitors, as suggested by the graphical model. The ripple amplitude on the phase

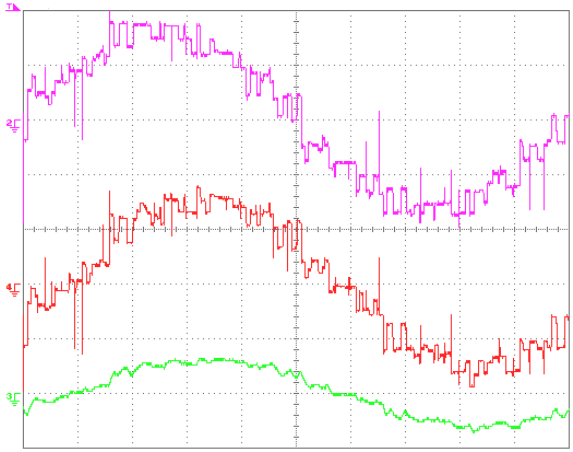


Figure 4.15.: *X-axis: time [2ms/div]. Y-axis: 1-Purple: Line to line voltage [40V/div]. 2-Green: Output current phase 1[4A/div]. 3-Red: Phase 1 pole voltage [20V/div].*

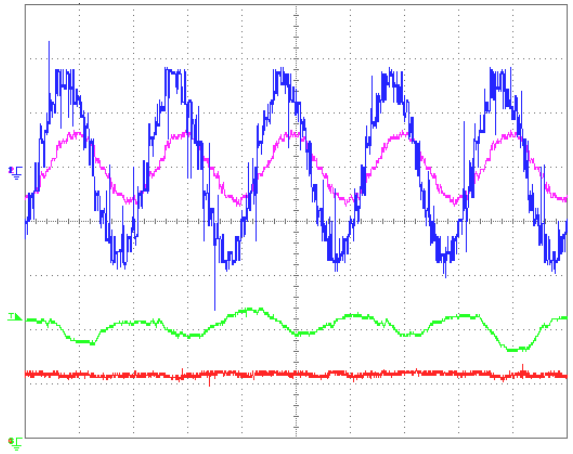


Figure 4.16.: *X-axis: time [10ms/div]. Y-axis: 1-Blue: Line to line voltage [40V/div]. 2-Purple: Output current phase 1[10A/div]. 3-Green: Phase 1 capacitor voltage [10V/div]. 4-Red: PEBB capacitor voltage [10V/div].*

capacitors equals roughly 15%, while the PEBB capacitor ripple is about 5-10%.

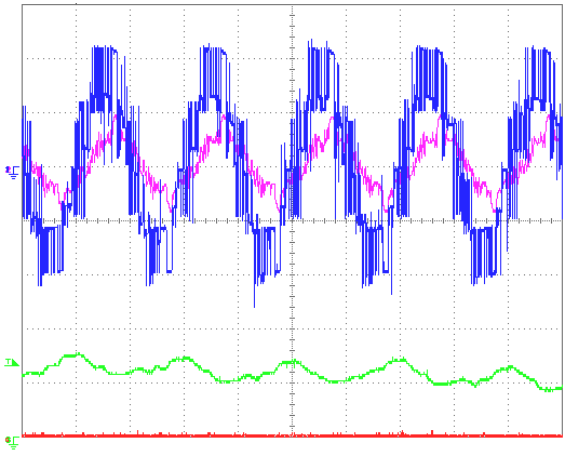


Figure 4.17.: *X-axis: time [10ms/div]. Y-axis: 1-Blue: Line to line voltage [40V/div]. 2-Purple: Output current phase 1[10A/div]. 3-Green: Phase 1 capacitor voltage [10V/div]. 4-Red: PEBB capacitor voltage [10V/div].*

4.3.3. Findings

Capacitor ripple amplitudes

The energy stored in the phase capacitors of the prototype is $288mJ$ and in the PEBB $173mJ$. The energy in the phase and PEBB capacitors of the simulated medium voltage design are respectively $2560J$ and $1920J$. In order to be able to compare the ripples observed in simulation and in the prototype, a common base must be defined. The ripple amplitude in the capacitors is defined by:

$$i = \quad C \cdot \frac{dU}{dt} = \quad C \cdot \frac{\Delta U}{\Delta t} \tag{4.1}$$

The energy in the capacitors is given by:

$$E_C \quad = \quad \frac{1}{2} C \cdot U^2 \tag{4.2}$$

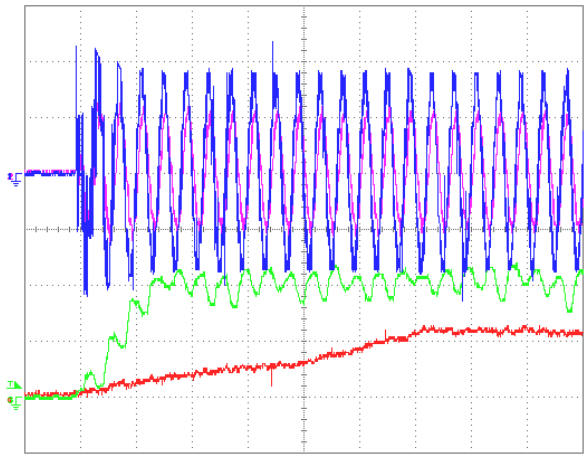


Figure 4.18.: *X-axis: time [50ms/div]. Y-axis: 1-Blue: Line to line voltage [40V/div]. 2-Purple: Output current phase 1[6A/div]. 3-Green: Phase 1 capacitor voltage [10V/div]. 4-Red: PEBB capacitor voltage [10V/div].*

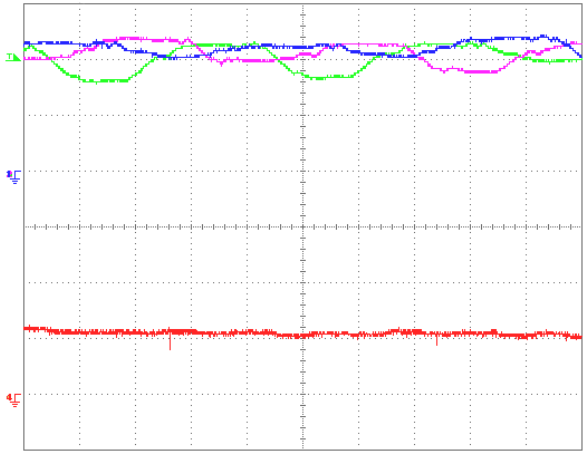


Figure 4.19.: *X-axis: time [5ms/div]. Y-axis: 1-Blue, 2-Purple and 3-Green: 3 phase capacitor voltages [10V/div]. 4-Red: PEBB capacitor voltage [10V/div].*

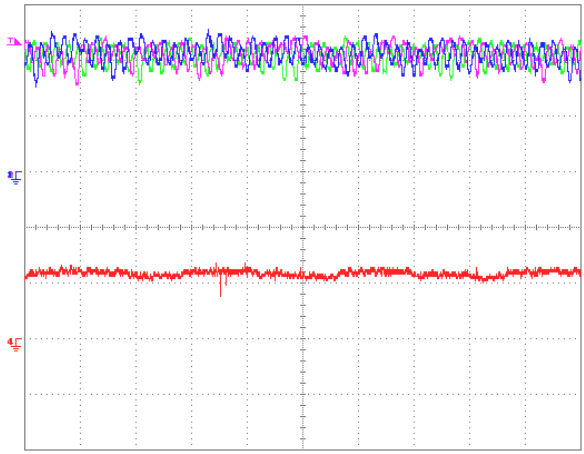


Figure 4.20.: *X-axis: time [100ms/div]. Y-axis: 1-Blue, 2-Purple and 3-Green: 3 phase capacitor voltages [10V/div]. 4-Red: PEBB capacitor voltage [10V/div].*

so combining the two equations gives:

$$E_C = \frac{1}{2}\frac{i \cdot \Delta t}{\Delta U} \cdot U^2 \tag{4.3}$$

Defining the voltage variation ΔU as $\eta \cdot U$:

$$\frac{E_C}{I \cdot U} = \frac{1}{2} \cdot \Delta t \cdot \frac{1}{\eta} = K \cdot \frac{1}{\eta} \tag{4.4}$$

The last equation says that the normalized capacitor energy over the converter power gives an inverse proportional value to the ripple amplitude η, since the factor K is constant and identical for both converters (same switching frequency).

The medium voltage design gives an energy over power ratio of 0.0018 and 0.0027 for the phase and PEBB capacitors. For the prototype, the ratios are 0.0030 and 0.0036 for the phase and PEBB capacitors respectively. Thus, the ripple ratio between the prototype and the simulation is 1.67 and 1.33 for the phase and PEBB capacitors respectively.

The measured ripple amplitude on the prototype is 15% on the phase, and 5−10% on the PEBB capacitors. In simulation, the amplitudes are 15% and 6%. Since the energy in the prototype is 1.3 and 1.7 times higher, and

the ripple have roughly the same amplitude, it can be directly concluded that the capacitor ripple amplitude on the prototype is 1.3 to 1.7 times larger than in simulations.

Differences in modulation indexes and in switching frequencies might be the cause of the differences observed here.

Modulation index

The maximum reachable modulation index on the setup is $m = 0.88$. This result is quite close to the simulation results and demonstrate the good correlation between simulation and real life. It seems here also that further optimization of the modulator can help to balance the capacitors at higher modulation indexes.

Additionally, the predicted behavior around modulation indexes $m = 0.77$, §3.5.1, can be clearly observed during prototyping. The control of the phase and PEBB capacitor voltages is quite smooth for all the modulation indexes, except for those around 0.75 to 0.78, for which the phase capacitors get harder to balance. This is an important result for validation of the graphical model.

Observed waveforms

A $2f$ ripple is appearing on the phase capacitors ripple and the PEBB capacitor ripple does not exhibit a 6th harmonic ripple as pronounced as in the simulations.

Recalling the graphical model results of §3.5.1, the observed waveforms can be explained. Concerning the low PEBB capacitor ripple, recalling the average phasor repartition for the PEBB capacitor, figure 3.33-top, the observed results are the result of the fact that, on average, the actions on the phase capacitor are quite often zero. Thus, the ripple is not so important and the observed results confirm this.

The reason why a 6th harmonic ripple is more visible in simulations can be caused by the difference in the modulation indexes.

Concerning the second harmonic ripple, the figures of §3.5.1 regarding the average actions on the phase capacitor can also be used to analyze the result. Close to the maximum modulation index, and $m = 0.88$ is a maximum modulation index in the case of the prototype, it is seen that during one period, there are always 2 regions (for instance, for the phase 1 capacitor at the top and bottom of the hexagon, Figure 3.33-top) where the range of actions allow to charge the capacitor, while during the rest of the period it can only be discharged. Thus, a $2f$ ripple will appear and this is what is observed.

The experimental results therefore validate the graphical model proposed for the analysis of the capacitors within the CCCS topology.

Modulator differences

The modulator design is of course different from the simulation to reality. However, because the modulation strategy is very clearly defined, the two modulators, although they are implemented on different platforms, are very similar from the point of view of functionality.

The main difference between the simulation and the setup is the score calculation weights. The weights define what combination of switching states is retained, thus what is the influence on the capacitors stabilization of the retained switching states combination. Since the weights (capacitor priority and current, see §3.4) have an important role in the final score, and because they cannot be the identical between the Matlab and the VHDL programs, due to different architectures and base for the numbers, the scores will not necessarily give the same results for the same converter states.

The tuning of the weights of the VHDL program to match the Simulink program is not done, because recompilation of the modulator is time consuming, and additionally would result in a trial and error strategy which is not desirable. It is possible that a given combination of weights leads to similar result, but the setups main interest is to demonstrate and validate the C^3S concept, model and control strategy, and not to offer the highest performances possible.

4.3.4. Implementation issues

Observed waveforms

Of what can be seen from the observed waveforms, for instance Figure 4.14, there is a low frequency ripple and unoptimized switchings on the outputs produced by the test setup. Several voltage steps are skipped which leads to a low frequency ripple.

It is clear from simulation results that the observed waveforms are not due to the proposed regulation or control concept, but to the implementation. Debugging of the VHDL software code is not a straightforward task when the complexity of the program is high.

The implemented “switching state calculator” instance (see §4.2.2) is by itself 10’000 lines long. Because of lack of experience with such a complex program structure, it is likely that the produced code is not optimized and could be written in a more efficient way. There are several steps in the programming sequence that are likely to have produced the observed errors.

The first step in the VHDL implementation is the transcription of the lookup tables. Initially the lookup tables contain the information calculated from Matlab about the repartition of the space phasors in the complex plan, with information about the possible PEBB states, and the charging and discharging informations. Transfer into VHDL of these large matrices requires an adaptation of the syntax. The chosen procedure was to use Excel to produce a VHDL compliant syntax. A this point, there is already the possibility of some data consistency error.

The next step is to optimize the lookup procedure. Typically, in VHDL, reading one line of the table requires one clock cycle. Because of the very large number of possible phasors, the size of the lookup table is problematic and a search can take really a very long time. For that reason, the information of the table was split into several subtables, 6 in total, which cover each one sixth of the hexagon. Thus, when knowing in which part of the hexagon the reference signal is, it is possible to choose the correct subtable to use. At this point as well, some sorting is necessary, and it must be carefully verified that each subtable contains actually the phasors it should, no more and no less. If there were a mistake at that point, the search in the lookup table would fail, since no values would be found, and thus, the modulator would fall back into a safe state which is "using the last applied gate signal".

Once the subtables are correctly defined, it is a question of finding the correct values by an incremental search in the tables, calculating the scores and storing the results. The score calculation is a sensitive algorithm. It must take into account the physical constraints of the system (for instance, the PEBB capacitor can only be charge every sixth of a period with large modulation indexes), and tuning of the weights can be tricky (see §3.4.2).

Besides these aspects, there are some other steps which are likely to produce errors on the phase voltages. The generation of the reference signal and calculation of the duty cycles, the application of the calculated gate signals to the gate drivers with the proper duration and the transition execution which takes care of the switching mechanisms.

Simulation of the VHDL code

With the help of the Xilinx System Generator toolbox, it is possible to simulate the VHDL code software using Matlab Simulink. In such a simulation, the VHDL code is run into an environment which can provide some help for debugging. However, the simulations can require a very long execution time, and the complexity of the simulated VHDL file must be restrained.

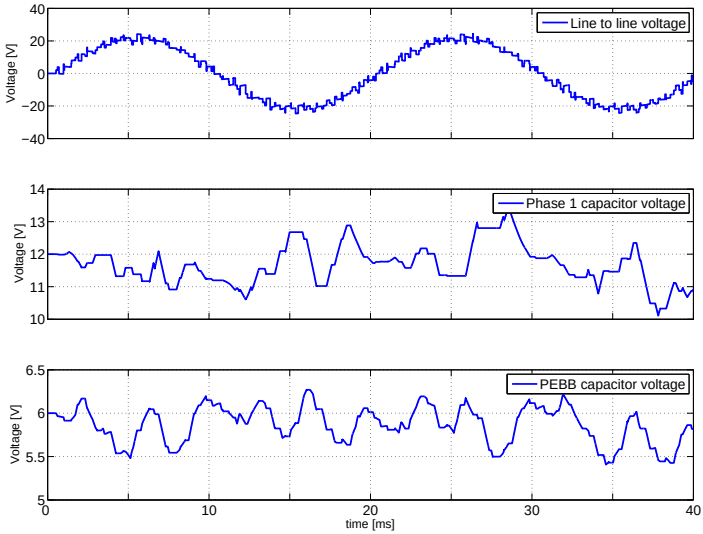


Figure 4.21.: *Simulation of the VHDL modulator instance "switching state calculator", $m = 0.9$.*

The simulation results of the "switching state calculator" are presented hereafter. The switching state calculator instance contains only the main part of the modulation algorithm, which is the lookup table search, the score calculation and the determination of the gate signals.

The simulation is run with operating conditions similar to the test setup, in terms of voltage ratings and load. From what can be seen, the modulation and score calculation seem to be executed in a proper way.

From this information, several conclusions can be drawn. First, it seems the main modulator instance, the score calculation and the determination of the phasor to be applied works in VHDL simulation and for some operating point. The capacitors can be balanced for the modulation index $m = 0.9$ which is not the case on the prototype.

This does not mean, however, that the problems observed on the test setup come from some other instances. The reason is that the other instances (sequence generator, transition execution, etc) have also been checked in simulation (sometimes using ModelSim, sometimes using Matlab Simulink) and all the instances have shown proper functionality.

The main question is whether there is the possibility that some part of the software code works fine with simulation but shows some errors in real time implementation, which can happen with simulation of VHDL programs. Or another possible issue is some sort of error produced by connecting the blocks together (synchronization issues for instance).

To be able to point out the problem, the modulator needs to be broken down into separate parts, and each of the parts needs to be verified first in simulation and then on the control board. Once the individual functionalities are verified, the parts can be put together progressively and tested.

Thus, finding out where this low frequency ripple comes from is not a light task. The implementation of the modulator in VHDL was demonstrated, showing that the proposed concept can actually be used on a FPGA chip. On the other hand, the implementation complexity was also revealed.

Final considerations

There is a whole chain of elements that are critical for the final result. The previous analysis gives some clues to where the errors might come from. Since VHDL is not so simple to debug, a careful and step by step implementation should be considered. Ideally, simulations should be run with growing VHDL program complexity, making sure at each step that the complete functionality works as expected, and then confirmation from the real setup should be obtained (at least observing with an oscilloscope some test signals from the control platform), since, as it is demonstrated here, simulation of VHDL is not always sufficient to demonstrate full functionality.

This has not been done carefully enough from the beginning in this work, because the complexity of the resulting code has been underestimated. The reprogramming of the modulator, taking into account each of these aspects, will certainly lead to a modulator implementation that offers the expected performances on the system.

However, from the actual status of the work, the basic principles are demonstrated. It is possible to show that the proposed balancing strategy works and that FPGA implementation is realistic, although it requires careful attention due to high complexity.

4.4. Conclusions

The prototyping phase was realized on the base of existing hardware modules for the 5L ANPC. A 9L C^3S inverter was realized and the results obtained are presented in this chapter. It is possible to demonstrate and validate the topology, the concepts and the control of the CCCS inverter.

The two main activities of the prototyping are on one side the development and testing of the VHDL modulator, and on the other hand the design and conception of the prototype hardware. The extensive use of simulation software tools did maybe not reduce the development time too much, but it allowed to do most of the debugging away from the real prototype. This certainly helps to discover problems before they lead to hardware failures.

Validation of the CCCS topology is a major result since it is a totally new topology and concept for multilevel inverters. The maximum modulation index observed on the setup is close enough to the simulation results to show that the implemented solution works in real life with very similar performances as observed in simulations.

The proposed modulation strategy allows to develop a functional modulator by following a certain number of generic steps, but the performances delivered vary depending on how exactly the solution is implemented. There is therefore clearly some room for the development of optimal modulation strategies.

The power ratings used for the tests are not high enough to get correct loss estimation. The limiting factor is the available supplies at the time of the tests. A grid connected configuration with a larger 3 level power supply could be done with the same setup. However because of time constraints, theses tests were not run.

The main results that are obtained from the prototype are that the system works correctly with the proposed model and balancing scheme and that the intrinsic dissymmetry (nonequal stray inductances) does not affect the operation of the converter at the considered switching speeds. It is also demonstrated that the converter can be started up with discharged capacitors and is able to bring the voltages up to their nominal values within a few hundred of milliseconds even for the highest achievable modulation index.

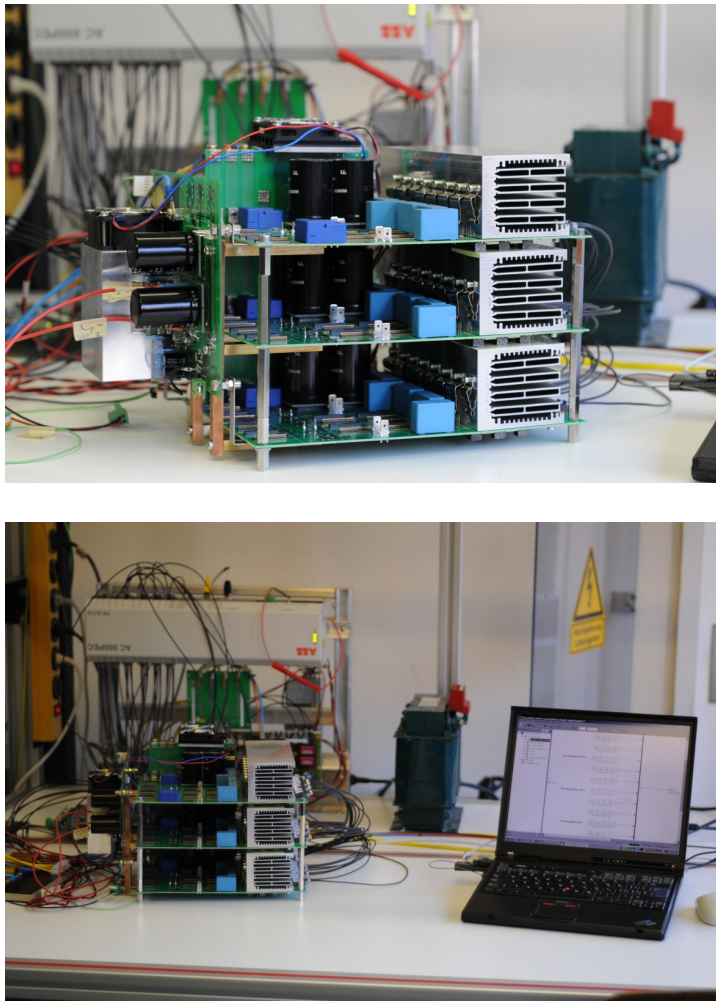


Figure 4.22.: *9L CCCS Prototype*

CHAPTER 5

Conclusions

5.1. Objectives and overview

Since the introduction of multilevel inverter topologies, there have been many different solutions proposed up to this day. It seems that multilevel solutions are becoming industry standards due to the multiple advantages they offer. Among all the existing topologies, it does not seem that any is really taking a technical lead in the domain. A short analysis of their characteristics shows that they have very different kind of properties, thus making them more or less adapted depending on the application.

The 5L ANPC multilevel topology has been the starting point of this work. It is a key topology at ABB and there have been several developments around it, notably this one. The main contributions of this thesis are, in that sense, two different modifications of the 5L ANPC leading to topologies characterized by a higher blocking voltage requirement, but offering higher reliability, ought to a lower number of components compared to some other classical solutions. For medium voltage applications, especially in renewable energy generation where the quality standards are very stringent, the output filter is usually bulky and expensive. Since the topology is already multilevel, increasing the number of generated outputs to further reduce the filter size seems to be a logical evolution.

Out of this work, two new topological families came out. They are intrinsically completely different approaches to the multilevel world, one being

more “standard”, the CCIL, while the other could be qualified of more “disruptive”, the CCCS. Both topologies have in common the use of a new cell called the Cross Connected Stage.

The interesting aspect of these topologies, besides their originality in the sense that they did not exist before, is that they position themselves in a segment of characteristics for which not many topologies were available prior to this work. The newly elaborated solutions can generate large number of output levels with a reduced number of components, compared to many traditional solutions. The price to pay for this is a larger blocking requirement.

The initial analysis, characterizing the topologies concerning the number of components compared with the number of levels generated, can now be completed with the solutions proposed in this work. The CCIL and CCCS topologies allow the generate more levels with a reduced number of components, thus filling in a previously open area, Figure 5.1.

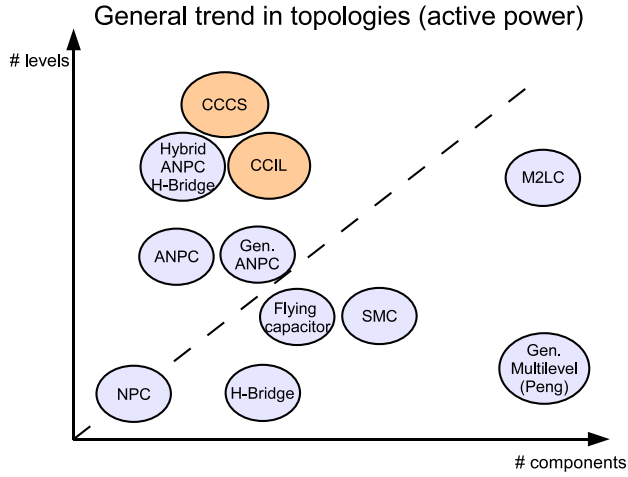


Figure 5.1.: *General trend observed in multilevel topologies regarding the number of components versus the number of generated levels, the CCIL and CCCS cover an area not previously represented*

The hybrid ANPC-H-Bridge topology also appears now in the graphic, as it is discussed in §2.6.2. It had not been considered initially, but during the work, it was found that this topology has similar characteristics as the CCIL. It is possible that other hybrid solutions also appear in that

range of topologies, but since there is virtually a unlimited number of hybrid topologies to be built, the present comparison cannot consider all of them. Similarly, the existing topologies with asymmetric voltage ratios are susceptible to go into that region of the graph, but here also, the analysis did not focus on these topologies.

Since this is only a one sided view of the characteristics, it can be kept in mind that a graph comparing the blocking voltage requirement would look liked a inversion of this graph.

It cannot be stated straightforwardly that the Cross Connected solutions offer great advantages and are the most suitable topologies for multilevel inverters. It cannot either be stated that because of their large blocking voltage requirement, they are unadapted solutions. In fact, the most interesting aspect of this investigation is that the designers have now the choice to pick a topology having either an optimized number of components or an optimized use of semiconductors, depending on what are their criteria of choice, and being aware of the trade off which exists.

5.2. CCIL topology

The Cross Connected Intermediate Level Voltage Source Inverter is the first topology developed on the base of the cross connected stage. It resulted in a patent, [57]. This PEBB can be used as well on the 3L ANPC or on any other kind of multilevel inverter, including also in a stand alone configuration.

Because it can make use of several voltage ratios and produce uniform output levels in redundant and non redundant state configurations, the topology gives a large freedom to the designer. In general, the non redundant solution requires higher blocking voltage but fewer components, and the redundant solution reduces a little the blocking voltage requirement but requires more switches and capacitors.

Besides their electrical characteristics, there is another big difference between the two elaborated topologies: the control. The redundant state topology has the advantage of offering a trivial capacitor balancing scheme, whereas the non redundant state case requires a common mode scheme and is limited in modulation index.

The non-redundant state topology offers the highest ratio of the number of generated levels on the number of passive components necessary. It is however found that the hybrid ANPC-H-Bridge topology has the exact same characteristics and allows to reduce a little the blocking voltage and the number of components.

Based on the analysis of the topology and the influence of the levels on the capacitor balancing, a graphical model is proposed. This model gives a global overview on the system's behavior for all kind of modulation indexes and power factors and allows developing a appropriate modulation strategy.

To demonstrate the controllability of the topology, a fuzzy logic regulator was developed with the help of the graphical model. The modulator is then implemented in simulation and the results indicate that the topology can be stabilized for modulation indexes up to $m = 0.91$ at active power. The developed modulator can also be used directly on the hybrid topology, since the two topologies are identical from the point of view of control. The limitation in the modulation index is caused by the physical constraint on the system which imposes that the energy delivered by the phase capacitors must be zero on average.

Benchmarking of this topology shows that compared to standard solutions, the number of single switches is reduced by a factor of more then 1.5, and the stored energy is reduced by a factor 5 and more, for the same number of levels. The difference also increases with increasing number of levels. On the other hand, the total blocking voltage is larger than with standard solutions by a factor of 2 to 4.

The signal quality delivered by the 9L CCIL converter is high enough to be able to get ride, to a large extent, of the output filter, which is one of the main criteria of choice. But the proposed modulator exhibits a low frequency ripple on the currents, in open loop configuration, which could be caused by control delays. Since the optimization of the modulation algorithm is not the main topic of interest, further investigations were not done on that aspect. It is likely that the modulation can be optimized to get ride of that problem.

The redundant CCIL topology does not suffer from modulation index limitation. The capacitors can be stabilized at all modulation indexes and for all power factors. In the non-boosting configuration the total blocking voltage requirement is a little lower than in the non redundant boosting case.

The stored energy for the redundant state CCIL inverters is a bit higher, because more capacitors are necessary for generating the same number of levels as the non-redundant configurations. But compared to more traditional solutions, the redundant CCIL still offers notable advantages with respect to the number of components.

Besides being interesting in the MV range, the CCIL redundant topologies can be interesting for low voltage applications. With some increase of the blocking voltage, which is not a real issue in low voltage (from the

technical point of view), and addition of some capacitors, it is possible to build a ultra high-quality signal output. For instance, one domain where there could be some benefit to removing the output filter and increasing the number of levels is the UPS (Uninterruptible Power Supply) applications.

Another domain of power electronics where such a solution could be interesting, but which is not linked to energy management or power production is the high power D-class audio amplifier applications. In the audio field, the price often grows with the signal quality, and therefore this sort of solutions can have interesting potentials.

5.3. CCCS topology

The CCCS topology introduces a completely new concept in the field of multilevel inverter topologies. This topology was also patented, [58]. The Common Cross Connected Stage is connected to the DC-link, and is used in common by the three phases of the inverter. This implies that some part of the topology can be reduced by a factor 3 and that the number of necessary components is therefore further reduced compared to the traditional per phase approach.

Connected to the 5L ANPC topology, the C^3S PEBB can offer a large number of levels depending on how many stages are cascaded. Due to the configuration of the C^3S topology, upgrade from the 5L ANPC configuration is very straightforward and the solution actually offers a truly modular approach. From the electrical characteristics point of view, some switches of the ANPC part require a higher blocking voltage than for the standard configuration, since they have to block the additional PEBB capacitor voltages. Once again, the trade off can be clearly seen between reducing the number of components and increasing the blocking voltage requirements. The addition of levels cannot be done without a price to pay.

Since the PEBB is commonly used by the three phases, analytical analysis is not very straightforward and can become tedious. Every combination of the three phase switching states and of the PEBB switching state must be considered, which makes the analysis quite complicated for the general case. Additionally, various voltage ratios are possible, which further increase the analytical complexity of the system.

As the switching states must be considered globally for the three phases, a space phasor graphical approach is proposed. The developed graphical model allows to understand the principal characteristics of the circuit, and helps to predict the behavior and dynamics of the capacitors for various modulation indexes. With the informations of the model, a generic modulation scheme is proposed for the balancing of the capacitors.

With the help of the model, a set of voltage ratios could be chosen, [4;2;1], which ensure uniformity of the output and controllability of the capacitors of the circuit. Based on the generic modulation description, a specific modulator for the 9L case is programmed in simulation.

The results show that the proposed topology works and that the capacitors can be stabilized with the developed modulation scheme. The simulation results also show that the CCCS offers good performances concerning signal quality and maximum modulation index. From the theoretical analysis, it was predicted that the maximum modulation index would be in the range of $m = 0.958$ and in simulations, the capacitors can be stabilized for modulation indexes up to $m = 0.925$.

The modulation index limitation can be overcome, since the CCCS 9L can fall back into a 5L operating mode. At the price of reduced signal quality, the inverter is able to work at higher modulation indexes for disturbances rejection, for instance. The 5L operating mode is not limited in modulation index whatever the power factor used.

The CCCS solution is then benchmarked versus the other topologies discussed in this work, and also against the CCIL. The result show that, globally, the CCCS allows to reduce a bit more the number of passive components compared to the CCIL, thus increasing a bit more the reliability, but the price to pay is once again an increase in the total blocking voltage.

However, the CCCS is a flexible solution and different voltage ratios can be considered. The 9L case study, discussed later in these concluding sections, imposes certain capacitor voltage ratios, but non uniform output steps can also be considered with voltage ratios such as [5;3;1] which do not increase so much the blocking voltage of the inverter. Since these solutions offer non uniform output steps, they were not benchmarked or discussed here. But they can offer potentially interesting results and could deserve some more study.

A prototype for the 9L CCCS inverter was built. The modulator is implemented in VHDL, following the generic modulator conception steps, and is made to work without any particular tuning. The experimental results show that the topology actually works, thus validating all the work done on this topology.

The maximum modulation index observed on the prototype is $m = 0.88$. The balancing of the capacitors works well, but comparison of the waveforms between the prototype and the simulation indicates that there is a difference between the two systems. The cause is identified to be at the level of the modulators, which are different in simulation and in reality (VHDL),

due to implementation platform differences. It can be expected that with an optimization of the modulator, better performances would result.

The development of the modulator aimed at the demonstration of the technology and not at getting the maximum performances out of the prototype. For that reason, the simplest functional modulator was designed to speed up the validation and demonstration of the topology. The modulator is definitely not optimized. It seems anyhow that different modulation strategies, based for instance on MPC schemes, offer high potentials regarding capacitor stabilization, and could be investigated.

Experimental validation of the results not only demonstrates the technology, it also validates the graphical model: the capacitor voltage ripple measured on the prototype can be explained by the model, and the correlation is really good at several operating points.

Additionally, it is shown that the system can be started with fully discharged capacitors and reaches the nominal operating point, with charged capacitors, within a few hundreds of milliseconds. This demonstrates that increased modulation index strategy, based on 5L operation, is possible. The capacitors can be brought back to their nominal operating point as soon as the modulation index falls back into a range allowing the 9L operation.

5.4. 9L solutions

Throughout this work, all the topologies discussed were 9L. The reason is that with the advanced multilevel topologies proposed, 9L seem to be almost the smallest inverters which can be designed. In the benchmarking sections, the comparison carried out on several 9L topologies, and the main characteristics were highlighted, especially in §3.6.4.

It is not so straightforward to define one solution as the winner, since the characteristics are quite different between all of them. In particular, the 9L double capacitor CCIL, the 9L hybrid ANPC-H-Bridge and the 9L CCCS topologies were compared to a 9L flying capacitor solution. The three first families of topologies are completely opposite in electrical characteristics compared to the last one, the flying capacitor, and the comparison showed quite well that each have their own advantages.

The 9L flying capacitor has got the lowest blocking voltage requirement of the comparison, but it requires a lot of components and a lot of stored energy. At the other end there is the hybrid topology. The hybrid boosting topology requires a higher DC-link voltage, because it cannot offer the maximum modulation index, and the highest total blocking voltage, but the number of components is the smallest and so is the stored energy. Between

these two extreme topologies (from characteristics point of view), it can be clearly seen that the design focuses on the optimization of completely different aspects.

In between, there are the 9L double capacitor CCIL and 9L CCCS topologies. The CCCS, from the point of view of electrical characteristics, has a certain advantage on the double capacitor CCIL. Fewer components, less stored energy and an almost similar total blocking voltage. But the topology, on the other hand, does not allow to reach the maximum modulation index with the full signal quality.

At the end, the final choice depends on what the designer is ready to pay for. More components and stored energy, more blocking voltage, or an average solution. In the latter case, once again a choice has to be made regarding number of components and maximum signal quality.

5.5. Perspectives and improvements

With this work, a new choice in the conception phases of multilevel topologies is possible. It is now clear that a choice must be made between reliability and increased blocking voltage. But whatever the choice, there are possible solutions available. Solutions offering optimization of the blocking voltage already existed and are quite numerous (flying capacitor, SMC, M2LC, cascaded H-Bridge, NPC, etc), while new solutions offering low number of components (ANPC, hybrid ANPC-H-Bridge) have now been proposed, with the CCIL and the CCCS.

There is obviously still room for improvements on these topologies. The work done here is only an introductory phase, which proposes some models and modulation schemes, but certainly that rising interest in one or the other topology will lead to more optimized models and modulators.

Some of the most interesting topics for further investigations are listed as follows: Improvement of the CCIL fuzzy logic regulator for getting rid of the low frequency ripple. In the same direction, a research and assessment of MPC schemes for the CCIL, based on the information given by the graphical model can be of high interest.

Investigation of the potential for loss balancing over the switches of the non redundant boosting CCIL topology is another interesting subject matter. It could allow to improve the efficiency of the converter which, else, is characterized by increased conduction losses due to increased use of silicon.

Optimization of the space phasor modulator for improved signal quality and higher modulation index, and MPC strategies are among of the most interesting research subjects for the CCCS converter. Here also, based

on the space phasor model, MPC schemes could offer efficient balancing solutions.

An important aspect is defining a systematic implementation strategy for the VHDL code. The main issues have been highlighted and the idea is to find a method to optimize the data consistency and lookup strategy for finding the correct vectors. A proper tuning strategy for the weights in the score calculation must also be defined to avoid trial and error tuning.

An interesting research direction would be to see if and how it would be possible to use more traditional 3 phased multilevel inverters instead of the CCCS PEBB, as common hybrid stages, to boost the number of levels produced by, for instance, the 5L ANPC topology. This can open up some new perspectives in modularity concepts for 3 phases multilevel inverters.

Finally, last but not least, the investigation regarding non-uniform output step CCCS converter configurations could reveal more adapted or more performing configurations regarding blocking voltage requirements or stabilization properties of the capacitors.

A medium voltage demonstrator could reveal the potentials and the problems of the CCCS configuration in real industrial applications.

APPENDIX A

Comparison of topologies

A.1. Stored energy calculation

The stored energy calculation is based on the following assumptions: All the topologies are considered to be switched at the same frequency, and with the same nominal values and operating point. The value of the capacitor depends on the voltage ripple that is wanted and the current that flows across the device, following the equation:

$$i = C_n \cdot \frac{\Delta U_{cn}}{\Delta t} \tag{A.1}$$

The desired maximum voltage ripple on the capacitor, in %, is given by the factor η. For instance, a 10% voltage ripple on the capacitors leads to a $\eta = 0.1$.

The equation (A.1) can be then rewritten in function of the capacitor voltage U_{cn} as:

$$i = C_n \cdot \frac{\eta U_{cn}}{\Delta t} \tag{A.2}$$

$$C_n(U_{cn}) = \frac{i \cdot \Delta t}{\eta U_{cn}} \tag{A.3}$$

Since the energy in the capacitor is defined by the well known equation (A.4):

$$E(U_{cn}) = \frac{1}{2} \cdot C(u) \cdot U_{cn}^2 \tag{A.4}$$

the final equation is be obtained by replacing (A.3) in it:

$$E(U_{cn}) = \frac{1}{2} \cdot \frac{i \cdot \Delta t}{\eta U_{cn}} \cdot U_{cn}^2 \tag{A.5}$$

$$E(U_{cn}) = \frac{i \cdot \Delta t}{2 \cdot \eta} \cdot U_{cn} \tag{A.6}$$

As given in hypothesis, all the converters assume the same nominal operating point and the same switching frequency. It can therefore by assumed that the current i and the time Δt are the same for all the converters. In the same way, the η factor is assumed identical for all the capacitors, which is a reasonable assumption. It results then that the stored energy per capacitor is a linear function of the capacitor voltage U_{cn} and that therefore the energy is represented directly by the voltages and the number of capacitors present in the topology.

$$E(U_{cn}) = K \cdot U_{cn} \tag{A.7}$$

The total stored energy in the converter is then be given by the sum of the stored energy in each capacitor, which is the weighted sum of all the capacitor voltage ratios present in the converter :

$$E_{cap} = K \cdot \sum_{n=1}^{\#\text{ of caps}} U_{cn} \tag{A.8}$$

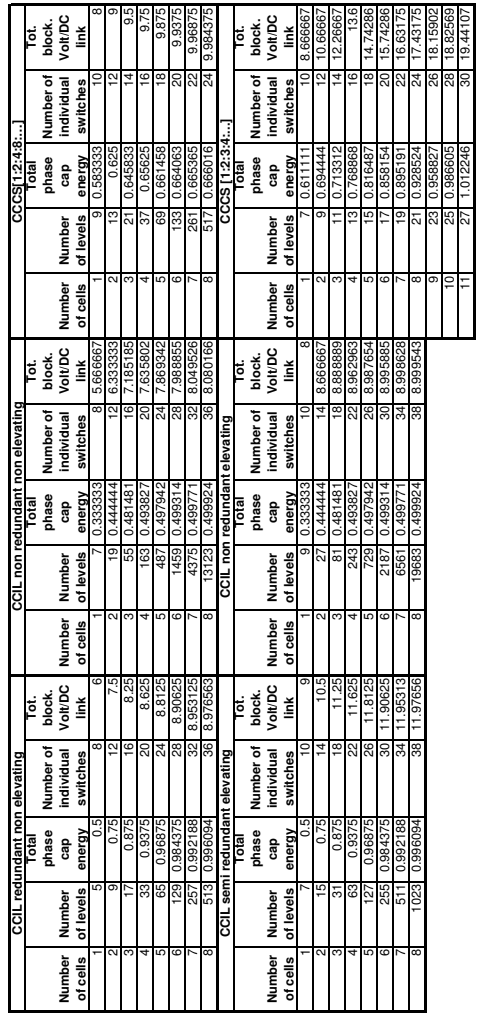
For plotting the results, the sums are normalized by the factor K. The DC-link voltage is 1 and thus, the capacitor voltages are fractions $\frac{1}{n}$.

A.2. Comparison table of values

The Tables A.1 and A.2 regroup the values obtained for the comparison.

	NPC					H-B					flying cap				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link	Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link	Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	2	0	2	2	1	3	1	4	4	1	2	0	2	2
2	3	0	4	2	2	5	1	8	4	2	3	0.5	4	2
3	4	0	6	2	3	7	1	12	4	3	4	0.707107	6	2
4	5	0	8	2	4	9	1	16	4	4	5	0.866025	8	2
5	6	0	10	2	5	11	1	20	4	5	6	1	10	2
6	7	0	12	2	6	13	1	24	4	6	7	1.118034	12	2
7	8	0	14	2	7	15	1	28	4	7	8	1.224745	14	2
8	9	0	16	2	8	17	1	32	4	8	9	1.322876	16	2
9	10	0	18	2	9	19	1	36	4	9	10	1.414214	18	2
10	11	0	20	2	10	21	1	40	4	10	11	1.5	20	2
11	12	0	22	2	11	23	1	44	4	11	12	1.581139	22	2
12	13	0	24	2	12	25	1	48	4	12	13	1.658312	24	2
13	14	0	26	2	13	27	1	52	4	13	14	1.732051	26	2
14	15	0	28	2	14	29	1	56	4	14	15	1.802776	28	2
15	16	0	30	2	15	31	1	60	4	15	16	1.870829	30	2
16	17	0	32	2	16	33	1	64	4	16	17	1.936492	32	2
17	18	0	34	2	17	35	1	68	4	17	18	2	34	2

Figure A.1.: *Numerical values of the comparison between the topologies*



CCIL redundant non elevating				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	5	0.5	8	6
2	9	0.75	12	7.5
3	17	0.875	16	8.25
4	33	0.9375	20	8.625
5	65	0.96875	24	8.8125
6	129	0.984375	28	8.90625
7	257	0.992188	32	8.953125
8	513	0.996094	36	8.976563

CCIL semi redundant elevating				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	7	0.5	10	9
2	15	0.75	14	10.5
3	31	0.875	18	11.25
4	63	0.9375	22	11.625
5	127	0.96875	26	11.8125
6	255	0.984375	30	11.90625
7	511	0.992188	34	11.95313
8	1023	0.996094	38	11.97656

CCIL non redundant non elevating				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	7	0.333333	8	5.666667
2	19	0.444444	12	6.333333
3	55	0.481481	16	7.185185
4	163	0.493827	20	7.635802
5	487	0.497942	24	7.869342
6	1459	0.499314	28	7.988855
7	4375	0.499771	32	8.049526
8	13123	0.499924	36	8.080166

CCIL non redundant elevating				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	9	0.333333	10	8
2	27	0.444444	14	8.666667
3	81	0.481481	18	8.888889
4	243	0.493827	22	8.962963
5	729	0.497942	26	8.987654
6	2187	0.499314	30	8.995885
7	6561	0.499771	34	8.998628
8	19683	0.499924	38	8.999543

CCCS[1;2;4;8;...]				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	9	0.583333	10	8
2	13	0.625	12	9
3	21	0.645833	14	9.5
4	37	0.65625	16	9.75
5	69	0.661458	18	9.875
6	133	0.664063	20	9.9375
7	261	0.665365	22	9.96875
8	517	0.666016	24	9.984375

CCCS [1;2;3;4;...]				
Number of cells	Number of levels	Total phase cap energy	Number of individual switches	Tot. block. Volt/DC link
1	7	0.611111	10	8.666667
2	9	0.694444	12	10.66667
3	11	0.713312	14	12.26667
4	13	0.768868	16	13.6
5	15	0.816487	18	14.74286
6	17	0.858154	20	15.74286
7	19	0.895191	22	16.63175
8	21	0.928524	24	17.43175
9	23	0.958827	26	18.15902
10	25	0.986665	28	18.82569
11	27	1.012246	30	19.44107

Figure A.2.: *Numerical values of the comparison between the topologies*

APPENDIX B

Average phasor repartition 7, 11L CCCS

B.1. Average phasor repartition, 7L CCCS

The average repartition gives an idea of the ripple shape and the capacitor control voltage constraints. The detailed analysis for the 9L C^3S is done in §3.5.1. The equivalent plots for the 7L [3;2;1] are given on Figures B.1 and B.2.

B.2. Average phasor repartition, 11L CCCS

The average repartition gives an idea of the ripple shape and the capacitor control voltage constraints. The detailed analysis for the 9L C^3S is done in §3.5.1. The equivalent plots for the 11L [5;3;1] are given on Figures B.3 and B.4.

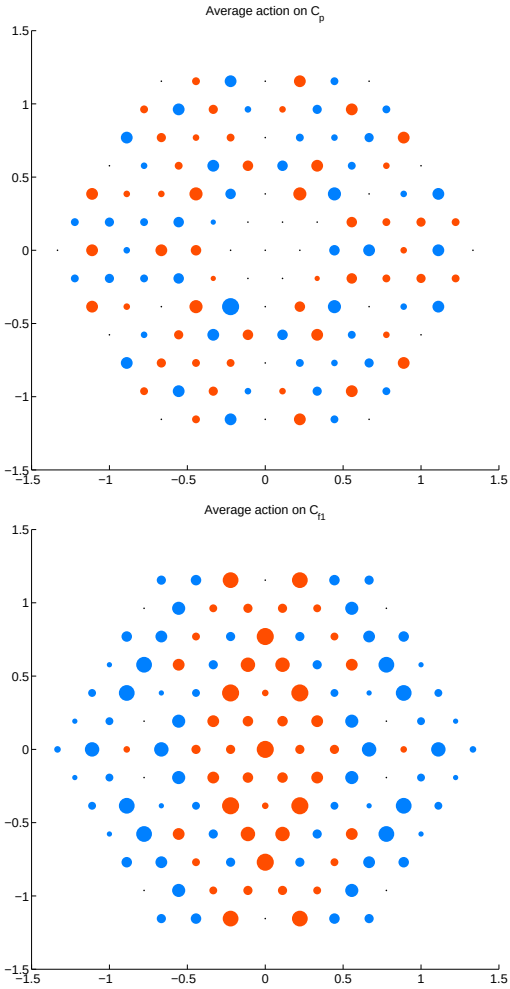


Figure B.1.: *Average phasors action on the capacitors C_p and C_{f1}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

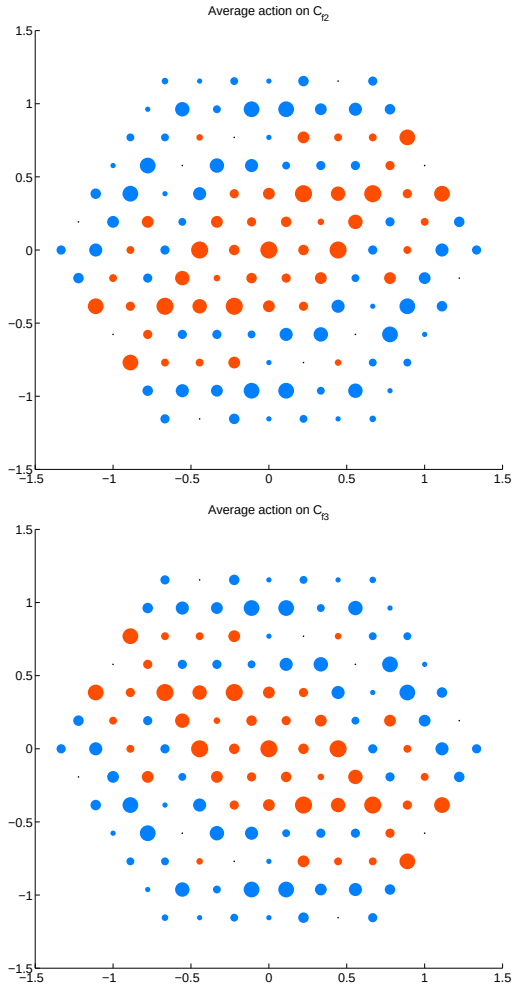


Figure B.2.: *Average phasors action on the capacitors C_{f2} and C_{f3}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

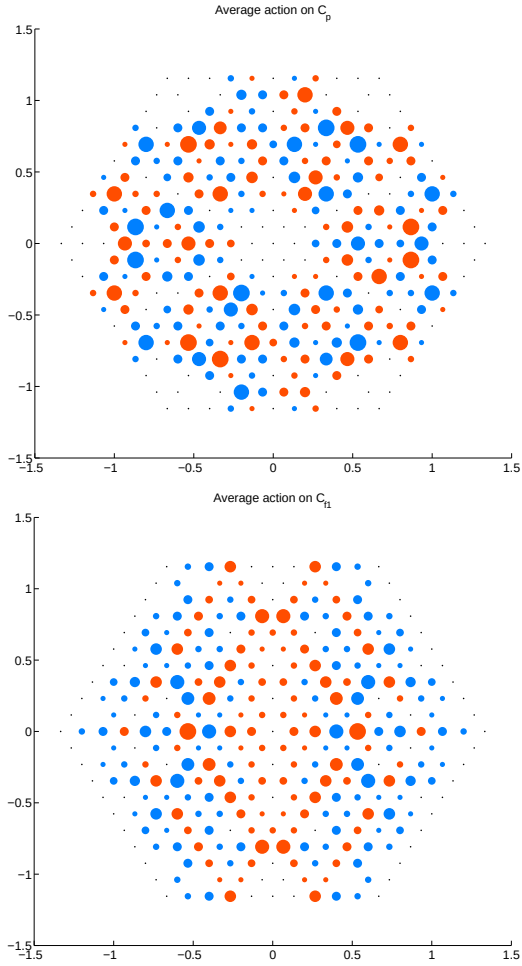


Figure B.3.: *Average phasors action on the capacitors C_p and C_{f1}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

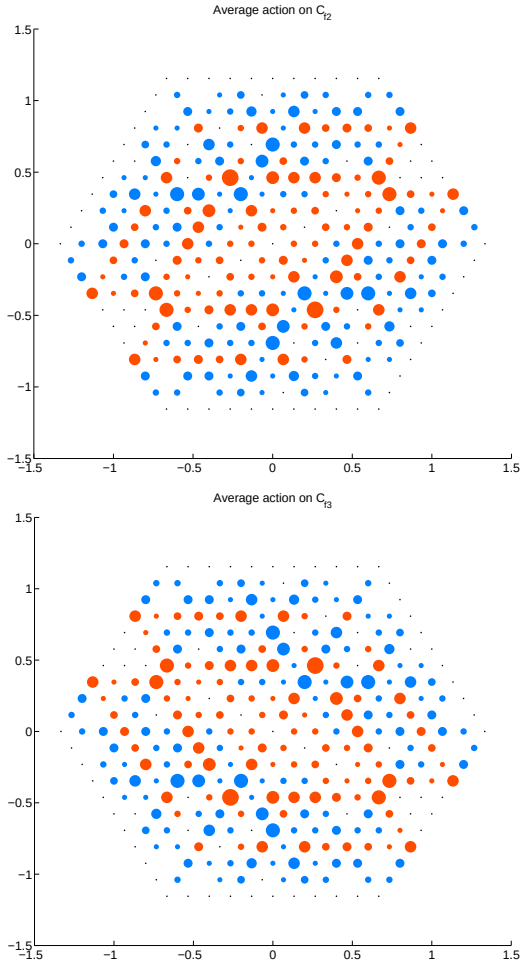


Figure B.4.: *Average phasors action on the capacitors C_{f2} and C_{f3}. The red dots indicate charging, the blue discharging and the black dots indicate zero contribution. The size of the dot indicates the amplitude*

APPENDIX C

List of simulation software used

The list of the simulation software tools used.

- MATLAB Version 7.1.0.246 (R14) Service Pack 3
- MATLAB Version 7.3 (R2006b)
- PLECS Version 1.5.6
- Xilinx System Generator Version 9.2.00
- OPCoDe Library Version 4.1.2 (ABB Commercial Software)
- PEC Library Version 4.1.2 (ABB Commercial Software)
- ModelSim SE Plus 5.7e
- Synpify 8.9
- Xilinx ISE 9.2i

List of Figures

List of Tables

Bibliography

[1] A.Nabae, I.Takahashi, and H.Akagi, "A New Neutral-Point Clamped PWM Inverter", *IEEE Trans. Ind. Applicat., Volume: IA-17, Issue: 5, Page(s): 518 - 523*, Sept./Oct. 1981.

[2] P.W. Hammond, "A New Approach to Enhanced Power Quality for Medium Voltage Applications", *IEEE 42nd Annual Petroleum and Chemical Ind. Applicat. Soc. Conf., Page(s): 231 – 235*, 11-13 Sept. 1995.

[3] P.Barbosa, P.Steimer, J.Steinke, M.Winkelnkemper, and N.Celanovic, "Active Neutral-Point Clamped Multilevel Converters", *EPE 2005, Page(s): 10*, 11-14 Sept. 2005.

[4] Richard H. Baker, "Bridge Converter Circuit", *United States Patent 4,270,163*, May 26, 1981.

[5] H.-P.Krug, T.Kume, and M.Swamy, "Neutral-Point Clamped Three-Level General Purpose Inverter - Features, Benefits and Applications", *IEEE PESC 35th Annual Meeting, Volume: 1, Page(s): 323 - 328*, 20-25 Jun. 2004.

[6] M.Marchesoni and P.Tenca, "Diode-Clamped Multilevel Converters: A Practicable Way to Balance DC-Link Voltages", *IEEE Trans. Ind. Elect., Volume: 49, Issue: 4, Page(s): 752 – 765*, Aug 2002.

[7] M.Fracchia, T.Ghiara, M.Marchesoni, and M.Mazzucchelli, "Optimized Modulation Techniques for the Generalized N-Level Converter",

IEEE PESC 23rd Annual Meeting, Volume: 2, Page(s): 1205 – 1213, 29 Jun. - 3 July 1992.

[8] H.K.Al-Hadidi and R.W.Menzies, "Investigation of a Cascade Multilevel Inverter as a STATCOM", *IEEE Pow. Eng. Soc. Gen. Meeting, Volume: 1, Page(s): 187 - 193*, 13-17 Jul. 2003.

[9] F.Z.Peng, J.W.McKeever, and D.J.Adams, "A Power Line Conditioner Using Cascade Multilevel Inverters for Distribution Systems", *IEEE Trans. Ind. Applicat., Volume: 34, Issue: 6, Page(s): 1293 - 1298*, Nov./Dec. 1998.

[10] Y.Fukuta and G.Venkataramanan, "DC Bus Ripple Minimization in Cascaded H-bridge Multilevel Converters under Staircase Modulation", *37th IAS Annual Meeting, Volume: 3, Page(s): 1988 – 1993*, 13-18 Oct. 2002.

[11] T.A.Meynard and H.Foch, "Multi-Level Choppers for High Voltage Applications", *EPE Journal, Page(s): 45 - 50*, Mar. 1992.

[12] T.Meynard, H.Foch, F. Foest, C.Turpin, F.Richardeau, L.Delmas, G.Gateau, and E.Lefeuvre, "Multicell Converters: Derived Topologies", *IEEE Trans. Ind. Elect., Volume: 49, Issue: 5, Page(s): 978 – 987*, Oct. 2002.

[13] T.Meynard and H.Foch and P.Thomas and J.Cournault and R.Jakob and M.Nahrsteadt, "Multicell Converters: Basic Concepts and Industry Application", *IEEE Trans. Ind. Elec., Volume: 49, Issue: 5, Page(s): 955 - 964*, Oct. 2002.

[14] R.H.Wilkinson, T.H.Meynard, and H.du Toit Mouton, "Natural Balance of Multicell Converters: The General Case", *IEEE Trans. Pow. Elec., Volume: 21, Issue: 6, page(s): 1658 - 1666*, Nov. 2006.

[15] L.Delmas, T.Meynard, H.Foch, and G.Gateau, "SMC : Stacked Multicell Converter", *PCIM 2001, Page(s): 63 – 69*, 19-21 Jun. 2001.

[16] T.A.Meynard, H.Foch, L.Delmas, and G.Gateau, "Stacked Multicell Converter (SMC): Control and Natural balancing", *IEEE PESC 33rd Annual Meeting, Volume: 2, Page(s): 689 – 694*, 23-27 Jun. 2002.

[17] T.Brueckner, S.Bernet, and P.Steimer, "The Active NPC Converter for Medium-Voltage Applications", *40th IAS Annual Meeting, Volume: 1, Page(s): 84 – 91*, Oct. 2005.

[18] F.Z.Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", *IEEE Trans. Ind. Applicat., Volume: 37, Issue: 2, Page(s): 611 – 618*, Mar/Apr 2001.

[19] A.Lesnicar and R.Marquardt, "An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range", *IEEE Power Tech Conf. Proc., Volume: 3, page(s): 6*, 23-26 Jun. 2003.

[20] S.Mariethoz and A.Rufer, "New Configurations for the Three-phase Asymmetrical Multilevel Inverter", *39th IAS Annual Meeting, Volume: 2, Page(s): 828 – 835*, Oct. 2004.

[21] Jean-Sébastien Mariethoz, *Etude Formelle pour la Synthèse de Convertisseurs Multiniveaux Asymétriques : Topologie, Modulation et Commande*, PhD thesis, Lausanne, EPFL, PhD N°3188, 2005.

[22] A.Rufer, M.Veenstra, and K.Gopakumar, "Asymmetric Multilevel Converter for High Resolution Voltage Phasor Generation", *EPE Journal*, Sep. 1999.

[23] P.Barbosa, P.Steimer, and L.Meysenc, "Converter Circuit For Switching A Number Of Switching Voltage Levels", *Patent Publication Number: WO2006053448 A1*, 24 oct. 2007.

[24] M.Manjrekar, P.Steimer, and T.Lipo, "Hybrid Multilevel Power Conversion System: A Competitive Solution for High-Power Applications", *IEEE Trans. Ind. Applicat., Volume: 36, Issue: 3, Page(s): 834 - 841*, May 2000.

[25] VDEW, *Eigenerzeugungsanlangen am Mittelspannungsnetz, 2. Ausgabe*, VWEW, 1999.

[26] J.S.Lai and F.Z.Peng., "Multilevel Converters-A New Breed of Power Converters", *IEEE Trans. Ind. Applicat., Volume: 32, Issue: 3, page(s): 509 - 517*, May/Jun. 1996.

[27] T.Chaudhuri, P.Barbosa, P.Steimer, and A.Rufer, "Cross Connected Intermediate Level Voltage Source Inverter", *IEEE PESC 38th Annual Meeting, Page(s): 490 - 496*, 17-21 Jun. 2007.

[28] Joseph Song-Manguelle, *Convertisseurs Multiniveaux Asymetriques Alimentes par Transformateurs Multi-Secondaires Basse-Frequence: Reactions au Réseau d'Alimentation*, PhD thesis, Lausanne, EPFL, PhD N°3033, 2004.

[29] Martin Veenstra, *Investigation and Control of a Hybrid Asymmetric Multi-level Inverter for Medium Voltage Applications*, PhD thesis, Lausanne, EPFL, PhD N°2846, 2003.

[30] M.Veenstra and A.Rufer, "Control of a Hybrid Asymmetric Multilevel Inverter for Competitive Medium-Voltage Industrial Drives", *IEEE Trans Ind. Applicat., Volume: 41, Issue: 2, Page(s): 655 - 664*, Mar./Apr. 2005.

[31] S.J.Qin and T.A.Badgwell, "A Survey of Industrial Model Predictive Control Technology", *Control Engineering Practice, 11, Page(s): 733 – 764*, 2003.

[32] R.E.Kalman, "Contributions to the Theory of Optimal Control", *Bulletin de la Societe Mathematique de Mexicana, 5, Page(s): 102 – 119*, 1960.

[33] R.E.Kalman, "A New Approach to Linear Filtering and Prediction Problems", *Transactions of ASME, Journal of Basic Engineering, 87, Pages(s): 35 – 45*, 1960.

[34] R.Findeisen and F.Allgöwer, "An Introduction to Non-Linear Model Predictive Control", *Benelux Meeting on Systems and Control (http://www.wfw.wtb.tue.nl/benelux2002/nmpc.pdf)*, 19-21 March 2002.

[35] F.Allgöwer and A.Zheng, *Non-Linear Model Predictive Control, Progress in systems and control theory, Vol.26*, Basel-Boston-Berlin, Birkhäuser, 2000.

[36] J.B.Rawlings and K.R.Muske, "The Stability of Constrained Receding Horizon Control", *IEEE Trans. Automat. Contr., Volume: 38, Issue: 10, Page(s): 1512 - 1516*, Oct. 1993.

[37] T.Meynard, G.Gateau, and P.Maussion, "Fuzzy Phase Control of Series Multicell Converters", *6th IEEE Int. Conf. Fuzzy Sys., Volume: 3, Page(s): 1627 - 1633*, 1-5 Jul. 1997.

[38] Byung-Jae Choi, Seong-Woo Kwak, and Byung Kook Kim, "Design and Stability Analysis of Single-Input Fuzzy Logic Controller", *IEEE Trans. On Systems, Man, and Cybernetics — part B, Volume: 30, Issue: 2, Page(s): 303 - 309*, Apr. 2000.

[39] T.Brueckner, S.Bernet, and H.Gueldner, "The Active NPC converter and Its Loss-Balancing Control", *IEEE Trans. Ind. Elec., Volume: 52, Issue: 3, page(s): 855 - 868*, Jun. 2005.

[40] T.Brueckner and S.Bernet, "Estimation and Measurement of Junction Temperatures in a Three-Level Voltage Source Converter", *IEEE Trans. Pow. Elec., Volume: 22, Issue: 1, page(s): 3 - 12*, Jan. 2007.

[41] IEC-61000-2-12, *Electromagnetic compatibility (EMC) – Part 2-12: Environment – Compatibility levels for low-frequency conducted disturbances and signaling in public medium-voltage power supply systems*, International Standard, First Edition 2003-04.

[42] T.Chaudhuri, P.Steimer, and A.Rufer, "Introducing the Common Cross Connected Stage (C3S) for the 5L ANPC Multilevel Inverter", *IEEE PESC 39th Annual Meeting*, to be published 15-19 Jun. 2008.

[43] F.Jenny and D.Wueest, "The Optimization Parameters of Space Vector Modulation", *5th EPE Brighton, Volume: 4, page(s): 376 - 381*, 13-16 Sep. 1993.

[44] R.Teodorescu, F.Blaabjerg, J.K.Pedersen, P.Enjeti, and E.Cengelci, "Space Vector Modulation Applied to Modular Multilevel Converters", *PCIM 1999, Page(s): 363 – 368*, May 1999.

[45] N.Schibli, A.Schaller, and A.Rufer, "Online Vector Modulation and Control for Three-Phase Multilevel Converter", *NORPIE98: Nordic Workshop on Power Electronics, Helsinki, Finland*, Aug. 1998.

[46] N.Celanovic and D.Boroyevich, "A Fast Space-Vector Modulation Algorithm for Multilevel Three-Phase Converters", *IEEE Trans. Ind. Applicat., Volume: 37, Issue: 2, Page(s): 637 - 641*, Mar./Apr. 2001.

[47] B.P.McGrath, D.G.Holmes, and T.Lipo, "Optimized Space Vector Switching Sequences for Multilevel Inverters", *IEEE Trans. Pow. Elec., Volume: 18, Issue: 6, Page(s): 1293 - 1301*, Nov. 2003.

[48] A.Schönnung and H.Stemmler, "Geregelten Drehstrom-Umkehrantrieb mit gesteuerten Umrichter nach dem Unterschwingungsverfahren", *BBC-Nachrichten, Page(s): 699 - 721*, Dec. 1964.

[49] K.Zhou and D.Wang, "Relationship Between Space-Vector Modulation and Three-Phase Carrier-Based PWM: a Comprehensive Analysis", *IEEE Trans. Ind. Elec., Volume: 49, Issue: 1, page(s): 186-196*, Feb. 2002.

[50] "Technical Information, IGBT-Module FF1200R17KE3", *Eupec*, 27 july 2004.

[51] "Technical Information, IGBT-Module FF1200R12KE3", *Eupec*, 27 july 2004.

[52] "Reverse Conducting Integrated Gate-Commutated Thyristor 5SHX 10H6004", *ABB Switzerland Ltd, Semiconductors*, 3 january 2002.

[53] Frederic Mermod, "Prototype for C3S PEBB", *Master Thesis, LEI-EPFL, Lausanne*, 7 march 2008.

[54] ABB, *ControlIT AC 800PEC - Hardware Guide*, Dokman AG, Naglerwiesenstrasse 2, CH-8049 Zürich, 22 December 2004.

[55] A.M.Lienhardt, G.Gateau, and T.Meynard, "Digital Sliding-Mode Observer Implementation Using FPGA", *IEEE Trans. Ind. Elec., Volume: 54, Issue: 4, page(s): 1865 - 1875*, Aug. 2007.

[56] Anne-Marie Lienhardt, *Etude de la Commande et de l'Observation d'une Nouvelle Structure de Conversion d'Energie de type SMC (Convertisseur Multicellulaire Superposé)*, PhD thesis, Toulouse, INPT, PhD N°2399, 2006.

[57] T.Chaudhuri, P.Barbosa, and P.Steimer, "Converter Circuit For Switching a Large Number of Switching Voltage Levels", *Patent Publication Number: WO 2008/046772 A1*, 24 apr. 2008.

[58] T.Chaudhuri, P.Barbosa, and P.Steimer, "Schaltzelle sowie Umrichterschaltung zur Schaltung einer Vielzahl von Spannungsniveaus mit einer solchen Schaltzelle", *Patent Pending*, 2008.

Curriculum Vitae

Toufann Chaudhuri

Born 14 December 1980
toufann.chaudhuri@a3.epfl.ch

WORK EXPERIENCE

Since June 2005: **ABB Corporate Research Center**, Baden-Daettwil, Switzerland
Position held: Scientist
Power electronics research and development activities on medium voltage industrial converters. Development of new multilevel topologies and associated modeling, control and modulation schemes. Programming of industrial standard controllers.

March-May 2005, June-August 2006, August 2007: **PuissanceL**, Lausanne
Position held: Civil Servant
Professional reinsertion activities for workless and drug addicted peoples in cure.

EDUCATION AND TRAINING

1999-2003 : **Ecole Polytechnique Federale de Lausanne**, Lausanne, Switzerland
Title awarded: Master degree in Science
Orientation in power electronics, industrial electronics, automatics. Good background knowledge in electromechanics, mechatronics, railway technologies, industrial automation, electronics.

1996-1999: **Gymnase de Morges**, Morges, Switzerland
Title awarded: Federal Maturity Type C - Bilingual French-German
Mathematics and Science orientation.

PUBLICATIONS

Cross Connected Intermediate Level Voltage Source Inverter, T.Chaudhuri, A.Rufer, P.Steimer, P.Barbosa, IEEE 38th Annual Power Electronics Specialists Conference, Page(s): 490-496, 17-21 June 2007.

Introducing the Common Cross Connected Stage (C3S) for the 5L ANPC Voltage Multilevel Inverter, T.Chaudhuri, A.Rufer, P.Steimer, IEEE 39th Annual Power Electronics Specialists Conference, to be published 15-19 June 2007.

PATENTS

Converter Circuit For Switching a Large Number of Switching Voltage Levels, T.Chaudhuri and P.Barbosa and P.Steimer, Patent Publication Number: WO 2008/046772 A1, 24 april 2008

Schaltzelle sowie Umrichterschaltung zur Schaltung einer Vielzahl von Spannungsniveaus mit einer solchen Schaltzelle, T.Chaudhuri and P.Barbosa and P.Steimer, Patent Pending, 2008

PERSONNAL INTERESTS

Photography, squash, badminton, biking, travel. Interest for languages, notions of Bengali and Italian.