

# LOW-POWER HERMETICALLY SEALED ON-CHIP PLASMA LIGHT SOURCE MICROMACHINED IN GLASS

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## ABSTRACT

We report on the fabrication and testing of a chip-scale plasma light source. The device consists of a stack of three anodically bonded Pyrex wafers, which hermetically enclose a gas-filled cavity in which electrodes are used to ignite a low power (<500 mW) RF plasma.

## 1. INTRODUCTION

Plasma discharges can be very efficient and stable light sources, for instance widely used as pixels in plasma TVs (<1 W/pixel), as Rubidium lamps in commercial compact Rb atomic frequency standards (few W), or even proposed as bright sources for EUV lithography (>10 W). Plasma discharge light sources can offer long lifetimes, important for application such as atomic clocks: although lasers offer higher optical efficiency, commercial Rb atomic clocks rely on Rb discharge lamps because of their very slow frequency drift (aging) and long lifetime. We have developed a *sealed* chip-scale plasma light source that is low power (as required for portable applications), versatile and compact.

Research to date on micromachined plasma source has been on *unsealed* electrode arrays, typically atmospheric plasmas for medical or chemical applications [1-3], gas chromatography [4] or spectroscopy [5,6]. We instead optimized our electrode geometry for efficient operation at 10-500 mbar in different gases (Ar, He and N<sub>2</sub>). We minimized the RF power required for ignition and stable operation by patterning sharp corners in the electrodes and by using an on-PCB circuit to match the capacitive impedance ( $Z > 1 \text{ k}\Omega$ ) of the chips to the  $50 \Omega$  RF source, while also providing more than a factor of 50 of voltage amplification. RF operation (near 20 MHz) was chosen in order to extend device lifetime by minimizing erosion of the cathode as occurs with DC plasmas [7].

## 2. FABRICATION

The key features of the fabrication process are: 1) the use of powder blasting on Pyrex as a versatile technology to create through-wafer holes of any geometry on the same substrate (unlike ultrasonic drilling), and 2) Pyrex-to-Pyrex anodic bonding to create hermetic cavities. A cross-section of the process flow is shown in Fig. 1.

As a first step, two microns of amorphous silicon (a-Si) are sputtered on a 100-mm Pyrex wafer (Wafer#1) and patterned by dry-etching. This film acts as a mask for the following dry-etch of 2  $\mu\text{m}$ -deep cavities in Pyrex. To enable anodic bonding, the a-Si is not removed [8]. Next, 3  $\mu\text{m}$  of aluminum are sputtered and interdigitated electrodes are dry-etched in the cavities using an inductively coupled plasma (ICP) process based on Cl<sub>2</sub>/BCl<sub>3</sub> chemistry. Fig. 2a shows typical anisotropic patterns with very sharp corners

enabled by the ICP process. Wafer#1 is then coated with 4  $\mu\text{m}$  of sputtered SiO<sub>2</sub> and chemical-mechanical polishing (CMP) is performed with a stop on the remaining a-Si film. SiO<sub>2</sub> is then etched in CF<sub>4</sub> plasma, which is highly selective towards Al, in order to open via-holes for electrical contacts and to locally remove residual SiO<sub>2</sub> from the electrode area (Fig. 2b). A first anodic bonding is performed at 350°C and 1.2 kV between Wafer#1 and a second Pyrex substrate (Wafer#2). The latter has through-wafer holes created by powder blasting (Fig. 2c) [9]. In this process, the Pyrex surface, which is protected with a photolithographically defined polymer mask, is eroded by a jet of alumina particles with a diameter of 30  $\mu\text{m}$ . The etch-rate of Pyrex achieved in static mode is 50  $\mu\text{m}/\text{s}$ . Furthermore, unlike wet-etching, powder blasting avoids mask undercutting thus enabling the fabrication of anisotropic holes with wall angles of about 15-18°. According to the manufacturer [10], a processing time of about 1 hour and 45 minutes is required for drilling an array of through-wafer holes in a 500  $\mu\text{m}$ -thick Pyrex substrate with diameter of 100-mm.

The bonded stack (Fig. 2d) is then diced into 10x10 mm<sup>2</sup> chips. Using the previously mentioned conditions, a second anodic bonding is performed under a controlled gas pressure to a third Pyrex chip in order to hermetically seal the cell enclosing the electrodes (Fig. 2e). Again, Pyrex-to-Pyrex anodic bonding is made possible by the a-Si film (100 nm) deposited on Wafer#2 before powder blasting. The low temperature used for the anodic bonding protects the Al electrodes while enabling an excellent adhesion between bonded wafers.

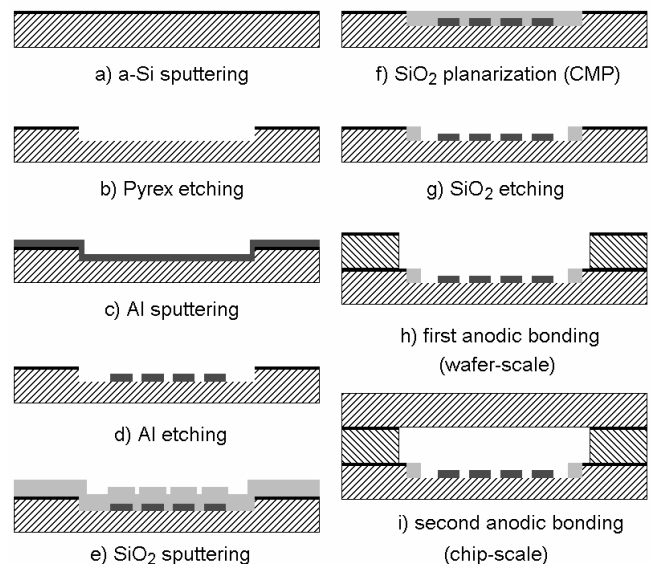


Fig. 1: Schematic process flow. All substrates are 100-mm Pyrex wafers with a thickness of 500  $\mu\text{m}$ .

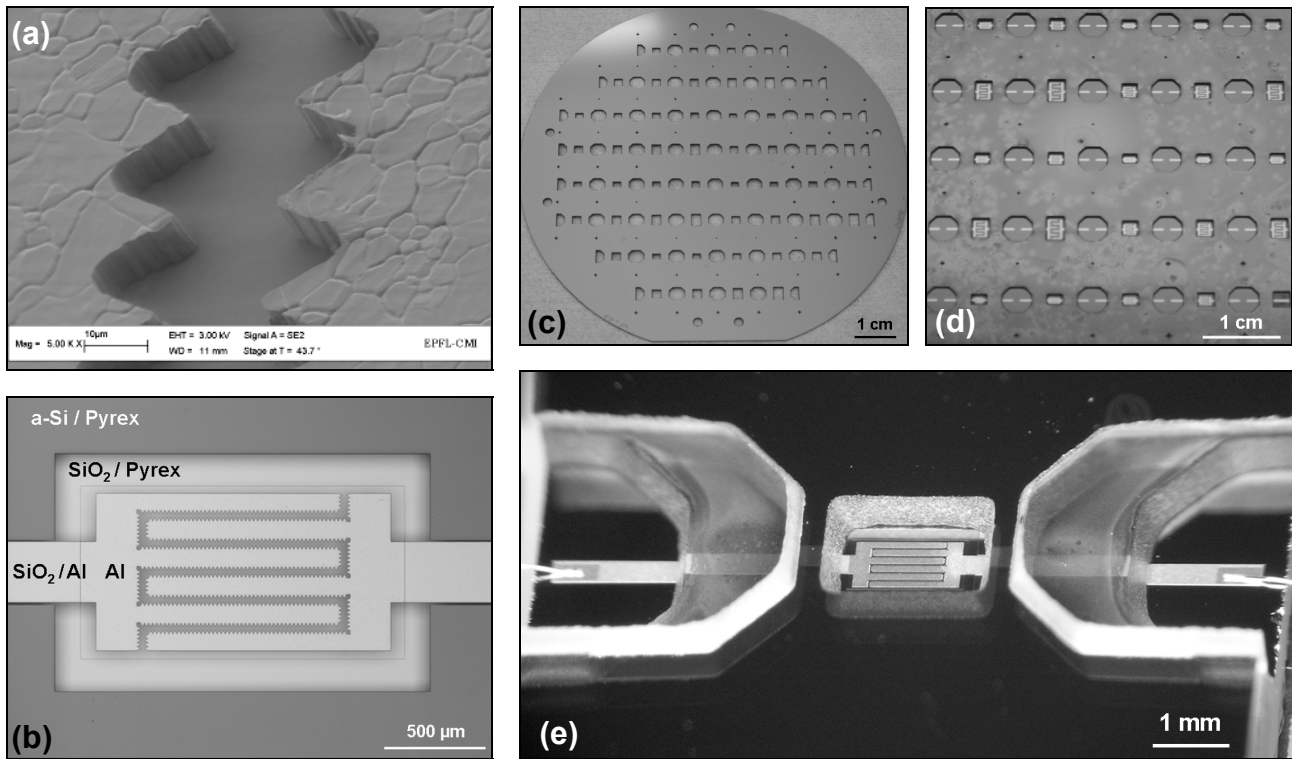


Fig. 2: Details of the fabrication process: (a) SEM micrograph of dry-etched Al electrodes, (b) Pyrex cavity with interdigitated electrodes after CMP and SiO<sub>2</sub> etching (Wafer#1), (c) powder blasted Pyrex wafer coated with 100 nm of amorphous Si (Wafer#2), (d) Wafer#1 and Wafer#2 after the first anodic bonding, and (e) final sealed triple-stack chip.

### 3. IMPEDANCE MATCHING

An impedance matching network (see Fig. 3) has been implemented on-PCB (printed circuit board) and serves two purposes: 1) to allow maximum power transfer from the  $Z_s = 50 \Omega$  source (a variable gain 10 W RF amplifier 1-500 MHz, model BBM1C3KAJ, Empower RF Systems, Inc.) to the load,  $Z_{chip}$ , corresponding to the  $>1 \text{ k}\Omega$  capacitive impedance of the chip, and 2) to amplify the voltage in order to reach the 200 to 300 V needed to ignite the plasma discharge (500 mW into  $50 \Omega$  corresponds to 5 V peak voltage).

The main challenge with this circuit is designing and tuning it such that the maximum in voltage amplification and the  $50 \Omega$  matching occur at the same frequency. The discrete components (inductors and capacitors) must have sufficiently high quality factors at those frequencies. Fig. 4 shows a plot obtained using the PSpice simulation tool [11] of the circuit in Fig. 3, but including a number of parasitics accounting for stray capacitances, wire-bonds inductance and series resistances of the metal traces. Real and imaginary components of the circuit impedance, as well as the voltage amplification on the chip are plotted as a function of frequency. One can see that in this simulation the voltage peak occurs at 21.2 MHz, which is the frequency where  $\text{Re}(Z) = 50 \Omega$ .

The impedance matching circuit of Fig. 3 is realized using two trimmer capacitors ( $C_1$ : 5 to 110 pF and  $C_2$ : 1.2 to 6 pF) and a fixed value inductor ( $L_p = 10 \mu\text{H}$ ). After a chip is mounted on the impedance-matching PCB (see Fig. 5), the circuit's impedance is measured with a network analyzer (HP 8753D) and displayed in Smith chart form, while the trimmer capacitors are tuned until  $50 \Omega$  purely resistive impedance is obtained. This determines the operating frequency that will be later programmed on the signal generator (HP 8642A) for igniting the RF discharge.

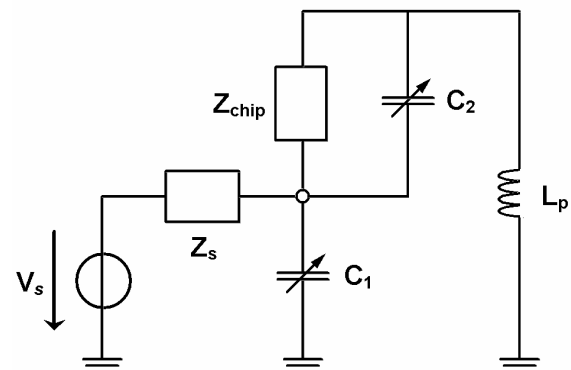


Fig. 3: Equivalent circuit used for impedance matching.

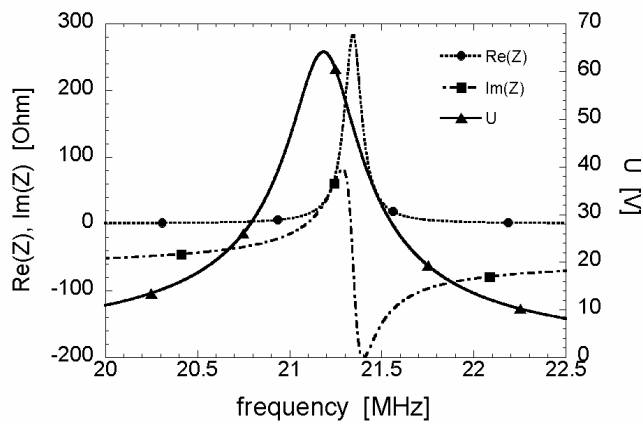


Fig. 4: Simulated curves of complex impedance  $Z$  and voltage  $U$  for a 1 V input signal. If the values of the discrete elements are properly chosen, both  $\text{Re}(Z)=50 \Omega$  and maximum voltage amplification occur at the same frequency (here 21.2 MHz).

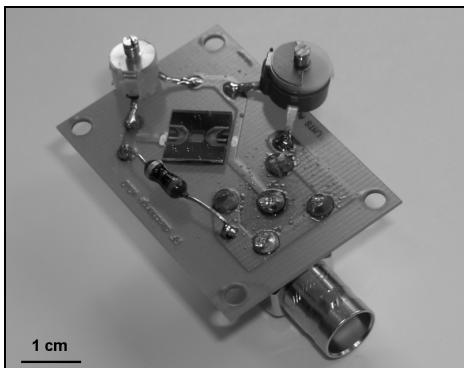


Fig. 5: The completed chip is mounted on a PCB with the discrete elements (two trimmer capacitors and one fixed-value inductor) used to implement the impedance matching circuit.

Fig. 6 shows the Smith chart corresponding to the measured impedance of the circuit after tuning:  $\text{Re}(Z)=50 \Omega$  and  $\text{Im}(Z)=0 \Omega$  occur at 21.2441 MHz.

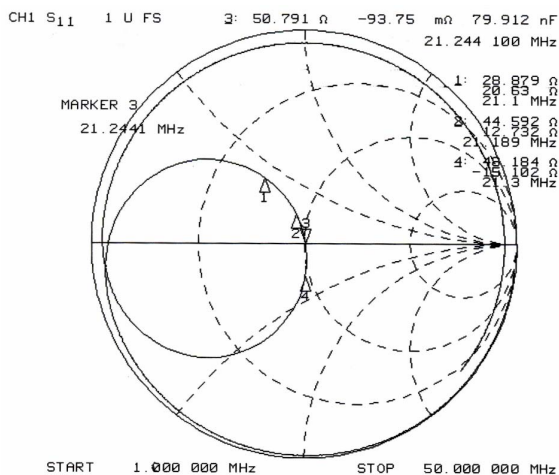


Fig. 6: Smith chart displaying the circuit impedance measured between 1 and 50 MHz. Accurate  $50 \Omega$  matching is achieved at 21.2441 MHz.

#### 4. RESULTS AND DISCUSSION

Fig. 7 shows a bright and stable plasma discharge generated in one of the fabricated devices sealed in a 50 mbar He atmosphere. The RF power required to ignite the discharge was 350 mW at a frequency near 20 MHz (the plasma is readily ignited within 1 MHz of the “ideal” frequency). In general, the plasma discharges cover uniformly the whole electrode area.

We have successfully ignited plasmas with electrode gaps from  $10 \mu\text{m}$  to  $500 \mu\text{m}$ , and with different electrodes geometries including corrugated edges to enhance the electric field and reduce the voltage (hence power) required for ignition.

Spectroscopy measurements are performed using a USB4000 fiber-optic spectrometer from Ocean Optics. The measurements were realized by placing the multimode optical fiber ( $600 \mu\text{m}$  core diameter) on top of the device. Figure 8 displays two measured spectra corresponding to plasma discharges in He and Ar. These two spectra reveal the expected different peak patterns characteristic of each gas. Continuous operation for a few hours at constant power levels of 300-600 mW has been demonstrated without degradation of the electrodes. Longer-time stability tests will be performed in order to assess the lifetime of these chip-scale plasma discharges. Since the plasma is RF rather than DC powered, the electrode lifetime could be enhanced if necessary by adding an extra passivation step to the fabrication process, i.e., by depositing a dielectric film such as  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$  or  $\text{Al}_2\text{O}_3$  on top of the Al electrodes.

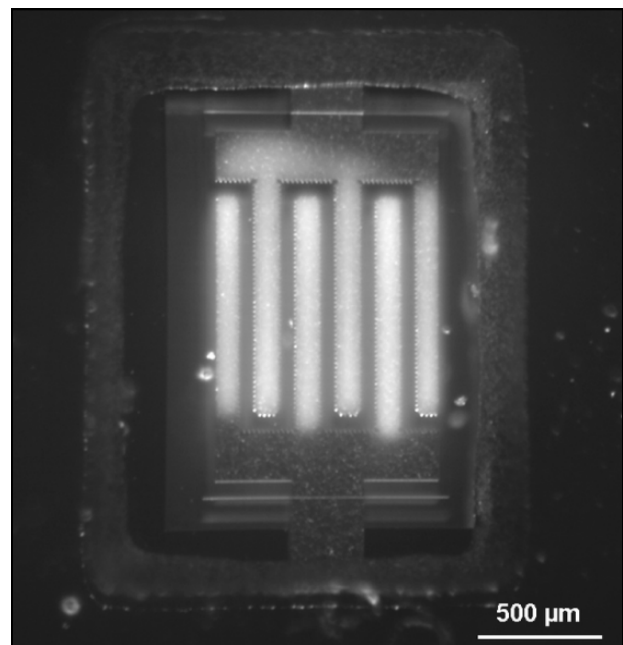


Fig. 7: Optical micrograph showing a stable plasma discharge ignited in He (50 mbar) covering the whole area above the interdigitated electrodes. The power required for ignition was 350 mW at a frequency around 20 MHz.

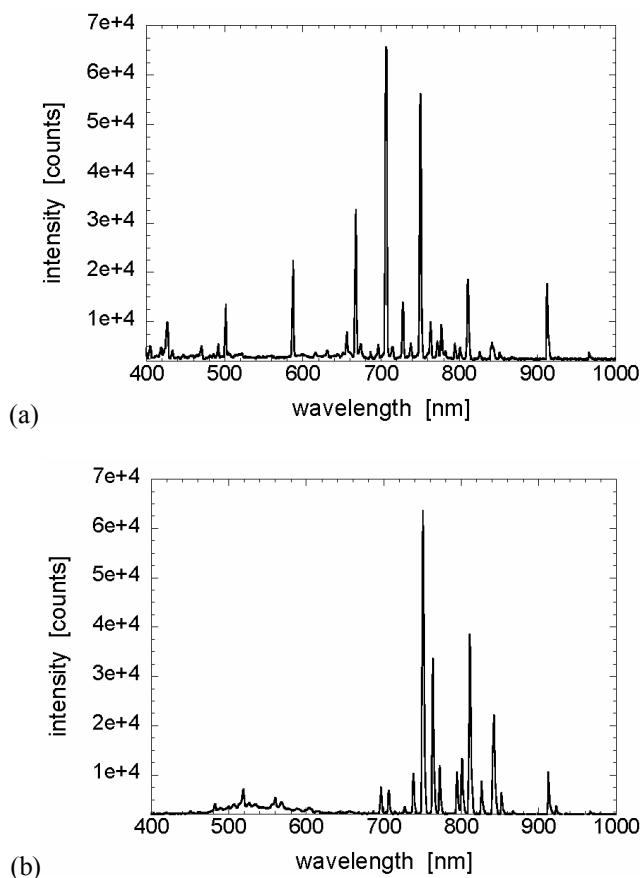


Fig. 8: Optical spectra of plasma discharges on the microfabricated chips ignited in He at 50 mbar with 350 mW RF power (a), and in Ar at 200 mbar with 670 mW (b).

## 5. CONCLUSION

Hermetically sealed cells enclosing interdigitated electrodes have been fabricated in glass. These devices have been used to generate low-power millimeter-size plasma discharges operating continuously in He or Ar at pressures ranging from 10 to 500 mbar. Future work will include a more comprehensive study of the effect of electrode geometry, gas type and pressure on the characteristics of the plasma discharge (power required for ignition, intensities of different lines). The goal is the determination of the most suitable electrode geometry enabling the ignition of a stable and long-term operation glow discharge with the lowest RF power level at a given gas pressure. The proposed sealed plasma light sources will find applications in chip-scale atomic clocks and allow direct spectroscopy of gases in sealed cavities, for instance for long-term leak testing of wafer-level packaged devices.

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