Proceedings of the 3rd IEEE Int. Conf. on
Nano/Micro Engineered and Molecular Systems
January 6-9, 2008, Sanya, China

Sub-100 nm-scale Aluminum Nanowires by Stencil Lithography: Fabrication and Characterization

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***Abstract*— We present the fabrication process and electrical characterization of sub-100 nm scale Al nanowires (NWs) fabricated by stencil lithography (SL). We use a stencil with sub-100 nm wide nanoslits patterned by focused ion beam (FIB) milling. The stencil is aligned and clamped onto a substrate containing predefined electrical contacts. Then a 60 nm-thick layer of Aluminum (Al) is deposited through the stencil producing NWs with lengths of ~1, 2 and 5 μm and widths down to 65 nm. The NWs show an ohmic behavior with values varying from 30 Ω up to 300 Ω, depending on the dimensions of the structures. We have extracted a resistivity for the Al NWs of ~10 x 10^{-8} Ωm. We also show that stencils can be cleaned and reused, proving that SL is a cost-efficient and scalable manufacturing method for the direct fabrication of metallic NWs on a full wafer scale.**

Keywords- nanowires, stencil lithography

I. INTRODUCTION

Nanowires are expected to become important components for the coming generation of micro and nanoelectronic devices [1, 2]. Their novel physical properties and their favorable surface-to-volume ratio make them excellent candidates for electronic [3, 4], and sensing applications [5]. The two main approaches for the fabrication of nanowires have been the bottom-up and top-down approach. The bottom-up method is based on the chemical/physical assembling of atoms into well defined nanostructures [6]. This technique offers highly crystalline structures, however, the positioning of the nanowires and their integration into current technological platforms is still a major problem. The top-down approach is based on the lithographic definition of nanostructures followed by material deposition or etching [7, 8]. This method allows a high control of the positioning of the structures and is based on standard microfabrication methods, facilitating the integration with current technologies. However, this approach requires complex and costly equipment like E-Beam (EBL) or Deep Ultra-Violet (DUV) lithography.

Stencil lithography (SL) is a novel technique for the fabrication of nanostructures [9, 10]. It is based on shadow mask evaporation and it allows the patterning of diverse materials and substrates without the need of any resist processing (Fig. 1) [11]. Recently, SL was used to fabricate sub-micron resonators on CMOS circuits [12], showing the capability of the technique for high resolution patterning and its integration into current microelectronic fabrication methods. The stencils can also be used multiple times, offering a potentially low-cost, efficient and reusable tool [13].

In this contribution we report the fabrication of sub-100 nm Al NWs using stencil lithography. We describe the stencil fabrication process and characterize the NWs obtained after an Al deposition through a stencil. We extract the wire resistivity from their resistance and dimensions. Finally, we show that the stencils can be reused for the fabrication of Al nanowires.

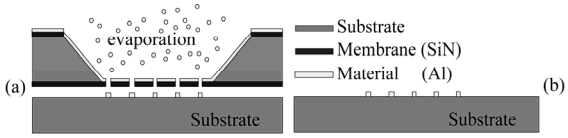

Figure 1. Deposition process by stencil lithography. (a) The stencil is placed on top of the substrate and material is evaporated through the membrane apertures onto the substrate. (b) After deposition, the stencil is removed from the substrate.

II. STENCIL FABRICATION

The fabricated stencils have 100 nm thick low-stress silicon nitride membranes supported by a conventional silicon wafer. The membranes are reinforced by micrometric corrugations that increase their moment of inertia [14] and release the stress, making them more stable. The stencils contain micrometric apertures fabricated with conventional UV lithography and nano-apertures defined by FIB milling.

The fabrication process is shown in Fig. 2. First, we define trenches on the surface of a Si wafer with conventional photolithography and a dry etching process (Fig. 2a). Then we deposit 100 nm of low stress Silicon Nitride (LS SiN) by chemical vapor deposition (Fig. 2b). We then use conventional UV lithography and SiN dry etching to define the micrometric apertures (3-5 μm) of the stencil. On the backside we open windows in the silicon nitride for the bulk Si etching (Fig. 2c). The Si is etched using anisotropic KOH etching (Fig. 2d). Once the membranes are released, we use FIB milling to fabricate the nanoslits (Fig. 2e) in between the micro-apertures.

Fig. 3 shows a SEM picture of the fabricated stencil. The width (w) of the nanoslits ranges from 150 nm down to 50 nm with lengths (L) of ~1, 2 and 5 μm. The micro-apertures facilitate the electrical contact of the predefined pads to the NWs. Fig. 4 shows a closer picture of an aperture in a stencil

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membrane. It consists of a nanoslit with L=5 μm and w=50 nm.

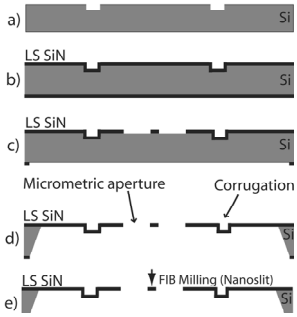

Figure 2. Stencil fabrication and deposition. a) Definition of corrugations on silicon. b) LS SiN deposition. c) Patterning of membrane apertures and backside apertures. d) Membrane release using KOH etching. e) Patterning of nanoapertures using FIB milling.

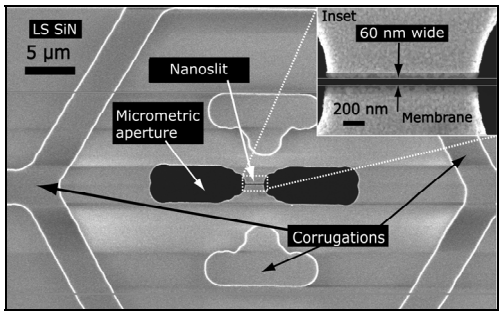

Figure 3. Stabilized stencil membrane**.** Stencil membrane containing corrugations, micrometric apertures and a nanoslit. Inset: Close up of the 60 nm wide nanoslit.

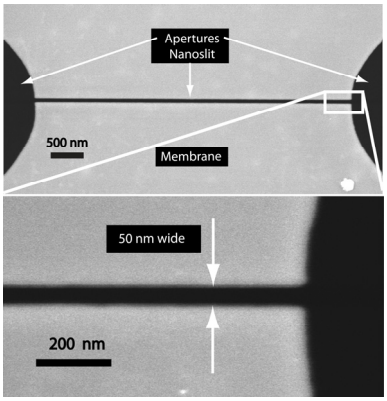

Figure 4. Aperture in a stencil membrane. Top) The aperture consists of a nanoslit 5 μm long and 50 nm wide in between two micron-sized apertures. Bottom) Close-up of the nanoslit.

III. NANOWIRE FABRICATION

To fabricate the Al nanowires we have used the stencils described in the previous section. Before the deposition of the Al, the stencil is aligned and clamped onto a substrate using a bond wafer aligner with a modified chuck. The stencil-substrate configuration is illustrated in Fig. 5. As shown, there is an inherent gap between the stencil and the substrate due to the wafer's curvature. This gap causes a blurring of the structures (size enlargement) that limits the resolution of the pattern transfer from the stencil to the substrate. This gap lies typically between 5 and 20 μm when full wafer (100 mm diameter) stencil and substrate are used.

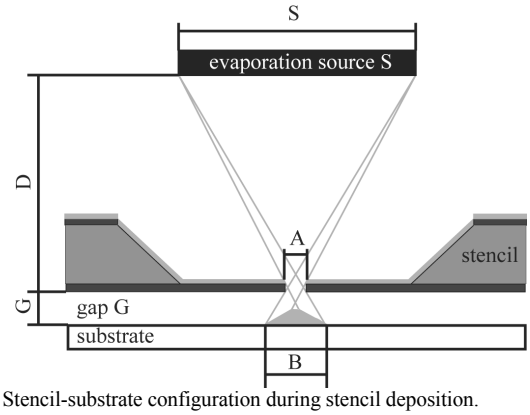

Fig 5. Stencil-substrate configuration during stencil deposition.

The substrate used has a 200 nm thick silicon oxide layer and it contains alignment markers and predefined contact pads (Pt 40 nm / Ti 5 nm) to measure the electrical properties of the structures deposited through the stencil. After the alignment of the stencil and the substrate, they are put into an evaporator for the e-beam physical vapor deposition of 60 nm thick Al. The Al is deposited at a rate of 5 A/sec. The Al that passes through the nanoslits forms nanowires on the substrate. Fig. 6 shows an SEM micrograph of the Al structures deposited through the stencil and the predefined contacts.

In Fig. 7 we show a nanowire deposited by SL through the aperture shown in Fig 4 (aperture dimensions: L=5 μm and w=50 nm). Fig. 7a and 7b are the SEM images showing a length of 5 μm and a width of 65 nm. Fig. 7c and 7d are Tapping Mode AFM images of the structure using a tip with a nominal 10 nm radius. From Fig. 7d we measure a nanowire width of 65 nm, which corresponds to the measurement from the SEM image. Fig. 7e shows two cross-sections (CS1 and CS2) extracted from Fig. 7c through the white vertical lines [15]. CS1 corresponds to the structures deposited through the micrometric apertures while CS2 corresponds to the nanowire.

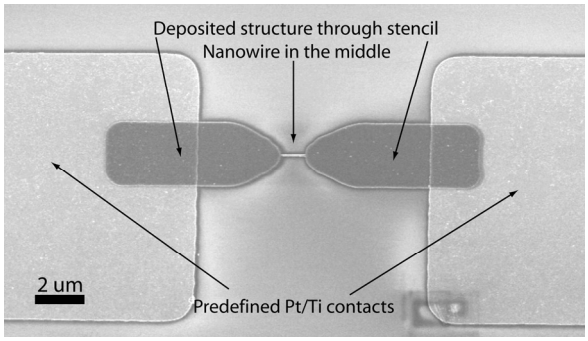

Figure 6. Al structure and Ti/Pt contacts**.** Al structure (60 nm thick) aligned and deposited in between the predefined contacts (Ti 5 nm/ Pt 45 nm).

Fig. 8 illustrates two NWs of 1 and 2 µm in length. Fig 8.a shows a nanowire with L=2 µm and w=80 nm. The corresponding stencil aperture has a length L=2 µm and a width w=75 nm. In Fig 8.b the nanowire is 1 µm long and 75 nm wide. The stencil aperture has a length L=1 µm and width w=65 nm.

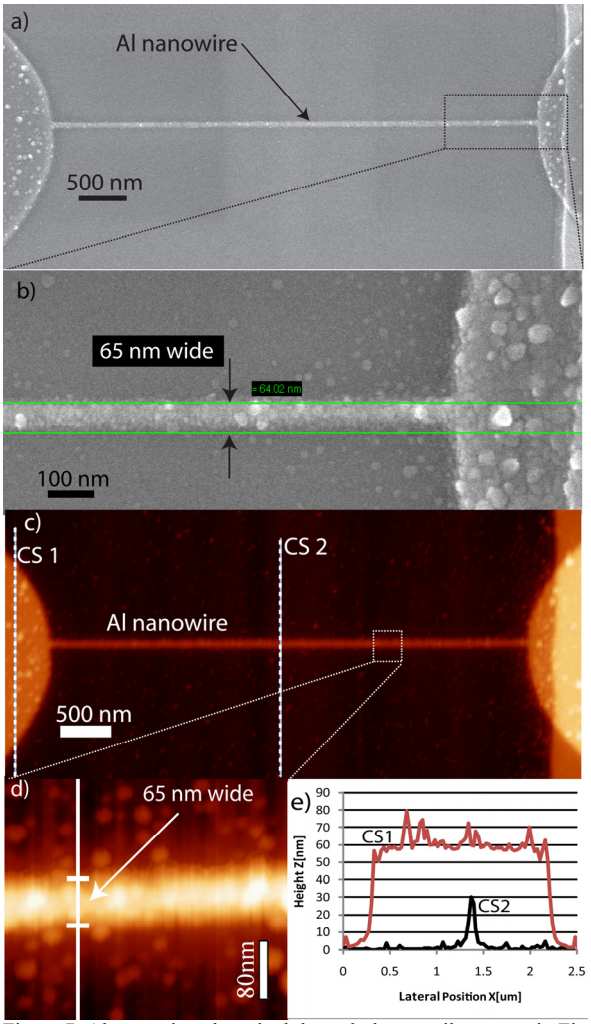

Figure 7. Al nanowires deposited through the stencil aperture in Fig 4. a) SEM image of the 5 µm long Al NW. b) Close up from the SEM image. Width of the nanowire: 65 nm. c) TM AFM image of the same NW. d) AFM close up showing w=65 nm. e) Cross sections of the micrometric structures (CS1) and the nanowire (CS2) extracted from white vertical lines in the AFM image in c).

From the SEM and AFM analysis, we observe that the nanowires have a poly-crystalline structure with different grain sizes between 5 and 30 nm. We also measured that the thickness of the deposited nanowires is smaller than the thickness of the micron-sized structures. AFM measurements show that the structures deposited through the micron-sized apertures have a thickness of 60 nm (CS1 in Fig. 7e), corresponding to the nominal value set for the deposition controller of the evaporator. However, the thickness of the nanowire is 30 nm (CS2 in Fig. 7e). We believe that the flux of material through the nanoapertures is lower compared to the micron-sized apertures. Due to clogging (reduction in size aperture due to material deposition), the width of the apertures is also gradually decreased during evaporation [13, 16]. This reduces the amount of material passing through the apertures, thus affecting the thickness of the deposited structures. Further analysis is ongoing to find the effect and relation of the width of the apertures and the thickness of the deposited structures

The blurring due to the inherent gap between the stencil and substrate is observed in Fig. 7d. As shown, there is some material deposited on the sides of the nanowire. This blurred part forms a thin layer <5 nm thick and grains around the nanowire.

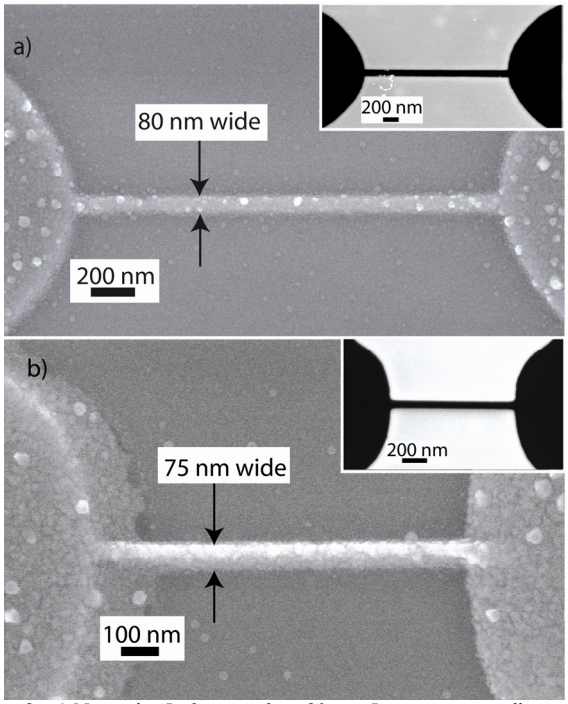

Figure 8. a) Nanowire L=2 µm and w=80 nm. Inset: corresponding stencil aperture: L=2 µm, w=75 nm. b) Nanowire L=1 µm and w=75 nm. Inset: corresponding stencil aperture: L= 1 µm, w= 55 nm.

IV. ELECTRICAL CHARACTERIZATION

The electrical resistance of the wires was measured in DC mode at room temperature using a probe station. The Al nanowires were contacted using the Ti/Pt predefined contacts. In Fig. 9 we show three nanowires of 2 µm in length and their corresponding current *vs.* voltage (I *vs.* V) curves. The wires show the characteristic linear behavior for metals of the current as a function of the voltage (Ohm's law). The resistance R of the wires increases as the width decreased, as expected from the expression for the resistance of a conductor

$$R=\rho L/wt \qquad (1)$$

where ρ is the resistivity and t the thickness of the structure.

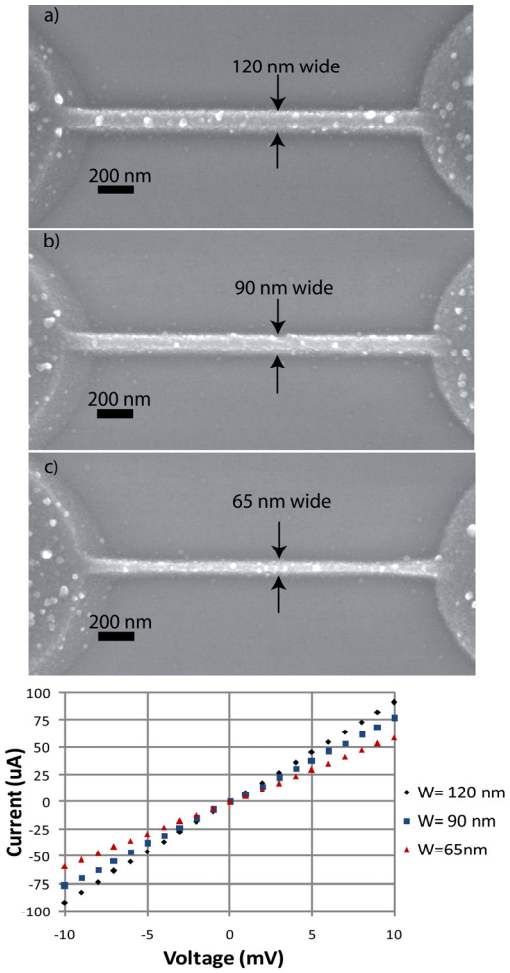

Figure 9. Al nanowires and I *vs.*V curves. a,b,c): Three different Al NWs 2 µm long. Their respective widths are 120, 90 and 65 nm. The graph shows the I *vs.*V curves for each of the wires. The respective resistances are 105 Ω, 120 Ω and 170 Ω, including the contact resistance (~ 70 Ω).

Fig. 10 shows the resistances of the NWs as a function of the inverse of the width for lengths of 1, 2 and 5 µm. For this analysis, the contact resistance was estimated (~70 Ω) by extrapolating the values of the measured resistances for $w \rightarrow \infty$ and then subtracting it for each measured nanowire resistance. The resistance increases when the width of the nanowires is reduced and the slope of the curves is proportional to the length of the wires, as expected from (1). The extracted resistivity of the structures is ρ_{NW}=10±1.7 µΩcm using a thickness of 30±5 nm. This value is higher than the bulk resistivity of Aluminum ρ_0=2.65 µΩcm.

It is known that the conductivity of metal thin films and nanowires decreases when the scale lengths are comparable or smaller than the electronic mean free path (EMFP). This is due mainly to grain boundaries and surface scattering [17]. Fuchs and Sondheimer [18] studied the effect of surface scattering on the resistivity of nanowires when the dimensions are smaller than the EMFP. Later, Mayadas and Shatkes [19] demonstrated the effect of the scattering at grain boundaries on the conduction of electrons for thin films with thickness comparable to the EMFP.

In the case of bulk Al, the EMFP is ~15 nm [20]. Since the NWs we have fabricated present a grainy structure in the 5-30 nm range, we believe that grain boundary scattering plays an important role in the electrical conductivity of NW deposited through stencils. Even though the thickness of the deposited wires is larger than the EMFP, the roughness of the surface may increase the effect of the surface scattering as well.

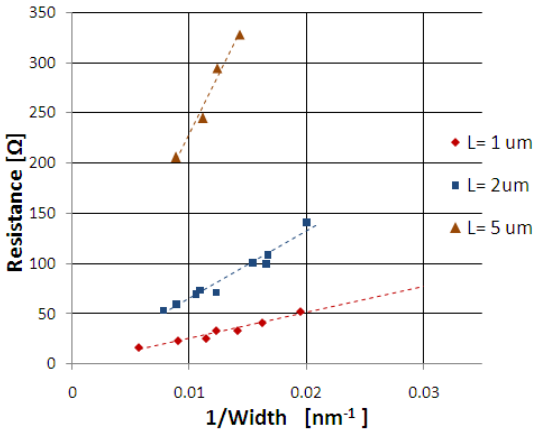

Figure 10. Resistance as a function of length and width. The resistance increases as the width decreases. The slope of the curves is also proportional to the length of the wires.

V. REUSABILITY OF STENCIL

As mentioned before, the material deposited on the stencil accumulates in the edge of the apertures, reducing the size of the apertures and eventually closing them completely. This reduces the usable-life of the stencils containing nanoapertures. To solve this problem, we have removed the Al deposited using a conventional wet etching solution based on nitric and phosphoric acid. Fig. 11 shows a stencil aperture after the evaporation of 50 nm of Al, where the deposited Al has reduced the size of the aperture. After the Al removal, the aperture recovers its original width and the stencil remains intact without any observable damage. Using the same Al removal procedure, we have been able to use the same stencil (used for these experiments) 12 times so far, achieving sub-100 nm Al nanowires[13].

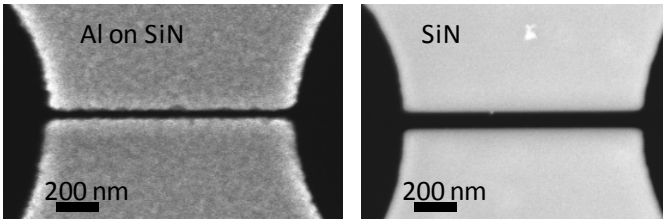

Figure 11. Stencil clogging and cleaning. Left: Clogged stencil membrane after 50 nm Al evaporation. Right: Stencil after Al removal.

VI. CONCLUSIONS

We have demonstrated that stencil lithography is capable of patterning sub-100 nm Aluminum nanowires using a full wafer stencil. The fabrication of NW using stencils is fast and clean process. The fabricated stencils are stable and contain sub-100 nm features. The Al NWs show the expected ohmic behavior and a higher resistivity compared to Al bulk due to known size effects. Since the stencils can be used multiple times, they are a cost-effective tool for the patterning of nanowires. These results show that stencil lithography is a novel and versatile technology that offers new capabilities for low cost nanowire patterning.

ACKNOWLEDGMENT

This effort is sponsored by the Swiss Federal Office for Science and Education (OFES) in the framework of the EC-funded FP6 project NaPa (NMP4-CT-2003-500120), the Swiss National Science Foundation (Project IC-Nano, 200021-112291/1) and the EPFL-STI Seed Funding. The authors are very grateful to the EPFL Centre of Micro-Nano-Technology and its entire staff, as well as to our colleagues at the Microsystems Laboratory for their very valuable support and help.

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