ASIC for high speed gating and free running operation of SPADs

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ABSTRACT

Single photon detection at telecom wavelengths is of importance in many industrial applications ranging from quantum cryptography, quantum optics, optical time domain reflectometry, non-invasive testing of VLSI circuits, eye-safe LIDAR to laser ranging. In practical applications, the combination of an InGaAs/InP APD with an appropriate electronic circuit still stands as the best solution in comparison with emerging technologies such as superconducting single photon detectors, MCP-PMTs for the near IR or up-conversion technique.
An ASIC dedicated to the operation of InGaAs/InP APDs in both gated mode and free-running mode is presented. The 1.6mm^2 chip is fabricated in a CMOS technology. It combines a gate generator, a voltage limiter, a fast comparator, a precise timing circuit for the gate signal processing and an output stage. A pulse amplitude of up to +7V can be achieved, which allows the operation of commercially available APDs at a single photon detection probability larger than 25% at 1.55µm. The avalanche quenching process is extremely fast, thus reducing the afterpulsing effects. The packaging of the diode in close proximity with the quenching circuit enables high speed gating at frequencies larger than 10MHz. The reduced connection lengths combined with impedance adaptation technique provide excellent gate quality, free of oscillations or bumps. The excess bias voltage is thus constant over the gate width leading to a stable single photon detection probability and timing resolution. The CMOS integration guarantees long-term stability, reliability and compactness.

Keywords: Single photon detection, active quenching, InGaAs/InP avalanche photodiode, gated-mode, CMOS technology

1. INTRODUCTION

Single photon detection at telecom wavelengths has received a growing interest since the mid-1990's. Though Germanium APDs (avalanche photodiodes) were initially tested in the single photon counting regime [1][2], they have to be cooled at liquid nitrogen temperature and are not efficient at 1550nm. Near-IR PMT-MCPs (photomultiplier tubes – microchannel plates) based on InP/InGaAs or InP/InGaAsP photocathodes are commercially available but suffer from a poor single photon detection probability, typically less than 1%. More recently, approaches employing superconducting materials have been proposed and tested [3]. However, because of their cooling requirements, 4K or lower, these detectors are today impractical for most applications and high-T_c superconducting films have to be developed [4]. In [5], Thew et al. proposes a hybrid single photon detection scheme based on non linear sum-frequency generation and silicon SPADs (single photon avalanche diodes). Though promising timing resolution and detection probability have been obtained, the detection scheme still suffers from a large dark count rate.
Small bandgap InGaAs/InP APDs were early acknowledged as the most efficient way to detect single photons at telecom wavelengths [6][7]. An impinging photon absorbed in the narrow bandgap InGaAs layer generates a macroscopic current pulse by successive impact ionizations in the larger bandgap InP layer. Up to now, two techniques have been separately used or combined to operate the InGaAs/InP APDs in the Geiger mode. First, when the arrival time of the photons on the detector is known, the diode can be biased above breakdown voltage for a set time window. In the so-called gated mode [6][8][9], a trigger signal is used to apply a gate to the detector. Photons can only be detected within this gate of typical duration of a few nanoseconds. The trigger signal is often a high frequency and large amplitude square signal with excessively well defined rise and fall times. The generation of a carrier within the junction by the absorption of a single photon triggers a macroscopic self-sustaining avalanche current. The avalanche quenching is efficient at the falling edge of the gate pulse. Precise timing circuits are required to differentiate between an avalanche

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signal and the end of the gate. Periodical signals can also be applied on the APD: in [10] for instance, a sine wave gating operation is proposed. If gated mode is essential to reduce noise, synchronous operation is unfortunately not well suited to applications like in spectroscopy, biology or astronomy, where photons usually do not arrive at a predefined time. These fields represent however a very interesting market for high-sensitivity detectors.

When the diode is operated in asynchronous mode or in gated mode with gate duration larger than typically 10ns, an active quenching circuit must be used [11]. In this mode, a remote active quenching circuit senses the avalanche current pulse and quickly reduces the voltage below breakdown to stop the impact ionization process. The operating voltage is then restored after a so-called hold-off time. The feedback loop duration must remain as short as possible in order to limit the number of carriers that flows in the diode during a Geiger pulse and thus the afterpulsing rate.

Several commercial detector modules are based on these operating schemes (see for instance, [12]) and have been used in worldwide research laboratories. They found applications in quantum cryptography, LIDAR, quantum optics, failure analysis of electronic circuits, single photon source characterization, optical fiber testing and spectroscopy. The InGaAs/InP APD is often cooled with a multi-stage Peltier element and combined with a quenching circuit made of discrete components. Because of form factor and power consumption considerations, the electronic circuit cannot be included in the cooled enclosure where the APD is located. This causes an increase of the quenching time which degrades the detector performance, more specifically due to large afterpulsing rates. Furthermore, the APD must be connected to the circuit by cables. Because of impedance mismatch, signal reflections occur. The applied voltage during the gate is thus non-uniform leading to important variations of the single photon detection probability and timing resolution over the gate. This non-uniformity is highly problematic in applications such like optical fiber characterization by OTDR (optical time domain reflectometry) or failure analysis of electronic circuits, when long gates are required. In addition to the performance limitations of the current devices, two significant trends make their improvements essential. First, some applications are mature for large scale industrialization. Quantum cryptography [13] addresses highly demanding markets: encryptor production costs must be controlled, a high degree of reliability and long-term stability are required, and system miniaturization is at times desirable. Second, and besides the obvious requirement of larger signal-over-noise ratio shared by all the applications, single photon detection at higher frequencies becomes progressively crucial. Among other applications, quantum cryptography and VLSI circuit testing would benefit from a high-speed gating scheme.

A fully integrated electronic circuit that can be placed in close-proximity with the APD and can provide high-speed gating or asynchronous operation modes is thus desirable. In this paper, we present a CMOS integrated ASIC, called idQ-P, optimized for the operation of state-of-the-art commercial InGaAs/InP APDs in both gated and free-running modes. The idQ-P is first presented in Section 2. The performances, including the dark count rate and afterpulsing, the single photon detection probability and its uniformity over the gate, and the timing resolution, are discussed in Section 3 while conclusion and outlooks are provided in Section 4.

2. IDQ-P ASIC PRESENTATION

A photomicrograph of the idQ-P ASIC is shown in Figure 1. The 1.6mm^2 chip is fabricated in an industrial 0.8µm CMOS technology. The process is qualified for automotive applications, thus assuring a high degree of reliability. Furthermore, it is well modeled at low temperatures making the circuit simulation efficient. The idQ-P block diagram is provided in Figure 2. It is subdivided in separate blocks which can be identified in Figure 1 as well. In order to operate in the gated mode, the APD must be biased above its breakdown voltage V_{bd} during defined gate duration at a given frequency. In between the gates, the APD remains below breakdown. Using the idQ-P ASIC, the APD cathode is connected to node C via a pad, while the anode is biased to the negative operating voltage V_{op} as shown in Figure 2. At node C, the idQ-P produces fast rising and falling edge pulses of amplitude equal to the power supply VDD. During a gate, the APD is thus biased to VDD+$|V_{op}|$ which exceeds the breakdown voltage V_{bd}. Between the gates, the voltage at node C is GND, i.e. V_{op} must remain lower than V_{bd}. Though supply voltage up to 7V can be applied without damages or performance degradation, VDD has been set to +5V for the experiments presented in Section 3.

The gate width and frequency are externally controlled through the GATE-IN input pad shown in Figure 2. For a proper operation, the signal amplitude must reach 2,5V. A level shifter converts the GATE-IN signal to GND/VDD pulses. The level shifter output pulse generates two correlated pulses for the command of the large p-mos and n-mos switches. The w/l ratios of the command switches are large enough to provide gate pulses with extremely fast rising and falling edges. As shown in Figure 2, the switch power supply VDD-SW is thus decoupled to the power supply of the remaining building blocks. A short duration charge pulse is provided to the p-mos switch in order to load the APD cathode to

VDD. The charge pulse duration is set with an inverter chain. It is adjustable with PR-TRIM0 and PR-TRIM1 input pads allowing the charge optimization with the APD and parasitic capacitances. Prior to the p-mos switch closing, the n-mos switch is open. It remains open until the end of the gate when no avalanche is triggered or until active quenching when a photon triggers an avalanche during the gate. The parallel buffer chains for the control of the command switches are identical to reduce signal skews and avoid conduction overlapping during the charge. However, a short delay made of two inverters is added on the p-mos command path to ensure no overlapped conduction of both switches.

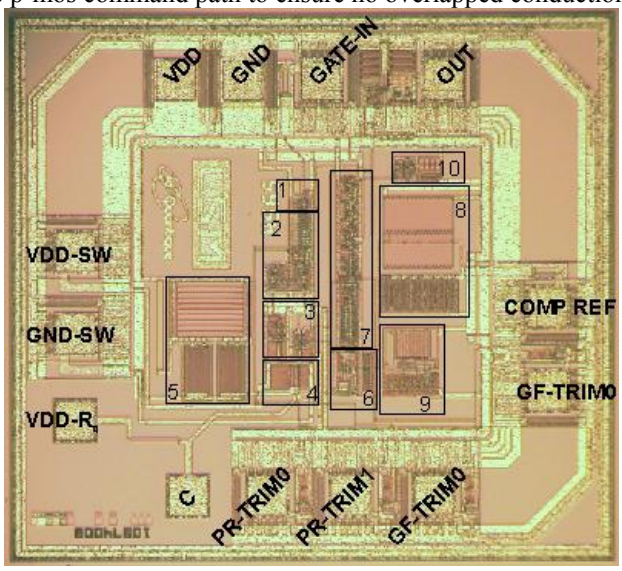

Fig. 1. Photomicrograph of the idQ-P pulser ASIC. The different building blocks can be seen: 1-level shifter, 2-pulse generator, 3-buffer chain, 4-command switches, 5-limiter, 6-comparator, 7-glitch filter & synchronization stage, 8-comparator voltage reference, 9-comparator current reference, 10-power on reset.

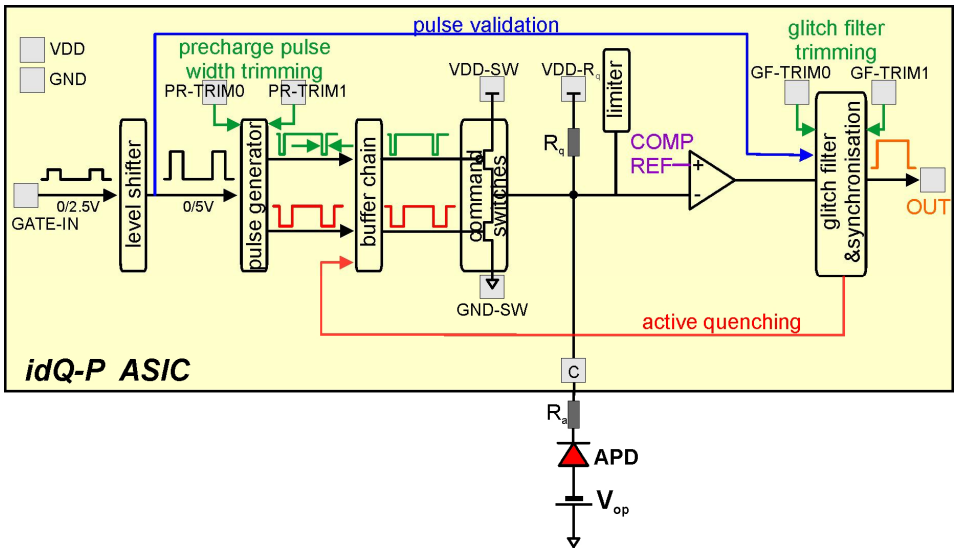

Fig. 2. idQ-P block diagram and its connection to the avalanche photodiode.

Figure 3 provides a timing diagram showing the idQ-P basic operation. The charge pulse applied to the p-mos switch can be seen as well as the quenching pulse on the n-mos transistor gate. If an avalanche is triggered during a gate, the avalanche current induces a voltage drop over R_q. The voltage drop at node C is equal to the excess bias voltage V_e, with $V_e=VDD+|V_{op}|-V_{bd}$. When the voltage at node C crosses the comparator reference COMP REF, the comparator output switches to VDD. The transition is reflected through the glitch filter and synchronization stage at the chip output

(phase 1 in Figure 3). An active quenching feedback signal is sent to the buffer chain stage. The n-mos switch is then closed (phase 2 in Figure 3) allowing an active quenching of the avalanche (phase 3 in Figure 3). One can note that when no avalanche occurs within the gate, the gate falling edge is sensed at node C by the comparator and might be reflected at the chip output. The synchronization and glitch filter stage avoids the mixed-up of the end of the gate and a photon detection by providing a pulse validation. The GF-TRIM0 and GF-TRIM1 input pads allow the adjustment of the timing selection performed at the synchronization and glitch filter stage.
In addition, when an avalanche occurs within a gate, the feedback signal sent to the buffer chains induces an on-chip dead time equal to the GATE-IN signal period. The gate following a detection is thus cancelled by the buffer chain (phase 4 in Figure 3) and the idQ-P output remains high until its falling edge (phase 5 in Figure 3). The on-chip dead time is of interest when the system operates at high frequencies. Indeed, commercially available InGaAs/InP APDs exhibit detrimental afterpulsing effects. At usual working temperature (typically -50°C), a dead time of up to 10µs must be applied. Assuming that the APD and the idQ-P ASIC are combined with a remote hardware that sequentially -generates the GATE-IN signal, -recovers the output pulse, -applies a dead time, it may take several nanoseconds to complete this loop. Following a detection, a GATE-IN signal might be sent before the dead time enforcement. The internal dead time provides an additional duration for this feedback loop.

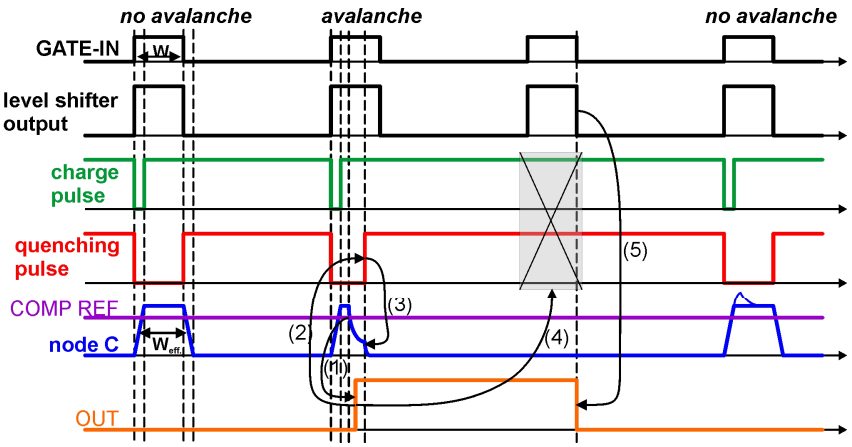

Fig. 3. Timing diagram describing the idQ-P basic operation.

Besides, for ensuring a high uniformity of the applied voltage within the gate, a voltage limiter made of two diodes and a RC filter is implemented as shown in Figure 2. As suggested by the pulse on the right in Figure 3, the extra charges resulting from the injection during the p-mos transistor closing are absorbed by the filtering capacitance. A stable single photon detection probability, directly linked to the excess bias voltage, is thus expected over the gate. To further improve the uniformity, a SMD resistor R_a is placed between the GATE-IN pad and the APD cathode to find the best compromise between charge speed and RLC oscillation damping.
Finally, the idQ-P can be operated in the free running mode by applying a high level at the GATE-IN output until an avalanche triggering. In order to detect a subsequent photon, the external board must successively send a pulse of short duration and restore the high level at GATE-IN pad.

3. IDQ-P PERFORMANCES

The experimental set-up is first described in Section 3.1. The pulser performances including the dark count rate and afterpulsing, the single photon detection probability and its uniformity over the gate, and the timing resolution are successively presented in Section 3.2.

3.1 Experimental set-up

An experimental set-up schematic used for the idQ-P characterization is provided in Figure 4. A low dark current ETX-40 InGaAs/InP APD from JDS Uniphase is mounted on the top of a 4-stage TEC (thermo-electric cooler). The APD is

pigtailed to a single mode fiber. The TEC hot plate is glued on a heat sink cooled by an air fan. The idQ-P ASIC is mounted and wire-bounded on a flexible printed circuit board. Decoupling capacitances for V_{op} and VDD power supplies are added in close proximity with the silicon chip. In order to regulate the APD temperature at -50°C, two thermistors are used: a SMD thermistor mounted on the PCB for the cold side, a discrete thermistor for the hot side temperature control.

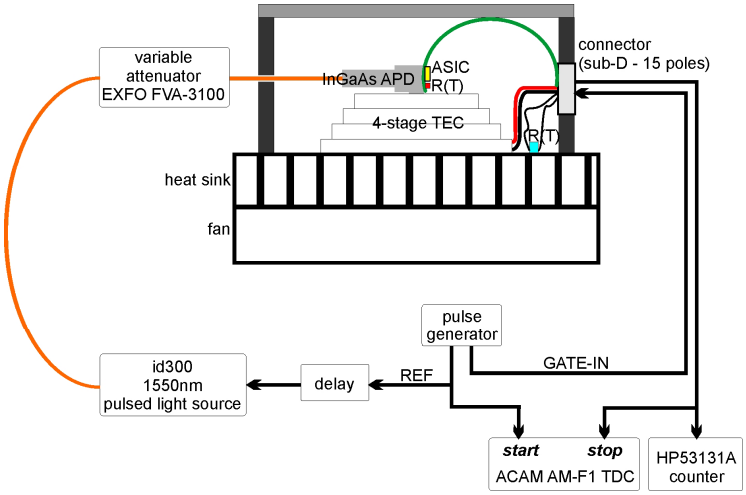

Fig. 4. Experimental set-up description.

A home-made pulse generator provides two signals (GATE IN and REF) whose frequency can be selected from 1Hz to 120MHz. The pulse duration and timing delay between the signals can be adjusted by step of 100ps. The reference signal triggers a id300 short-pulse laser source from idQuantique. The source is based on a Fabry-Perot laser diode emitting at 1550nm. The id300 optical power is measured with a EXFO PM-1600 power meter. The mean number of photons per pulse sent in the pigtailed APD is adjusted with a EXFO FVA-3100 variable attenuator. The delayed reference signal is adjusted to send the light pulse within the gate. The detection output feeds a HP53131A counter. For the timing resolution measurement, a ACAM AM-F1 time-to-digital converter is used. The start signal is given by the pulse generator while the stop is provided by the detection output.

3.2 idQ-P performances

3.2.1 Dark count rate and afterpulsing

In any APD, avalanches are not only cause by the arrival of a photon on the detector but can be generated by thermal, tunneling or trapping processes taking place in the junction. If the used electronic circuit has in theory no impact on thermal and tunneling generations which are intrinsic features of the APD itself, the operating scheme can have a significant impact on the afterpulsing probability. Afterpulsing is probably the major problem limiting the performance of commercial InGaAs/InP APDs. This effect arises from the trapping of charge carriers during an avalanche event by levels inside the high field region of the junction. When subsequently released, these trapped carriers can trigger afterpulses. Obviously, the larger the number of carriers that flows in the APD during a Geiger pulse, the larger is the trapping probability.

In Figure 5, the dark count rate has been measured as a function of the applied voltage V_{op} at trigger frequencies ranging from 10Hz to 1MHz and for a 100ns GATE-IN pulse width. The operating temperature was -50°C. For an accurate evaluation of the dark count rate per nanosecond of gate, two corrections have been done on the measured output count rate. First, the GATE-IN signal width slightly differs from the effective gate width in which avalanches are detected. This difference is explained by the cathode node charge duration at VDD and by the timing selection at the end of the gate. A direct measurement of the gate width at node C (see Figure 2) would irremediably result in signal distortions. Consequently, the effective gate width has been indirectly measured by the acquisition of a noise histogram using the TDC. Second, the idQ-P internal dead time results in an effective trigger rate decrease when the output count rate increases. The measured output count rate has been corrected using the well known formula:

$N_{corrected} = N_{measured} / (1 - N_{measured} \times \text{dead time})$.

As can be seen in Figure 5, the dark count rate increases with the applied voltage V_{op} on the 5V useful voltage range.

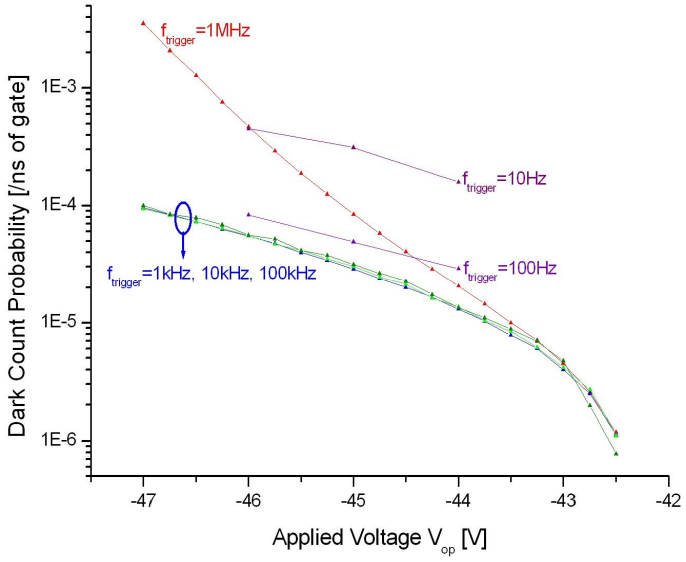

Fig. 5. Dark count rate versus V_{op} at different trigger frequencies.

Whatever V_{op}, i.e. whatever the excess bias voltage, the measurements at 1kHz, 10kHz and 100kHz are almost superimposed, revealing a negligible afterpulsing rate. Please note that the corresponding internal dead times are respectively 1ms, 100µs and 10µs. These acquisitions set the floor level where the dark count rate is not enhanced by the afterpulsing rate. At lower trigger frequencies of 100Hz and 10Hz, a significant noise increase is visible. This 1/f behavior was previously observed with other quenching circuits made of discrete components. Consequently, this effect is confirmed to be an intrinsic feature of the APD itself. At 1MHz (corresponding internal dead time of 1µs), the dark count rate is increased by the afterpulsing. When V_{op} is raised, the gap with the floor level becomes larger. Indeed, the number of trapped carriers and the probability for a released carrier to induce an afterpulse increase with the excess bias voltage.

In Figure 6, the dark count rate is plotted as a function of the single photon detection probability. The measurement has been done with the same diode combined with the idQ-P and a remote active quenching circuit made of discrete components. The operating conditions are strictly identical: the temperature is -50°C, the trigger frequency is 1MHz, a dead time of 1µs is applied following a detection, and the gate width is 100ns. The positive impact of the idQ-P is clearly visible. If the remote quenching circuit leads to saturation (avalanche within each 100ns gate) at high detection probability levels, the saturation is definitely not observed with the idQ-P. At high excess bias voltages, the afterpulsing rate is strongly reduced. Indeed, the idQ-P connection to the APD cathode consists of a 5mm length wire on the flexible board, minimizing the parasitic capacitance. The charge in the Geiger pulse is then limited favoring the trapping reduction. In addition, the number of carriers is further limited by the fast active quenching. According to simulation, a quenching time of less than 5ns is expected.

3.2.2 Single photon detection probability and uniformity over the gate

The single photon detection probability results from three factors: the optical coupling efficiency from the optical fiber onto the detector active area, the probability of photon absorption in the InGaAs layer and the probability that the photogenerated carriers trigger an avalanche by successive impact ionizations. The operating mode, i.e. asynchronous or asynchronous, and the quenching circuit should in principle have no influence on the single photon detection probability. However, the quenching circuit sets the operating voltage range and thus the maximum and minimum detection probability levels that can be reached. In Figure 6, one can see that the idQ-P allows the operation of commercial InGaAs/InP APDs from less than 5% up to 22% detection probability level. Please note that a higher detection probability up to 25% can be reached when the power supply VDD is raised to 7V.

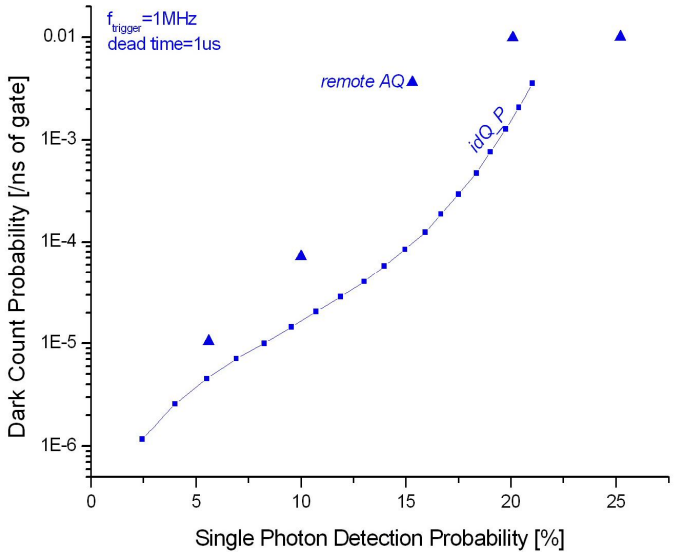

Fig. 6. Single photon detection probability versus dark count probability using the idQ-P and a remote active quenching circuit.

Moreover, the quenching circuit and its connection to the APD can impact strongly on the photon detection uniformity over the gate. In Figure 7 (respectively in Figure 8), the laser pulse has been shifted over a 100ns (respectively 3ns) gate. Only minor variations are observed whatever the single photon detection probability level. The beginning of the gate is free of large oscillations thanks to the cable length limitation, to the voltage limiter and the optimization performed with the resistor R_a. When several peaks must be distinguished within the gate, this uniformity is crucial. This is for instance the case in the measurement of the transistor switching frequencies for non-invasive tests of VLSI circuits.

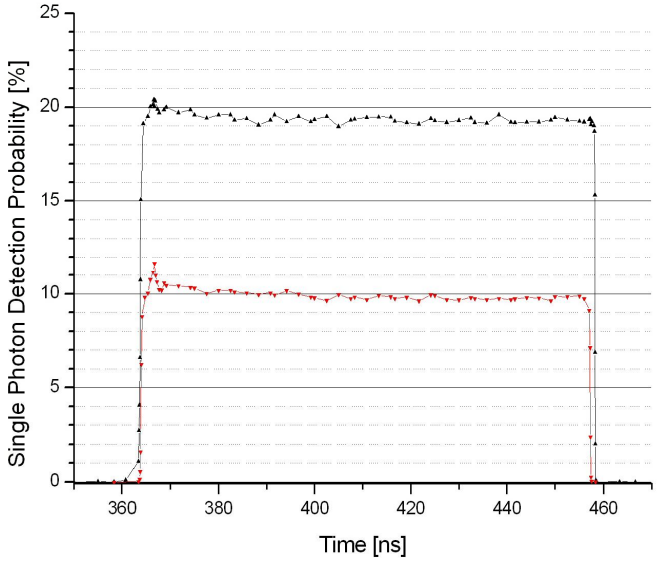

Fig. 7. Single photon detection probability uniformity over a 100ns gate. Levels at 10% and 20% are shown.

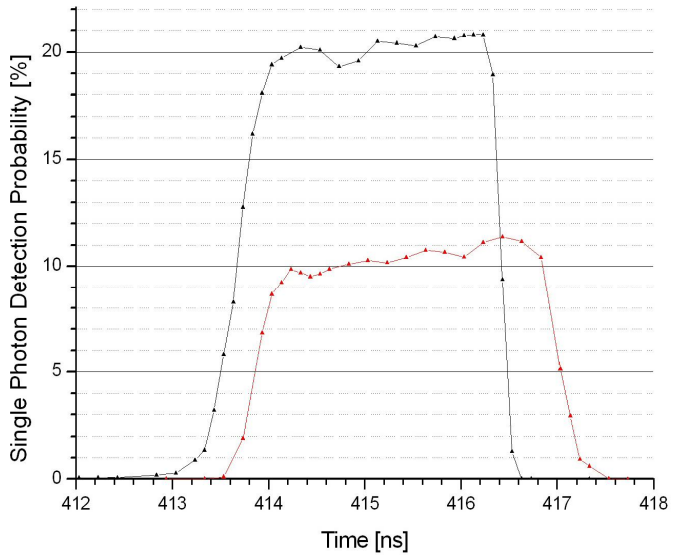

Fig. 8. Single photon detection probability uniformity over a 3ns gate. Levels at 10% and 20% are shown.

3.2.3 Timing resolution

For many applications, the timing resolution is a key feature. In principle, the timing resolution only depends on the fluctuations of the time it takes for a photogenerated carriers to be swept out of the absorption zone into the multiplication zone. However, if not properly designed, the quenching circuit can significantly destroy the final instrument response function.

In Figure 9, the timing resolution has been measured at different V_{op} values corresponding to 5%, 10%, 15% and 20% detection probabilities. The trigger frequency is 100kHz and the gate width is 100ns. The attenuator is set in order to

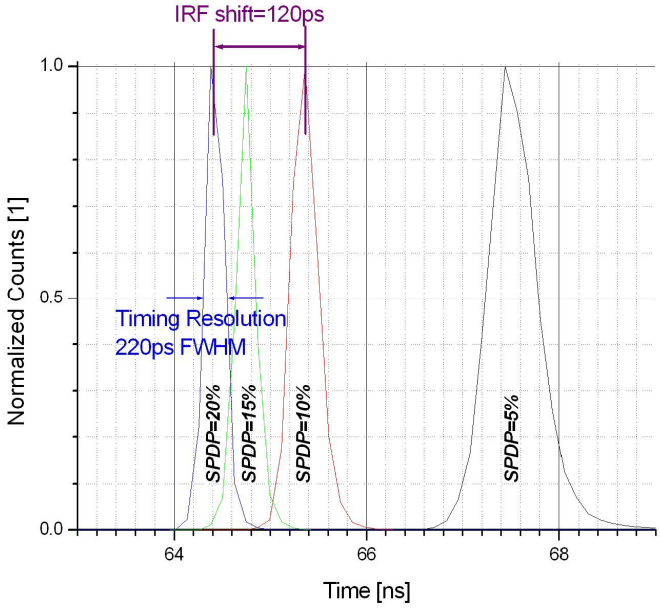

Fig. 9. Timing resolution for different values for V_{op} corresponding to single photon detection probability levels of 5%, 10%, 15% and 20%.

have one photon per pulse. The delay is adjusted in order to place the laser pulse at the middle of the gate. The FWHM timing resolution is 560ps at -42.9V (corresponding a single photon detection probability of 5%) and decrease to around

220ps at high excess bias voltages. Though satisfactory, this measurement is limited by the TDC accuracy and the id300 pulse duration. Further measurements must be performed to rigorously evaluate the timing resolution and the contribution, if any, of the idQ-P.
The IRF (instrument response function) shift with V_{op} is limited to 120ps when the detection probability changes from 10% to 20%. This shift is due to the exponential decrease of the cathode voltage when an avalanche is triggered. At large excess bias voltages, the cathode voltage crosses the comparator reference faster.
In Figure 10, the timing resolution has also been measured as a function of the trigger frequency ranging from 100Hz to 1MHz. The gate width is still 100ns and one photon per pulse is sent in the optical fiber. The idQ-P introduces no timing resolution degradation or IRF shift with the trigger frequency.

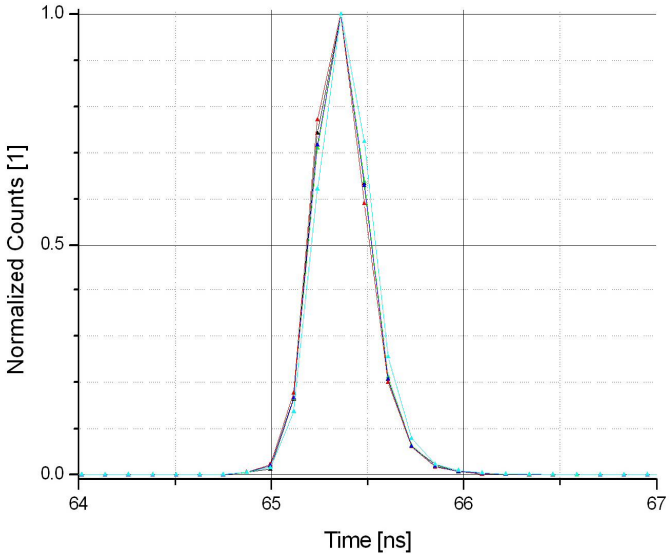

Fig. 10. Timing resolution measured at different trigger frequencies: 100Hz, 1kHz, 10kHz, 100kHz and 1MHz.

Finally, the timing resolution has been measured as a function of the number of photons in the pulse. No significant change of the timing resolution or IRF shift is observed.

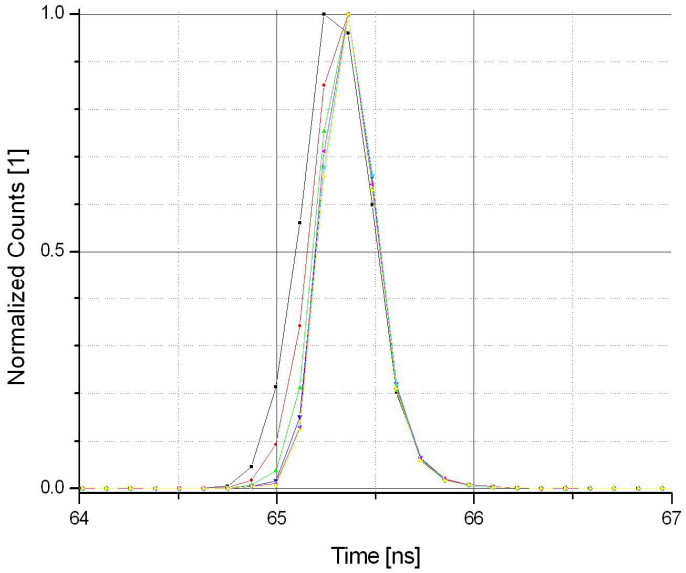

Fig. 11. Timing resolution measured with different photons/pulse value ranging from 0.1 to 10 photons/pulse.

4. CONCLUSIONS

A fully integrated circuit for the synchronous and asynchronous operations of commercial InGaAs/InP APDs has been presented. The 1.6mm^2 chip is fabricated in an industrial 0.8µm CMOS process. In comparison with discrete peripheral electronics, the reduction of parasitic capacitances and fast avalanche quenching lead to a significant decrease of the afterpulsing, detrimental effect that currently limits the performance of InGaAs/InP APDs. Single photon detection probability level of up to 22% is demonstrated when the circuit is supplied to 5V. A higher detection probability can be achieved when the idQ-P is biased to 7V. In contrast with remote active quenching schemes, where bias voltage oscillations are often noticed, a high uniformity of the single photon detection probability is achieved over the full gate width. The internal dead time equal to a period of the GATE IN signal makes high speed gating possible. A timing resolution, independent of the trigger frequency or illumination level, of 220ps has been measured. However, it is limited by the measurement set-up and a more accurate evaluation is necessary. The circuit does not only provide better performance but increases the reliability and long term stability needed in industrial applications such as quantum cryptography. Moreover, compact packaging and more effective cooling solution become possible. Finally, the idQ-P can be combined with low breakdown voltage silicon SPADs or high performance InP-based 1064nm APDs. These last devices find applications in free space optical telecommunications, LIDAR systems for the measurement of wind, weather patterns or air pollution, and in biomedical applications.

REFERENCES

1. P.C. Owens, J.G. Rarity, P.R. Tapster, D. Knight, and P.D. Townsend, Photon counting with passively quenched germanium avalanche photodiodes, Applied Optics 33, 6895-6901 (1994).
2. A. Lacaita, P.A. Francese, F. Zappa, and S. Cova, Single-photon detection beyond 1um: performances of commercially available germanium photodiodes, Applied Optics 33, 6902-6918 (1994).
3. W. Słysz et al.**,** Fiber-coupled detector based on NbN superconducting single-photon nanostructures for quantum cryptography and photon correlation studies, Applied Physics Letters 88, 261113 (2006).
4. http://www.sinphonia.org/.
5. R. Thew, S. Tanzilli, L. Krainer, S.C. Zeller, A. Rochas, I. Rech, S. Cova, H. Zbinden, and N. Gisin, Low jitter up-conversion detectors for telecom wavelength GHz QKD, New J. Phys., 8(32), (2006)
6. G. Ribordy, J.D. Gautier, H. Zbinden, and N. Gisin, Performance of InGaAs/InP avalanche photodiodes as gated-mode photon counters, Applied Optics 37 (12), 2272-2277 (1998).
7. A. Lacaita, P.A. Francese, F. Zappa, and S. Cova, Single-photon detection beyond 1um: performances of commercially available InGaAs/InP detectors, Applied Optics 35, 2986-2996 (1996).
8. A. Yoshizawa, R. Kaji, and H. Tsuchida, Gated-mode single photon detection at 1550nm by discharge pulse counting, Applied Physics Letters 84 (18), 3605-3607 (2004).
9. G. Wu, C. Zhou, X. Chen, X. Li, and H. Zeng, Single-photon detector at 1550nm with gate-mode quenched InGaAs/InP Avalanche Photodiode, SPIE APOC'2003, 02-150 (2003).
10. N. Namekata, S. Sasamori, and S. Inoue, 800MHz single-photon detection at 1550nm using an InGaAs/InP avalanche photodiode operated with a sine wave gating, Optics Express 14 (21), 10043-10049 (2006).
11. S. Cova, M. Ghioni, A. Lolito, I. Rech, and F. Zappa, Evolution and prospects for single photon avalanche diodes and quenching circuits, Journal of Modern Optics 51(9-10), 1267-1288 (2004).
12. http://www.idquantique.com/products/files/id201-specs.pdf
13. D. Stucki, N. Brunner, N. Gisin, V. Scarani, and Hugo Zbinden, Fast and simple one-way quantum key distribution App. Phys. Lett. 87, 194108 (2005).