

Reverse transfer of nanostencil patterns using intermediate sacrificial layer and lift-off process

Chan Woo Park,^{a)} Oscar Vazquez Mena,
Marc A. F. van den Boogaart, and Jürgen Brugger^{b)}

Microsystems Laboratory, Ecole Polytechnique Fédérale de Lausanne (EPFL), CH-1015 Lausanne, Switzerland

(Received 12 July 2006; accepted 27 September 2006; published 30 November 2006)

We propose a new process by which patterns produced by nanostencil lithography can be reversed, so that the final pattern on the substrate has the same contrast (filled or empty) as that of the stencil. In this process, the stencil pattern is first formed on an intermediate sacrificial layer, and then transferred onto the underlying substrate in a reverse manner. Using this process, we can form various pattern structures that cannot be produced by the normal stencil process, such as an array of pores or multiple parallel bridges. Because a bridge in the stencil is transferred also as a bridge on the substrate, we can not only avoid the widening of a narrow bridge pattern by the stress-induced bending of the membrane, but also reduce the width of the bridge even further using the pattern blurring. Using SiO₂ as an intermediate layer, we have fabricated various reversed Cr patterns on Si, including an array of 800 nm circular pores and a 100-nm-wide and 150-nm-long nanobridge. © 2006 American Vacuum Society. [DOI: 10.1116/1.2366610]

I. INTRODUCTION

Among many emerging nanopatterning techniques for overcoming some intrinsic limitations of conventional photo or electron beam lithography, such as nanoimprinting,¹ microcontact printing,² dip pen,³ nanodispensing,⁴ and nanostencil lithography,⁵ nanostencil lithography⁵ has a particularly simple process flow, low cost, little restriction on substrate or pattern materials, and high compatibility with organic or biological surfaces. In a stencil lithography process, a material is evaporated onto a substrate through a stencil membrane with micro/nanoscaled apertures, by which those patterns are transferred onto the substrate (Fig. 1). As the stencil itself is used as a shadow structure during deposition and then lifted away, patterns are formed directly on the substrate without using any resist layer. Because the whole process is free from any mechanical or chemical constraints of typical resist processing (e.g., spin coating, baking, developing, and stripping), patterns can be formed on mechanically fragile,⁵ chemically vulnerable,⁶ or even three-dimensional⁷ structures.

However, the nanostencil lithography has some drawbacks as a shadow mask deposition technique. First, as the pattern transfer occurs by deposition through holes of a stencil, only isolated filled shapes can be formed. Because we cannot fabricate a stencil containing floating islands, it is nearly impossible to obtain isolated empty shapes with their surrounding area filled with a certain material. Although it was demonstrated that an island suspended by narrow bars in a stencil could be transferred as an isolated empty area due to

the pattern blurring, it was applicable only for the scale larger than tens of micrometers.⁸ In addition, when we produce a nanowire connecting two large pads (nanobridge), which is commonly used for electronic or sensor devices,^{9,10} it is difficult to control the width of the bridge precisely. In that case, we need a stencil with a slit connecting two large openings, where the slit is composed of two freestanding cantilevers (Fig. 2). Such a freestanding cantilever is readily bent by thermal or intrinsic stress induced by the deposition of a different material,¹¹ which increases the slit width during the deposition process.¹²

In the present work, we propose a new process by which patterns produced by nanostencil lithography can be reversed, so that the final pattern on the substrate has the same contrast (filled or empty) as that of the stencil. Because an open region and a closed region of the stencil are transferred as an empty area and a filled area on the substrate, respectively, we could not only produce isolated empty shapes but also avoid the widening of a narrow bridge pattern by the stress-induced bending of the membrane. In addition, by utilizing the pattern blurring, we could reduce the width of a bridge pattern even further.

II. EXPERIMENT

A. Nanostencil fabrication

A 150- or 500-nm-thick low-stress silicon nitride (SiN) layer was grown on a 380- μ m-thick double-side polished Si wafer by low-pressure chemical vapor deposition. By deep-ultraviolet lithography and dry etching of SiN, large apertures (larger than 200 nm in width) of the stencil were patterned on the front side. The windows for KOH etching of Si were defined on the backside by conventional photolithography and dry etching of SiN. Then, the entire thickness of the Si wafer was removed by anisotropic wet etching in a KOH

^{a)}Author to whom correspondence should be addressed; present address: Electronics and Telecommunications Research Institute, 161 Gajeong-dong, Yuseong-Gu, Daejeon 305-700, Korea; electronic mail: chanwoo@etri.re.kr

^{b)}Electronic mail: juergen.brugger@epfl.ch

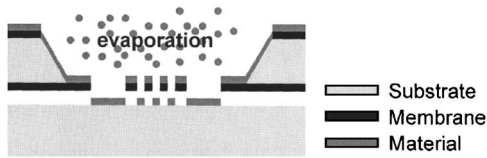


FIG. 1. Schematic representation of the stencil lithography process.

solution for obtaining the SiN membrane structure. On the membrane, small apertures (less than 150 nm in width) were added by focused ion beam (FIB) milling using Ga^+ ions ($V=30$ kV, $I=10$ pA). Before the FIB process, the membrane was coated with 20 nm of Al for minimizing electrical charging and enhancing the resolution of the milling process.

B. Reverse nanostencil lithography

A Si wafer was oxidized to have a 50-nm-thick SiO_2 layer, as a substrate for the reverse patterning process [Fig. 3(a)]. By evaporating 20 nm of Cr onto the substrate through the nanostencil [Fig. 3(b)], the primary Cr pattern was formed on the oxide layer [Fig. 3(c)]. Using the Cr pattern as an etch mask, the oxide layer was dry etched and then slightly wet etched so that an undercut of ~ 50 nm was formed along the periphery of the pattern [Fig. 3(d)]. In the next step, 15 nm of Cr was evaporated again over the entire substrate area with no mask, whereby the deposition of Cr on the oxide sidewall was prevented by the overhanging structure of the primary Cr layer [Fig. 3(e)]. Finally, the Cr/ SiO_2 layer was lifted off in a 7:1 buffered HF (BHF) solution, leading to the formation of a reversed Cr pattern on the Si substrate [Fig. 3(f)].

III. RESULTS AND DISCUSSION

Figures 4(a)–4(c) show the evolution of the pattern structure during the reversing process. After dry etching the oxide layer using the primary Cr pattern as an etch mask, the sidewall of the oxide pattern coincided with the edge of the Cr pattern [Fig. 4(a)]. However, after an additional wet etching of the oxide in the lateral direction, a small undercut of ~ 50 nm was produced along the periphery of the pattern [Fig. 4(b)]. Such an overhanging structure functioned as an

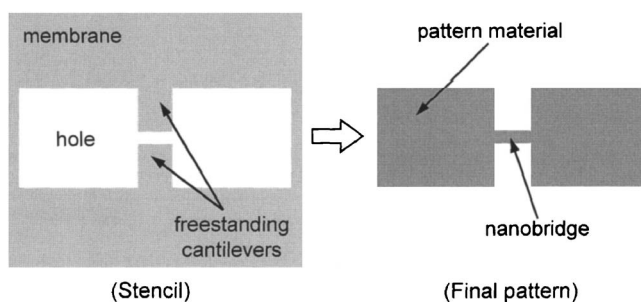


FIG. 2. Formation of a nanowire pattern connecting two large pads (nanobridge) by the normal nanostencil lithography. The narrow slit connecting two large openings in the stencil is composed of two freestanding cantilevers.

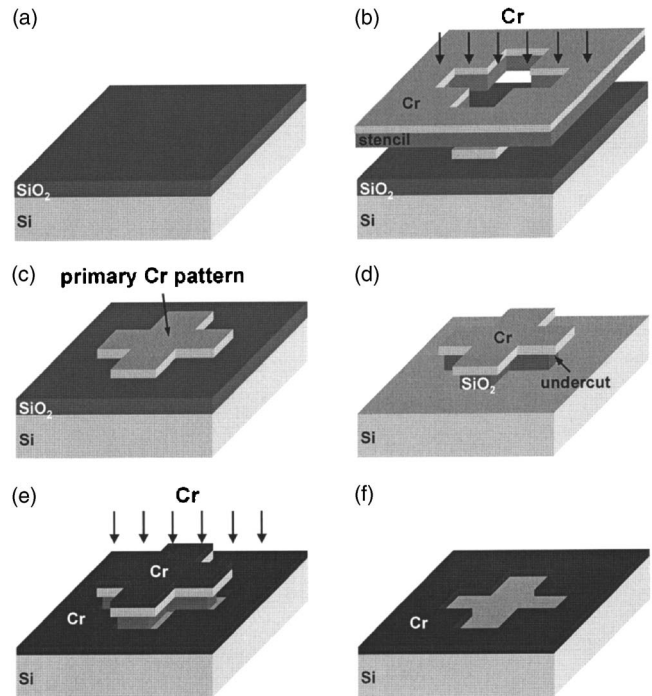


FIG. 3. Reverse nanostencil lithography process. (a) Growth of 50-nm-thick thermal SiO_2 on the Si substrate. (b) Evaporation of 20-nm-thick Cr onto the substrate through the stencil. (c) Formation of the primary Cr pattern on the SiO_2 layer. (d) Dry and wet etching of the SiO_2 layer using the Cr pattern as an etch mask. (e) Secondary deposition of 15-nm-thick Cr on the entire substrate. (f) Formation of the reversed Cr pattern by lift-off in a BHF solution.

in situ shadow mask during the deposition of the second Cr and formed a discontinuity along the boundary so that the BHF solution could penetrate during the lift-off process [Fig. 4(c)]. Figure 5(a) shows a primary Cr pattern formed by the stencil deposition on a SiO_2/Si substrate, and Fig. 5(b) shows the reversed pattern on Si. Those two patterns have exactly the same shape and size, but their contrasts are opposite to each other.

Although the nanostencil lithography has been used for forming various structures such as nanodots,¹³ nanobridges, and nanocantilevers,¹⁴ all of those patterns were the combination of only isolated filled polygons. By using the reverse process, however, we could also produce an array of pores because reversed patterns have isolated empty shapes [Fig. 6(a)]. It implies that now we can form both filled and empty shapes by choosing the normal or reverse process properly, as in the cases of photo and electron beam lithographies where both positive and negative resist processes are available.

Figure 7(b) shows the scanning electron microscopy (SEM) image of a Cr nanobridge pattern, which was formed by the reverse patterning process from a stencil in Fig. 7(a). Such a nanobridge structure can be fabricated also by the normal stencil technique, using a stencil with a narrow slit connecting two large openings. In that case, however, two freestanding cantilevers composing the slit are very vulnerable to the stress induced by the deposition of a pattern

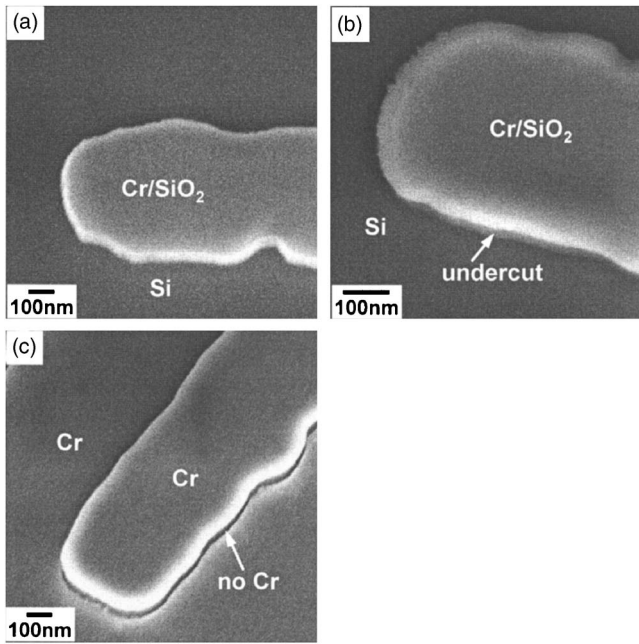


FIG. 4. Evolution of the pattern structure during the reversing process: (a) after dry etching of the SiO₂ layer, (b) after the additional wet etching, and (c) after the deposition of the second Cr.

material.¹² As the pattern material is deposited on the membrane, those cantilevers are easily bent and cause the widening of the slit. In the reverse stencil process, such a stress effect can be eliminated because the stencil itself has a bridge structure without any freestanding cantilevers. Instead, the final bridge pattern was narrower than the stencil bridge structure (Fig. 7), which was caused by the blurring of the primary Cr pattern. The blurring effect, which is induced by a gap between the stencil and the substrate during the deposition process, makes the deposited pattern larger than the original aperture size.^{12,15} Therefore, in the normal stencil process, we need to minimize blurring to achieve a highly miniaturized bridge structure. In the reverse process, however, we can make use of blurring to reduce the width of a bridge even further, as a bridge structure of the stencil is first transferred as a narrower gap on the intermediate SiO₂ layer [Fig. 7(c)].

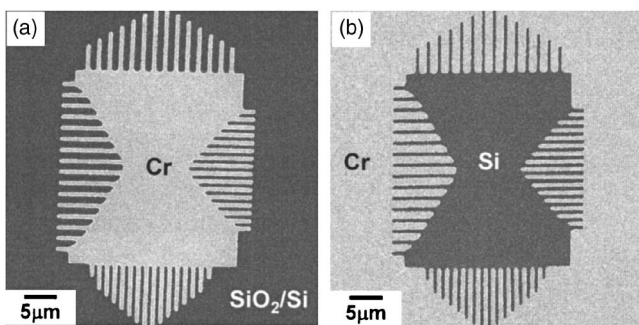


FIG. 5. Reversing behavior of a Cr stencil pattern. (a) The primary Cr pattern on the SiO₂/Si layer formed by the stencil deposition and (b) the reversed Cr pattern on Si.

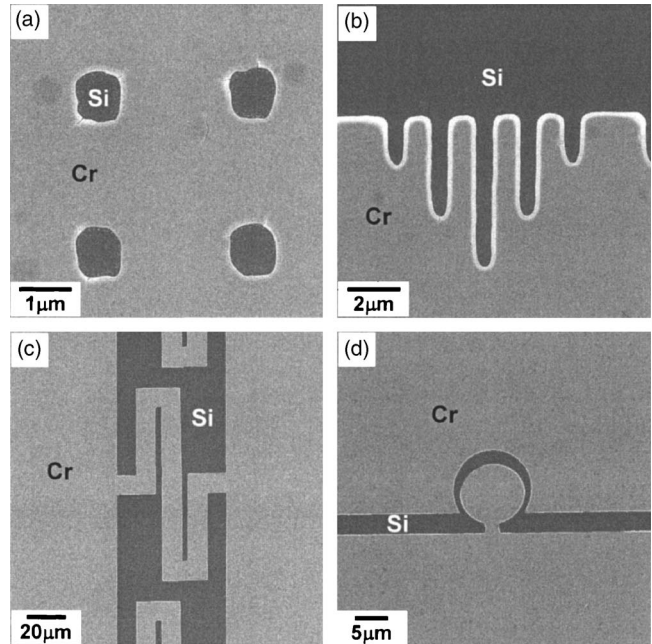


FIG. 6. Various types of the Cr pattern on Si formed by the reverse nanostencil process.

In fabricating a narrow bridge with the normal stencil technique, it is also required to keep the aspect ratio of the aperture (height to width) as small as possible to prevent the clogging of the aperture by the deposition onto the aperture sidewall.¹⁶ A thinner membrane is needed to obtain a narrower bridge, which reduces the mechanical strength of the membrane. In the reverse process, it is not necessary to use a thinner membrane for a narrower bridge pattern because the deposition occurs through two relatively large holes composing a stencil bridge.

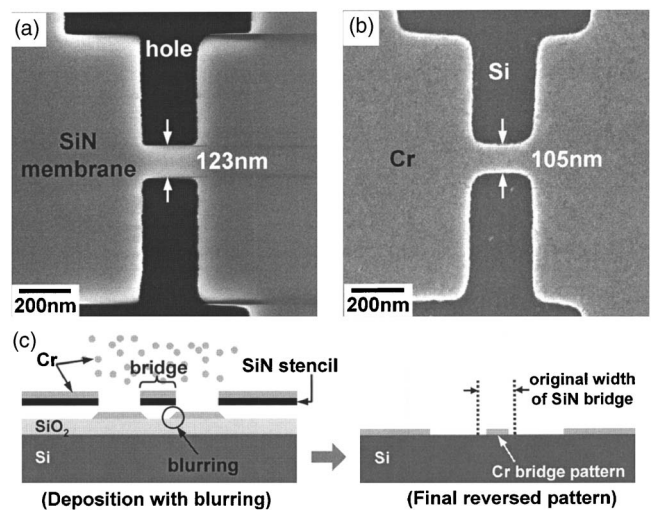


FIG. 7. SEM images of (a) the nanobridge structure in a SiN stencil and (b) the Cr pattern obtained from it by the reverse nanostencil process. The beneficial effect of pattern blurring is schematically shown in (c). Due to the pattern blurring during the stencil deposition, the final Cr bridge pattern is narrower than the original SiN bridge in the stencil.

Another advantage of the reverse process is that a multiple bridge structure can be produced. Although an array of parallel nanobridges is a quite useful configuration for various electronic or sensor devices,^{17,18} it cannot be fabricated by one deposition step in the normal stencil process because it is impossible to make more than one slit connecting two large openings in a stencil. In the reverse process, there is no limit on the number of bridges because a bridge of the stencil is transferred also as a bridge in the final structure.

On the other hand, it should also be pointed out that the reverse stencil process has some inherent limitations. Because the reverse process employs an intermediate sacrificial layer as a medium for the dual pattern transfer, the substrate has to undergo deposition, dry etch, and lift-off processes for the intermediate layer. Unlike the normal stencil process where the final pattern is directly formed on a desired substrate by a single deposition step, the reverse process requires the substrate material to be robust enough to survive those additional process steps. For this reason, the reverse stencil process is hardly applicable to organic or biologically active surfaces. In addition, as the etching selectivity between the pattern material and the sacrificial layer should be very high for the lift-off process, only certain combinations of the pattern and sacrificial materials are possible.

As we have discussed, the normal and the reverse nanostencil processes have their own unique characteristics which are complementary to each other. By combining both processes properly, we can utilize the nanostencil lithography technology as a more powerful tool for producing various kinds of micro- or nanostructures.

IV. CONCLUSIONS

We developed a new process for reversing the patterns formed by nanostencil lithography using a dual pattern transfer through an intermediate sacrificial layer. In this process, the final pattern structure has the same contrast as that of the stencil, which enables us to produce various pattern structures that cannot be formed by the normal stencil process. Equipped with both positive and negative pattern transfer processes, the nanostencil technology can be used as a more competitive tool for overcoming the limitations of conventional lithography techniques.

ACKNOWLEDGMENTS

The authors are pleased to acknowledge the EPFL Center of Micro-Nano-Technology (CMI) and its entire staff as well as our colleagues at the Microsystems Laboratory for their very valuable discussions and help. This project is partially funded by the European Commission and OFES within the project NaPa (Contract No. NMP3-CT-2003-500120) and by the Swiss National Science Foundation project NANO-IC (Contact No. 200021-101847). This work was also supported by the Korea Research Foundation Grant (KRF-2005-214-D00129).

- ¹S. Y. Chou, P. R. Krauss, and P. J. Renstrom, *J. Vac. Sci. Technol. B* **14**, 4129 (1996).
- ²J. L. Wilbur, A. Kumar, H. A. Biebuyck, E. Kim, and G. M. Whitesides, *Nanotechnology* **7**, 452 (1996).
- ³R. D. Piner, J. Zhu, F. Xu, S. Hong, and C. A. Mirkin, *Science* **283**, 661 (1999).
- ⁴A. Meister, M. Liley, J. Brugger, R. Pugin, and H. Heinzelmann, *Appl. Phys. Lett.* **85**, 6260 (2004).
- ⁵J. Brugger, J. W. Berenschot, S. Kuiper, W. Nijdam, B. Otter, and M. Elwenspoek, *Microelectron. Eng.* **53**, 403 (2000).
- ⁶E. A. Speets *et al.*, *Adv. Funct. Mater.* **16**, 1337 (2006).
- ⁷J. Brugger, C. Andreoli, M. Despont, U. Drechsler, H. Rothuizen, and P. Vettiger, *Sens. Actuators, A* **76**, 329 (1999).
- ⁸A. Tixier, Y. Mita, J. P. Gouy, and H. Fujita, *J. Micromech. Microeng.* **10**, 157 (2000).
- ⁹Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadata, M. Nagase, and K. Murase, *IEEE Trans. Electron Devices* **43**, 1213 (1996).
- ¹⁰Z. Li, B. Rajendran, T. I. Kamins, X. Li, Y. Chen, and R. S. Williams, *Appl. Phys. A: Mater. Sci. Process.* **80**, 1257 (2005).
- ¹¹J. A. Thornton and D. W. Hoffman, *Thin Solid Films* **171**, 5 (1989).
- ¹²M. A. F. van den Boogaart, M. Lishchynska, L. M. Doeswijk, J. C. Greer, and J. Brugger, *Sens. Actuators, A* **130–131**, 568 (2006).
- ¹³F. Vroegindewey, E. A. Speets, J. A. J. Steen, J. Brugger, and D. H. A. Blank, *Appl. Phys. A: Mater. Sci. Process.* **79**, 743 (2004).
- ¹⁴G. M. Kim, S. Kawai, M. Nagashio, H. Kawakatsu, and J. Brugger, *J. Vac. Sci. Technol. B* **22**, 1658 (2004).
- ¹⁵Z. Racz, J. He, S. Srinivasan, W. Zhao, A. Seabaugh, K. Han, P. Ruchhoeft, and J. Wolfe, *J. Vac. Sci. Technol. B* **22**, 74 (2004).
- ¹⁶M. Kölbl, R. W. Tjerkstra, J. Brugger, C. J. M. van Rijn, W. Nijdam, J. Huskens, and D. N. Reinhoudt, *Nano Lett.* **2**, 1339 (2002).
- ¹⁷Y.-K. Choi, T.-J. King, and C. Hu, *IEEE Electron Device Lett.* **23**, 25 (2002).
- ¹⁸R. A. Beckman, E. Johnston-Halperin, N. A. Melosh, Y. Luo, J. E. Green, and J. R. Heath, *J. Appl. Phys.* **96**, 5921 (2004).