

# Bit vs. Symbol Interleaving for Parallel Concatenated Trellis Coded Modulation

Christina Fragouli and Richard D. Wesel  
Electrical Engineering Department  
University of California, Los Angeles

*Abstract*— This paper compares bit v.s. symbol interleaving for parallel-concatenated trellis-coded turbo codes, employing the turbo encoder structure proposed in [1]. To compare systems optimized with the same techniques, the paper extends the turbo-encoder design procedure proposed in [2] to bit-interleaved systems. We discuss a method to jointly design the multiple required interleavers for the bit-interleaved system, and a procedure to select constituent encoders that can take advantage of the interleaver structure to achieve a low error floor.

Simulation results for the designed bit-interleaved system show better performance than bit-interleaved performance reported in the literature. The symbol-interleaved system though achieves an earlier convergence, especially with an increased number of decoder iterations, but at the cost of a slightly higher error floor.

## I. INTRODUCTION

The purpose of this paper is to compare bit v.s. symbol interleaving for parallel-concatenated trellis-coded turbo codes (PCTCM), with constituent encoders of rate  $k/n$ ,  $k > 1$ .

The turbo encoders for trellis-coded modulation proposed in the literature employ either bit-interleaving, where  $k$  bit interleavers keep the bit-streams separate [1], or symbol interleaving [3], [4], [2], where the  $k$  binary inputs are treated as one symbol over the extension field  $GF(2^k)$ .

The performance difference among these turbo encoders does not allow a fair comparison between bit and symbol interleaving since each approach includes additional design choices, such as the con-

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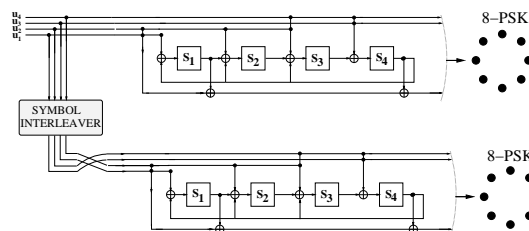


Fig. 1. Symbol-interleaved 2 bits/sec/Hz PCTCM turbo code with rate  $4/3$  constituent encoders

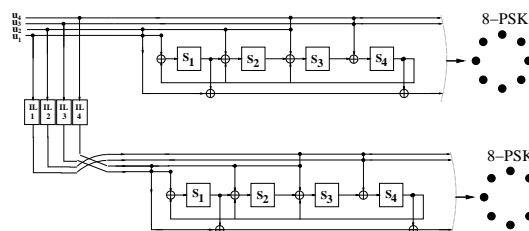


Fig. 2. Bit-interleaved 2 bits/sec/Hz PCTCM turbo code with rate  $4/3$  constituent encoders

stituent encoder, interleaver, and iterative decoding implementation.

In [2] a careful turbo encoder design for symbol-interleaving achieved a performance advantage over the symbol and bit interleaved systems previously reported in the literature. The turbo encoder structure in [2], combined the bit-interleaved encoder structure in [1] with a symbol interleaver. Fig. 1 and 2 show an example of the bit and symbol interleaved turbo code in [1] and [2] respectively, that employ 8 PSK modulation in connection with rate  $4/3$  constituent encoders, each with  $\frac{k}{2} = 2$  systematic and  $r = 1$  parity outputs.

This paper extends the design procedure proposed in [2] to the initial bit-interleaved system in [1],

which makes possible comparison of bit vs. symbol interleaving in two systems that are optimized by the same techniques and employ the same basic structure. Moreover, the performance of the designed bit interleaved system is compared to previously reported bit-interleaved results in the literature.

The turbo encoder design consists of two components, the interleaver design and the constituent encoder design, which are examined in Sections II and III respectively. More specifically, Section II proposes to jointly design the multiple interleavers required for a bit-interleaved system, and presents a semi-random interleaver construction method. Section III investigates a method to select the constituent encoders that leads to a lower error floor. Section IV presents simulation results, and Section V concludes the paper.

## II. MULTIPLE INTERLEAVER DESIGN

The role of the interleaver is to lower the error floor, as is called the flattening of the bit error rate curve turbo codes exhibit for moderate to high values of SNR. The error floor depends upon the free distance of the turbo code. The error events with small number of inputs typically determine the free distance, thus the interleaver is designed to avoid them.

An interleaver of length  $N$  is completely described by a mutually exclusive and collectively exhaustive listing of the integers from 1 to  $N$ . Define  $f(i)$  to be the integer in the  $i^{\text{th}}$  position in the list. The input symbol in position  $i$  before interleaving is in position  $f(i)$  after interleaving.

The spread interleaver is described in [5] as a semi-random interleaver based on the random selection without replacement of  $N$  integers from 1 to  $N$  under the following constraint.

**Constraint 1** *Reject the  $i^{\text{th}}$  randomly selected integer  $f(i)$  if there exists  $j < i$ , such that*

$$0 < i - j \leq S_1 \quad |f(i) - f(j)| \leq S_2. \quad (1)$$

An extension of the spread interleaver [2], [6] takes into account multiple error events, by impos-

ing two additional constraints on the interleaver construction

**Constraint 2** *Reject the  $i^{\text{th}}$  randomly selected integer  $f(i)$  if there exist  $j, k, l < i$ , such that*

$$\begin{aligned} 0 < i - j \leq T_1 \quad & |f(i) - f(k)| \leq T_2 \\ 0 < |k - l| \leq T_1 \quad & |f(j) - f(l)| \leq T_2. \end{aligned}$$

**Constraint 3** *Reject the  $i^{\text{th}}$  randomly selected integer  $f(i)$  if there exist  $j, k, l, m, n < i$ , such that:*

$$\begin{aligned} 0 < i - j \leq X_1 \quad & |f(i) - f(k)| \leq X_2 \\ 0 < |k - l| \leq X_1 \quad & |f(j) - f(m)| \leq X_2 \\ 0 < |m - n| \leq X_1 \quad & |f(n) - f(l)| \leq X_2 \end{aligned}$$

Bit-interleaved systems for high spectral efficiency typically employ  $k > 1$  parallel bit interleavers, as for example in Fig.1. The above criteria can be applied to individually create each required interleaver independently. However, to avoid error events with inputs that span different interleavers, the same design criteria can be applied across the interleavers, in a joint multiple interleaver design.

We propose to sequentially design the interleavers, where each new interleaver has to satisfy not only constraints applied on itself, but also constraints with respect to the already constructed interleavers.

Let  $f_p, p = 1 \dots k$  denote the  $k$  different interleavers, and assume that the  $l - 1, l > 1$  interleavers are already constructed. The first constraint can be applied across the interleavers to create the  $f_l$  interleaver as

**Constraint 4** *For the  $l > 1$  interleaver, the  $i^{\text{th}}$  randomly selected integer  $f_l(i)$  must be rejected if there exists  $j$  and  $f_p, p < l$ , such that*

$$0 < |i - j| \leq S_{1m} \quad |f_l(i) - f_p(j)| \leq S_{2m}. \quad (4)$$

The extension is straightforward for the second and third constraints.

High values of  $S$ ,  $T$ , and  $X$  help the interleaver to avoid more error events and thus achieve a lower error floor [7], but make more difficult to identify an interleaver that satisfies them. We propose a semi-random interleaver construction technique that allows interleavers that achieve substantial values of  $S$ ,  $T$ , and  $X$  in practice.

#### A. Construction Procedure

A uniform interleaver of length  $N$  is created by randomly selecting without replacement integers from 1 to  $N$  with equal probability. For a semi-random interleaver the randomly selected integers need to satisfy a set of constraints. This subsection presents a technique for constructing such interleavers.

The generation of a length  $N$  interleaver consists of  $N$  steps, where each step selects an integer for the respective position. At the  $i^{\text{th}}$  step of the interleaver generation the interleaver contains  $i - 1$  assigned numbers and there exist  $N - i + 1$  unassigned numbers. Randomly select one of the  $N - i + 1$  unassigned numbers with equal probability, for example number  $j$ . Check if placing number  $j$  at interleaver position  $i$  violates any of the imposed constraints. If it does not violate any constraints, then continue with the next step  $i + 1$ . The procedure described up to this point was proposed by Divsalar et al. [5]. We extend it as follows:

If  $j$  does violate a constraint, try to place it in between two other previously assigned indices. Uniformly choose one of the  $i$  candidate positions and check if placing  $j$  there violates any of the constraints. Continue until either all previously assigned indices have been examined or a suitable position is found. If there does not exist an appropriate position, repeat for a number selected among the unassigned and not already examined  $N - i$  numbers  $k$ ,  $k \neq j$ .

### III. CONSTITUENT ENCODER DESIGN

Let  $d_s$  denote the minimum output weight for input Hamming weight equal to  $s$ . Typically in the

literature, the constituent encoders are required to have infinite  $d_1$  and optimized for effective distance  $d_2$  [8]. Because many encoders achieve the optimal  $d_2$ , a more refined search may examine the distance for additional small input weights such as  $d_3$ ,  $d_4$  etc.

This method to assess the performance examines only the minimum output weight, and does not take into account how the output weight varies with the error event length.

However, to achieve a low error floor using the interleaver designed in Section II, it is important that the output weight increases with the error event length, so that further dispersing the inputs may lead to increased output weight. More specifically, for semi-random interleavers constructed to satisfy specific constraint parameters (see Sec. II), the free distance of the overall turbo encoder depends on the minimum output weight of small input-weight error events with length greater than the constraint parameters.

The typical approach for turbo code design selects constituent encoders and then designs the interleaver(s) specifically tailored to the constituent encoders. In this paper we propose a reversed procedure. First, for a specific interleaver length identify a semi-random interleaver that satisfies constraints with as high parameters  $S_o$ ,  $T_o$ ,  $X_o$  ([2], [9]) as possible. Consider one interleaver, since the extension to a set of jointly designed interleavers is straightforward.

Let  $d_{s,l}$  denote the minimum output weight for error events with input weight equal to  $s$  and error event length greater than  $l$ . To calculate  $d_{s,l}$  it is sufficient to calculate the output distance for error events of length up to  $l + 2^m$ , where  $m$  is the number of memory elements for the encoder.

Identify the set of encoders (for example using the search space proposed in [2], [10]) with infinite  $d_1$  that achieve the highest  $d_2$ , and have good  $d_3$ ,  $d_4$  distance properties. The set of such encoders is usually large. Among them, the encoders with the largest  $d_{2,S_o}$ ,  $d_{2,T_o}$  and  $d_{2,X_o}$  distance lead to a higher overall free distance with the selected interleaver, and

thus a lower error floor.

An additional good property of a constituent encoder is that the output weight increases with the error event length, for small input weights. This implies that small input weight error events do not contain a zero-input zero-output loop, which can be checked for example by examining whether  $d_{2,2^m} < d_{2,2^{m+1}}$ . The codes presented in the simulation results were designed with this procedure.

#### IV. SIMULATION RESULTS

This section provides simulation results for 4 bits/sec/Hz employing 64-QAM=  $2 \times 8$ -PAM and 2 bits/sec/Hz employing 8-PSK.

Table I contains in octal notation codes identified through exhaustive search, for the 8-PAM reordered labeling  $\{0\ 1\ 2\ 3\ 6\ 7\ 4\ 5\}$ , optimized for squared Euclidean distance. The encoder polynomials are as described in [2]. Fig. 3 plots the performance for a 4-bits/sec/Hz/ turbo code employing 8-PAM with the first encoder in Table I. The encoder employed four interleavers of length 4,096 bits each, designed according to the procedure described in Section II with parameters  $(S, T, X, S_m) = (30, 5, 1, 20)$ . The same plot shows the performance of the bit-interleaved system in [1] and the symbol-interleaved system in [2]. The proposed bit-interleaved encoder performs better than the encoder in [1], and has a lower error floor than the symbol-interleaved system in [2]. However, the symbol-interleaved system converges earlier. Symbol interleaving imposes less constraints on the iterative decoding, as argued in [2].

Fig. 4 plots for 2 bit/sec/Hz and 8-PSK (labeling  $\{0\ 1\ 2\ 3\ 6\ 7\ 4\ 5\}$ ), the performance with bit-interleaving and constituent encoders  $\{031, 06, 011, 012, 017, 07, 03\}$  and the performance with symbol-interleaving in [2]. The four bit interleavers of length 2500 were designed with parameters  $(S, T, X, S_m) = (20, 4, 0, 10)$ . Again the symbol-interleaved system converges earlier. Fig. 5 shows that the designed bit-interleaved system performs better than the bit-interleaved system in [1].

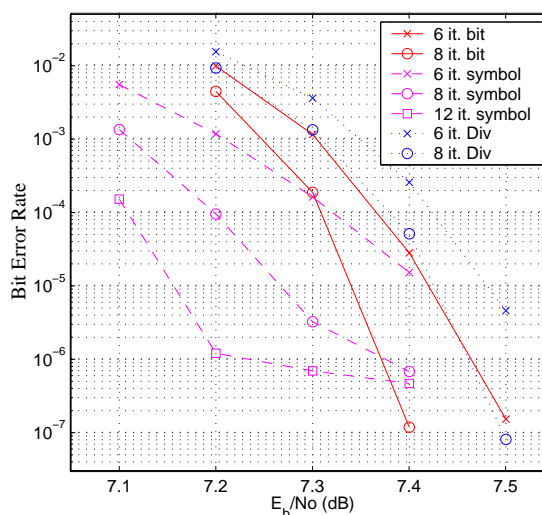


Fig. 3. 4 bits/sec/Hz/ turbo code employing 8-PAM. Capacity 5.74 dB. Constrained Capacity 6.6 dB. Interleaver length 4,096 symbols. Input block size  $4,096 \times 4$  bits.

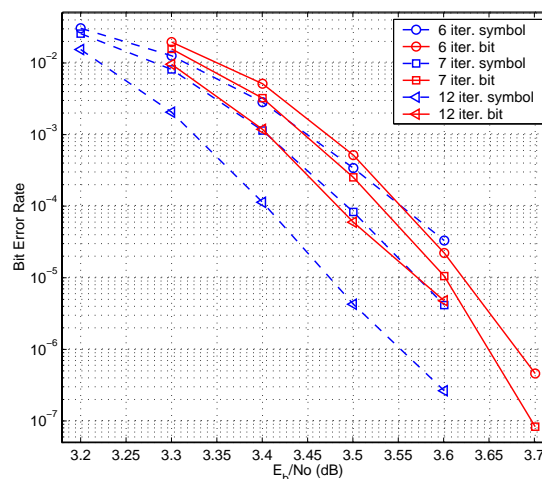


Fig. 4. 2 bits/sec/Hz/ turbo code employing 8-PSK. Capacity=1.76 dB. Constrained capacity=2.8 dB. Interleaver length 2,500 symbols. Input block size  $2,500 \times 4$  bits.

TABLE I  
ENCODERS FOR  $8 \times 8$  PAM=64 QAM

#	encoder polys			
1	{031, 01, 05, 013, 017, 015, 03}			
2	{023, 03, 07, 011, 015, 05, 03}			
3	{023, 010, 012, 015, 017, 012, 03}			
4	{027, 02, 05, 07, 010, 02, 03}			
5	{035, 02, 05, 07, 016, 016, 03}			
6	{027, 03, 010, 013, 016, 013, 03}			

#	$d_2$	$d_3$	$d_{2,5}$	$d_{2,10}$
1	1.14(4)	0.38(7)	1.143	1.9
2	1.14(4)	0.38(7)	1.143	1.9
3	1.14(4)	0.38(7)	1.143	1.9
4	1.14(4)	0.38(4)	1.143	1.9
5	1.14(4)	0.38(4)	1.143	1.9
6	1.14(4)	0.38(4)	1.143	1.9

#	$d_{2,20}$	$d_{2,30}$	$d_{3,5}$	$d_{3,10}$
1	2.67	3.42	0.76	1.14
2	2.67	3.42	0.76	1.14
3	2.67	3.42	0.76	1.14
4	2.67	4.19	0.76	1.14
5	2.67	4.19	0.76	1.14
6	2.67	4.19	0.76	1.14

## V. CONCLUSIONS

We presented a method to select constituent encoders and jointly design the interleavers for a bit-interleaved trellis-coded modulated turbo encoder. The designed system performs better than the bit-interleaved approach in [1]. However, a symbol-interleaved system optimized with the same techniques [2] can converge earlier at the cost of a slightly higher error floor.

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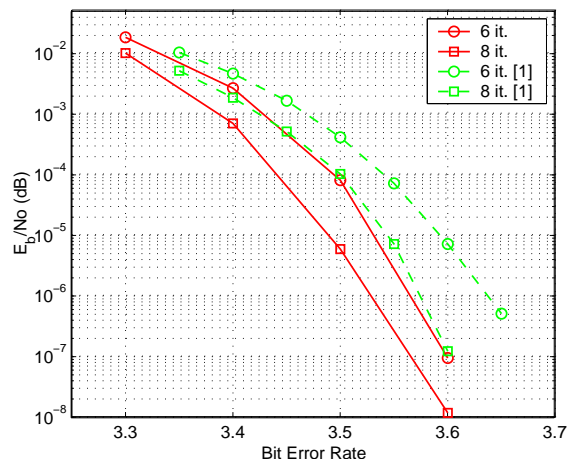


Fig. 5. 4 bits/sec/Hz/ turbo code employing 8-PSK. Interleaver length 4, 096 symbols. Input block size  $4, 096 \times 4$  bits.

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