Deep-ultraviolet–microelectromechanical systems stencils for high-throughput resistless patterning of mesoscopic structures

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We describe a combination of 100-mm wafer scale deep-ultraviolet (DUV) exposure and a microelectromechanical systems (MEMS) process to fabricate silicon nitride membranes with submicrometer apertures to be used as miniature shadow masks or nanostencils. Apertures down to a lateral resolution of 200 nm were made in a 500-nm-thick membrane by DUV exposure and dry plasma etching. The membranes were released by a combination of wet silicon etching using potassium hydroxide (KOH) and dry silicon etching using a plasma process. The millimeter-size stencils were used for single-step, local deposition of metal micro- and nano-patterns without the need for photoresist process steps. We have performed stencil deposition on full wafer scale for micro- and nano-patterns in a variety of metals (e.g. Al, Au, Ni, etc.). Dry under-etching of the nanowires resulted in free-standing cantilevered nanoelectromechanical systems (NEMS) structures with resonance frequencies in the megahertz range. The resistless method allows us to pattern micrometer and nanometer scale patterns in a single step without any further processing. It is promising for the surface processing of MEMS/NEMS devices having sensitive or fragile surfaces, such as biochips, organic polymer layers, and self-assembled monolayers. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1802931]

I. INTRODUCTION

The miniaturization of devices into the submicron range can be achieved by advanced lithography techniques using deep-ultraviolet (DUV), x-ray, electron beam, or ion beam exposure. These high-end photoresist-based methods however have major limitations if they are aimed at the processing of micro- and nano-electromechanical systems (MEMS/NEMS) where often mechanically fragile and chemically functionalized surfaces need to be structured. Recently, the increasing demand of micron and submicron scale features for non-integrated circuit applications has given rise to a series of versatile and flexible surface patterning methods. These include scanning probe lithography,[1] thermomechanical indentation of polymers by nanoimprint lithography,[2] local deposition of molecules via a stamp by microcontact printing or soft-lithography,[3,4] or via nanotips in dip-pen,[5] and nanoscale dispensing.[6] A further emerging micro/nanopatterning method is based on a highly localized material deposition through ultra-miniature shadow-masks (nanostencils).[7–9]

Patterning using nanostencils allows for a wide choice of materials and surfaces to be structured as no etching pro-cesses need to be performed, which might damage or contaminate material layers. The use of thin membrane shadow-masks for the pattering of surfaces has been used as early as 1984.[10] The stencils were fabricated by means of standard MEMS processes to obtain micron scale membrane apertures. They were applied for the patterning of micron scale features on reasonably large membranes (14×18 mm^2). Submicron features down to the 10–100 nm scale have been demonstrated on small areas (typically a few 10 μm^2).[8]

The main reason for the limited throughput is mainly due to the lack of a suitable high-resolution and high-throughput lithography and MEMS fabrication methods for creating nanoscale structures on large areas combined with well-controlled wafer-through etching of thin solid-state membranes. Serial fabrication technologies like focused ion beam [7,9] and electron beam lithography[8,11] have been used to obtain apertures at nanoscale, however with limited throughput. Laser interference lithography can achieve 100 nm scale patterning on large areas, but is limited to periodic structures only.[12]

In order to overcome the limitation for the fabrication of large-area nanostencils with arbitrary apertures, we developed a 100 mm wafer size combined DUV/MEMS fabrication process. Using this method, aperture patterns covering

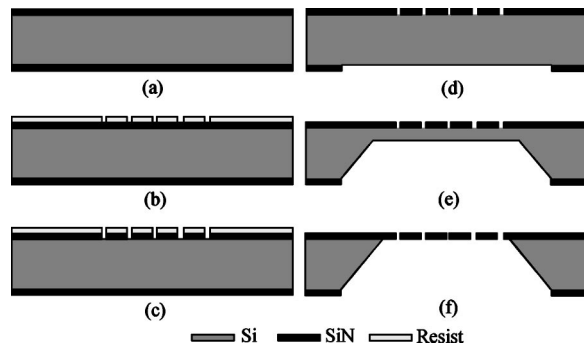[a)]Electronic mail: marc.vandenboogaart@epfl.ch

FIG. 1. Simplified schematic illustration of the fabrication process for a DUV-MEMS stencil. (a) 500-nm-thick LPCVD low-stress SiN deposition, (b) exposure and development of using DUV lithography (minimum feature size is 200 nm), (c) dry etching transfer of the resist patterns into SiN, (d) membrane etch window definition by backside lithography and pattern transfer, (e) KOH etching of the bulk Si until a 10-μm-thick Si membrane is left, and (f) final membrane releasing using dry etching, membrane size is 1×1 mm^2.
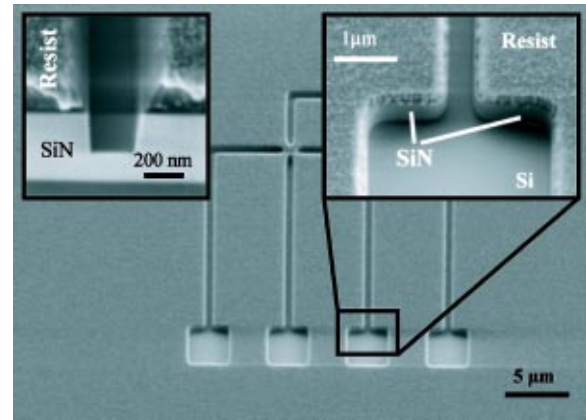

FIG. 2. Scanning electron micrograph showing a micro/nano structure after dry etch transfer into the SiN membrane. The left inlet shows a cross-section of the midprocess details of 200 nm line patterns. The right inlet shows details of an electrode pattern at submicron scale. The etch profiles demonstrate the high selectivity and process control for the transfer of the 500-nm-thick DUV resist pattern into the 500-nm-thick SiN layer.

multiple length scales, from 200 nm up to 300 μm, were defined in a thin silicon nitride layer by a wafer stepper DUV-exposure followed by dry etching.

II. DUV BASED MICRO/NANO-STENCIL FABRICATION

The micro/nano-stencils were fabricated using a combination of an industry standard DUV exposure and a standard MEMS processing. Figure 1 shows a schematic overview of the DUV/MEMS-based fabrication process of a full-wafer stencil. The process begins with the deposition of 500-nm-thick low-stressed silicon nitride (LS-SiN) by low pressure chemical vapor deposition (105 sccm SiH$_2$Cl$_2$, 27 sccm NH$_3$, 135 mTorr, 838.5 °C, stress 200 MPa tensile) on a 100 mm double side polished, 380-μm-thick silicon (Si) wafer as illustrated in Fig. 1(a). Mesoscopic patterns which will form the membrane apertures were defined in a 500-nm-thick DUV resist (DX 5400P from AZ® Electronic Materials, Windsor, UK) followed by a 4× reduced projection exposure using a DUV wafer stepper (ASML PAS5500/ 300, 248 nm wavelength, 10 W KrF laser source). The patterns were developed [Fig. 1(b)] and then transferred into the 500-nm-thick LS-SiN layer by means of anisotropic etching [Fig. 1(c)]. The key process parameters for the transfer of the 500-nm-thick patterned DUV-resist into a 500-nm-thick LS-SiN layer is the selectivity of the etching agent between the DUV-resist mask layer and the SiN structural layer. In order to optimize the pattern transfer conditions, we have used a C$_2$F$_6$ gas flow of 20 sccm with additional 20 sccm of CH$_4$. Figure 2 shows a scanning electron micrograph (SEM) of the midprocess details of a typical 200-nm-scale DUV-pattern after the inductively coupled plasma (ICP) transfer into the LS-SiN. This confirms the high accuracy and selectivity of the ICP transfer process at this length-scale to maintain the edge definition of the structures. The backside patterns were defined in a 1.7-μm-thick positive photoresist (S1818, Shipley, Coventry, UK) by means of conventional

photolithography (MA-150 aligner, SUSS MicroTec, Garching, Germany). The SiN layer on the backside was opened using ICP anisotropic etching (Alcatel 601E:C$_2$F$_6$ 20 sccm, 20 °C, 1800 W). This backside patterned SiN [Fig. 1(d)] forms the etch mask for the subsequent membrane releasing [Figs. 1(e) and 1(f)].

Previous work on freestanding thin membranes often used potassium hydroxide (KOH) etching for the release of membranes from the bulk Si. Wet-chemical release however is often limited due to a buildup of pressure[13] which can cause membrane rupture, or wet-rinsing and drying related stiction or sticking of fragile membrane features.[14] Attractive capillary forces may bring mechanically compliant structures into contact with the substrate or to other parts of the membrane. After complete drying the structures remain stuck to their acquired position. In a first process we observed both wet-chemical process related effects during membrane release and drying step.

As a remedy for this problem we used a combination of KOH and dry etching for the release of the membrane from the bulk Si. First, KOH was used to etch into the bulk Si until an about 10–20-μm-thick Si membrane remained. Subsequently, the remainder of the Si was etched using ICP at low temperature in order to increase the selectivity of LS-SiN to Si (Alcatel 601E:CF$_6$ 200 sccm, O$_2$ 10–15 sccm, −110 °C, 800 W, selectivity LS-SiN to Si, 375:1). The wet/dry process combination allows for a high yield of thin stencil membranes with compliant structures.

Figure 3(a) shows an optical picture taken from a finished full wafer (100 mm) containing a large variety of membrane stencils, each containing numerous mesoscopic geometrical apertures [Figs. 3(b) and 3(c)].

III. APPLICATION OF DUV STENCIL AS FULL WAFER-SCALE SHADOW MASK

The fabricated stencil can be used as a full wafer size shadow mask, or can be cleaved in smaller chips, and ap-
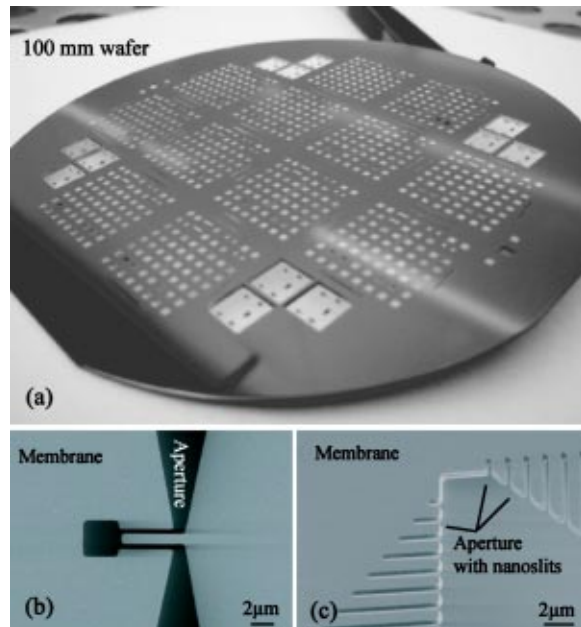
FIG. 3. (a) Optical image of a full wafer scale (100 mm) stencil containing various membranes, each containing numerous geometrical apertures, (b) released SiN membrane containing simultaneous micro- and nano-apertures ranging from 350 nm up to 30 μm, and (c) released SiN membrane containing micro- and nano-apertures ranging from 400 nm up to 300 μm (not shown).

plied for local thin film deposition processes. To this extend the stencil was positioned and mechanically clamped to a substrate. Figure 4 shows a schematic illustration and SEM images of a typical stencil deposition process.
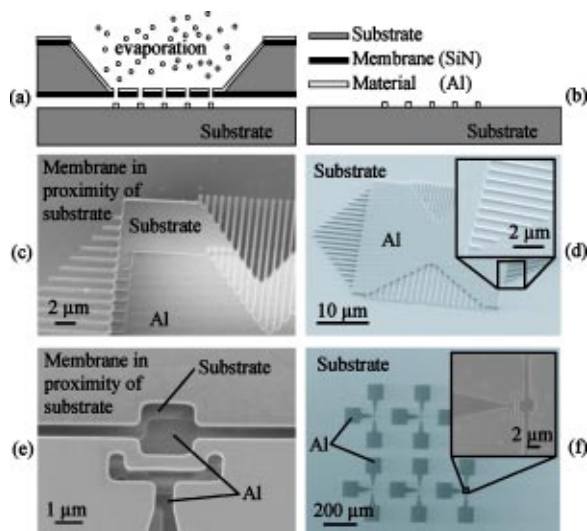

FIG. 4. Deposition process using a stencil. (a) The stencil is placed in contact or in close proximity to the substrate and a material is evaporated from a distant source and deposited through the apertures in the membrane onto the substrate, (b) the stencil is removed from the substrate, (c) and (e) the SEM-images show a stencil mask with a gap to a substrate after evaporation. The membrane in Fig. 4(c) has a gap of approximately 5 μm, whereas a gap of approximately 1 μm is observed in Fig. 4(e), and (d) and (f) the SEM-images show the corresponding Al pattern from Figs. 4(c) and 4(e).

A physical vapor deposition evaporation system (Alcatel EVA 600) with a planetary system that can hold up to 15 wafers was used. For the stencil evaporation process the planetary rotation system was removed. The clamped stencil/substrate was centered and placed perpendicular to the material flux at a distance of 50 cm from the material evaporation source. A variety of metals such as Al, Au, Bi, Cr, Cu, Ni, and Ti were locally deposited via the stencil apertures onto substrates [Fig. 4(a)]. Several substrate surfaces were successfully used such as materials that are relevant to standard semiconductor processing, e.g., Si, SiN, SiO$_2$ or that are used in optoelectronic applications (GaAs). Unconventional substrates for (Bio) MEMS and NEMS have also been applied such as highly ordered pyrolytic graphite (HOPG), polydimethylsiloxane (PDMS), and epoxy based photoresist (SU-8).

Finally the stencil was removed from the substrate as shown in Fig. 4(b). Figures 4(c) and 4(e) show a stencil membrane in proximity of a substrate after evaporation of 100 nm Al. The corresponding surface structures are shown in Figs. 4(d) and 4(f) and demonstrate excellent pattern definition.

IV. RESULTS AND DISCUSSION

A variety of structures with dimensions ranging from 200 nm up to 300 μm were produced in large quantities and with high throughput and reproducibility on a full-wafer scale. These results show that full wafer mesoscopic stencils can be applied to a large variety of surfaces for direct rapid patterning without lithography of multiple length scale patterns on large surface areas.

The demonstrated nanostencil patterning is a practically contact-free micro- and nano-patterning method. It allows depositing small amounts of materials only at location where needed. The process can be compared to the liftoff method using a mechanical mask instead of a sacrificial photoresist layer. Using a nanostencil reduces the patterning process to a single step. Indeed, it makes other operations such as spin coating, baking, exposure, development, and etching obsolete. Hence, it can be applied on arbitrary surfaces including fragile substrates.

The deposition through stencils suffers from limitations such as the clogging of aperture, and the membrane deformation due to material induced stresses. Clogging, e.g., occurs as the evaporated material is also deposited on the membrane itself and inside the apertures. This phenomenon changes the geometrical shape of the aperture during the deposition process and leads to deformation of the deposited pattern and eventually to the complete closure of the aperture. Kölbel *et al.*[15] demonstrated the use of self-assembled monolayers (SAM) as an antiadhesion layer. The SAM-coated SiN membranes showed a reduced aperture clogging, which improved their performance and lifetime.

A second major limitation of the membrane stencil is the stress-induced bending. The mechanically "unstable" membranes deform under influence of the deposited material due to a different thermal expansion coefficient and deposition

related internal stress. Efforts have been made to stabilize the membrane locally by introducing some stabilization structures,[12,13,16] a subject that deserves further investigations.

V. CONCLUSIONS AND FURTHER DEVELOPMENTS

In this article a fabrication process for the realization of full wafer stencils (100 mm) containing mesoscopic apertures (between 250 nm and 300 μm) using a combination of an industrial wafer stepper technology and an advanced MEMS process has been demonstrated. Micro- and nano-scale apertures were defined in a thin solid state SiN layer by means of DUV exposure and dry plasma etch process. The stencil membranes were released using a combination of wet chemical etching of the bulk silicon until approximately 10 μm silicon bulk was left and subsequent dry etch releasing. This combination allows a higher yield of the membranes due to reduced risk of stiction and membrane rupture. Micro- and nano-scale structuring using this full wafer stencil allows a large choice of materials and surfaces to be nanopatterned, as no etch steps need to be applied.

We have studied nanopatterns of various materials such as Al, Au, Bi, Cr, Cu, Ni, and Ti for various mesoscopic experiments, on various surfaces such as Si, SiN, SiO$_2$, GaAs, HOPG, PDMS, and SU-8. Future work will comprise the incorporation of stabilization structures locally built into the membranes. This will allow the deposition of highly stressed materials without pattern deformation due to membrane deflection.

This fabrication process confirms the compatibility of industry standard DUV and research based MEMS technologies to achieve process selectivity and accuracy for MEMS technology at the submicrometer level.

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