Jitter Tolerance Analysis of Clock and Data Recovery Circuits using Matlab and VHDL-AMS

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Abstract

In the scope of the development of a complete top-down design flow targeting clock and data recovery circuits for high-speed data links, we present two methods to analyze the jitter tolerance of such links, based on statistical simulation of incoming data jitter and its effects on the recovered data bit error rate using Matlab. The second method is based on time-domain simulation using VHDL and VHDL-AMS, where the bit-error rate is estimated based on the eye opening in the eye diagram.

1. Introduction

As jitter blurs the data edge information in the incoming data stream, it is the dominant contributor to bit errors in clock recovery circuits which are designed to extract the clock information contained in the data. In this paper, we discuss jitter tolerance (JTOL) and apply its analysis to a recently presented multi-channel clock recovery circuit [Mul05]. The presented paper extends the concepts of jitter tolerance simulation using standardized test methods in VHDL-AMS. It also presents improved statistical models for bit error rate estimations of the discussed clock recovery topology.

Serial data links can be realized either using electrical signals over copper wires and printed circuit board traces or optical signals using optical fibers and on-board waveguides. In both cases, the incoming signal must be conditioned, i.e. amplified and equalized, before entering the clock and data recovery (CDR) block (Figure 1a). Proper clock recovery in the receiver requires a sufficient number of data transitions, guaranteed in short-distance communications by data encoding. The commonly used 8b/10b encoding scheme for gigabit-rate links guarantees a transition density of 0.6 and a maximum number of consecutive identical digits (CID) of five.

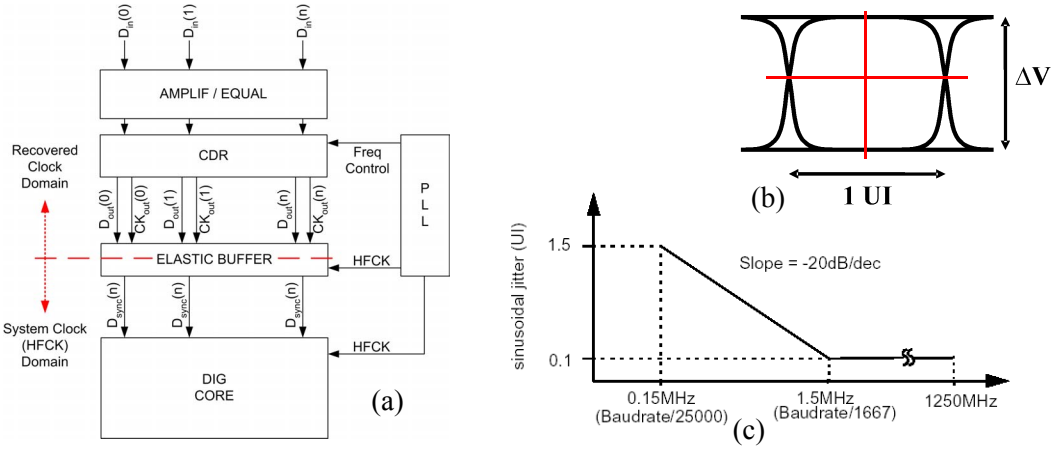


Figure 1: a) System view of digital core with serial I/O, b) eye diagram with optimum sampling point, c) InfiniBand™ jitter tolerance specification [IBTA01]

Although the data rate of each channel is tightly controlled by its local oscillator (typically to ±100ppm), the phases of the incoming data streams are independent. The lowest bit error rate (BER) is achieved when the incoming data is sampled at the ideal sampling instant, typically located in the middle of two possible transitions of the eye diagram (Figure 1b). Such an eye diagram is built from the received data waveform by superimposing all bit periods in the data stream. Timing jitter, the time-domain analogy of phase noise, expresses the uncertainty of the data edges with respect to the sampling instant due

to device noise (random jitter) and systematic errors (deterministic jitter). Random jitter (RJ) is related to thermal, flicker and shot noise sources. Deterministic jitter (DJ) is related to crosstalk, intersymbol interference (ISI) and other bounded jitter sources [KS04], [Ou04]. The tolerance to jitter on the incoming data stream is tested by superimposing to the existing jitter a sinusoidal jitter (SJ) component, which amplitude and frequency can be adjusted for the purpose of the measurement. The maximum sinusoidal jitter amplitude, at which the receiver guarantees a given BER (typically 10^{-12} or 10^{-15}) is called jitter tolerance and shall meet the specification curve in Figure 1c.

2. The Gated Oscillator Topology

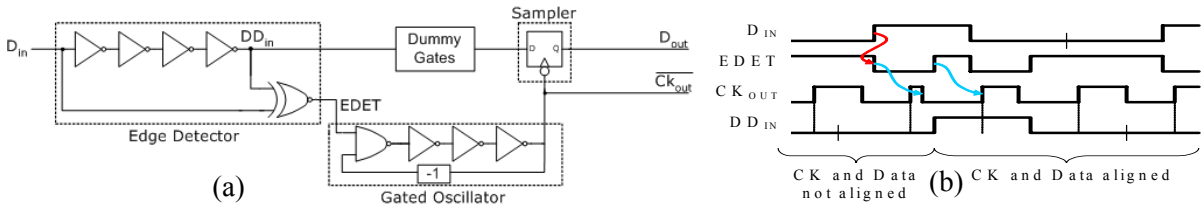


Figure 2: a) Single channel schematic and b) timing diagram

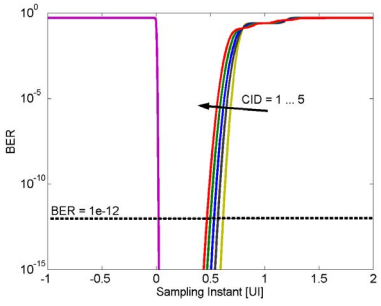
The gated oscillator topology (Figure 2a), with its shared PLL and one oscillator per channel, achieves high data rates while consuming little power per channel and occupying minimum silicon area. The shared PLL multiplies the low-frequency reference clock to obtain a high-frequency reference at 2.5GHz. A copy of the CCO tuning current in the PLL is distributed to each of the gated CCOs (GCCOs) to obtain the same nominal frequency. The input delay line generates an edge detection (EDET) signal at each data edge, used to reset the oscillator's phase. Frequency offsets between the different GCCOs due to device mismatch and power supply variations in the supply grid and the absence of memory in the system require careful analysis of the frequency tolerance (FTOL) of the presented topology.

3. Statistical Modeling

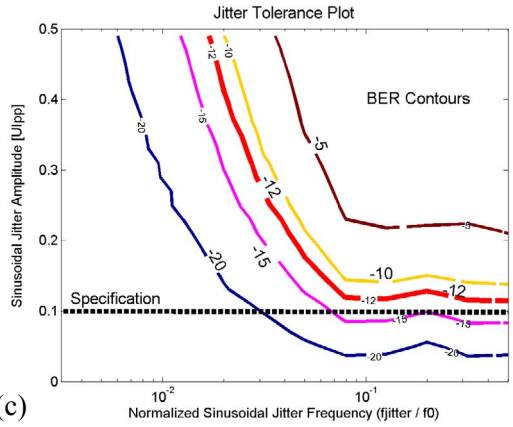
The statistical model does not take into account actual implementation details and delivers insight on the jitter and frequency tolerance in limited simulation time. A statistical model can either consider jitter on data edges and clock edges [Max02] or refer all jitter components to one of the two signals, the other being considered ideal. As each data edge retimes the GCCO, jitter and frequency offset accumulate differently on both edges in the eye diagram. For this reason, we consider an ideal sampling point at 0.5UI and apply all jitter components to the data edges.

```
edge2_off = d2ck_del + delta_f_rel * (CID-0.5);
edge2_sigma = gvco_k * sqrt(CID-0.5) + RJ;
pdf_rjdj_edge1=normpdf(x, edge1_off, edge1_sigma);
pdf_rjdj_edge2=0.5*normpdf(x, 1.0-DJ/2+edge2_off, edge2_sigma)
              +0.5*normpdf(x, 1.0+DJ/2+edge2_off, edge2_sigma);
```

(a)



(b)



(c)

Figure 3: (a) Statistical Model, (b) Bathtub curves for CID=1...5 (not weighted) and (c) BER Estimation

The initial model has been improved in several points:

- The transition probability of 0.5 for random data is taken into account in the calculation of BER.
- The deterministic jitter model is more accurate, using two Dirac functions instead of a uniform distribution. [KS04]
- The sinusoidal jitter probability distribution has been modeled more accurately. The initial model used a waveform, the new model is based on the explicitly derived PDF.

- Sampling points exceeding -0.5UI or 1.5UI are accounted for in the BER calculation. A data edge beyond these limits must be accounted for as a true error.
- The BER estimation considers the resulting bit error rate of a 1-n CID and calculates the resulting BER as a weighted sum of these individual BER=f(CID). The weights are determined by the probability of occurrence of a given number of CID in an encoded random data stream.

Figure 3b shows the resulting probability densities for both data edges. The bit error rate (Figure 3c) can be estimated by integrating the area under the curves on the opposite side of the ideal sampling point.Time-Domain Modeling

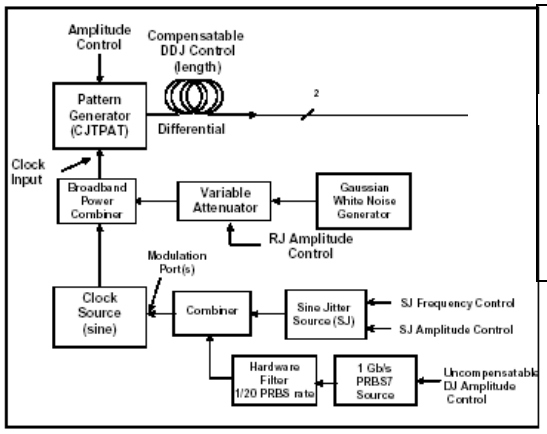
3.1. Clock Recovery Model

The statistical model previously discussed gives a good estimate of the achievable performance, but it cannot perform verification of the time-domain behavior of the selected topology. However this verification enables the analysis of jitter and frequency tolerance as a function of gate delays and jitter sources.

The clock recovery circuit being an event-driven circuit and operating on two-level (binary) signals, the initial time-domain model presented in [Mul05] is based on a pure VHDL description. The limitations of this model are:

- The phase noise of each delay cell is modeled using a VHDL random number generator. We can thus not guarantee statistically decorrelated jitter values for each cell.
- As the clock recovery simulation uses event-based models, no amplitude noise or input sensitivity can be analyzed. Even in a full-featured AMS model, it is difficult to include amplitude noise and sensitivity analysis in a convenient way, without excessive increase in simulation time.
- The deterministic jitter is modeled using a uniform probability density function. This is an acceptable approximation for first guess analysis, but not sufficient for exact performance analysis.
- Random jitter in the data stream is modeled as a phase modulation signal instead of being added in power to the reference clock, although this is subject to ongoing discussion [BvE01].

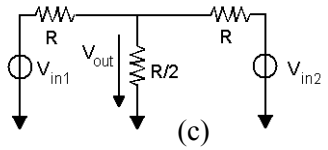
3.2. Input Data Source with Extended Jitter Model



(a)

```
architecture bhv of sin_clk_src is
  [...]
begin
  -- All quantities considered in a 50 Ohm environment
  -- Voltage source is 2 * effective voltage
  vmod_in == imod_in * 25.0;
  -- Voltage is centered around Vdd/2=0.9V and scaled to full - scale
  dph == (vmod_in - 0.9) * kvco * MATH_2_PI / 0.9;
  vsin_clk_int == 2.0 * (0.9 + 0.9 * sin(MATH_2_PI*freq*NOW+dph));
  vsin_clk == vsin_clk_int + isin_clk * 50.0;
end bhv;
```

(b)



(c)

Figure 4: a) Example of an electrical signal tolerance source [IN04], b) VHDL-AMS code of the electrical signal tolerance source and c) equivalent schematic of the power combiners

In order to obtain more accurate deterministic and random jitter components, the following data source, defined in [IN04] (Figure 4a), has been implemented in VHDL-AMS. The pattern generator delivers a so-called *compliant jitter tolerance pattern* (CJTPAT), composed of the data words representing the worst case condition for jitter tolerance measurement of the receiver. The *compliant* term indicates that the effective stress pattern is embedded into data frames including delimiters, fill words and CRC, which is necessary when physical links are tested. For simulation of clock recovery and data retiming, the *jitter tolerance pattern* (JTPAT), which corresponds to the payload of the CJTPAT, is sufficient. Deterministic, random and sinusoidal jitter contributions are applied to the signal around the pattern generator. Uncompensatable deterministic jitter (UDJ) is generated using a low-pass filtered pseudo-random

bit sequence (PRBS), which is combined with the sinusoidal jitter source and applied as a modulation signal to the clock source. A sinusoidal clock source is used to allow proper modulation by the previously mentioned components. Random jitter is then added to the clock signal, the resulting signal being applied as a timing reference to the pattern generator. The resulting pattern is bandwidth limited by a first order filter resulting in compensatable deterministic jitter (DDJ, according to Equation 1).

$$DDJ[UI] = \frac{\tau}{T} \cdot \ln\left(\frac{1 + e^{\frac{-T_{MIN}}{\tau}}}{1 + e^{\frac{-T_{MAX}}{\tau}}}\right) \qquad (1)$$

$$DDJ[UI] \cong \frac{\tau}{T} \cdot \ln\left(1 + e^{\frac{-T_{MIN}}{\tau}}\right)$$

$$vsin\_clk = 0.9 + 0.9 \cdot \sin(2\pi f_{clk} t + d\phi)$$

$$\text{with} \quad d\phi = \frac{vmod_{in} - 0.9}{0.9} \cdot k_{VCO} \cdot 2\pi \qquad (2)$$

$$\text{and} \quad vmod_{in} = 0.9 + 0.9 \cdot \sin\left(2\pi \frac{f_{jit}}{f_{clk}} f_{clk}\right)$$

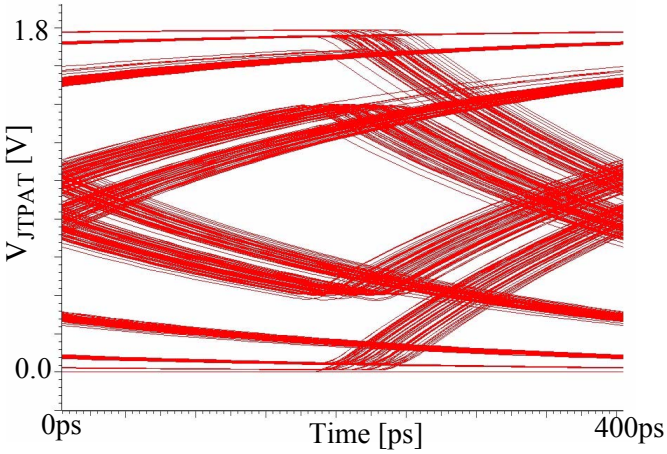


Figure 5: VHDL-AMS JTPAT data source for SJ_{amp}=0.1 SJ_{freq}/f_{ck}=0.0211 UDJ=0.1 DDJ=0.2 RJ=0.001

The signal combiners are modeled as Thévenin-equivalent voltage sources with a source resistance of 50Ω driving a shared load resistance of 25Ω (Figure 4c), where the ideal voltage sources deliver twice the output voltage. The supply voltage is set to 1.8V, output voltages are centered around $V_{DD}/2$=0.9V. Phase modulation is applied to the sinusoidal clock *vsin_clk* according to Equation 2. The multiplication of source voltage by 2 for impedance matching is omitted in the equations below. The k_{VCO} factor of 2.0 compensates for the 6dB loss of the power combiner for each of its inputs. Figure 5 shows the eye diagram of the data output by the JTPAT data source with different jitter components applied.

4. Conclusion

We introduced a simulation flow for jitter and frequency tolerance analysis of clock and data recovery circuits, leading to a quick comparison of CDR topologies through statistical simulation. Time-domain VHDL-AMS simulation increases the reliability of the results, due to accurate modeling of real jitter mechanisms. We believe this simulation flow allows fast and accurate analysis of CDR topologies and improves the performance of low-power clock recovery designs for multi-channel serial data interfaces.

This work has been supported in part by the Swiss National Science Foundation Grant 200021-100625.

5. References

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