Realization of Compact Low-Power Ripple-Flash A/D Converter Architectures Using Conventional Digital CMOS Technology

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Abstract

In this paper, we present a generalized approach for the construction of ripple-flash ADC architectures that consist of cascade-connected capacitive threshold gates, realized using conventional CMOS technology. The main advantages of the proposed ADC architecture are the very small layout area, simple operation, high input-to-output response speed, and very low power dissipation. A new differential output voltage comparator is presented to ensure high precision and low propagation delay times. Several different ADC implementations are explored, including 4-bit, 5-bit and 6-bit ripple-flash circuit that demonstrate highly accurate DC transfer characteristics with INL errors smaller than 0.1 LSB, and near-ideal SNR levels for sampling frequencies of up to 50 MHz. Test circuits manufactured with 0.8 um CMOS technology have shown that sampling rates in excess of 50 MHz are possible with this approach, while the silicon area and the power dissipation of the tested ADC circuits remain at least one order of magnitude smaller than those of similar flash ADCs built with the conventional approach.

1. Introduction

Fully capacitive (charge-based) 4-bit ripple-flash ADC circuits that are implemented with mixed-input threshold logic gates were presented earlier [1], [2], [3]. It was shown that the capacitive ripple-flash circuit architecture offers numerous advantages for the realization of very compact ADC blocks, including a high response speed, low power dissipation, and small silicon area. The basic circuit architecture is fully CMOS compatible, operates on a single-phase clock scheme, and it requires no externally generated reference voltage levels other than VDD and GND for its operation. Extensive simulation results and experimental verification of test circuits have already demonstrated that 4-bit ADC structures based on this architecture can achieve high accuracy (INL less than 0.1 LSB) and sampling clock rates of up to 20 MHz [3].

The realization of accurate 5-bit and 6-bit ADC blocks using this circuit architecture, however, depends very heavily on the precision and the response speed of the output voltage comparators that are used to evaluate the output signal of each threshold gate. Since the voltage perturbations that need to be evaluated in 5-bit and 6-bit ADCs are much smaller that those encountered in 4-bit ADCs, implementation of larger ADCs was not considered feasible using the previous voltage comparator structures. In this paper, we propose a new differential output voltage comparator that allows significantly more accurate evaluation of threshold gate output signals and faster response times, compared to the CMOS inverter-based voltage comparators used in earlier designs. Thus, the proposed voltage comparator allows, for the first time, compact realization of larger bit-length ADCs that are based on the capacitive ripple-flash circuit architecture. Also, a generalized design approach is presented for the construction of ripple-flash converters. The ADC blocks presented here offer significant advantages in terms of silicon area, power dissipation, and propagation delay time.

In the following, the voltage comparator circuit structure, its operation and implementation in the capacitive ripple-flash ADC architecture are described in Sections 2 and 3. Simulation results of 5-bit and 6-bit ADC circuits are presented in Section 4. Finally, Section 5 provides a summary of our results and conclusions.

2. Description of the Ripple-Flash ADC Architecture

The proposed analog-digital converter architecture essentially consists of threshold logic gates, which can process analog and digital input signals simultaneously and produce a digital output signal as the result of a simple thresholding function. The block diagram of a 4-bit threshold-logic based ADC is given in Fig. 1. Here, each block represents a mixed-input thresholding function. At the functional level, the operation of the four threshold logic gates can be described as follows:

$$V_{out3} = V_{DD} \quad if \quad V_A > \frac{8}{16}V_{DD}$$

$$V_{out2} = V_{DD} \quad if \quad V_A > \frac{12}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}}$$

$$V_{out1} = V_{DD} \quad if \quad V_A > \frac{14}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}} - \frac{4}{16}\overline{V_{out2}}$$

$$V_{out0} = V_{DD} \quad if \quad V_A > \frac{15}{16}V_{DD} - \frac{8}{16}\overline{V_{out3}} - \frac{4}{16}\overline{V_{out2}} - \frac{2}{16}\overline{V_{out1}}$$

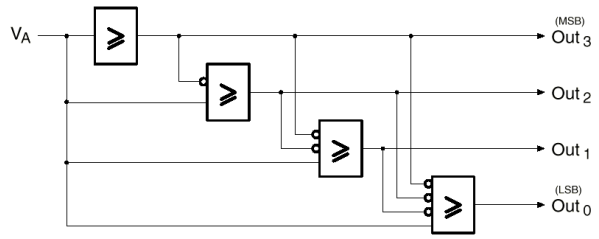

Figure 1: Block diagram of the 4-bit ripple-flash ADC.

Note that the four output bits (Out_0 through Out_3) are generated by four threshold decisions, each of which is performed by a mixed-input threshold gate. The entire conversion operation described above can be completed in a single clock cycle, hence, the 4-bit ADC circuit presented here is called a ripple-flash ADC. The mixed-input threshold relations given for the 4-bit ADC case can also be generalized for larger bit-length ADC structures. The accuracy of the proposed ADC circuit, however, will depend very heavily on the accuracy of the voltage comparators that are used to evaluate the output of each threshold gate.

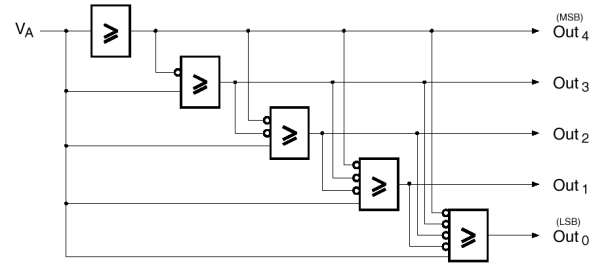

Figure 2: Block diagram of the 5-bit ripple-flash ADC.

Figure 2 shows the block diagram of a 5-bit ripple-flash ADC circuit, and its operation can be described by the following equations:

$$V_{out4} = V_{DD} \quad if \quad V_A > \frac{16}{32}V_{DD}$$

$$V_{out3} = V_{DD} \quad if \quad V_A > \frac{24}{32}V_{DD} - \frac{16}{32}\overline{V_{out4}}$$

$$V_{out2} = V_{DD} \quad if \quad V_A > \frac{28}{32}V_{DD} - \frac{16}{32}\overline{V_{out4}} - \frac{8}{32}\overline{V_{out3}}$$

$$V_{out1} = V_{DD} \quad if \quad V_A > \frac{30}{32}V_{DD} - \frac{16}{32}\overline{V_{out4}} - \frac{8}{32}\overline{V_{out3}} - \frac{4}{32}\overline{V_{out2}}$$

$$V_{out0} = V_{DD} \quad if \quad V_A > \frac{31}{32}V_{DD} - \frac{16}{32}\overline{V_{out4}} - \frac{8}{32}\overline{V_{out3}} - \frac{4}{32}\overline{V_{out2}} - \frac{2}{32}\overline{V_{out1}}$$

3. Circuit Implementation of Ripple-Flash ADC Architectures

For the realization of mixed-input threshold functions described in Section 2, a slightly modified version of the charge-based Capacitive Threshold Logic (CTL) gate structure is being used. The simplified circuit diagram of the four-bit ADC is shown in Fig. 3, while the circuit diagram of a five-bit ADC is shown in Fig. 4. Note that each CTL gate consists of a row of weighting capacitors, and a voltage comparator to sense and amplify the row voltage perturbation [3].

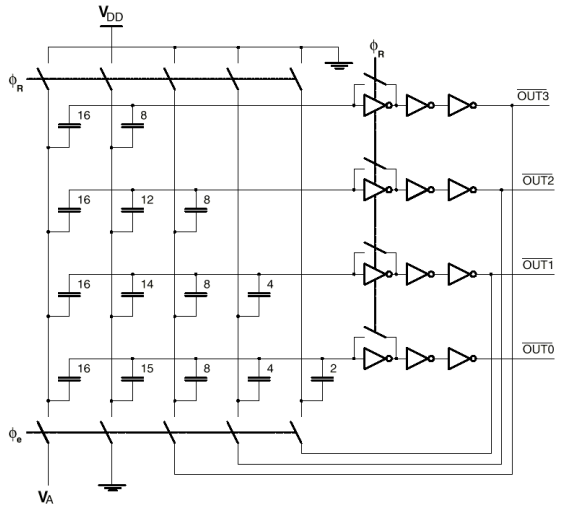

Figure 3: Simplified circuit schematic of the 4-bit ADC.

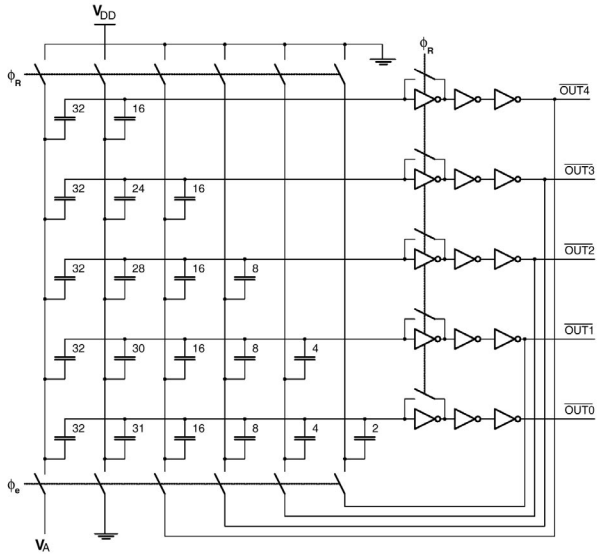

Figure 4: Simplified circuit schematic of the 5-bit ADC.

The generalized input-output relationship of each individual capacitive row in this structure is :

$$V_A \cdot C_A + \sum_{i=1}^{m} V_i \cdot C_i > V_{DD} \cdot C_T \rightarrow V_{out} = V_{DD}$$

$$V_A \cdot C_A + \sum_{i=1}^{m} V_i \cdot C_i < V_{DD} \cdot C_T \rightarrow V_{out} = 0$$

$$\Rightarrow \quad V_A > V_{DD} \cdot \frac{C_T}{C_A} - \sum_{i=1}^{m} V_i \cdot \frac{C_i}{C_A} \quad \rightarrow \quad V_{out} = V_{DD}$$

where C_A denotes the weight capacitor of the analog input V_A, C_i denotes the weight capacitors of the digital inputs V_i and C_T is the threshold capacitor. This, it is demonstrated that the mixed-input CTL structure is capable of realizing the thresholding functions described earlier in Section 2. The same basic circuit architecture has also been used for the implementation of the 6-bit ripple-flash ADC.

A new differential voltage comparator is used to sense and evaluate the voltage perturbation in each row. The circuit diagram of the proposed output voltage comparator circuit is shown in Fig. 3. When CLK is low, the feedback in M3, M4, M6 and M7 is overcome by switch M5. When CLK is high, the regenerative amplifier M1-M4 amplifies the input perturbation, and the pair M6-M7 switches the output difference. The output of the comparator is latched at the end of the clock cycle.

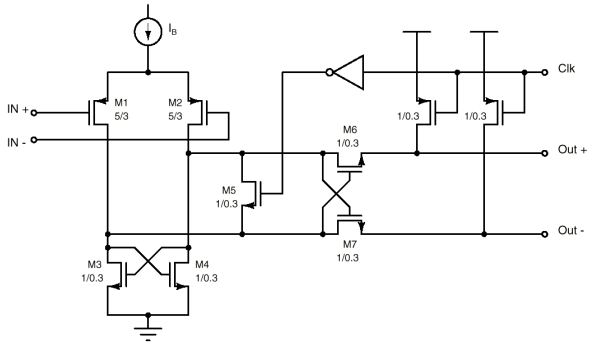

Figure 5: Circuit schematic of the differential comparator.

4. Silicon Realization of Ripple-Flash ADCs

Four-bit and five-bit ripple-flash ADC circuits have been realized using a 0.8 micron double-polysilicon CMOS process, while five-bit and six-bit ADCs with the new differential voltage comparator were realized using a 0.35 micron double-polysilicon CMOS process. The layouts of the 4-bit and the 5-bit ADC circuits are shown in Fig. 6 and Fig. 7, respectively.

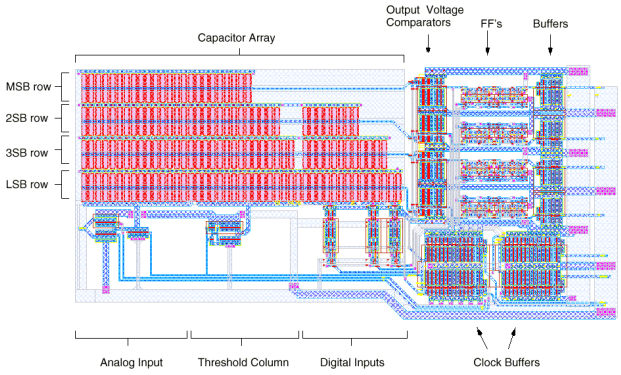

Figure 6: Mask layout of the 4-bit ripple-flash ADC circuit.

The silicon area occupied by the 4-bit ADC circuit is 0.08 sqmm, while the area of the 5-bit ADC circuit is 0.15 sqmm. In both cases, it can be seen that the capacitor array is the dominant circuit block of the ADC architecture, flanked by the input switches, output voltage comparators, and output latches. Note that the silicon area compares very favourably with other flash ADC realizations that offer a similar performance.

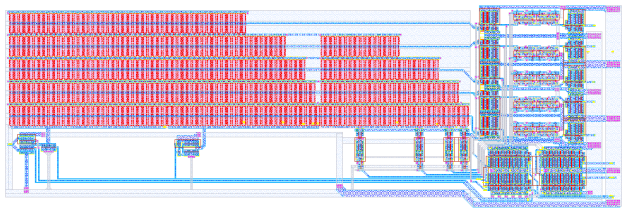

Figure 7: Mask layout of the 5-bit ripple-flash ADC circuit.

5. Measurement Results and Circuit Performance Evaluation

All of the designed ripple-flash ADC circuits exhibit correct monotonic output behavior over the entire range, with no missing output codes. Figures 8, 9 and 10 show the integral non-linearity error of 4-bit, 5-bit and 6-bit ADC circuits, respectively. Note that the INL value remains smaller than 0.1 LSB over the entire input range. The DNL error is less than 0.05 LSB over the full range. The typical input-to-output transient response time of the ADC is smaller than 40 ns on average, and it does not exceed 60 ns, which qualifies the simple charge-based ADC architecture for high-speed applications. The signal to noise ratio of the 4-bit ADC as a function of the sampling frequency is plotted in Figure 11, indicating a 3-dB limit of about 50 MHz.

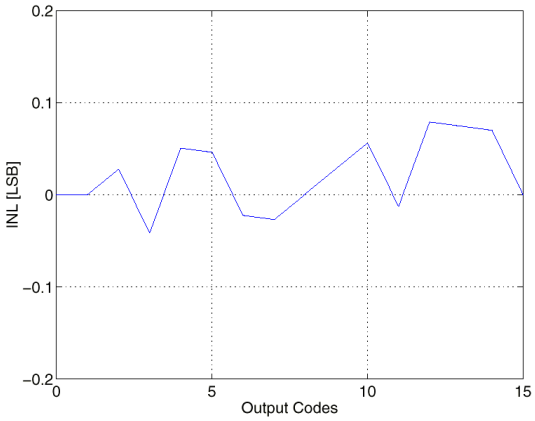

Figure 8: Measured INL error of the 4-bit ADC.

The measured power dissipation of the 4-bit ADC increases linearly with the clock frequency, and remains lower than 15 mW at a sampling frequency of 20 MHz. To evaluate the performance under fair conditions, the power dissipation of the CTL-based ripple-flash ADC circuit has been normalized with respect to the number of bits, the sampling clock frequency and the fabrication technology (feature size), and then compared with 25

previously published flash converter results. Figure 12 shows that the proposed circuit architecture (3 different variants plotted) is clearly superior to other circuit architectures in terms of normalized power dissipation.

A similar comparison has been made for the silicon area occupied by the ADC, where the area has been normalized with respect to the number of output bits and the fabrication technology. Again, the proposed CTL architecture offers a clear area advantage of about one order of magnitude.

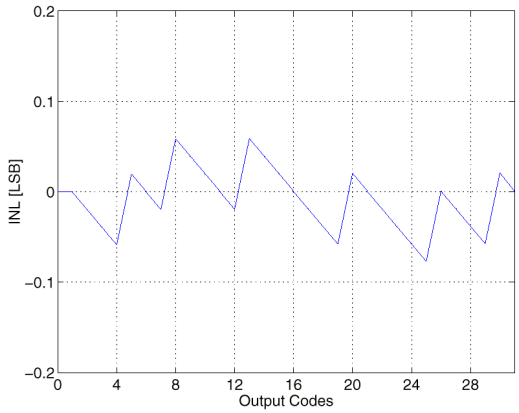

Figure 9: Measured INL error of the 5-bit ADC.

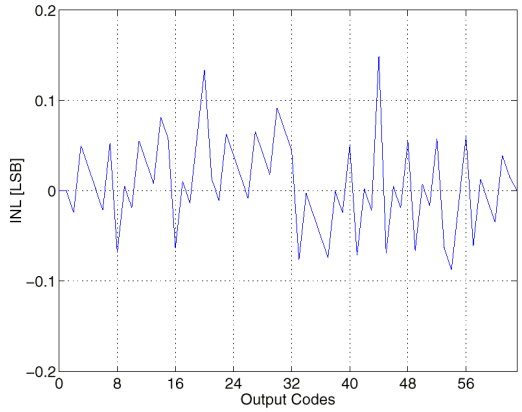

Figure 10: Measured INL error of the 6-bit ADC.

6. Conclusion

In this paper, the circuit architecture and operation of a class of novel analog-digital converters has been presented, which is based on cascade-connected mixed input capacitive threshold gates. The circuit structure, which is realized using conventional CMOS technology, offers a very small layout area, simple operational requirements, low power dissipation, and very high input-to-output response speed. Fabricated four-bit, five-bit and six-bit flash ADC circuits have been tested to exhibit highly accurate DC transfer characteristics, and very fast response times. In particular, the normalized power dissipation and the normalized silicon area of the new class of ADCs have been shown to be clearly superior to conventional designs. The charge-based ADC circuits proposed here can also be used as reliable building blocks in high-speed pipelined ADC architectures with higher accuracy.

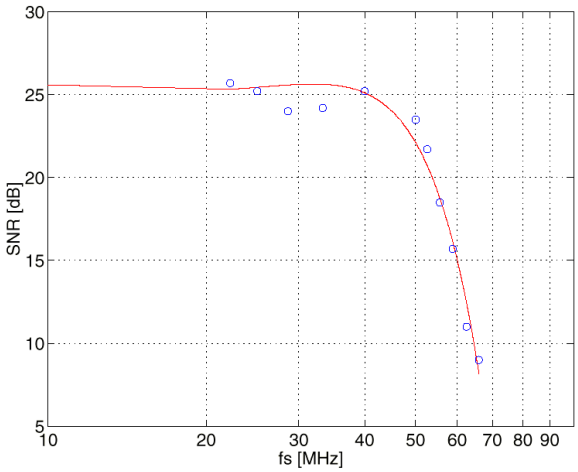

Figure 11: SNR of the 4-bit ADC, as a function of the sampling clock frequency (input signal frequency 0.9 MHz)

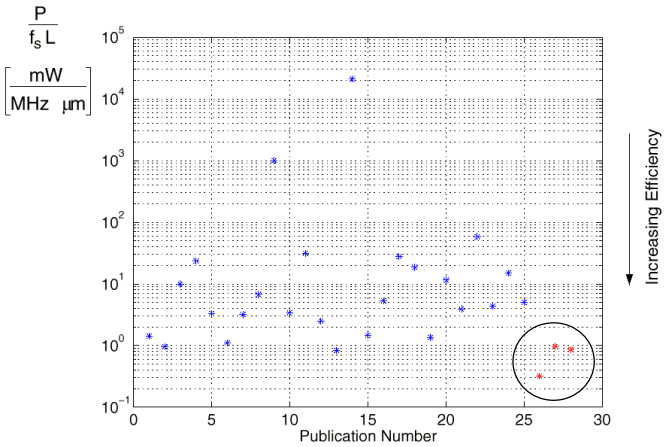

Figure 12: Comparison of the normalized (per bit) power dissipation of published flash converters in the literature. The three points circled in the lower right corner belong to three different variants of CTL-based ripple-flash ADCs.

References

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[2] B. Onat et al., "Implementation of a charge-based neural Euclidian classifier for a 3-bit flash analog-to-digital converter," *IEEE Transactions on Instrumentation and Measurement*, vol. 46, pp. 672-677, June 1997.

[3] A. Schmid et al., "A novel analog-digital flash converter architecture based on capacitive threshold logic gates," Proceedings of *1999 IEEE International Symposium on Circuits and Systems*, May 1999, Orlando, FL.