Implementation of a Low-Power 200 MSample/s 12-bit Pipelined ADC Macro Using Deep-Submicron Digital CMOS Technology

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Abstract

In this paper, we present the design, verification, system integration and the physical realization of a fully integrated high-speed analog-digital converter (ADC) macro block with 12-bit accuracy. The entire circuit architecture is built with a modular approach, consisting of identical units organized into an easily expandable pipeline chain. A bit-overlapping technique has been employed for digital error correction between the pipeline stages to reduce possible errors that occur during analog signal processing. The circuit has been realized using 0.18 μm digital CMOS technology.

The ADC macro presented in this work is capable of operating at sampling frequencies of up to 200 MHz, and still can achieve the nominal bit-resolution that was intended for 12-bit accuracy. The maximum range of the input signal amplitude can be as high as 1.6 Vpp, with 1.8 V supply voltage. The overall power consumption is estimated as 67.5 mW at 200 MHz sampling rate. The overall silicon area of the ADC is approximately 0.25 mm^2. The presented ADC architecture qualifies as a very versatile embedded macro block that can be used in deep-submicron SoC design.

1. Introduction

High-performance analog-to-digital converter (ADC) blocks are needed for a very wide range of applications in wireless telecommunications, instrumentation, medical imaging, audio and video processing. Sampling rates in excess of 100 MHz and a bit-resolution of more than 10 bits are usually required to accommodate the very high bandwidth demands in wireless applications [1]-[3], where portability and low power dissipation are very significant concerns. In addition, the increasing trends towards using deep-submicron CMOS technologies and system-level integration create the need to develop compact, high-performance ADC macro blocks that can be realized with mainstream digital CMOS processes and integrated as embedded building blocks in SoC designs.

In this paper, we present the design, verification, system integration and the physical realization of a high-speed analog-digital converter macro (ADC) with 12-bit accuracy. The architecture of the ADC has been realized as a pipelined structure consisting of four pipeline stages, each of which is capable of processing the incoming analog signal with 4-bit accuracy. A bit-overlapping technique has been employed for digital error correction between the pipeline stages so that the influence of possible errors that occur during analog signal processing can be minimized. The entire circuit architecture is built with a modular approach, consisting of identical blocks organized into an easily expandable pipeline chain.

All analog as well as digital sub-blocks of the ADC architecture presented in this work operate on a single clock signal, which significantly simplifies the design while ensuring a more robust performance. Other important features of this ADC include small area, single power supply, low power consumption, capability to operate at very high sampling clock rates, and the ability to handle a wide range of input signal amplitudes.

The presented ADC architecture was realized using a conventional 0.18 micron digital CMOS technology (Foundry: UMC), to ensure the portability for the design. In the following, the main building components of the ADC architecture and the construction of the pipeline stages are discussed in Sections 2 and 3, respectively. The overall system integration is described in Section 4. Finally, Section 5 provides a summary of conclusions.

2. Description of the Main Building Blocks

To realize the proposed circuit architecture, four basic building blocks were required: (i) high-speed voltage comparators, (ii) very high bandwidth op-amps with low offset, (iii) high-speed multiplying DAC (capacitive MDAC), and (iv) the digital correction circuitry including a 11-bit ripple carry adder. Initially, these key components were designed to meet the desired specifications, and then, the overall physical design of the ADC has been constructed by following a simple modular approach [4].

The voltage comparator is one of the most important components that dictate the resolution of the overall A/D converter as well as the conversion speed of the converter. Several different topologies were studied, all of which were derived from the same basic structure. The full complementary circuit architecture shown in Fig. 1 was chosen as the final design, aided with a simple inverter based output stage to further improve the

response times. The worst-case input voltage offset of the improved complementary comparator was found to be less than 4 mV, allowing conversion with 8-bit accuracy at a dynamic input range of 1.6 V_{pp}. The worst-case INL and DNL errors remain within ± 0.01 LSB for the 4-bit application. Typical response times obtained for this voltage comparator are less than 450 ps, allowing operation speeds of up to 1 GHz. The circuit occupies a silicon area of about 320 μm^2 and consumes 800 μW at 200 MHz sampling frequency.

Using the designed voltage comparator as the main building block, a 4-bit flash A/D converter was built which is capable of operating at sampling clock frequencies up to 800 MHz with a signal-to-noise ratio of greater than 22.84 dB. It was verified that the designed 4-bit flash A/D converter is capable of processing input signal frequencies up to 80 MHz with 200 MHz sampling clock rate. The SNR plot vs. the sampling frequency is shown in Figure 2.

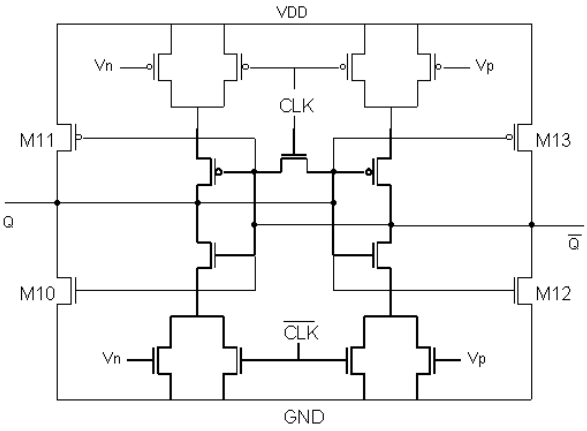

Figure 1: Circuit diagram of the voltage comparator.

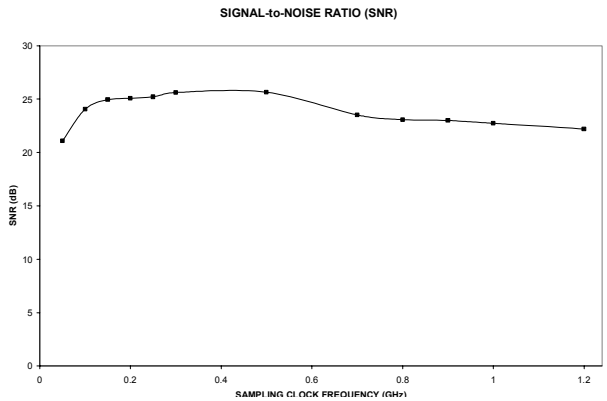

Figure 2: Variation of the 4-bit ADC signal-to-noise ratio (SNR) as a function of the sampling frequency.

A very high bandwidth operational amplifier with low output offset is needed as the key building block of the 4-bit multiplying DAC unit, in order to realize the residue signal amplification and to achieve the required isolation of the analog pipeline stages. The single ended OTA-based circuit architecture shown in Figure 3 was preferred in both of the designed versions, using a 1.8 V single power supply. The open-loop unity-gain frequency of the designed high gain op-amp is 2.16 GHz, while its open-loop gain is approximately 48.5 dB. Consequently its closed-loop 3dB frequency is 665 MHz, and input referred offset is 1.2 mV. The second implementation is a unity-gain stable (low gain) op-amp with an open-loop gain of 33.4 dB and 1.4 GHz unity gain frequency. Its closed-loop (unity gain configuration) 3dB frequency is 1.43 GHz. The input referred offset of the second op-amp implementation is less than 4 mV. With these operational characteristics, both of the designed op-amps are suitable for 12-bit data conversion at 200 MHz sampling clock frequency. The transient pulse response of the unity-gain amplifier stage is shown in Figure 4, with a pulse frequency of 200 MHz and the input signal amplitude of 10 mV.

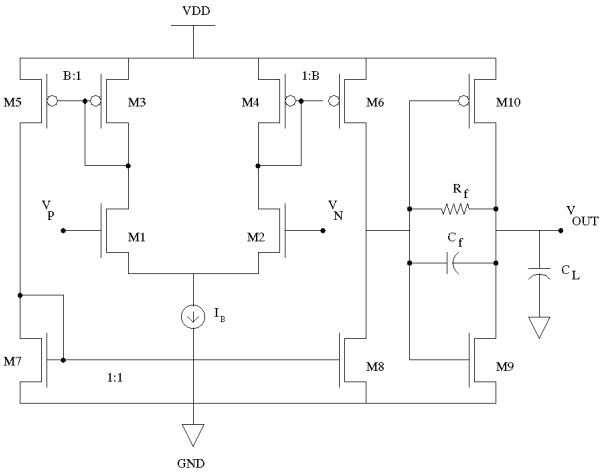

Figure 3: Circuit diagram of the OTA-based opamp.

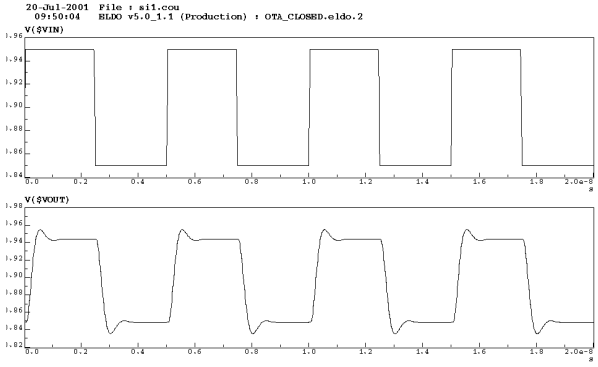

Figure 4: Pulse response of the unity-gain stable opamp at a pulse frequency of 200 MHz and amplitude of 10 mV.

3. Construction of the Pipeline

The D/A converter play a very critical role in pipelined ADC architectures. Resolution and conversion speed mostly depend on how fast and accurate the DAC can generate its response. Based on the residue amplifier

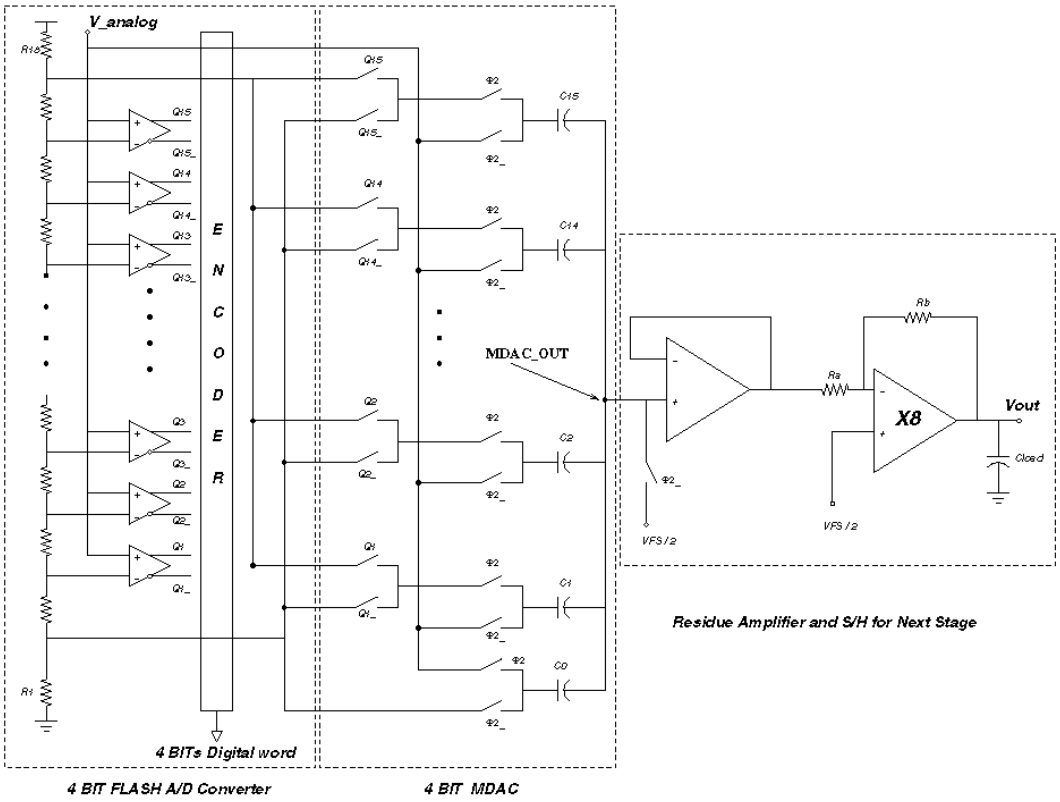

Figure 5: Complete circuit diagram of the 4-bit analog pipeline stage consisting of the 4-bit flash ADC and the MDAC.

blocks described above, the typical response time of the monotonic MDAC (multiplying DAC) that was designed for this architecture is about 400 ps, allowing 200 MHz operation speed in the analog pipeline. Figure 5 shows the overall circuit diagram of the 4-bit analog pipeline stage, consisting of the 4-bit flash ADC, output data encoder, multiplying DAC and the residue amplifiers. Figure 6 shows the time-dependent variation of the amplified residue voltage at the output of the 4-bit stage with a sampling clock frequency of 200 MHz.

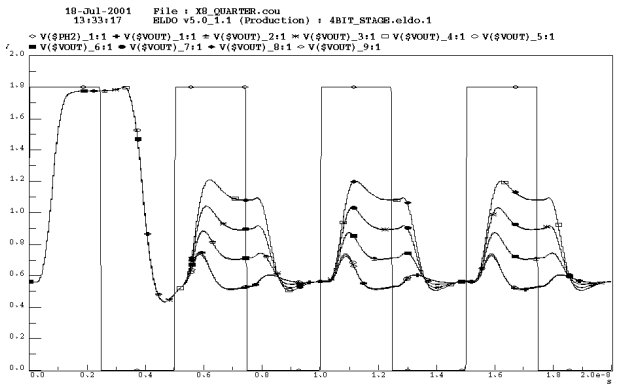

Figure 6: Time-dependent variation of the amplified residue voltage at a sampling clock frequency of 200 MHz, for four different input voltages.

The variation of the amplified residue voltage as a function of the input voltage is shown in Figure 7, proving that the 4-bit analog pipeline exhibits near-ideal characteristics.

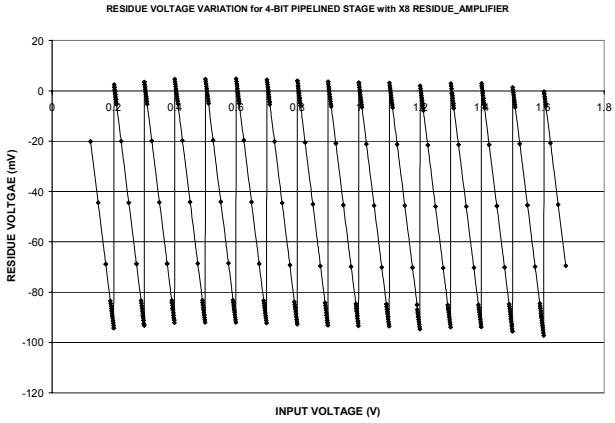

Figure 7: Amplified residue voltage as a function of the input voltage.

Finally, the performance of the digital pipeline depends critically on the response time of the error correction circuit that includes the 11-bit adder chain. Totally symmetric 1-bit full adder circuits were designed and used in a ripple-carry adder chain to facilitate the required 11-bit addition. Typical response time of the

eleventh carry-out signal is about 1.8 ns, which is sufficient for operation at 200 MHz clock frequency.

4. System Integration

The pipelined ADC architecture consists of four 4-bit stages, where the necessary error correction is achieved by a bit-overlapping technique. All analog as well as digital sub-blocks of the ADC architecture presented in this work operate on a single clock signal (and its inverse), which significantly simplifies the design while ensuring a more robust performance. The clock signal distribution is based on a balanced clock tree that runs between the analog and the digital pipeline blocks. The ADC architecture was realized using a conventional 0.18 micron digital CMOS technology (Foundry: UMC), which ensures a lower overall cost and better portability for the design. The mask layout of one 4-bit analog pipeline stage is shown in Figure 8.

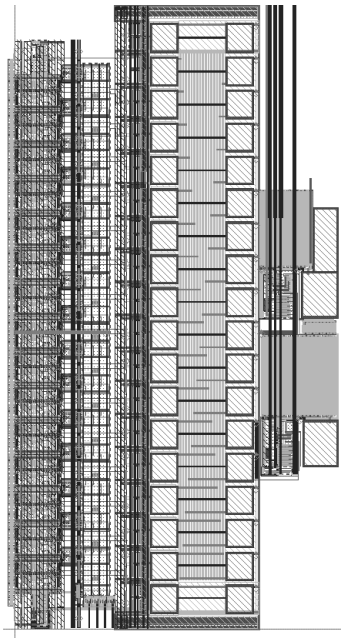

Figure 8: Mask layout of a 4-bit analog pipeline stage.

The ADC architecture presented in this work is capable of operating at sampling frequencies of up to 200 MHz, and still can achieve the nominal bit-resolution that was intended for 12-bit accuracy. The entire circuit is designed with single 1.8 V power supply. The maximum range of the input signal amplitude that the ADC can handle is 1.6 Vpp, with 1.8 V supply voltage. The input signal range as well as the operating points of critical components can be adjusted externally using dedicated control pins. The overall power consumption is estimated as 67.5 mW at 200 MHz sampling rate. Each 4-bit pipeline stage consists of a 4-bit flash A/D converter, a fully capacitive multiplying DAC (MDAC) and the corresponding digital encoding circuitry. The overall silicon area of the ADC is approximately 0.25 mm^2. The top-level mask layout of the entire ADC macro block is shown in Figure 9.

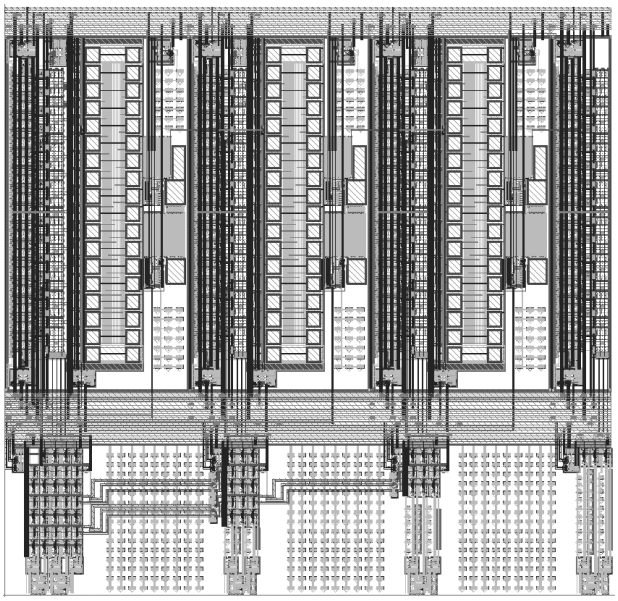

Figure 9: Top-level mask layout of the 12-bit pipelined ADC macro block. The silicon area is approximately 0.25 mm^2.

5. Conclusions

In this paper, we presented the design, verification, system integration and the physical realization of a fully integrated high-speed analog-digital converter (ADC) macro block with 12-bit accuracy. The entire circuit architecture is built with a modular approach, consisting of identical units organized into an easily expandable pipeline chain. A bit-overlapping technique has been employed for digital error correction between the pipeline stages to reduce possible errors that occur during analog signal processing. The circuit has been realized using 0.18 mm digital CMOS technology. The presented ADC architecture qualifies as a very versatile embedded macro block that can be used in deep-submicron SoC design.

References

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