Design and Realization of a 2.4 Gbps – 3.2 Gbps Clock and Data Recovery Circuit Using Deep-Submicron Digital CMOS Technology

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Abstract

This paper presents the design, verification, system integration and the physical realization of a high-speed monolithic phase-locked loop (PLL) based clock and data recovery (CDR) circuit. The architecture of the CDR has been realized as a two-loop structure consisting of coarse and fine loops, each of which is capable of processing the incoming low-speed reference clock and high-speed random data. Important features of this CDR include small area, single 1.2 V power supply, low power consumption, capability to operate at very high data rates, and the ability to handle between 2.4 Gbps and 3.2 Gbps data rate. The CDR architecture was realized using a conventional 0.13-µm digital CMOS technology, which ensures a lower overall cost and better portability for the design. The circuit is capable of operating at sampling frequencies of up to 3.2 GHz, and still can achieve the robust phase alignment. The overall power consumption is estimated as 18.6 mW at 3.2 GHz sampling rate. The overall silicon area of the CDR is approximately 0.3 mm^2 with its internal loop filter capacitors.

1. Introduction

The performance of many digital systems today is limited by the interconnection bandwidth between chips, boards, and cabinets. Although the processing performance of typical integrated systems has increased dramatically since the inception of the integrated circuit technology, the communication bandwidth between chips has not enjoyed a similarly dramatic increase. To facilitate off-chip communication, most VLSI circuits drive un-terminated lines with full-swing CMOS drivers and use CMOS gates as receivers. Hence, the bandwidth of such full-swing CMOS interconnect is limited by the length of the line rather than the performance of the semiconductor technology. Thus, as VLSI technology scales, the pin bandwidth does not improve with the technology, but rather remains limited by board and cable geometry, making off-chip bandwidth an even more critical bottleneck.

Serial data transmission is based on sending/receiving binary bits of information as a series of optical or electrical pulses. However, the transmission channel generally distorts the signal in various ways. From this distorted signal, the clock and the data must be recovered at the receiver side, and the clock must also be aligned with the recovered data. Phase-locked loop (PLL) based clock and data recovery (CDR) architectures are among the most widely preferred approaches to realize this functionality [1], [2].

This paper presents the design, verification, system integration and the physical realization of a monolithic high-speed clock and data recovery circuit with an operation range between 2.4 Gbps and 3.2 Gbps. The circuit is implemented and produced by using commercially available 0.13-µm digital CMOS technology. The entire circuit architecture is built with a fully differential approach, consisting of symmetrical blocks and signal paths organized with special low-voltage design and layout techniques.

2. General Architecture of the CDR Block

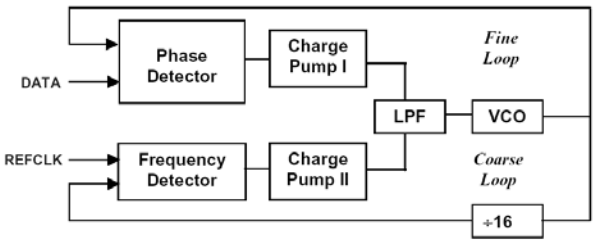

Figure 1: Block diagram of the two-loop CDR block.

The circuit architecture has been realized as a two-loop structure consisting of coarse and fine loops, each of which is capable of processing the incoming reference low-speed clock and high-speed random data respectively. The block diagram of the two-loop clock recovery circuit is given in Fig. 1. To realize the proposed circuit architecture, dynamics of the two separate loops have been determined individually and specifications of each block were evaluated. In the initial stages of the design, the CDR has been modelled and simulated by using MATLAB and *Simulink* software. Basic building blocks of the two-loop architecture are: (i) phase-frequency detector for coarse loop, (ii) charge pump for the coarse loop, (iii) phase

detector for the fine loop, (iv) charge pump for the fine loop, (v) differential voltage-controlled oscillator (VCO), and (vi) differential loop filter.

The phase-frequency detector in the coarse loop guarantees that the device locks to the proper data frequency, and a phase detector then aligns the clock edges with the input data edges. The first loop for frequency acquisition is called “coarse loop”, since it helps VCO clock frequency to reach data frequency by bigger steps. The second loop for phase alignment is called “fine loop”, since it shifts the phase of the VCO clock to retime the data with smaller steps. Two loops are necessary because a phase-locked loop alone has a slow and unreliable frequency acquisition range. First, the frequency detector reduces the error in frequency between input data and the VCO. Once the frequency error is sufficiently small, the phase detector takes over and aligns the phase of the clock to match the input data. During this final stage of the operation, the output of the phase-frequency detector is equal to zero, and no longer affects the operation of the circuit.

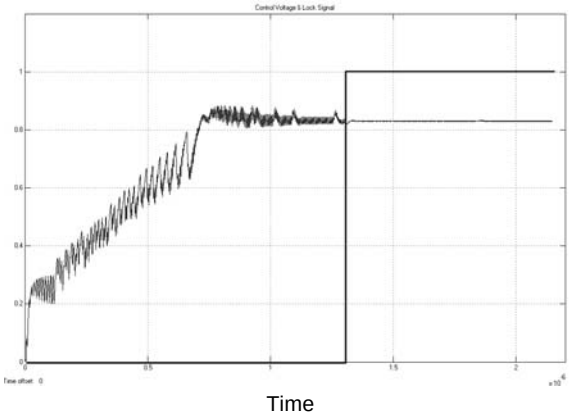

Figure 2: Variation of the control voltage and the lock signal during a typical clock recovery operation.

Figure 2 shows the simulated VCO control voltage variation and the “lock” signal generated by the lock detector. Note that the coarse loop ceases its operation when the lock signal is raised and the fine loop takes over. Since the frequency locking is a coarse process, the control voltage of the VCO is allowed to fluctuate in a very wide range during frequency detection part of the data recovery operation. However, phase locking requires more precise and fine adjustment, thus, the VCO control voltage variation is much more limited during the phase alignment part.

3. CDR Architecture Components

A number of completely novel and innovative circuit blocks have been implemented as key building blocks of the CDR architecture, which will be presented in the following. While the circuit speed in general benefits from the advantages of the 0.13-µm digital CMOS technology, limitations imposed by the technology also represent significant design challenges. In the coarse loop, the phase-frequency detector was designed for operating frequencies between 2.4 GHz / 16 = 150 MHz and 3.2 GHz / 16 = 200 MHz. Since the operation speed is relatively limited, classical logic building blocks were deemed to be sufficient for the construction of the PFD.

A completely symmetric differential charge-pump (see Fig. 3) was designed for the coarse loop. The circuit receives the differential UP and DN signals generated by the PFD, and controls the amount of charge deposited at its capacitive output nodes. An innovative common-mode feedback (CMFB) circuits has also been designed to sense and to correct the differential output of the charge-pump circuit.

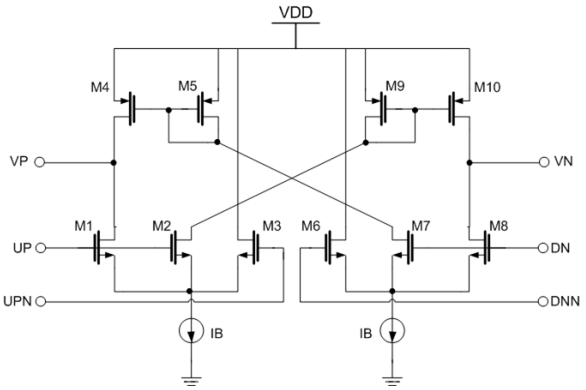

Figure 3: Differential charge-pump circuit used in the coarse loop.

The differential phase detector (PD) in the fine loop section has been realized as a Hogge-type PD (Fig. 4), which is well known in the literature [3]. Since fine loop operates at a frequency range of up to 3.2 GHz, however, special attention must be paid to the transient performance of its components in order to ensure minimum static phase offset. Note that the set-up and hold times as well as the overall delay of the DFF directly influence the fine loop performance. Similarly, the XOR gates must be able to detect phase differences around a few picoseconds.

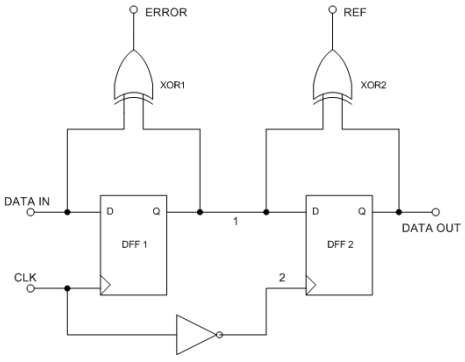

Figure 4: Simplified block diagram of the Hogge-type phase detector (PD).

The circuit diagram of the fully differential master-slave flip-flop used in the Hogge-type PD is shown in Fig. 5. Note that the use of pseudo-nMOS gates allows very high-speed operation while also providing a large output voltage swing. The differential flip-flop consists of two latches, which are connected together to form a master-slave structure. Each latch consists of sense pairs (M3-M6 in the master and M13-M16 in the slave), a regenerative loop (M4-M5 in master and M14-M15 in the slave), two pull up devices, (M1-M2 in master and M11-M12 in slave) and two pairs of clocking switches.

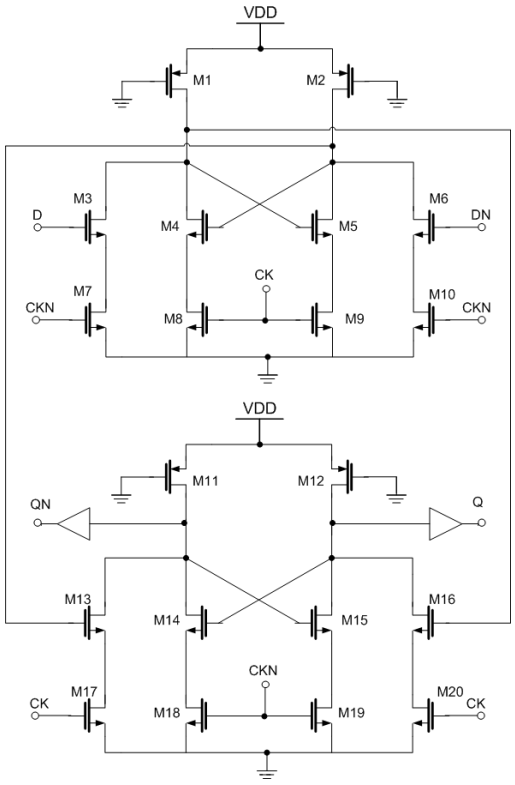

Figure 5: Fully differential master-slave DFF circuit.

When CK is low, transistors M7, M10, M18 and M19 are on and the master stage is in the transparent (hold) mode, while transistors M8, M9, M17 and M20 are off and the slave is in the sense mode. When CK is low, the reverse case occurs. When the master stage is in sense mode, the M3-M6 pair senses the data signal variations. At the same time in the slave part of the circuit, the M14-M15 pair latches the previous value of the data. It is obvious that, since the master is in transparent mode when CK is high, the overall flip-flop circuit operates as a rising edge triggered DFF. Note that the circuit uses no stacked or pass transistors. Also, the gate capacitance of the clock input transistors hardly affects the critical path because these devices are saturated during most of the input voltage swing.

Simulation results show that differential flip-flop has a minimum setup time of 8 ps and a hold time that is almost equal to zero (< 1 ps). With a 3.2 GHz clock, the circuit draws 1.2 mA from 1.2V power supply, which means 1.44 mW of power consumption under typical conditions. The operation of the DFF is shown in Fig. 6, where it is used as the key component of the divide-by-16 circuit, with an input clock frequency of 3.2 GHz.

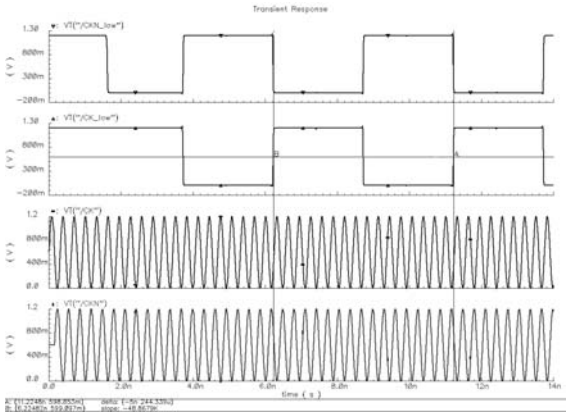

Figure 6: Operation of the divide-by-16 circuit with an input clock frequency of 3.2 GHz.

Matching of the transistors in the fine loop control circuitry has considerable effect on the overall system performance. Thus, special attention has been paid on the layout of the circuit. The dead zone of the circuit, which corresponds to the static phase offset at the output of the CDR, is 12 ps under worst-case conditions at 3.2 Gbps data rate.

The VCO of the system is common for both coarse and fine loops. The VCO has differential control voltages and differential output as the rest of the system blocks. A four-stage ring oscillator architecture has been used in the core of the VCO. The delay-interpolation in the delay stages of the VCO gives a wide linear tuning range opportunity to the overall CDR system [4]. The VCO also uses self-biasing, which completely avoids the need for external biasing such as bandgap circuits.

A digital buffer chain amplifies the VCO output in order to obtain a rail-to-rail clock output and a high drive capability. The supply current of the VCO is 6.21 mA while output amplifier consumes itself 4 mA of the total supply current.

The passive loop filter is also designed as a fully differential circuit. Capacitors of the loop filter have been implemented by using nMOS devices. Resistors of the loop filter have been implemented with unsalicided N-poly layer.

4. Top Level Design Considerations

The top-level layout of the CDR circuit is shown in Fig. 7. Note that the circuit has a very symmetric layout structure, with the VCO, CMFB and the divide-by-16 circuits placed in the center. Coarse-loop and fine-loop controls, as well as the loop filter components are placed on both sides of the symmetry axis. The circuit is

surrounded by large filter capacitors that are used to de-couple the power supply and the ground.

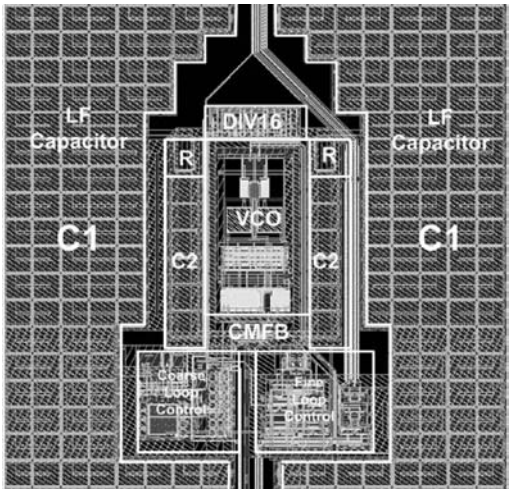

Figure 7: Top-level layout of the CDR circuit.

The clock and data recovery circuit presented here is intended as a key part of a serialization/deserialization (SERDES) macro that can be integrated in any serial link interface chip with large number of channels (> 64).

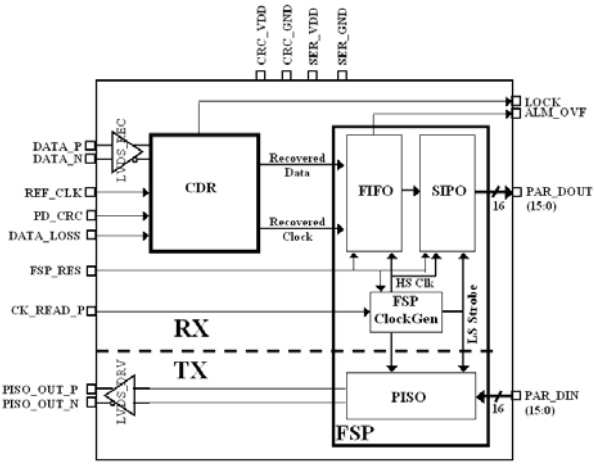

Figure 8: Block diagram of the SERDES macro.

The receiver side of the designed SERDES consists of an integrated PLL-based clock and data recovery block, an elastic memory and a serial-in-parallel-out block. In some applications, the high-speed system clock arrives the chip together with the data. The clock and data recovery block retimes the data with the generated write clock. The transition between the two same-frequency clock domains is accomplished by the elastic memory. The recovered data is synchronized to the read clock (the system clock) after this block. Thus, the entire interface operates synchronously with the high-speed system clock or its low speed derivative. The transmit side involves a parallel-in serial-out (PISO) block to serialize the parallel data coming from the digital core. The block diagram of the SERDES macro is given in Fig. 8.

A typical application for the use of SERDES macro can be a chip where N numbers of channels are employed in parallel (see Fig. 9). It is assumed in such a system that the external high-speed clock (> 2.4GHz) or a synchronous reference low speed clock is transmitted to the chip within the system from the PCB or the backplane. Each receiver channel has a dedicated clock recovery cell, which extracts the clock from the incoming data and aligns this clock in-phase with the data. The recovered data is deserialized with the system clock with a custom FIFO-SIPO circuitry and the low speed parallel data is transmitted to the digital core.

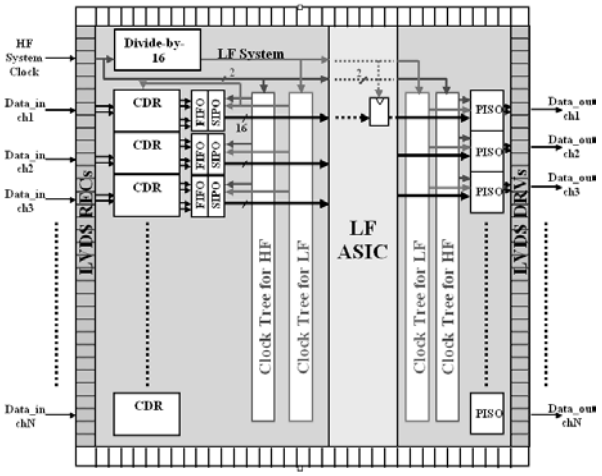

Figure 9: Conceptual block diagram of an N-channel SERDES chip.

5. Conclusions

A versatile and high-performance CDR architecture was realized using conventional 0.13-µm digital CMOS technology. The circuit is capable of operating at sampling frequencies of up to 3.2 GHz, and still can achieve the robust phase alignment. The overall power consumption is estimated as 18.6 mW at 3.2 GHz sampling rate. The overall silicon area of the CDR is approximately 0.3 mm^2 with its internal loop filter capacitors.

References

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