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SILICON RESONANT CAVITY ENHANCED 12X1 PHOTODETECTOR ARRAYS FOR OPTICAL INTERCONNECT RECEIVER INTEGRATION

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High bandwidth short distance communications standards are being developed based on parallel optical interconnect fiber arrays to meet the needs of increasing data rates of inter-chip communication in modern computer architecture. To ensure that this standard becomes an attractive option for computer systems, low cost components must be implemented on both the transmitting and receiving end of the fibers. To meet this low cost requirement all-silicon based receiver circuits are actively being pursued [1], however, manufacturing high speed, high efficiency silicon photodetectors presents a technical challenge.

Resonant cavity enhanced (RCE) photodetectors have been shown to provide the required bandwidth-efficiency product but have remained a challenge to reproduce through commercially available fabrication techniques. We have previously developed a method to produce silicon wafers with high reflectance buried distributed Bragg reflectors (DBR) [2]. The substrates consist of a two-period, 90% reflecting, DBR fabricated using a double silicon-on-insulator (SOI) process. Discrete RCE Si photodetectors have previously been fabricated with 40% quantum efficiency at 860 nm, a FWHM of 25 ps, and a 3dB bandwidth in excess of 10 GHz [3].

In this paper we present Si RCE 12x1 photodetector arrays that have been fabricated and packaged with silicon based amplifiers to demonstrate the feasibility of a low cost monolithic silicon photoreceiver array. The 12x1 photodetector arrays were designed for the PAROLI product line specification by Infineon [4]. The specification calls for 12 photodetectors with between 30 and 80 μm photodetector active area in a linear array on a 250 μm pitch. The fabricated 12x1 photodetector array can be seen in Fig. 1.

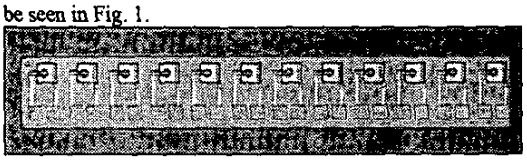

Fig. 1 12x1 photodetector array

The photodetectors consist of vertical Si RCE *p-i-n* photodiodes, a cross section is shown in Fig. 2, fabricated through standard Si processing techniques on double SOI reflecting wafers. The photodetectors have a 42 μm detection area. Several samples were prepared for packaging with Helix HXR2312 3.6 GHz 12 Channel Receiver arrays. The samples were sent to Helix in Zurich, Switzerland and were bonded to the Helix receiver array using 25 μm Gold wire wedge bonding. There were limitations in using this device but it was the only option for this testing. The first and perhaps most important limitation is the mismatch input impedance of the Helix amplifier. The Helix amplifier is designed to have a matched capacitive load of 450 fF, the typical capacitance of Optospeed InGaAs photodetectors which is the standard photodetector used in the optical interconnect standard. Our photodetectors have a 70fF capacitance. One other draw back is that even though the specification mentioned earlier called for 30 to 80 μm diameter photodetectors the testing was done with 50 μm core multi-mode fiber (MMF). This means that the 42 μm photodetector was only capturing 70% of the incident light at best.

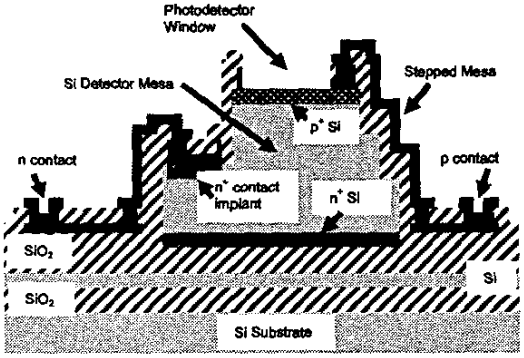

Fig. 2 Cross section schemtaic of Si RCE *p-i-n* photodiode

The photodetectors were tested with the Helix receiver to measure the bit error rate BER and the eye-diagram. The photoreceiver was tested using an HP8664A Synthesized Signal Generator connected to a HP70841B Pattern Generator which was connected to a laser driver and a New Focus Model-1780 850nm 10G Hz Laser Diode, which was coupled to MMF and sent through an EXFO FVA-3100C Variable Attenuator. The output fiber of the Variable Attenuator was butt-coupled with the photodetector by line of sight and by maximizing the received photocurrent. The receiver is then connected to a HP70842B Error Detector to measure BER and a Agilent infinium DCA Wide Bandwidth Oscilloscope with HP54743A TDR Module to measure the eye-diagram. During the test the photodetector is biased at 1.8V reverse bias.

Typically eye diagrams are measured on a photodetector connected to a transimpedance amplifier with a fixed gain. Therefore at higher frequencies a lowering of the output magnitude will occur due to 3dB roll off. The Helix HXR2312 has a rail-to-rail limiting

amplifier built in which means the magnitude of the output is constant for changing input magnitudes. Therefore the usefulness of the eye diagrams is questionable in this study as it can only reasonably measure the lateral eye opening due to diffusing carriers. Figure 3 shows the eye-diagram for the same randomly selected detector in a 12x1 array used in the BER results. The eye shows good opening at 3 GHz and -9.5 dBm optical power. The plot does not show any characteristic signs of long diffusion tails.

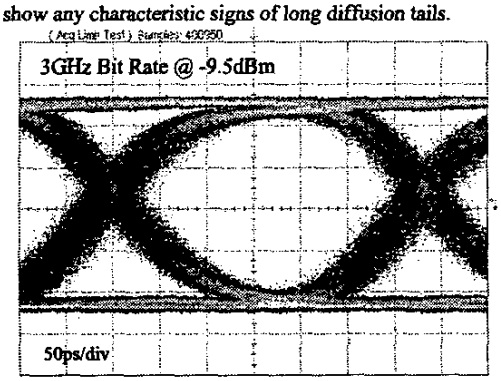

Fig. 3 Eye diagram for single device in 12x1 photodetector array at 3GHz

The HP70841B Pattern Generator was setup to send a PRBS 223-1 sequence to laser diode with a clock frequency of 1 GHz, 1.5 GHz, 2 GHz and 3 GHz on four separate runs. BER was measured using the HP70842B Error Detector which had the same pseudo random bit sequence (PRBS) 223-1 programmed for comparison. The BER was measured as a function of power by controlling the attenuation factor on the calibrated EXFO FVA-3100C Variable Attenuator. Figure 4 shows the measured BER from a randomly selected detector in a 12x1 array. Ideal "error free" transmission is considered to be 1 part in 1 trillion or a BER of 10-12. At 3 GHz the Si RCE photodetector was able to achieve a BER of 10-12 at -6.5 dBm an order of magnitude worse than Optospeed's InGaAs photodetectors which require -16.5 dBm at the same BER. The other thing to note in Fig. 4 is the 5.5 dBm shift in minimum received power for 1 GHz transmission to 3 GHz transmission. The designers at Helix felt that this shift in minimum received power is due to the mismatched load of the receiver on the photodetector caused by the lower capacitance. The other cause of an increase in minimum received power, at all frequencies, is the problem of not collecting all the light from the MMF as well as the reduced responsivity at 850 nm because of misaligned spectral peak.

This work has presented Si RCE *p-i-n* photodetector arrays designed for use in parallel optical interconnect systems. Photodetector arrays were wire bonded with existing Si based receiver circuits to make an all-Si photoreceiver operating at 3 GHz, showing performance that could soon compete with existing compound semiconductor photodetectors for a fraction of the cost. The wafers could also be used to fabricate a host of Si based integrated optoelectronics owing to the availability of Si processing and the availability of large wafer sizes. These wafers are well suited for large scale integration and are compatible with standard CMOS processing making them ideal for fabricating photodetectors monolithically with receiver circuits.

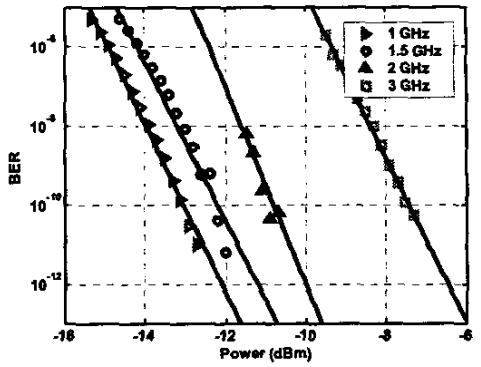

Fig. 4 BER measurment for single device in 12x1 photodetector array

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