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Regular Array of Nanometer-Scale Devices Performing Logic Operations with Fault-Tolerance Capability

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***Abstract* — This paper addresses the functional robustness and fault-tolerance capability of very-deep submicron CMOS and single-electron transistor (SET) circuits. A four-layer circuit architecture is proposed, and a set of guidelines is identified for the design of very high-density digital systems using inherently unreliable and error-prone devices. The proposed architecture is based on the principle of graceful degradation of circuit performance allowing recovery of information, where classical circuits would fail. The integration of the proposed architecture is shown as a regular and compact PLA-style design, allowing the adaptability of the redundancy factor.**

***Index Terms* — Nanotechnology, Semiconductor devices, ULSI, Yield optimization.**

I. Introduction

A very wide array of nano-scale quantum device architectures and related technologies are currently under investigation for future nano-scale computation, such as solid state nanoelectronic devices (RSFQ, RTD, SETs, spin transistor, etc.) and molecular electronics (architectures based on small conductive molecules, carbon nano-tubes and others). Single Electron Transistors (SETs) could be among the most interesting and promising candidates for future nano-electronics because of their particular functionality and complementary characteristics with respect to CMOS.

While the integration of SETs is still under research, it is kwown that these devices may experience permanent or transient failure due to background charge fluctuation, or fabrication failure [4], [5]. To ensure reliable operation and to reduce the sensitivity of SETs to background charge effects (especially at room temperature), the device dimensions must be reduced to sub-nanometer levels, which is not very feasible in the foreseeable future. At the same time, aggressive scaling of MOSFET dimensions to nanometer scale is expected to produce a number of fundamental reliability issues related to irregular dopant distributions, and parameter fluctuations. Thus, the necessity to cope with intrinsic errors at the device and circuit level must be recognized as a key aspect of nanoscale design.

A likely scenario is that the functional blocks be designed with a certain degree of fine-grained, built-in immunity to such permanent and transient faults, such that they are capable of absorbing a number of errors and still be able to perform their functions. This type of pervasive fault tolerance, which is based on the implicit acceptance that a certain percentage of devices in the system will fail in a random fashion, may require a novel approach to robust design that is quite different from classical techniques of fault-tolerance and redundancy.

It is also recognized that the very regular, array-like circuit architectures are likely to be preferred for the realization of Boolean functions using novel nanometer scale technologies (as opposed to standard-cell-like structures), mainly due to their inherent reliability advantages [1], [6], such as predictability and control of inter-device parasitic effects.

In Section 2, we propose an architecture which provides error absorbing capability, and show the circuit realizing the key averaging function. The regularity of nanometer-scale devices is expected to be a fundamental criterion to the construction of reliable devices [1]. The proposed fault-tolerant architecture is adapted to the design of very regular arrays of Boolean function, as shown in Section 3. Finally, the hardware realization of the proposed concepts is shown in Section 4, in the form of a robust PLA matrix.

II. Robust System Architecture

The proposed fault-tolerant architecture consists of four layers in which the data is strictly processed in a feed-forward manner (Fig. 1). The first layer is denoted as the input layer, accepting conventional Boolean (binary) signal levels. The core operation is performed in the second layer, which consists of a number of identical, redundant units implementing the desired logic function. It has been shown that the fault immunity increases with the number of redundant units, yet the operation is quite different from the classical majority-based redundancy [2]-[3]. The third layer receives the outputs of the redundant logic units in the second layer, creating a weighted average with re-scaling. Note that the output of

the third layer becomes a multiple-valued logic level. Finally, the fourth layer is the decision layer where a binary output value is extracted using a simple threshold function.

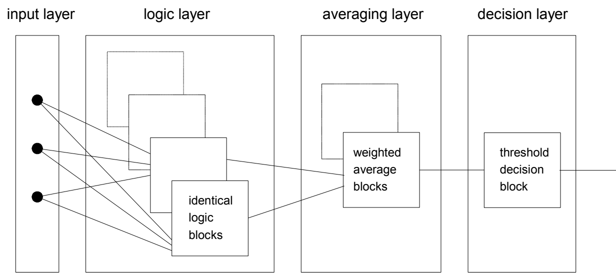

Fig. 1. The proposed fault-tolerant architecture based on multiple logic units and multiple layers for averagin/thresholding.

The averaging function processed in the third layer is a key component of the proposed fault-tolerant architecture. The circuit performing the averaging function has been designed to handle up to four inputs, and it has been developed based on the current mode of operation, as depicted in Fig. 2. The input stage is composed of four PMOS transistors operating either in cut-off or saturation modes. Each transistor gate is driven by the logic voltage level produced in the second layer. The NMOS current mirror replicates the input stage current to the next stage. The averaging function is realized by the voltage drop across the resistor.

It must be noted that the proposed circuit is not expected to operate in continuous analog domain. The main design constraint dictates that the output level be inside of one of four acceptance intervals, resulting from the switching on or off of the PMOS transistors. The magnitude of the acceptance intervals is imposed by the desired noise margin [3].

Also note that the averaging unit described here can be built with regular CMOS devices rather than nanometer-scale devices, since each averaging circuit actually serves a large number of function blocks in the second layer.

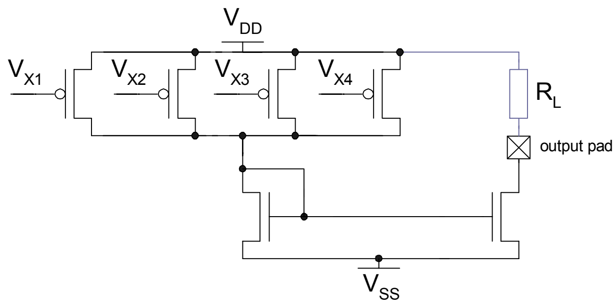

Fig. 2. Averaging unit circuit.

III. Regular Array of Boolean Functions

A regular programmable logic array (PLA) of unit building blocks has been adapted to provide fault-tolerance capability in the second layer using SETs or nanometer CMOS devices. The PLA is used for performing a programmable NOR Boolean operation of its inputs. Fig. 3 shows the structure of the array, made from one unit cell being replicated in the vertical direction to form the logic function as a slice. A number of slices are appended in the horizontal direction and share the same input variables to be connected to the DATA inputs. In our case, the Boolean function input variables can be modified by soft programmation using the PROG input. Dramatic failures modeled as stuck-on or stuck-off errors can also be simulated using the same programming scheme.

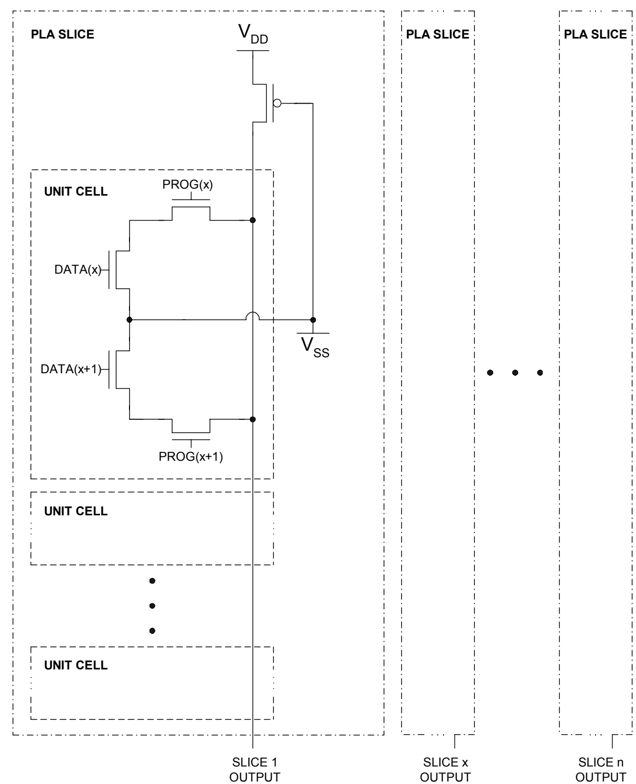

Fig. 3. Regula PLA array structure proposed for the second layer.

In a standard PLA array, every slice outputs a different logic function. However, in order to achieve fault-tolerance, redundancy in the slices is demanded. Applying the concepts presented in Section 2, a number of slices performing an identical Boolean logic function are to be connected to an averaging unit. However, in order to provide soft programmability of the redundancy factor, each output of a slice is connected to two four-inputs

averaging units, according to the scheme depicted in Fig. 4 for a PLA consisting of twelve slices.

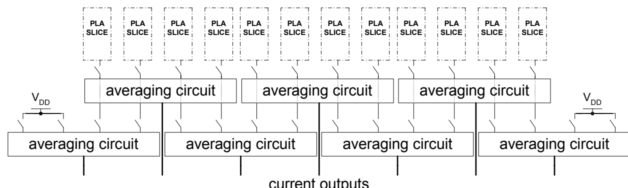

Fig. 4. Connection scheme of the averaging units, showing open switches.

The programmability scheme of the switches granting access to the averaging units allows redundancy factors of two, three or four for each logic function. It has been shown previously that the proposed four-layer architecture has the capability of absorbing errors which occur with a high-density pattern much more efficiently than majority voting shemes usually applied, even with a low redundancy factor, typically two or three [3]. Fig. 5 shows three programmation schemes, where a black dot represents an active switch connecting the PLA slice output to the averaging unit depicted as a dotted box gathering up to four connections. A white dot represents an open switch.

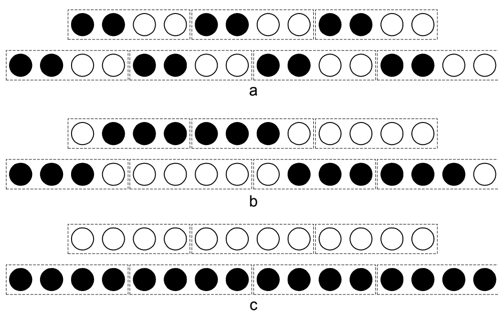

Fig. 5. Programmation pattern for the averaging unit access selectors, related to a PLA Boolean function redundancy factor of a) two, b) three, and c) four.

This arrangement allows a very flexible use of the available PLA area (i.e. number of columns) to adjust the redundancy factor, in order to address different levels of defect densities that are very technology-dependent.

IV. VLSI Implementation

A 8-input variables by 12-slices PLA array including fault-absorbing capability has been integrated in the deep-submicron UMC 0.18 CMOS technology, as a proof-of-concept. The PLA is soft programmable in order to guarantee optimal on-chip testing facility, and has a number of transistor per cell which is twice as much as required to perform expected functionality. Nevertheless, its core size is limited to $45X28um^2$, including the switches selecting the averaging units. The layout of the core PLA is depicted on Fig. 6. The averaging unit has been designed with the capability of driving the signal off-chip; hence the circuit size is not relevant.

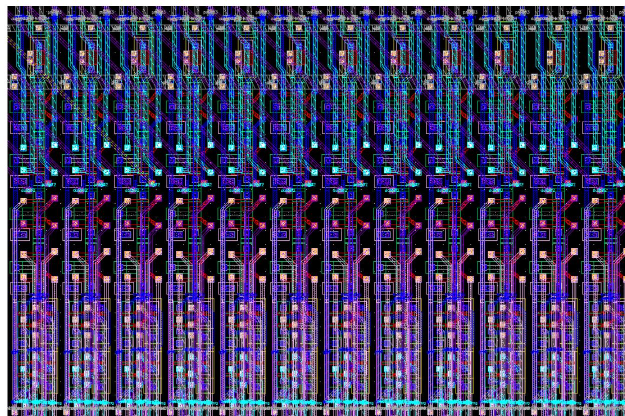

Fig. 6. Layout of the core PLA array.

V. Conclusion

This paper demonstrates the development of a fault-tolerant circuit which is suited to provide robust operation for nanometer CMOS technologies, as well as future SET devices, in the presence of transient and permanent errors. A regular array structure including functional redundancy is proposed to be coupled to an averaging circuit system. The architecture, circuit-level design, layout and reprogrammation schemes are presented. The proposed system offers a very versatile solution to the reduced yield expected to affect future nanometer-scale devices.

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