ELECTRICAL CHARACTERIZATION AND MODELING OF LATERAL DMOS TRANSISTOR – INVESTIGATION OF CAPACITANCE AND HOT CARRIER IMPACT

PRESENTEE AU DEPARTEMENT D'ELECTRICITE

ECOLE POLYTECHNIQUE FEDERAL DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR EN SCIENCES ET TECHNIQUES

PAR

Nasser HEFYENE

LAUSANNE, EPFL

2005

CONTENTS

CHAPTER 1: INTRODUCTION AND MOTIVATION

CHAPTER 2: DMOS TRANSISTOR AND THE INTRINSIC DRAIN VOLTAGE CONCEPT

CHAPTER 3: DRIFT RESISTANCE AND DC MODELING OF DMOS TRANSISTOR

CHAPTER 4: DRIFT RESISTANCE AND AC MODELING OF DMOS TRANSISTOR

CHAPTER 5: HOT CARRIER IMPACT ON THE CAPACITANCE OF DMOS TRANSISTORS AND RELIABILITY ISSUES

ABSTRACT

With the work reported in this manuscript we have essentially contributed to the electrical characterization and modelling of high voltage MOSFETs, more particularly DMOS architectures such as X-DMOS and L-DMOS able to sustain voltages ranging from 30V to 100V. The technology information and the investigated devices have been kindly provided by AMIS, Belgium (former Alcatel Microelectronics).

In general, all the initial defined targets in term of the orientation of our work, as defined in the introduction chapter, have been maintained along the progress of the work. However, sometimes, based on the obtained results we have decided to pay more attention to some less explored topics such as the hot carrier impact of DMOS capacitances and the combined effect of stress and temperature, which initially were not among the planned activities. However, we believe that we have contributed to some of the planned targets.

We experimentally validated the concept of intrinsic drain voltage; a modeling concept dedicated to the modeling of HV MOSFET and demonstrated its usefulness for the DC and AC modelling of HV devices. We proposed an original mathematical yet quasi-empirical formulation for the bias-dependent drift series resistance of DMOS transistor, which is very accurate for modelling all the regimes of operation of the high voltage device. We combined for the first time such a model with EKV low voltage MOSFET model developed at EPFL. We also have reported on models for the capacitances of high voltage devices at two levels: equivalent circuits for small signal operation based on VK-concept and large signal charge-based models. These models capture the main physical charge distribution in the device but they are less adapted for fast circuit simulation.

In the field of device reliability, we have originally contributed to the investigation of hot carrier effects on DC and AC characteristics of DMOS transistors, with key emphasis on the degradation of transistor capacitances and the influence of the temperature. At our knowledge, our work reported in this chapter is among the first reports existing in this field. We have essentially shown that the monitoring of capacitance degradation if mandatory for a deep understanding of the degradation mechanisms and, in conjunction with DC parameter degradation, could offer correct insights for reliability issues. Even more, we have shown situations (by comparing two fundamental types of stresses) when the capacitance degradation method by HC is much more sensitive than DC parameter degradation method. Of course, some of the combined stress-temperature investigations were too complex to find very coherent explications for all the observed effects but our work stress out the interest and significance of such an approach for defining the SOA of high voltage devices, in general.

Overall, our work can be considered as placed at the interface between electrical characterization and modelling of high voltage devices emerging from conventional low voltage CMOS technology, continuing the research tradition in the field established at the Electronics laboratory (LEG) of EPF Lausanne.

RESUME

Ce travail de thèse a été en sa majorité consacré a l'étude des dispositifs Métal Oxyde Silicium à effet de champs pour applications hautes tensions (HV-MOSFET), plus connus sous le nom de transistors DMOS, et dont deux différentes architectures latérales, LDMOS (canal auto aligné) et XDMOS (canal non-aligné), ont été le sujet de ce travail. L'étude fut portée essentiellement sur la caractérisation et la modélisation ainsi que la fiabilité électrique de ces dispositifs, y compris d'un point de vue capacitif, sur la gamme de température 25 – 125°C.

Il est important de souligner que ce travail fut réalisé en étroite collaboration avec l'industrie dans le cadre du projet Européen AUTOMACS et avec comme partenaires principaux AMI Semiconductor, Bosch, Silvaco et IMEC. La totalité des transistors analysés durant ce travail de thèse provenaient d'une technologie CMOS 0.7 μm fournis par le partenaire industriel AMI Semiconductor.

Le premier volet de cette thèse est consacré à l'élaboration du concept de tension de drain intrinsèque permettant la séparation des divers effets et phénomènes physiques intrinsèques a la structure, en particulier la quasi-saturation, entre la régions du canal et du drift de l'architecture DMOS.

La validité de ce concept a des fins de modélisations DC est démontré de façon expérimental à l'aide d'une expression quasi-empirique de la résistance variable du drift capable de modéliser avec grande précision les différent régimes et modes d'opérations du transistor haute tension. Cette expression est pour la première fois combinée avec le model analytique basse tension EKV (développé au sein de l'EPFL) et validé sur silicium, démontrant le potentiel de cette approche pour la modélisation électrique du transistor DMOS. Une partie de l'effort de modélisation est aussi consacré a la modélisation AC ou capacitive des architectures DMOS et cela à travers un modèle petit signaux basé sur un circuit équivalent et un modèle en charge basé sur une estimation géométrique de la charge du drift pour les applications grand signaux.

Le deuxième volet de cette thèse est dédié a la fiabilité des transistors hautes tensions, en termes de dégradations des caractéristiques électriques induites par porteurs chauds. L'accent est mit sur l'impact de la haute température sur la dégradation des capacités extrinsèques du transistor DMOS sujet à deux conditions principales de stress électrique. L'analyse des résultas révèle que la corrélation entre la dégradation des caractéristiques capacitives et DC permettent une meilleure compréhension des divers mécanismes de dégradations ainsi que la localisation de leurs origines à l'intérieur de la structure de façon précise et sans ambiguïté. A notre connaissance, cette analyse est la première du genre dans le domaine de la fiabilité des transistor DMOS et ouvre le débat sur l'importance de considérer l'aspect capacitif du transistor en général dans la définition de la zone de sécurité d'utilité (Safe Operating Area, SOA), en particulier dans les applications hautes fréquences ou l'aspect capacitif est primordial.

CHAPTER 1

Introduction and motivation

1. 1. HIGH-VOLTAGE AND POWER CMOS EVOLUTION

In this section a general overview on the "state-of-art" of high voltage semiconductor devices is presented, based on the most recent available literature. A special interest is dedicated to the High-Voltage Complementary Metal Oxide Semiconductor transistors (HV-CMOS). The investigation starts with a brief introduction on the CMOS evolution in the high voltage (or power) domain followed by a description of the high voltage CMOS transistor types and their actual and expected future applications. Then, a synthesis, based on the performed bibliographic research, concerning the status and trends of power and high voltage (HV) models for circuit simulation is presented. This discussion intends to highlight the interest of the LDMOS modeling activity for the scientific community and identify clear orientations for the proposed work in order to ensure successful results and visibility.

Starting with the huge success found by semiconductor materials, more precisely Silicon, in microelectronic applications in the 60's, passing by the emergence of the first ICs (Integrated Circuits) and up to our days, an important development activity for such circuits was focused upon signal processing applications, given rise to many different types of circuits (analog or digital). All these circuits share one common feature; they are designed to operate at *low-voltage and low-current levels*. In addition, the push to increase the integration density in VLSI (Very Large Scale Integrated) circuits is creating the need to reduce the power supply voltage down to the standard 5 volts. Similarly, the continuous scaling down of the physical dimensions of transistors in order to increase circuit functionality restricts the current handling capability of such devices to less than the milliAmpere. Knowing, that in such IC's (based on bipolar transistors) the power electronics was composed of complex multi-component circuits that required, for proper operating conditions, current input in the Ampere range and thick base regions. Adding to that the appearance of economical constraints with the vast cost reduction needed in information processing applications. All of these led to a dominant cost of the power section and a limited compatibility with the continuous progress of technology and applications.

As an attempt to answer the experienced limitations of bipolar transistors, a new power device technology based on the CMOS technology evolved. The first high-voltage MOSFET's were obtained by redesigning the standard lateral MOSFET in order to improve their blockage capability (i.e. voltage breakdown, V_{BD}). Two structures were developed in parallel: (i) the Vertical Double diffused MOS (VDMOS) and (ii) the Lateral Double diffused MOS (LDMOS) transistors. They are used in isolated and non-isolated configuration depending on the appropriate application (i.e. the non-isolated configuration is used in discrete power devices, while the isolated one is very suitable for implementing the low and the high-voltage device on the same chip). High-Voltage Integrated Circuits (HVIC's) and Power Integrated Circuits (PIC's) are typical representations of these implemented chips. The distinction between them is made at the current and voltage levels. While the PIC's are dedicated to handles currents between 0.5-30A at supplying voltages of 50-500V, the HVIC's are generally designed to operate at low currents (up to 0.1A) and high voltage (up to 1000V) [1]. It is important to note that the term "High-Voltage" is a relative notion, since the standard voltages used for IC's, in our days, may vary around few Volts; for example, with the improvements in sub-micron technology, nominal voltages tend to values of 1-2.5V [2]. Therefore any voltage supply rated to a higher value (e.g. 5V) is considered as a high voltage environment for these sub-micron devices.

The introduction of power MOSFET's was originally regarded as a major threat to power bipolar transistors. In our days power MOSFET's spread over a wide range of currents and voltage rating applications. For those applications requiring high current and voltage ranges, such as motor control and factory automation systems, discrete devices combined with high voltage ICs are used.

For applications necessitating either high voltage operation at low current levels (e.g., electrostatic, ink-jet printers and plasma display) or high current level at low voltage (e.g., linear and switching regulators, ac-motors controls, automotive control circuits and ballast for fluorescent lights) can be served by HVIC's and PIC's respectively. With the technological advances and the continuous performance improvement of the high-voltage MOSFET, applications in automobile and aircraft industries as well as telecommunication systems have found their way and became of great motivations to improve the high-voltage field. Fig. 1.1 presents the voltage and current handling needs for various applications.

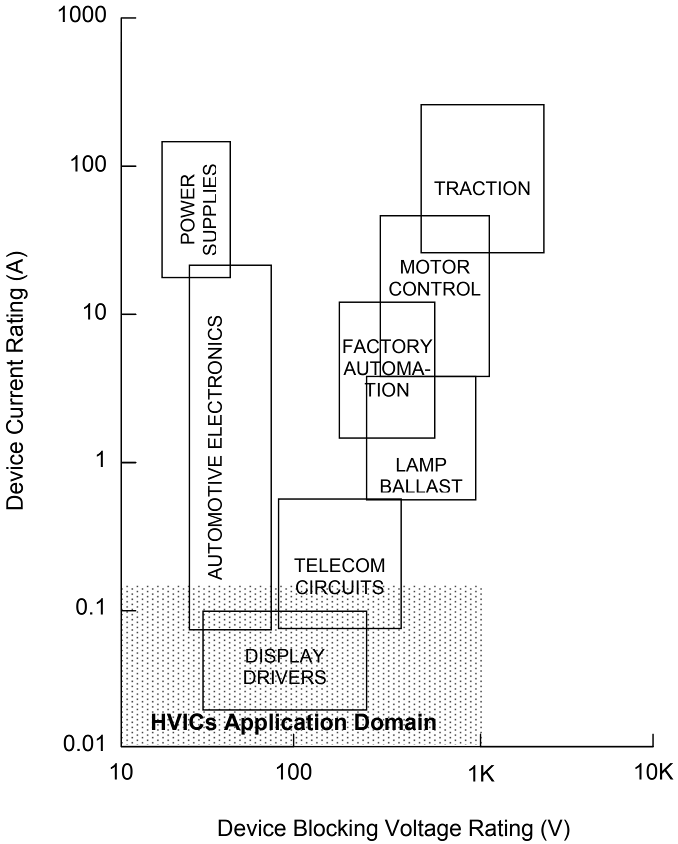


Fig.1. Illustration of power and high-voltage MOSFET applications in term of current and voltage ratings (after [1]).

1. 2. HIGH-VOLTAGE AND POWER MOSFET MODELING OVERVIEW

In the following a brief critical synthesis, based on a bibliographic research, concerning the status and trends of high voltage (HV) and power models for circuit simulation is presented. This discussion intends to highlight the interest of the HV-DMOS modeling activity for the scientific community and identify clear orientations for the modeling task, part on this PhD work, in order to ensure successful results and visibility. In recent years, research on HV and power semiconductor device models for circuit simulation has been intensified as a result of higher demands on improved efficiency and reliability in the design and realization of specific integrated circuits. Several research groups through the world have elaborated new concepts for trimming the basic physical equations to the requirements of HV/power device models for circuit simulations [3]. The challenges for such models result from: (I) *high quantitative accuracy in DC and AC regimes*, (II) *fast computation capability* and (III) *physical and easy accessible model parameters*. The LDMOS modeling activity is focused to formulate at least a favourable trade-off between these potentially contradicting requirements. Some of the traditional simulation and design standard tools for power/HV were based on simplified semiconductor models, which are below the nowadays state-of-the-art in the design of integrated circuits. Moreover, the required device models improvements are now fully justified by the introduction by main industrial companies of new products with new functionalities, in order to compete on the international market. Note that specialized software vendors (e.g. Anacad, Mentor, Meta-Sofware, Micro-Sim, Silvaco, ISE, etc.) have already reacted to support simulation and design for HV and/or power electronic circuits.

From a physical point of view, modeling a physical component or a device can allows a better comprehension and control of the different phenomena encountered as well as it help to distinguish the more coherent explanations in order to clarify these phenomena. It is important to note that such models make possible the characterization of a wide range of devices through the extraction of their main electrical and technological parameters. In the other hand, the availability of simple and compact models permits the elaboration of powerful software tools that can simulate the functionality and efficiency of single devices, like transistors, or even a whole complex circuit. Also, they are very helpful to predict the impact of technology on the device performance. For the microelectronic industry (manufacturers and circuit designers) such features are very attractive since they present an effective cost-time reduction way to promote a continuous evolution of technologies and product performances.

The most advanced HV and power device models with the best accuracy are incorporated in simulation programs which enable an easy insertion of model equations (like Saber and Eldo), but despite that such programs are very powerful, they keep generally very expensive. However, the standard simulation program with the widest distribution is SPICE, since it is relatively inexpensive and can be run on common PC's.

Power device models are represented by subcircuits and thus, the incorporation of new models might require complex subcircuits and much more computation time (i.e., less efficient). An attempt to implement in SPICE simulator power models combined with mathematical functions derived from device physics (to provide very compact models and to guaranty a better accuracy) was proposed in [4]. Good matching with experimental results based on power diodes and IGBT's measures was presented. It should be noted that most of the models implemented in SPICE (e.g., BSIM3) were originally elaborated and dedicated to model standard components like MOSFET's rated to voltages and currents much lower than those assigned to power and HV MOSFET's and with different architectures and doping profiles. Therefore, major modifications taking into consideration the specificity of power MOSFET's should be introduced to these models to provide a better efficiency and accuracy of the simulator (a revised version of BSIM3 was released for such purposes).

The Lateral Double-diffused MOS or LDMOS transistor has attracted the attention of industry in the last ten years due to its very promising potential in term of performances and process compatibility with the actual planar Low Voltage technology in an attractive cost-effective way. In our day its applications cover a wide range, varying from simple DC-DC converters to ink-jet printers, plasma display, automotive and AC-motors control circuits passing by switching regulators and fluorescent lights ballast. With the technological advances and the continuous performance improvement of such devices, applications in automobile and aircraft industries as well as telecommunication systems found their way to it in the very near future. What was considered as promising applications in the near past for LDMOS devices applications like Radio-Frequency (or High-Frequency) IC's (RFIC's), Intelligent Power/HV IC's for automotive applications (e.g. power switches battery protection) became in now-a-days standard [5] [6].

LDMOS models exist in multiple versions: (i) analytical (or mathematical) formulations, (ii) subcircuits (macro-models) and (iii) mixed forms. *None of these is nowadays an industrial standard*. Some reasons for this are detailed in the following.

1. 2. 1. ***Models based on various levels of SPICE:*** Mixtures of MOSFET SPICE models complemented by JFETs and diodes have been used in order to model and simulate the LDMOS behaviour. Generally, these models use simplified structures (excessive simplicity in representing the drift region) and thermal considerations are not taken into account. They are used especially for fast matching on a specific device structure and related simplified parameter extraction. For example, a level-3 MOSFET model (complemented by a JFET and a diode) can provide less than 10% error on ID, gm-VG static characteristics and less than 12% error on power (or gain) transfer characteristics [7]. S-parameter measurements are also relatively well matched. The model accuracy is mirrored also by the evaluation error related to some key parameters: <3% for g_{max}, <5% for R_{ON}, <5% for C_{iss} and C_{oss} and ~15% error on C_{rss} [8]. However, such low numbers in terms of relative error correspond to *rms* error and to small or medium applied voltages; key phenomena at high voltage and power are never correctly captured by such models.

1. 2. 2. ***BSIM3V3 approach:*** Nowadays, BSIM3v3 is a recognized industrial standard with high modeling capabilities. It suffers essentially from the high number of parameters (most of them non-physical). It is important to note that the BSIM model basis has been founded at the University of California at Berkeley as low voltage MOSFET model. Today its extension to high voltage can be considered as relatively artificial and especially based on a series model of the drift region, resulting in an overall model with a very high number of parameters and questionable convergence.

1. 2. 3. ***Empirical models***: The characteristic of such models is that model equations are not entirely obtained by rigorous derivations from device physics [9], but, in part, by a selection of appropriate mathematical expressions [10]. A widely known LDMOS empirical model is Motorola's thermal model (MET) tailored for RF applications. The merit of this model is to include thermal effects in basic equations. The mathematical empirical functions guarantee very good continuity and matching in both DC (<10% relative error on I_D, gm -V_G) and AC regimes (S-parameters), from 25°C up to 75°C [11], [12]. The main drawback comes from the related high specificity, limited voltage/power range and lack of physical meaning of fitting parameters. MET model has been implemented in LIBRA and ADS harmonic balance simulators [13].

1. 2. 4. ***Lumped-charge models***: The Lumped-Charge Methodology (LCM), originally proposed by Linvill, is a systematic way to accurately represent device behavior using simple equations taking a minimum time to be solved. Lauritzen and Subramanian adapted for the first time this method to DMOS devices: the LDMOS is imagined to be made of two regions: the body MOS structure and the drain MOS structure. LC models for each of these are then developed [14] [15]. The authors compared performances obtained by their approach to BSIM2 model. It appears that this approach is very promising but the model does not account for: (I) thermal effects and self-heating, (II) parasitic bipolar (this is under construction) and (II) gradual channel doping. DC characteristics at room temperature are simulated with accuracy better than 5% as well as the AC behavior [7], [12]. It is clear that this class of models has an interesting potential for our purpose if improved. Its non-implementation in modern simulators is mainly motivated by lack of parasitic and temperature effects, correlated with a need of iterative calculations for some model equations (complex to be done in SPICE, but possible in SABER [16]).

1. 2. 5. *Parameters for DMOS modelling*

It was revealed that the huge number of parameters associated with BSIM3v3-like models prohibits their efficient adaptation for LDMOS transistor modeling. Therefore, setting-up a minimal basis of significant parameters for LDMOS and XDMOS modeling should be a mandatory target of any new model development. Moreover, in the ideal case, each parameter should have a certain physical significance and enable to study the effect of a particular process, geometry or physical phenomenon influence. Unfortunately, in practice this is usually impossible and many fitting parameters are used to describe effects that cannot be naturally captured in equations or, very commonly, the transitions between different regions of operation of the HV device.

1. 2. 6. *Criteria for model evaluation*

An important point for an overall comparison of different DMOS models, in general, is to define a common and clear model evaluation basis of merit criteria. Some of the proposed criteria used in this work are the following:

a) ***accuracy*** of predicted DC and AC characteristics at device level;
b) ***computation speed and convergence*** to achieve comparable results;
c) ***simplicity of parameter extraction*** using measured data;
d) ***limitation*** in utilization for various applications;
e) ***potential for further development*** (essentially scalability and extensions to other types of devices).

While criterion a) is essentially quantitative (measured in terms of different types of errors between experiment and simulations), all the others involve particular discussion and many associated trade-off's. For instance, even for criterion b) the targets can be completely different at single device level or if the device should be then simulated in a circuit environment. Criterion c) involves a robust procedure for parameter extraction and not very time consuming experiments. Criterion d) is more qualitative and less restrictive since even a single application could largely motivate the development of a good device model. Particularly interesting is criterion e) that is about the re-usability of developed models and their potential to be scaled for the next generation of high voltage models. For instance, models build on physical basis, with technological and physical parameters are answering in much part to the scalability and protability issues.

1. 3. CONCLUSION AND MOTIVATION FOR THIS WORK

The short review and discussion proposed in the previous parts of this chapter have been aimed to place our work in the context of the general advance and trends in the modelling of HV devices and, particularly, DMOS transistors. It is worth to mention that our work has been carried out as a collaborative effort between EPFL and AMIS Microelectronics, Belgium (presently AMIS) in order to establish new compact models for the X-DMOS and L-DMOS device technology of the industrial partner. Moreover, this work was part of the European research IST project AUTOMACS that brought together Alcatel Microelectronics, EPFL, Bosch, IMEC and Silvaco to address the challenges of modern HV devices and circuits. It should be then not surprising that our resulting approach is not purely academic (focused exclusively on device physics and its pure analytical modelling) but also includes some pragmatic approaches like quasi-empirical modelling of drift series resistances and the associated calibration of the parameters.

In addition, the results presented here are complementary to the PhD thesis elaborated at EPFL by my colleague Costin Anghel, which dedicated much of the focus to the development of a DC compact model (based on BSIM low voltage model and a full analytical drift model) and thermal (self-heating) effects in HV MOSFETs. Our work is addressing as main original points the **investigation of the DMOS capacitances** and the **hot carrier degradation** (including the effect of the temperature). We are also significantly contributing to the DC modelling by proposing pragmatic modelling approaches based on a simplified version of EKV model and an empirical mathematical expression of the bias-dependent drift series resistance.

In this context, the content of this manuscript is organised as in the following.

- **Chapter 1**: This chapter is proposing an **introduction and motivation for the work**.
- **Chapter 2**: The **concept of intrinsic drain voltage (or K-point)** and its use for the DC and AC modelling of HV devices, including also detailed numerical simulations and analysis of the operation DC regimes of X- and L-DMOSFETs, are detailed.
- **Chapter 3**: **DC modelling based on EKV** and **quasi-empirical model** (using adapted mathematical functions) **of the drift region resistance of DMOS transistors** are the main topics addressed in this part of the work.
- **Chapter 4**: This chapter shows **how the intrinsic drain voltage concept can be used for the modelling of the DMOS capacitances**; small signal and large signal approaches are separately addressed.
- **Chapter 5**: This chapter deals with **hot carrier effects on DC and AC characteristics of DMOS transistors**, with great emphasis on the **degradation of transistor capacitances and the influence of the temperature**. At our knowledge, our experimental work in this field reported in this chapter is among the first existing reports in the field. Moreover, the conclusions on the most significant stress conditions and the importance of capacitance degradation are, for the first time, demonstrating the acuteness of this point for HV device reliability, in general.

A final conclusion, stressing the contributions and the perspectives offered by this work is proposed at the end of the manuscript.

REFERENCES

[1] “*High Voltage Integrated Circuits*”, edited by B. J. Baliga, 1988, IEEE Press.

[3/2] “*High Voltage Devices and Circuits in Standard CMOS Technologies*”, edited by M. Declercq and H. Ballan, Kluwer Academic Publishers, Boston, 1998.

[3] R. Kraus and H. J. Mattausch, “*Status and Trends of Power Semiconductor Device Models for Circuit Simulation*”, IEEE Transaction on Electron Devices, 1998, Vol. 13, No. 3, pp. 452-465.

[4] R. Kraus, P. turkes and J. Sigg, “*Physical-based models of power semiconductor devices for the circuit simulator SPICE*”, PESC’98, vol. 2, pp. 1726-1731.

[5] K. Sakamoto, Y. Nunogawa, K. Satonaka, T. Kouda and S. Horiuchi, “*An Intelligent IC with Reverse Battery Protection for Fast-Switching High-Side Solenoid Drive*”, IEEE Transaction on Electron Devices, 1999, Vol. 46, No. 8, pp. 1775-1781.

[6] K. Sakamoto, N. Fuchigami, K. Takagawa and S. Ohtaka, “*A Three-Terminal Power MOSFET with Built-In Reverse Battery Protection for Automotive Applications*”, IEEE Transaction on Electron Devices, 1999, Vol. 46, No. 11, pp. 2228-2234.

[7] P. Perugupalli, M. Trivedi, K. Shnai and S. K. Leong, “*Modeling and characterization of an 80V silicon LDMOSFET for emerging RFIC applications*”, IEEE Transaction on Electron Devices, Vol. 45, No. 7, pp. 1468-1478, July 1998.

[8] M. Travedi, P. Khandelwal and K. Shenai, “*Performance modeling of RF power MOSFET’s*”, IEEE Transaction on Electron Devices, 1999, Vol. 46, No. 8, pp. 1794-1802.

[9] A. E. Schlogl, T. T. Mnatsakanov, H. Kuhn and D. Schroder, “*Temperature dependent characterization of silicon power semiconductors –a new physical model validating by device-internal probing between 400K and 100K*”, PESC’98, vol. 2, pp. 1720-1725.

[10] N. G. H. van Melick and F. V. Rijs, “*Optimization of a Lateral DMOS transistor for low voltage, RF power operation*”, ESSDERC’97, vol. 1, pp. 176-179.

[11] M. Miller, T. Dinh and E. Shumate, “*A new Empirical Large Signal Model for Silicon RF LDMOS FETs*”, Wireless Application Digest, 1997. IEEE MTT-S Symposium on Technologies for, pp. 19-22.

[12] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang and E. E. Shumate, “*A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF LDMOS FETs*”, Microwave Symposium Digest, 1999 IEEE MTT-S International, Vol. 2, pp. 419-422.

[13] “Motorola Electro-thermal (MET) LDMOS model”, available on the Motorola web site: http://mot-sps.com/models/ldmos/ldmosmodels.html.

[14]. C. L. Ma, P. O. Lauritzen, Pao-Yi Lin and I. Budihardjo, “*A systematic approach to modeling of power semiconductor devices based on charge control principles*”, PESC’94 record, vol. 1, pp. 31-37, 1994.

[15]. Y. Subramaniam, P. O. Lauritzen and K. R. Green, "*A compact model for an IC Lateral Diffused MOSFET using the lumped-charge methodology*", MSM'99.
Available also at the University of Washington web site:
http://www.ee.washington.edu/research/pemodels/modtext/ldmos.html

[16]. Y. Subramaniam, P. O. Lauritzen and K. R. Green, "*Two Lumped-Charge Based MOSFET Models*", Computer in Power Electronics, 1998. 6th Workshop on, pp. 1-10.

CHAPTER 2

DMOS Transistor and the Intrinsic Drain Voltage Concept

2. 1. HIGH-VOLTAGE DMOS ARCHITECTURES

Two main Lateral HV-MOSFET architectures issued from the I2T technology - 0.7µm CMOS process - of AMI Semiconductors (former Alcatel Microelectronics) are investigated in our work: the Lateral double-Diffused (LDMOS) and the eXtended-Drain MOS (XDMOS) transistors. Each of the architecture provides up to 100V breakdown capability has the features described in the next sections.

2. 1. 1. LDMOS transistor architecture:

The LDMOS investigated device is an n-channel HV transistor with short channel and self-aligned architecture. It has the particularity of a (lateral) gradually doped channel. The cross section of the LDMOS device is reported in Fig. 2.1.a.

1. 1. 2. XDMOS transistor architecture:

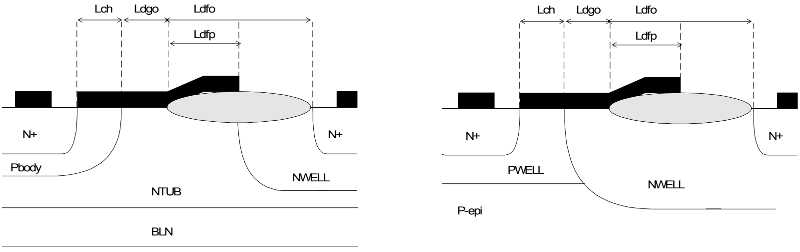
The XDMOS investigated device is an n-channel HV transistor with long channel and non-self aligned architecture. It has a uniformed doped channel, in contrast with the LDMOS device. The cross section of the XDMOS device is reported in Fig. 2.1.b.

Figs. 2.1 (a and b) show the investigated LDMOS and XDMOS architectures with the different regions and most relevant lateral dimension symbols, adopted in the proposed modeling strategy, and which stands for:

- L_{ch} for channel length;
- L_{dgo} for drift gate oxide length;
- L_{dfo} for drift field oxide length;
- L_{dfp} for drift field plate length;

The oxide thickness of both devices is 43nm.

Tables 2.1 and 2.2 present respectively the device dimensions and the various doping level per region for the investigated LDMOS and XDMOS architectures.



(a) *(a)*

Figs. 2.1. Schematic illustrations (cross sections) of the investigated n-channel (a) LDMOS and (b) XDMOS architectures.

Layout parameter	Definition	TCAD structure	
		LDMOS	XDMOS
L_{ch}	Channel length	0.8 μm	4 μm
L_{dgo}	Drift-length beneath gate oxide	1.2 μm	~ 0 μm
L_{dfo}	Drift-length beneath field oxide	2..2 μm	2.1 μm
L_{dfp}	Drift-length beneath field-plate	3.6 μm	3 μm
t_{ox}	Gate oxide thickness	43 nm	17 nm
W	Channel width	40 ÷ 250 μm	40 ÷ 250 μm

Table 2.1. Device geometry according to TCAD 2D-simulated n-channel LDMOS and n-channel XDMOS.

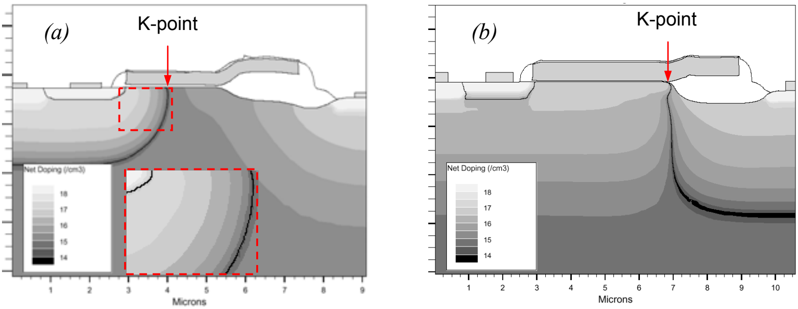
Region	TCAD structure doping level (cm^{-3})	
	LDMOS	XDMOS
p-body	$\sim 7\times10^{17} \div \sim(4\text{-}5)\times10^{15}$	
p-well		$\sim 7\times10^{16}$
n-tub	$\sim(2\text{-}4)\times10^{15}$	$\sim 10^{16}$
n-well	$\sim(3\text{-}4)\times10^{16}$	$\sim 6\times10^{14}$
p-body	$\sim(2\text{-}3)\times10^{15}$	
p-epi		$\sim 3\times10^{16} \div \sim 7\times10^{14}$
n-buried layer (BLN)	$\sim 4\times10^{18}$	

Table 2.2. Device doping levels according to TCAD 2D-simulated n-channel LDMOS and n-channel XDMOS.

2. 2. NUMERICALLY SIMULATED HIGH-VOLTAGE DMOS ARCHITECTURES

In order to model the different DMOS architectures, it is essential to first understand the inside device physics of each architecture and well identify and analyse different aspects related to HV-MOSFET's in general (e.g. carrier concentrations, electrical field, depletion extension, etc.) or specific effects and phenomena related to DMOS architectures like *quasi-saturation* and *drift pinch-off*. This is achieved through two-dimensional numerical simulations (known also as TCAD simulation) where it became in our days a standard evaluation and development tool for the micro-electronic field. Figs. 2.2 (a and b) illustrate the numerically simulated HV-DMOS structures where intrinsic channel doping profiles of both structures, gradual for the LDMOS (see Fig. 2.2.a, inset zoom) and uniform for XDMOS, can be clearly observed. In the same figures, we show the location of the intrinsic drain voltage (end of the intrinsic MOSFET channel or metallurgical junction), concept that will be introduced in the next section of this chapter.

It is worth to note that numerical simulated structures have been calibrated on real device (obtained by technological step-by-step simulations and calibrated on real parameterized cross sections) in order to fit as close as possible real device electrical characteristics and its different biases related phenomena and effects. For example the lateral doping profile of the LDMOS intrinsic channel has been calibrated on real device doping profile extracted with the SIMS technique (see Fig. 2.3).



Figs. 2.2. Illustrations of the 2D numerical simulation of the investigated n-channel (a) LDMOS and (b) XDMOS architectures. Inset is shown the location of the intrinsic drain of the transistor (metallurgical junction) called K-point.

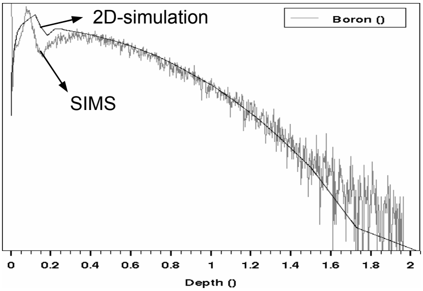
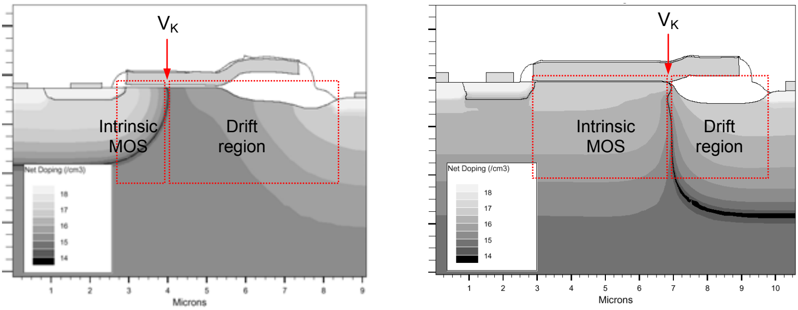


Fig. 2.3. Lateral doping profiles of n-channel LDMOS architecture with Boron: SIMS and numerically simulated profiles.

2. 3. INTRINSIC-DRAIN VOLTAGE (V_K) CONCEPT

The intrinsic-drain voltage, V_K, denotes the K-point potential, which corresponds to the surface potential of the physical metallurgical junction between the *p-body/n-tub* regions for LDMOS and *p-well/n-well* regions for XDMOS architectures illustrated in Figs. 2.2 and 2.4 (red arrows) and this is equivalent to drain voltage in standard low-voltage MOSFET transistors.

Lateral DMOS transistors have in common with standard MOSFET's the intrinsic channel-region and therefore the idea of considering the intrinsic channel of the HV-DMOS structure as a standard low voltage MOS in series with a drift region appeared an interesting approach for DMOS modeling purposes. The main advantage of such approach is the use of different available MOSFET models to describe the intrinsic channel-part and focussing the major effort on the drift-region modeling and its related specific phenomena like quasi-saturation. Accordingly, both DMOS structures have been divided into two main regions: intrinsic-MOS and drift-region as illustrated in Figs. 2.4 (a and b). As it can be seen, the K-point delimits the boundary between both regions, which explains its key-position the interest in its different electrical characteristics.



(a) *(b)*

Figs. 2.4. Illustration of (a) LDMOS and (b) XDMOS transistor division: intrinsic-MOS and drift-regions. Inset: location of the intrinsic-drain (K-point) potential.

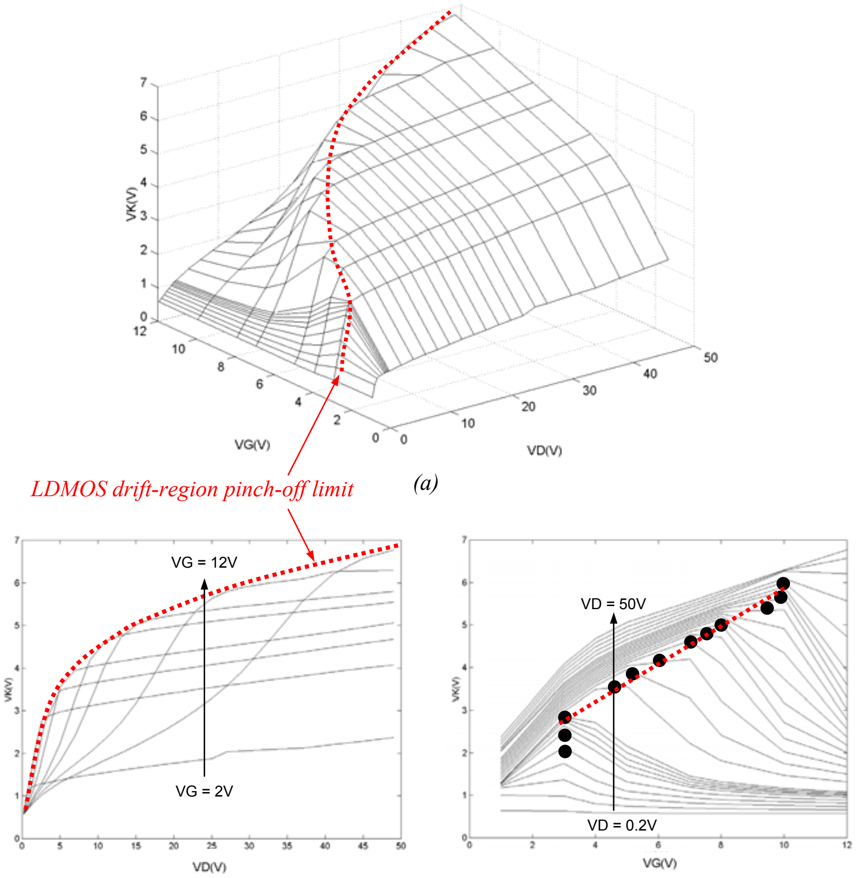
The next step is the detailed analysis of the intrinsic channel-region to verify the validity of the intrinsic MOS approach. Extracted K-point potential from numerically simulated LDMOS and XDMOS architectures indicates low V_K values with respect to V_D and V_G bias variations. In other words, *K-point remains at low potential despite the elevated gate and drain biases*. Extracted K-point potential (V_K) and other related electrical characteristics are presented and separately analysed for LDMOS and XDMOS architectures in the coming sections.

2. 3. 1. V_K potential in DMOS Architectures

Extracted K-point potential, V_K, for LDMOS structure when biased up to V_G = 12V indicates V_K values near 5V for V_D = 20V and up to around 7V for V_D = 50V (see Figs. 2.5), while for XDMOS structure when biased under equivalents V_G (12V) and V_D (20V) biases, V_K values remains as low as 3.5V (see Figs. 2.6). This confirms that the intrinsic channel can be considered as a standard low-voltage MOS with the K-point as its intrinsic-drain terminal.

From the analysis of 3D and 2D dependences of the V_K potential with the gate and drain biases in Figs. 2.5 and 2.6, two main observations are made:

(i) *V_K potential increase with V_D bias*: this is explained for a given V_G by the role played by the drift-region essentially designed to sustain the elevated applied voltages on the drain during normal device working conditions. The major part of the drain potential drops across the entire drift-region, while a limited part drops along the channel; therefore, increasing the applied V_D will naturally gives rise to an increase in potential drops in each parts, i.e. drift and channel regions. This is demonstrated in Fig. 2.5.b with a 50V applied on the LDMOS drain: 43V drops within drift-region and only 7V across the intrinsic-channel.

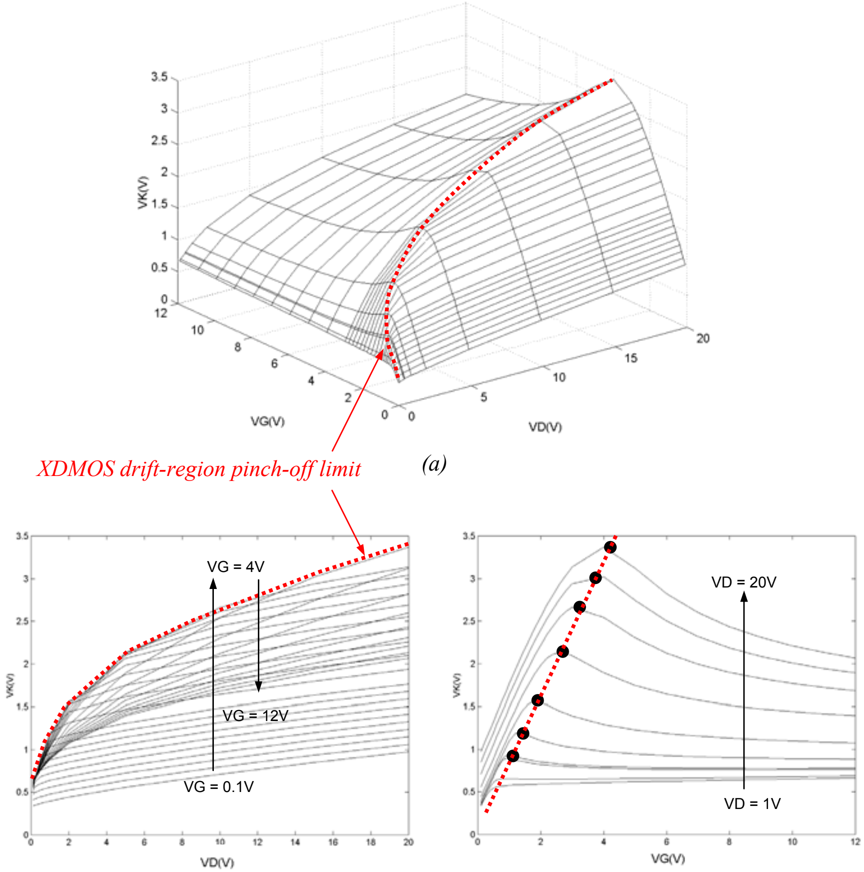


(a)

(b)

(c)

Figs. 2.5. LDMOS extracted K-point potential, V_K, variations with extrinsic biases: (a) V_K (V_G, V_D), (b) V_K (V_D) and (c) V_K (V_G).



(a)

(b)

(c)

Figs. 2.6. XDMOS extracted K-point potential, V_K, variations with extrinsic biases: (a) V_K (V_G, V_D), (b) V_K (V_D) and (c) V_K (V_G).

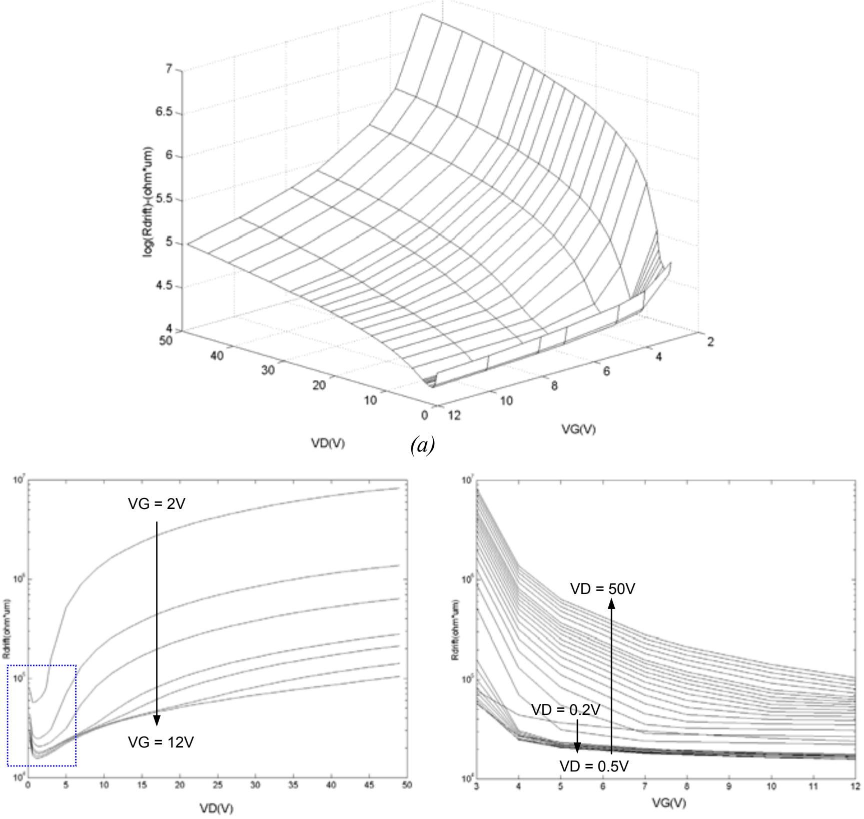
(ii) *V_K potential increase then decrease with V_G bias*: this unusual V_K dependence is observed for both architectures, where V_K is found to increase with V_G and then decreases after reaching a maximum as it can be seen from Figs. 2.5.c and 2.6.c. This is essentially due to the drift-region beneath the thin gate oxide when biased toward accumulation. In order to explain this unusual behaviour, let first consider the case of very low V_D bias (i.e. 0.1-0.2V); a depleted zone is already formed around the p-body/n-well (or n-tube) junction and tends to extend as V_D rises. As explained before most of the applied drain voltage drops across the depleted zone to reach only few volts at the intrinsic-channel end (or K-point). With increasing V_G towards positive biases the drift-region beneath the gate oxide to silicon interface turns from *depletion to electron accumulation*; the complete formation of the accumulated electron channel

corresponds to the peak value in V_K-V_G characteristics (solid circles, Figs. 2.5.c and 2.6.c). Therefore the V_K peak values with respect to V_G and V_D denoted by the doted red lines in Figs. 2.5 and 2.6 can be considered as the *depletion pinch-off limit in drift-region* (i.e. the bias limit at which the drift-region is entirely depleted).

2. 3. 2. Drift-Resistance vs. DMOS Architectures

As most of the drain potential drops across the drift-region (demonstrating, in fact, the effectiveness of the structures to sustain high voltages), it is very interesting to monitor the drift-resistance dependence on applied biases, as calculated from the extracted K-point potential (V_K) according to the following expression:

$$R_D \cong R_{drfit} = \frac{V_D - V_K(V_D, V_G)}{I_D} \tag{2.1}$$

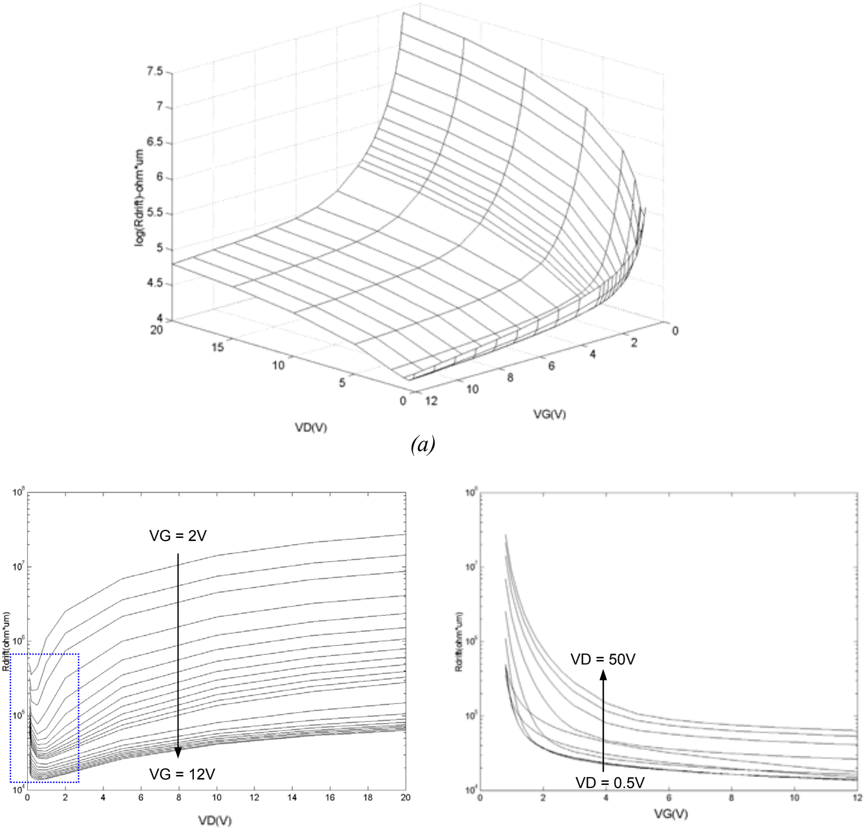


(a)

(b) (c)

Figs. 2.7. LDMOS extracted drift-resistance, R_{drift}, variations with extrinsic biases: (a) R_{drift} (V_G, V_D), (b) R_{drift} (V_D) and (c) R_{drift} (V_G).

Extracted R_{drift} characteristics for both LDMOS and XDMOS structures are illustrated in Figs. 2.7 and 2.8, respectively. The first obvious remark is the very similar drift-resistance characteristics despite their different channel and drift architectures. For low gate voltages (however larger than the threshold voltage, V_T), as V_D increases the depletion zone extends within the drift-region to reach the pinch-off limit and causing very important rises in R_{drift} over two decades. When V_G goes to higher values, drift accumulation beneath the gate oxide and electron-channel formation becomes more favourable and limits the depletion extension; consequently the drift-resistance rises in a less pronounced way as it can be seen from Figs. 2.7.b and 2.8.b. However when V_D is reduced toward linear region (i.e. <0.5V) an interesting simulation result is depicted; *a minimum followed by a resistance increase, more accentuated for high* V_G *appears* (Figs. 2.7.b and 2.8.b, doted boxes), a direct impact of the drift accumulation channel formation within the drift-region [1].



(a)

(b) *(c)*

Figs. 2.8. XDMOS extracted drift-resistance, R_{drift}, variations with extrinsic biases: (a) R_{drift} (V_G, V_D), (b) R_{drift} (V_D) and (c) R_{drift} (V_G).

The drift-resistance dependence with gate voltage is presented in Figs. 2.7.c and 2.8.c. As expected, with V_G rises a drift accumulation channel of electrons takes place; as a consequence R_{drift} drops rapidly till the channel is completely formed, then this drop becomes less sharp. This is observed at gate voltages in the range of ~4-5V for LDMOS and of ~2-4V for XDMOS architecture.

2. 3. 3. Saturation Mechanisms in DMOS Architectures

In this section a brief description of the different saturation mechanisms suspected to take place within DMOS transistors are presented. The most probable mechanisms are:

(i) ***Channel pinch-off mechanism***: it is more susceptible to occur in standard MOS transistors with long-channel features where the pinch-off of the inverted channel takes place at the drain side when $V_D \geq V_G - V_T$ (under forward bias conditions). According to the intrinsic-drain concept [2, 3], which considers the HV intrinsic-channel as a standard MOS transistor, this mechanism is more probable for long-channel DMOS architecture (i.e. XDMOS device with $L_{ch} \sim 4\mu m$).

(ii) ***Drift-depletion pinch-off mechanism***: this is specific to HV-DMOS transistors and related to the extension of the p-well/n-well (tube) depletion (similar to the JFET pinch-off mechanism) and the channel accumulation formation within the drift-region (see § 2.3.1). The bias dependence of this mechanism is strongly related to drift-region architecture (i.e. doping level and dimensions).

(iii) ***Carrier velocity saturation mechanism***: this mechanism is more probable in standard MOSFET's featuring short dimensions and elevated doping levels of the channel where both factors enhance the maximum local field. When at some point of the channel the critical field E_C is reached ($\sim 3\times10^4$ V/cm for n-channel device [4]) flowing electrons across the channel travel at a constant velocity ($v_s \sim 8\times10^6$ cm/s for electrons [4]). The investigated double-diffused LDMOS structure an intrinsic-channel relatively short ($L_{ch} \sim 0.8\mu m$) and which reveals a gradual doping profile with a $\sim 7\times10^{17}$ cm^{-3} peak value near the source side ($\sim 6\times10^{16}$ cm^{-3} for XDMOS channel). Due to the important potential drop across drift depleted regions in HV DMOS, high field conditions could appears and therefore velocity saturation of transient carriers could happen.

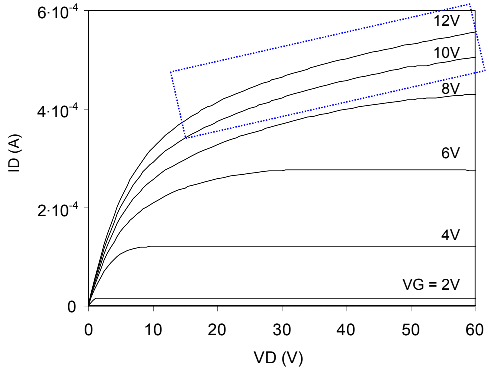


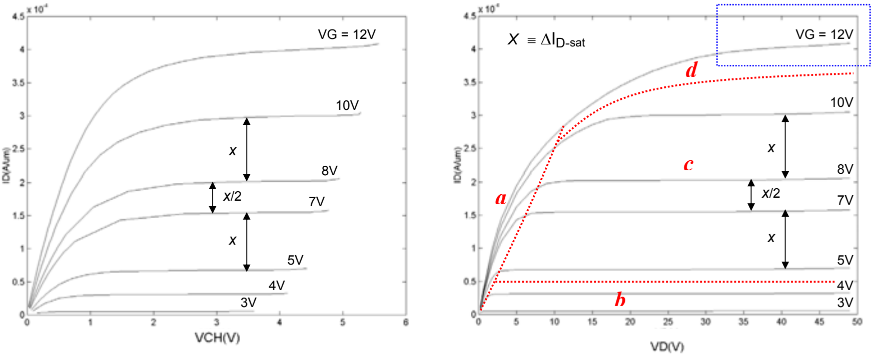
Fig. 2.9. n-channel XDMOS measured output characteristics at various gate biases (2, 4, 6, 8, 10 and 12V).

(iv) ***Quasi-saturation mechanism:*** this is unique for HV-DMOS structures and one the most discussed hot-topics. It is described as a limitation in the current level that can be reached within the device [5]. Despite the intensive reported efforts to investigate this particular phenomenon [6-9, 8-14, 17-20] there is no unique consensus about the origins and causes of the quasi-saturation. However there is a common agreement that the intrinsic MOS transistor remains in linear/quasi-linear mode of operation [5], which could explain the linear evolution of drain current with drain bias during; typical signature of quasi-saturation depicted from XDMOS output characteristics (see Fig. 2.9, doted box). Two major causes have been advanced as the origin of the phenomenon: carrier-velocity saturation in the drift [6, 7] and drift-depletion formation through which the current transits [8, 19, 20]. The investigated XDMOS and LDMOS architectures suggest the carrier-velocity saturation as the most plausible since quasi-saturation is observed only at high gate biases and where no depletion in the drift-region is depicted (see Figs. 2.11.b and 2.13.b, most of the drift-region is neutral)

2. 3. 4. Drain Current in DMOS Architectures

Another interesting feature, which can be explain by using the values of the intrinsic drain voltage, V_K, concerns the output characteristics. The analysis of the both intrinsic and extrinsic device output characteristics are very useful to identify the saturation mechanisms, for any type of device architecture and bias conditions.

(i) ***LDMOS Architecture:*** As it can be seen from Fig. 2.10.b extrinsic DMOS characteristics saturate with V_D at the early stage which indicates probable channel saturation. Extracted intrinsic MOS current characteristics (Fig. 2.10.a) confirm this where all curves show an early saturation too with V_K (intrinsic-drain potential).



(a) *(b)*

Figs. 2.10. Simulated n-channel LDMOS output characteristics at various gate biases for (a) intrinsic MOS transistor and (b) extrinsic DMOS transistor.

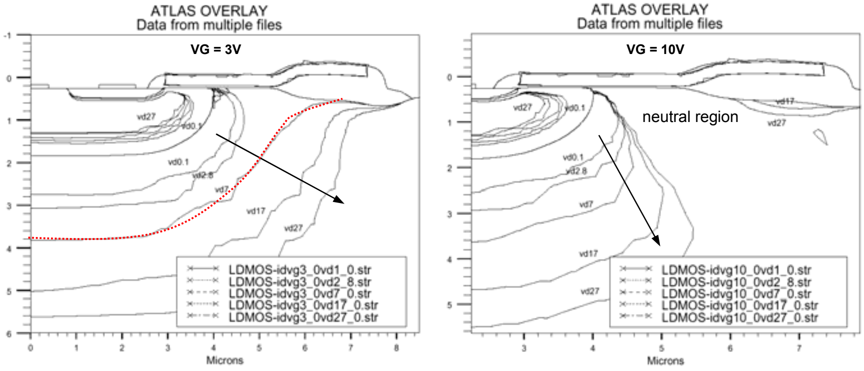
The only exception is for extrinsic I_D curve at $V_G = 12V$; it shows with V_D a continuous rise where a linear-like region starting at V_D ~30-35V and up to 50V is clearly depicted (see Fig.2.10.b, doted box). According to Figs. 2.10, it can be concluded for LDMOS architecture the following region separation:

Region (a): within this region the DMOS transistor is in linear regime.

Region (b): $V_T \leq V_G < 5V$: for gate biases near V_T the drift-region beneath the gate oxide is completely depleted at relatively low V_D bias; drift pinch-off is reached for $V_G = 3V$ and $V_D = 7V$ (see Fig. 2.11.a, doted line), while no intrinsic-channel pinch-off is depicted, therefore the saturation mechanism is drift pinch-off [5].

Region (c): $5V \leq V_G < 12V$: for moderate gate biases saturation takes place within the intrinsic MOS and carrier-velocity saturation mechanism prevails where the equal distance between saturated current lines when V_G is raised linearly is the signature of such saturation mechanism; Figs. 2.10 shows equal ΔI_{Dsat} when V_G rises from 5-to-7V and 8-to-10V) [5]. Also, the high peak in the channel doping profile is synonym of high peak in local electrical field, i.e. an enhancing factor toward carrier-velocity saturation mechanism.

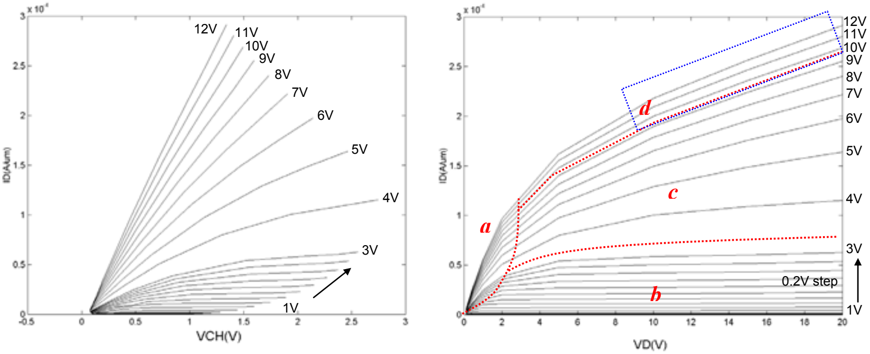
Region (d): $12V \leq V_G$: for high gate bias depletion extension within the drift is very limited and the intrinsic MOS transistor is in linear regime, therefore the most probable saturation mechanism is quasi-saturation mechanism (i.e. carrier velocity saturation within the drift-region).



(a) *(b)*

Figs. 2.11. LDMOS drift-depletion extension for several V_D biases (0.1 – 27V) at (a) $V_G = 3V$ and (b) $V_G = 10V$

(ii) ***XDMOS Architecture:*** Starting with low gate bias, extrinsic DMOS characteristics appear almost flat around $V_D \sim 5V$ (see Fig. 2.12.b) indicating a probable intrinsic-channel saturation. As V_G increases the tendency changes and current lines do not flatten any more but keep rising with V_D and progressively the increase becomes almost linear; this is for high gate biases (i.e. $V_G > 9V$). This is confirmed by the intrinsic MOS characteristic (Fig. 2.10.a), which tend to saturate at low V_G bias (up to 3V) and exhibits a perfect linearity at high V_G (12V).



(a) *(b)*

Figs. 2.12. Simulated n-channel XDMOS output characteristics at various gate biases for (a) intrinsic MOS transistor and (b) extrinsic DMOS transistor.

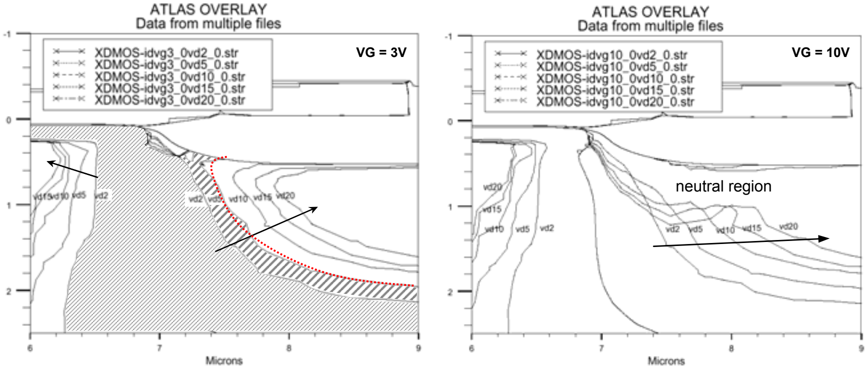
Therefore, region separation for XDMOS architecture can be concluded as following:

Region (a): within this region the DMOS transistor is in linear regime.

Region (b): $V_T \leq V_G \leq 3V$: for gate biases near V_T the drift-region depletes at relatively low V_D bias; pinch-off is reached for $V_G = 3V$ at $V_D = 5V$ (see Fig. 2.13.a) and as V_D rises drift-depletion keeps extending beneath the LOCOS. While no intrinsic-channel pinch-off is depicted, the most probable saturation mechanism is drift pinch-off [5].

Region (c): $3V < V_G < 10V$: for intermediate gate biases intrinsic current lines tend to progressively increase with V_D (see Fig. 2.12.a, $V_G = 4 \div 9V$), which indicates a saturation-to-linear regime transition of the intrinsic MOS transistor, as well a neutral drift-region appears for $V_G > 4V$ indicating drift pinch-off suppression.

Region (d): $10V \leq V_G$: for high gate bias depletion extension within the drift is very limited and a clear neutral channel can be depicted from Fig. 2.13.b. The intrinsic MOS transistor is in linear regime and DMOS output characteristics show a sharp linear current increase with V_D (see Fig. 2.12.b, doted box); typical signature of quasi-saturation mechanism.



(a) *(b)*

Figs. 2.13. XDMOS drift-depletion extension for several V_D biases (0.1 – 27V) at (a) $V_G = 3V$ and (b) $V_G = 10V$.

2. 4. CONCLUSION

Two different Lateral HV MOS architectures have been investigated: LDMOS and XDMOS transistors, which respectively stand for *lateral double-diffused* and *extended-drift* MOS architectures, both designed and fabricated by AMI Semiconductor. The careful analysis of the numerically simulated equivalent structures (TCAD) revealed that **the intrinsic drain voltage concept (or V_K) offers a very good basis of investigation for the most significant characteristics and phenomena related to HV-DMOS device physics**. We have also demonstrated the validity of considering the intrinsic-channel DMOS as a standard low voltage MOS transistor where the K-point (V_K) represents its drain terminal.

Two saturation mechanisms proper to HV-DMOS transistors are identified: **drift pinch-off** and **quasi-saturation** and a physical understanding of their origins and causes has been reported; for both HV device architectures **carrier velocity saturation is demonstrated as the most probable explanation for the quasi-saturation phenomenon**. The intrinsic output current has allowed identifying the various saturation mechanisms involved for each architecture, as well as determining the physical location of saturation (the intrinsic- channel region or the drift-region).

Moreover, the monitoring of **V_K-potential permits the access of some unique device characteristics like the intrinsic MOS output current and the drift-resistance**. Extracted drift-resistance has shown for both structures a strong bias-dependence (up to 4 decades), which demonstrates the great importance of developing an accurate DMOS model for the drift region resistance, aspect that is detailed in the next chapter.

REFERENCES

[1] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, "*An Experimental Approach for Bias-Dependent Drain Series Resistances Evaluation in Asymmetric HV MOSFETs,*" European Solid-State Device Research Conference (ESSDERC) 2001, pp. 403-406.

[2] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier, Y. Mourier, "*Investigation and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage,*" European Solid-State Device Research Conference (ESSDERC) 2001, pp.399 - 402.

[3] C. Anghel, N. Hefyene, A.M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier and Y. Mourier, "*Physical Modelling Strategy for (Quasi-) Saturation Effects in Lateral DMOS Transistor Based on the Concept of Intrinsic Drain Voltage,*" International Semiconductor Conference (CAS), 2001, pp. 417 - 420.

[4] Y. Tsivids, "*Operation and Modeling of the MOS Transistor*", McGraw-Hill, Second edition 1999, pp. 281.

[5] C. Anghel, "*High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling*", Ph.D. Thesis No. 3116, Swiss Federal Institute of Technology, Lausanne (EPFL), Lausanne 2004.

[6] M.N. Darwish, "*Study of the Quasi-Saturation Effect in VDMOS Transistors*" IEEE Transaction on Electron Devices, 1996, Vol. ED-33, No. 11, pp.1710 - 1716.

[7] J. Evans, G. Amaratunga, **"***The Behavior of Very High Current Density Power MOSFETs***",** IEEE Transaction on Electron Devices, 1997, Vol. 44, No. 7, pp.1148 - 1153, 1997.

[8] J. Rebollo, E. Figueras, J. Millán, E. Lora-Tamayo, F. Serra-Mestres, "*Analysis of the Quasi-Saturation Region of High Voltage VDMOS Devices*", Solid-State Electronics, 1987, Vol. 30, No. 2, pp. 177-180.

[9] E. Caquot, G. Guegan, M. Gamboa, H. Tranduc, P. Rossel, "*Phénomène de <<quasisaturation>> dans les transistors MOS*", Revue de Physique Appliquée, Vol. 15, 1980, pp. 1445 - 1450.

[10] U. Apel, H.G. Graf, C. Harendt, B. Hofflinger, T. Ifstrom, "*A 100-V lateral DMOS transistor with a 0.3-micrometer channel in a 1-micrometer silicon-film-on-insulator-on-silicon*", IEEE Transaction on Electron Devices, 1991, Vol. 38, No. 7, pp. 1655 – 1659.

[11] J. Paredes, S. Hidalgo, F. Berta, J. Fernandez, J. Rebollo, J. Millan, "*A steady-state VDMOS transistor model*", IEEE Transaction on Electron Devices, 1992, Vol. 39, No. 3, pp. 712 - 719.

[12] K.H. Lou, C.M. Liu, J.B. Kuo, "*An analytical quasi-saturation model for vertical DMOS power transistors*", IEEE Transaction on Electron Devices, 1993, Vol. 40, No. 3, pp. 676 - 679.

[13] C.-M. Liu, K.-H. Lou, J.B. Kuo, “*77 K versus 300 K operation: the quasi-saturation behaviour of a DMOS device and its fully analytical model*”, IEEE Transaction on Electron Devices, 1993, Vol. 40, No. 9, pp. 1636 – 1644.

[14] C.M. Liu, J.B. Kuo, Y.P. Wu, “*An analytical quasi-saturation model considering heat flow for a DMOS device*”, IEEE Transaction on Electron Devices, 1994, Vol. 41, No. 6, pp. 952 - 958.

[15] J. Zeng, P.A. Mawby, M.S. Towers, K. Board, “*Modelling of the quasi-saturation behaviour in the high-voltage MOSFET with vertical trench gate*”, IEE Circuits, Devices and Systems, 1996, Vol. 143, No. 1, pp. 28 - 32.

[16] A. Bleik, J. Guerin, M.K. El Cheikh, “*Le Transistor VDMOS en Régime de Quasi-saturation: Etude Analytique et Modélisation*”, J. Phys. III France, 1997, Vol. 7, pp. 1851 - 1868.

[17] Chung-Mon Liu, J.B. Kuo, “*Quasi-saturation capacitance behavior of a DMOS device*”, IEEE Transaction on Electron Devices, 1997, Vol. 44, No. 7, pp. 1117 - 1123.

[18] P. Rossel, H. Tranduc, G. Charitat, “*Power MOS devices: Structure evolutions and modelling approaches*”, Microelectronics Reliability, Vol. 37, No. 9, pp. 1375 – 1388, 1997.

[19] T. Myono, E. Nishibe, K. Iwatsu, S. Kikuchi, T. Suzuki, Y. Sasaki, K. Itoh, H. Kobayashi, “*Modelling technique for high-voltage MOS devices with BSIM3v3*”, Electronics Letters, 1998, Vol. 34, No. 18, pp. 1790 - 1791.

[20] E.C. Griffith, J.A. Power, S.C. Kelly, P. Elebert, S. Whiston, D. Bain, M. O'Neill, “*Characterization and modeling of LDMOS transistors on a 0.6 /spl mu/m CMOS technology*”, International Conference on Microelectronic Test Structures, (ICMTS), 2000, pp. 175 - 180.

CHAPTER 3

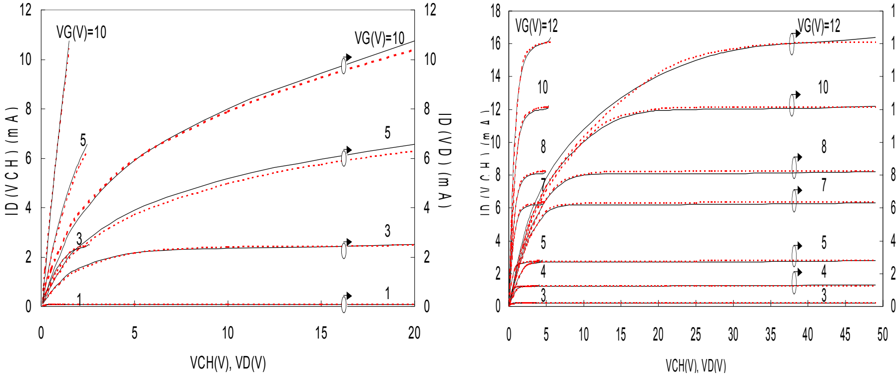
Drift resistance and DC modelling of DMOS transistor

3. 1. INTRINSIC-MOS REGION MODELING

As it was demonstrated in the previous chapter, the K-point potential of both X- and L-DMOS architectures remains at relatively low values when extrinsic drain terminals of both structure is biased to elevated voltages (see § 2.3). Accordingly the idea of considering the intrinsic channel region of both HV-structures equivalent to a standard low-voltage MOS transistor appeared to be an interesting approach for HV-DMOS modeling. This allows first the use of the various MOSFET models available on the market to describe the intrinsic channel-region and second concentrating the effort on modeling of the drift-region and its related specific characteristics and phenomena. Such approach is defined as the intrinsic-drain or VK-concept [1]. Based on this concept, a unified modeling strategy, for both architectures, has been elaborated and which consists essentially of dividing the global device into two main blocks: *Intrinsic MOSFET* block and *drift-region* block where each one is modeled separately and then together combined to form a macro model.

In this chapter, the modeling the drift-region as a *bias-dependent drift-resistor* is proposed and two different approaches are presented. The feasibility of each is then discussed in detail and their validity for HV-DMOS modeling purposes through the V_K-concept is reported.

The intrinsic MOS block is modeled using the standard low-voltage MOSFET model BSIM, more precisely; the BSIM3v3 version, which is implemented in the Smart-spice circuit simulator from Silvaco used for the purpose of this work. The model has been calibrated on the extracted intrinsic MOS output characteristics of both HV structures respectively illustrated in Figs. 2.10.a and 2.12.a. This calibration should be considered only as a good approximation since model parameters have been tuned only on output (I_D-V_K) curves (i.e. for precise model calibration, complementary tuning of model parameters on transfer characteristics is needed). Figs. 3.1 (a and b) show the good matching between modeled curves (solid lines) and intrinsic characteristics (doted lines) extracted from TCAD structures.



(a) *(b)*

Figs. 3.1. BSIM3v3 Output current (solid line) fitted on extracted intrinsic-channel I_D-V_K characteristics from TCAD data (doted lines) at various gate biases for n-channel (a) XMOS transistor and (b) LDMOS transistor.

3. 2. DMOS DRIFT-REGION MODELING

For the modeling of the drift region as a bias-dependent resistor, $R_{drift}(V_D,V_G)$, two quasi-empirical approaches have been privileged: (i) an experimentally based approach and (ii) a mathematical (however, quasi-empirical) approach. Next sections present the results obtained using these two selected possibilities.

3. 2. 1. Experimental Based Modeling Approach

The proper analytical modeling of HV-DMOS transistors requires adapted characterization of series resistances, with particular interest on the extended drain series resistance due to its bias-dependent on gate and drain biases. Special efforts have been dedicated [1-3] to develop and adapt methods for R_D or (R_D-R_S) evaluation dedicated at the origin to low-voltage MOSFET's. These works agree on the fact that the accuracy of a drain series extraction method is substantially increased as far as the technique is independent on the particular $R_D(V_D,V_G)$ relationship and requires a minimum assumption criteria. In this approach, the elaborated technique has the advantage to be independent of the extended drift region architecture and thus, can be used for any asymmetric HV-DMOS's. However, only the LDMOS architecture has been used to validate this methodology. The proposed extraction technique consists in two main successive steps:

Step-1 $\Rightarrow$ Extraction of the drain resistance at low drain voltage with gate voltage as a parameter, R_{D0}, using direct and reversed configurations measurements at constant current [12, 3]

Step-2 $\Rightarrow$ Evaluation of the series resistance derivative as a function of the drain voltage, dR_D/dV_D, followed by its integration [4]

Finally, the drain series resistance is evaluated as the sum of step (i) and (ii):

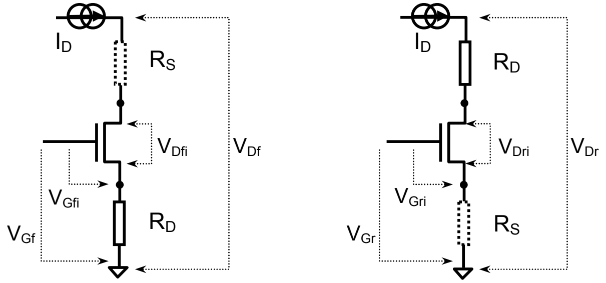
$$R_D(V_D,V_G) = R_{D0}(\sim 0,V_G) + \int_0^{V_D} \frac{\partial R_D}{\partial V_D} dV_D \qquad (31)$$

Each step is described in detail in the up-coming paragraphs:

***(i) Inter-changed drain-source measurement at constant current*:** Asymmetric source and drain series resistances, R_S and R_D, are expected to differently impact the related gate and drain de-bias if the extrinsic transistor is measured successively in forward (i.e. normal) and reversed (source and drain interchanged) configurations as illustrated in Figs. 3.2 (a and b). In order to efficiently exploit this idea [2, 3], an identical constant drain current is injected in forward and reversed configuration while recording the V_{Df} and V_{Dr} drain voltages as functions of V_{Gf} and V_{Gr}, respectively (superscripts '*f*' and '*r*' apply for forward and reverse terms respectively). The current level is kept low in order to ensure operation in the linear regime and ensure an identical R_D value in both configurations, in contrast to [4]. As a consequence, supposing $R_S << R_D$ (valid assumption for extended-drain MOS architectures), the drain series resistance is then calculated based on the difference between the gate voltages which ensure in forward and reverse modes identical extrinsic drain voltages, $V_{Df} = V_{Dr}$, with the DMOS transistor in quasi-linear operation.

As a consequence, supposing $R_S << R_D$ (valid assumption for extended-drain MOS architectures), the drain series resistance is then calculated based on the difference between the gate voltages which ensure in forward and reverse modes identical extrinsic drain voltages, $V_{Df} = V_{Dr}$, with the DMOS transistor in quasi-linear operation:

$$R_D \cong R_D - R_S = \frac{V_{Gr} - V_{Gf}}{I_D\left(1 + \frac{dV_T}{dV_{Sub}}\right)} \tag{3.2}$$



(a) *(a)*

Figs. 3.2. Schematic illustration of the experimental setup measurements dedicated to R_{D0} extraction: (a) forward and (b) reversed source and drain bias configuration.

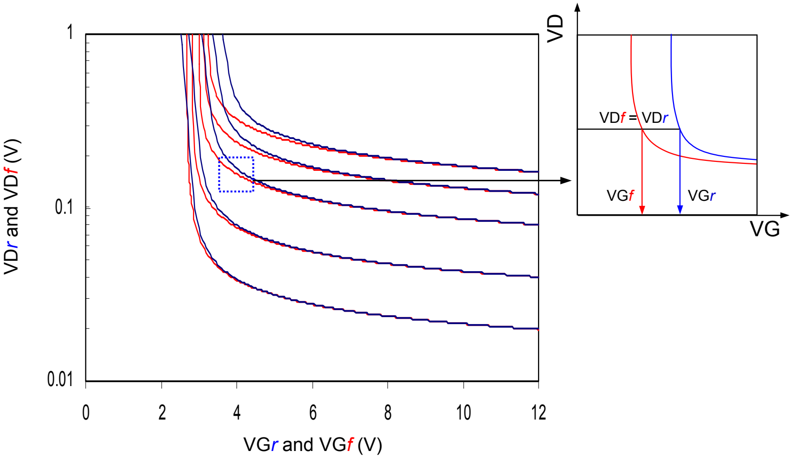


Fig. 3.3. Experimental dependence, V_{Df} and V_{Dr} versus V_G at constant injected I_D currents in n-channel LDMOS transistor.

Typical measurements on the n-channel LDMOS device and the extraction procedure are illustrated in Fig. 3.3. Based on this measurement, the low-voltage drain, R_{D0}, series resistances is plotted as a function of $V_G = V_{Gf}$, at constant current (see Fig. 3.4). For $V_G < 4V$, the drain series resistance decreases with V_G, independently on the current levels because of the reduction of the controlled drift-depleted region in the LDMOS device. Same comments apply for current levels > 250μA. An experimental R_{D0} increase for $V_G > 5V$ is observed with this method for $100\mu A < I_D < 250\mu A$ (see Fig. 3.4). This interesting effect can be explained by the onset of an accumulation channel in the drift region under the thin oxide. The effect of this accumulation layer is the increase of the effective MOS channel length, L_{eff}, which, at constant current, involves the increase of the extrinsic V_D (and an equivalent higher series resistance). Therefore, to correctly extract R_{D0}, the level of the injected current has to be carefully set.

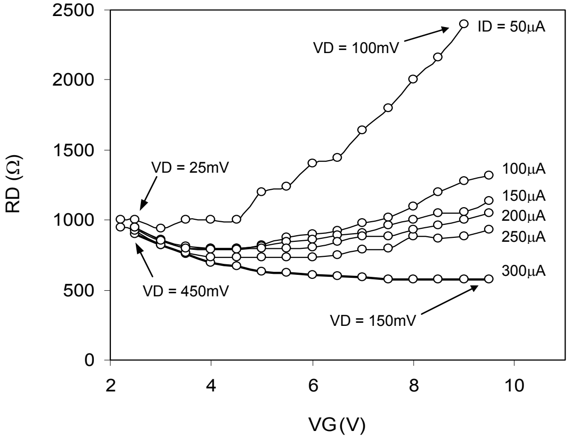


Fig. 3.4. Drain series resistance, R_D, values versus V_G extracted at various low current biases in n-channel LDMOS transistor.

As it can be observed from Table 3.1, experimental R_{D0} values extracted at $I_D = 100\mu A$ (equivalent to V_D ~50 ÷ 70mV) are in good agreement with numerically simulated data over the V_G range: 4 ÷ 7V extracted from LDMOS TCAD structure.

R_{D0} (Ω)	V_G (V)			
	4	5	6	7
Measured Simulated	~550 ~660	~500 ~530	~470 ~400	~450 ~340

Table. 3.1. Experimentally extracted and simulated R_{d0} values at various V_G biases.

***(ii) Experimental evaluation of drain series resistance derivative dR_D/dV_D*:** Generally, in case of MOS transistors with bias-dependent series resistances, it has been shown that a more complex modeling of the extrinsic conductances, g_d, g_b and g_m, as functions of the intrinsic ones, and including source and drain series resistance derivatives (with respect to the gate and drain voltages) must be used for accurate modeling. For the proposed extraction procedure, it is proposed to artificially re-construct the quantitative derivative dR_D/dV_D, by the use of a variable resistor in the drain of the LDMOS transistor.
With the extrinsic (measured) output conductance given by [1]:

$$g_d^{-1} = \frac{1+g_{di}\left(R_D+R_{Dadd}\right)+\left(g_{mi}+g_{bi}\right)\cdot R_S}{g_{di}\left(1-\dfrac{\partial I_D}{\partial V_D}\right)} \tag{3.3}$$

where, superscript '*i*' applies for the intrinsic transistor (see Fig. 3.1), it follows that the slope of dg_d^{-1}/dR_{Dadd} versus R_{Dadd} plot can be used for the dR_D/dV_D extraction according to:

$$\frac{dR_D}{dV_D} = \frac{1-\partial g_d^{-1}/\partial R_{Dadd}}{I_D} \tag{3.4}$$

Note that the usefulness of this type of extraction is expected to be somewhat limited in the saturation region of the intrinsic MOS transistor, when the drain current becomes practically independent of the drain series resistance. In contrast, the method appears particularly useful for the so-called HV DMOS quasi-saturation regimes when associated with a quasi-linear operation of the intrinsic MOS transistor. Fig. 3.5 presents the typical effect induced on the output characteristics of the LDMOS by adding various external series resistances. Relevant characteristics shifts are observed in the quasi-linear regions and in the saturation voltages.

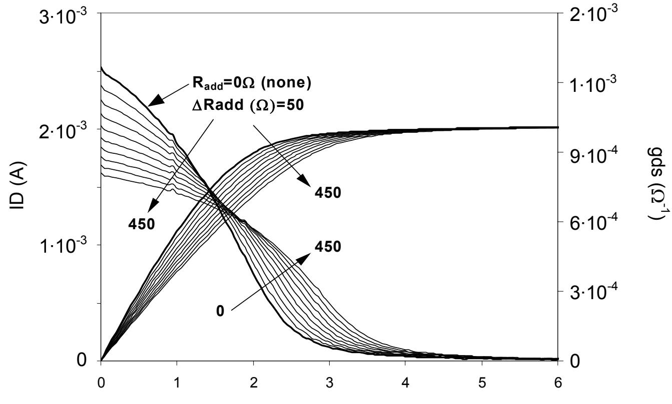


Fig. 3.5. Experimental I_D-V_D and g_{ds}-V_D characteristics of n-channel LDMOS transistor, without and with various added external drain series resistance, R_{Dadd}.

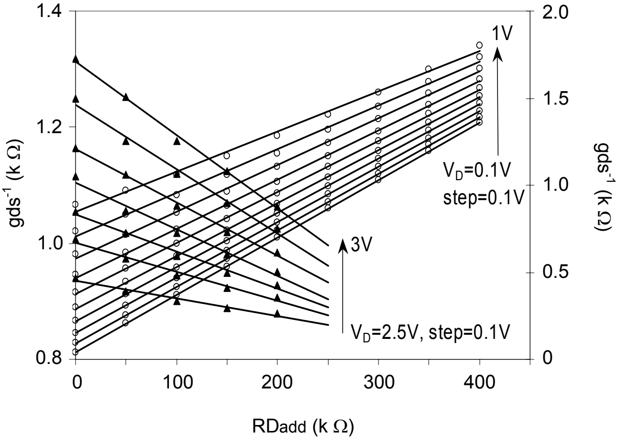


Fig. 3.6. Linear plot of g_{ds}^{-1} *versus* R_{Dadd} *at various drain voltages and constant* V_G *(data from Fig. 3. 4), in case of a n-channel LDMOS transistor.*

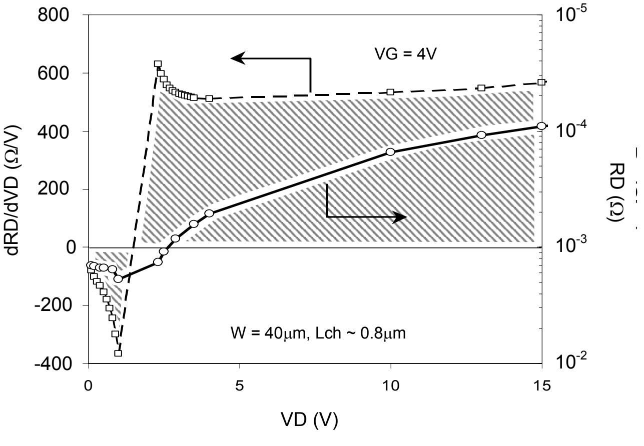


Fig. 3.7. Experimental dR_D/dV_D *and calculated (numerical integration)* R_D*, as functions of* V_D *at constant* V_G *(4V) for n-channel LDMOS transistor.*

Reported measured data in Fig. 3.5 permit to plot g_d^{-1} versus R_{Dadd} and estimate with acceptable accuracy its slope up to V_D = 15V (see Fig. 3.6). The subsequently calculated drain series resistance derivative, dR_D/dV_D, is presented in Fig. 3.7. Using a simple numerical integration procedure of the deduced derivative plot (i.e. equivalent to the dashed area), combined with eq. (3.1) and using the corresponding value of R_{D0} at same constant V_G, permits the estimation of the overall drain bias-dependence of $R_D(V_D)$ as shown in Fig. 3.7 (solid line).

Fig. 3.8 illustrates the good agreement between experimental data, using this technique, when compared to numerically simulated drift-resistances. Fig. 3.8 shows also the limited range of V_D bias over which the reported experimental technique allows accurate $R_D(V_D, V_G)$ extraction. For the characterized n-channel LDMOS transistor, the extraction has been limited up to 17V essentially due to the noisy nature of G_{DS}-V_D characteristic when device is biased toward saturation (i.e. for $V_D > V_{Dsat}$).

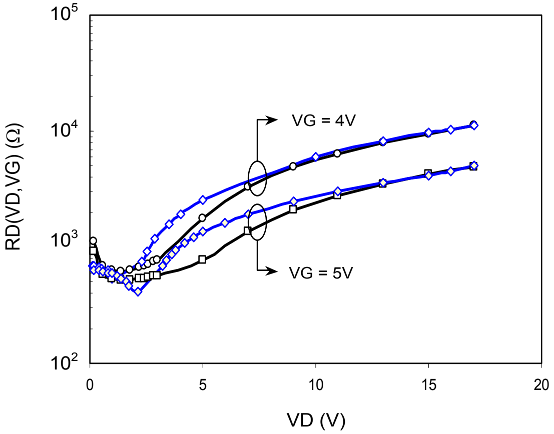


Fig. 3.8. n-channel LDMOS device $R_D(V_D, V_G)$ versus V_D characteristics: numerically simulated data in black and experimentally extracted data in blue.

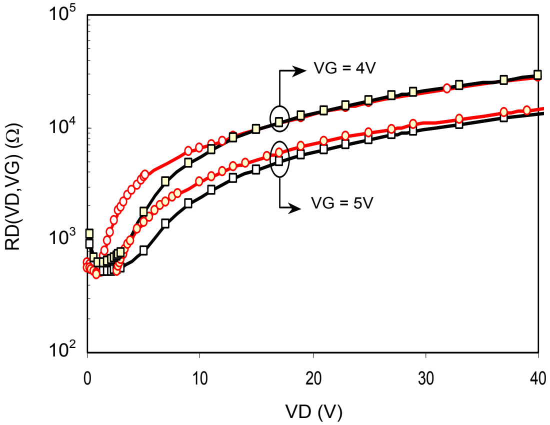


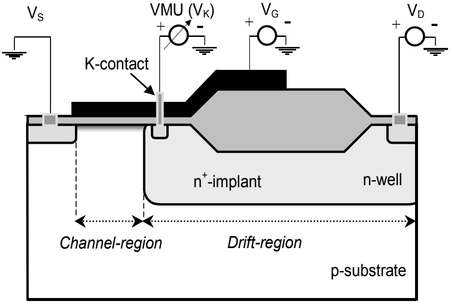
Fig. 3 9. n-channel LDMOS device $R_D(V_D, V_G)$ versus V_D characteristics: numerically simulated data in black and extracted data from simulated I-V characteristics in red.

However, when numerically simulated I-V characteristics from TCAD LDMOS structure are used, the experimental technique does not reveal any bias limitation for accurate $R_D(V_D,V_G)$ extraction where good matching up to 40V (far from V_{Dsat}) is reported in Fig. 3.9. This clearly confirms the validity of the technique. The reported results have been subject to publications in [5,6].

3. 2. 2. Mathematical Based Modeling Approach

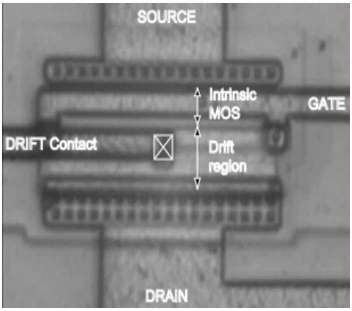
The performed investigation on numerically simulated DMOS architectures (TCAD structures) revealed the V_K-concept and its interest for device modeling requests. In this approach, the idea is to enable the probing of the V_K-potential (intrinsic drain-voltage) on real DMOS transistors, in order to confirm and validate experimentally the V_K-concept usefulness previously reported in [1]. For such purpose, AMI Semiconductors realized dedicated DMOS transistors called *MESDRIFT*.

3. 2. 2. 1. MESDRIFT architecture: In order to monitor the intrinsic drain-potential, an extra contact (called *K-contact*) is added to the original LDMOS (n-type) and XDMOS (n- and p-type) architectures, resulting in new MESDRIFT test structures [7-9]. A schematically illustration and top-view photography of the n-channel XDMOS MESDRIFT structure are respectively presented in Figs. 3.10 and 3.11. The structure is engineered by adding in the drift-region an *n^+ implant* at the proximity of the p-n junction, as close as possible to the K-point. The K-contact is designed with dimensions much smaller than the transistor width and consequently, no significant influence is expected on the overall transistor characteristics.



(a)

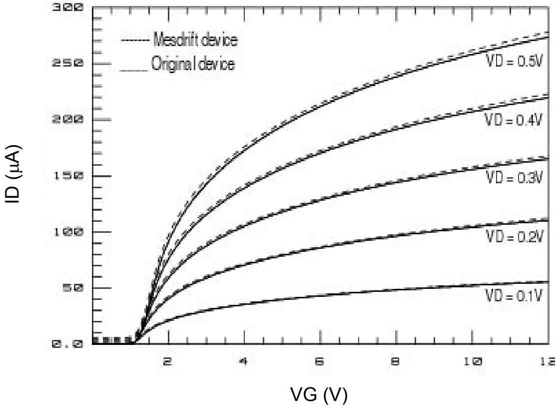
Fig. 3.10. Cross-section of the n-channel XDMOS MESDRIFT structure with n^+ implant location and parameter analyser (HP-4156) measurement setup used to monitor the intrinsic drain potential, V_K.



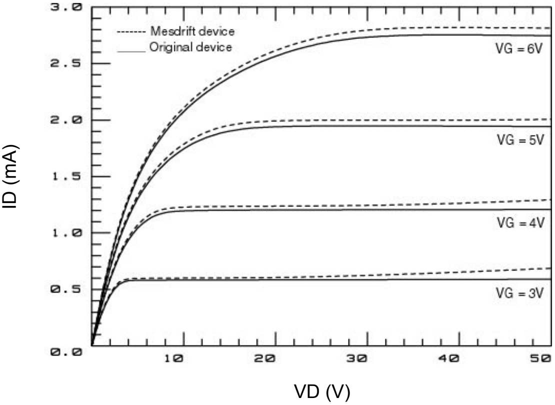
(b)

Fig. 3.11. Top-view photography of the n-channel XDMOS MESDRIFT structure with drift-contact (K-contact), intrinsic-MOS and drift-region locations.

Figs. 3.12 (a and b) report a comparison between transfer, I_D-V_G, and output, I_D-V_D, characteristics measured on both X-DMOS and its corresponding MESDRIFT structure: the very good matching of their characteristics (less than 10% difference in terms of current) appears to support the claim that fabricated MESDRIFT structures accurately reproduces the I-V behaviour of the original HV-DMOS structures, including drift resistance bias dependence. Only a slight reduction of the breakdown voltage (<5%) is observed in case of MESDRIFT.



(a)



(a)

Figs. 3.12. Experimental comparison between MESDRIFT (dashed line) and original n-channel XDMOS (solid line) characteristics: (a) I_D-V_G, and (b) I_D-V_D.

3. 2. 2. 2. MESDRIFT characteristics: With the measuring set up illustrated in Fig. 3.10 (based on a HP-4156 parameter analyzer), the potential of MESDRIFT K-contact (V_K) has been experimentally monitored with a high impedance voltmeter, while varying the drain and gate biases in all operation regimes of the DMOS transistor. From the monitored evolution of V_K with V_D and V_G, the bias-dependent drift-resistance is calculated with eq. (2.1). The reported characteristics from n-channel XDMOS MESDRIFT structure are:

***(i) V_K-potential vs. MESDRIFT architecture*:** monitored intrinsic-drain potential, $V_K(V_D, V_G)$, illustrated in Fig. 3.13 reveals very similar characteristics when compared to those extracted from numerically simulated XDMOS structure (Fig. 2.6.a). As it can be seen, V_K potential remains at low value (~ 4V) when V_D is biased up to 20V.

***(ii) Intrinsic-MOS drain current vs. MESDRIFT architecture*:** In Fig. 3.14, the reported drain current curves, I_D-V_K, from the XDMOS MESDRIFT structure shows a very similar characteristic to those illustrated in Fig. 2.12.a (TCAD structure), where at low V_G the current saturates (i.e. flattens) after few volts, while at higher V_G values I_D keeps rising with V_K (V_{CH}), clearly indicating that the intrinsic-MOS transistor is in linear regime of operation.

***(iii) Drift-resistance vs. MESDRIFT architecture*:** the experimental R_{drift} characteristics presented in Fig. 3.15 follow the predictions of numerical simulations in *all significant operation regimes* (Fig. 2.8.b) as well as its range of magnitude (i.e. $R_{drift} = 10^{3}$-10^{6} Ω). However, the unusual behaviour depicted from numerical simulated drift characteristics at V_D values below 1V, where R_{drift} decreases with V_D increases from zero to ~1V at all V_G biases (see Fig. 2.8.b, doted boxes), is not visible when extracting R_{drift} from the MESDRIFT structure. This can be explained by the change of the conduction from surface into volume, most probably due to the slightly shifted location of the n^+ implant (Fig. 3.10), which results in an equivalent mobility increase when V_D rises.

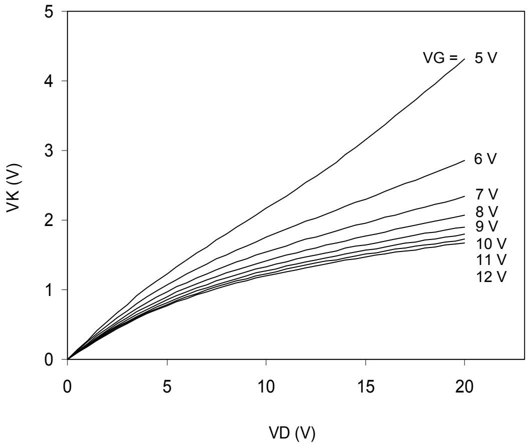


Fig. 3.13. Experimentally monitored V_K-V_D characteristics from n-channel XDMOS MESDRIFT structure.

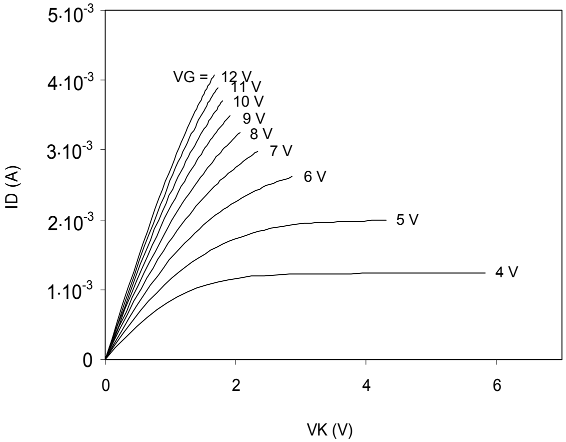


Fig. 3.14. Experimental I_D-V_K characteristics extracted from n-channel XDMOS MESDRIFT structure.

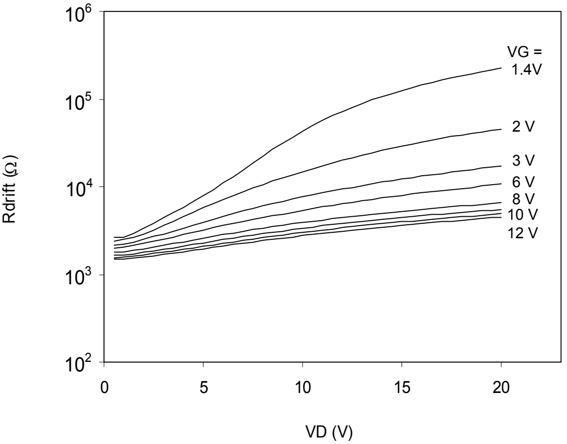


Fig. 3.15. Extracted drift-resistance characteristics from n-channel XDMOS MESDRIFT structure.

3. 2. 2. 3. Bias-dependent drift-resistance modeling: Based on the reported results in § 3.2.2.2, the idea of setting a modeling approach based on the MESDRIFT architecture raised, where the intrinsic drain-voltage, V_K, is experimentally extracted and from which the drift resistance is calculated and mathematically approximated by an appropriate function.
Concerning the mathematical expression, the first step has been to define an expression able to precisely track the specific characteristic with a minimum number of coefficients. Accordingly two criteria have been putted for a primary evaluation at room temperature: (i) *a maximum total number of fitting coefficients ≤ 10* and (ii) *a maximum error ≤ 20% and an average (mean) error < 10%*. Of course these numbers are subject to improvements, after identifying the adequate expression that fulfills these primary criteria.

Among the various mathematical functions investigated:

⇒ Polynomial function: $R_D(V_D) = A_n V_D^n + A_{n-1} V_D^{n-1} + ... + A_0$ (3.5)

⇒ Logarithmic function: $R_D(V_D) = B_2 \ln(B_1 V_D + B_0)$ (3.6)

where A_n, A_{n-1}, …, A_0 and B_2, B_1 and B_0 are all V_G dependent (i.e. $f(V_G)$).

Polynomial functions, of 3rd order and higher, (eq. 3.5) are able to adequately track the drift resistance characteristics, but the total number of coefficients is exceeding the fixed number of 10, where no less than 15 coefficients are needed for a 3rd order polynomial expression.

The logarithmic expression (eq. 3.6) has the advantage to require no more than 10 coefficients to adequately describe the $R_{drift}(V_D, V_G)$ features, but unfortunately not over the whole drain voltage range; the low V_D portion cannot be well tracked together with the remained V_D portion. To overcome this limitation, the idea to combine an additional term (function) together with the logarithmic expression has been investigated. Keeping in mind to satisfy the criterion, only simple functions have been considered:

⇒ 1st order polynomial function: $C_1 V_D + C_0$ (3.7)

⇒ Parabolic function: $(C_1 V_D + C_0)^{-1}$ (3.8)

Combining eq. (3. 6) with eq. (3. 7) or (3. 8) leads to possible final expressions:

$$R_{drift}(V_D) = (C_1 V_D + C_0) + B_2 \ln(B_1 V_D + B_0) \quad (3.9)$$

$$R_{drift}(V_D) = (C_1 V_D + C_0)^{-1} + B_2 \ln(B_1 V_D + B_0) \quad (3.10)$$

where C_1, C_0 and B_2, B_1 and B_0 are all $f(V_G)$. When fitted in V_G, eq. (3.9) couldn't adequately tracks the $R_{drift}(V_D, V_G)$ characteristics, while in eq. (3. 10) the total number of coefficients exceeded the specified limit (i.e. no less than 13 coefficients are necessary to fall with the criterion error). After many attempts, changes have been introduced to the idea of adding an extra term to the logarithmic function (i.e. eq. 3.6): by substituting the added term in eq. (3.9) or (3.10) by a constant term and including and exponential term within the logarithmic expression, encouraging results are obtained. The readjusted expression becomes:

$$R_{drift}(V_D) = R_0 + B_2 \ln\left(e^{B_1 V_D - B_0} + 1\right) \quad (3.11)$$

Parameters R_0 and B_2, B_1 and B_0 when fitted in V_G and the final number of coefficients when optimized to a minimum, the bias-dependent drift-resistance expressions takes the final form of:

$$R_{drift}(V_D, V_G) = R_0 + \frac{R_1}{(b_2 V_G - 1)} \ln\left(e^{(b_3 V_G + c_3)\cdot V_D - (a_4 V_G{}^2 + b_4 V_G + c_4)} + 1\right) \tag{3.12}$$

After being identifying the adequate mathematical expression able to fit the extracted drift-resistance characteristics at room-temperature, the next step has been to take into account the temperature factor. The temperature dependence of the drift-resistance is *physically* modeled according the following expression:

$$\frac{R_{drift}(T)}{Rdrift(T_0)} = \left(\frac{T}{T_0}\right)^{X_T} \quad \text{and} \quad X_T = (mV_D + n)^{-1} \tag{3.13}$$

where, T_0 is the nominal (i.e. reference) temperature in Kelvin, $R_{drift}(T_0)$ its corresponding bias-dependent drift-resistance and X_T the temperature dependence term, in which coefficients "*m*" and "*n*" are *f*(V_G, T). From eq. (3. 12) and (3. 13), the final bias-dependence drift-resistance becomes:

$$R_{drift}(V_D, V_G, T) = \left(R_0 + \frac{R_1}{(b_2 V_G - 1)} \ln\left(e^{(b_3 V_G + c_3)\cdot V_D - (a_4 V_G{}^2 + b_4 V_G + c_4)} + 1\right)\right)\left(\frac{T}{T_0}\right)^{\left(\frac{1}{mV_D + n}\right)} \tag{3.14}$$

From the beginning of the modeling work, a major effort has been putted in order to elaborate a *unique* $R_{drift}(V_D, V_G, T)$ expression valid for all investigated MESDRIFT DMOS architectures (i.e. n- and p-type XDMOS and n-type LDMOS structures). Eq. (3.14) is the result of such efforts.

***(i) Extracted vs. mathematically simulated drift-resistance at room-temperature*:** Figs. 3.16 - 3.18 present the experimental bias-dependent drift-resistance extracted from the various MESDRFIT architectures at room temperature and their corresponding fits using eq. (3.12). To note that only values of coefficients vary from architecture to another.

In term of accuracy and fitting precision at room-temperature, relative Maximum and Mean (average) errors between experimentally extracted and fitted (simulated) characteristics are calculated as follow:

$$\text{Relative Error}(\%) = \frac{\left|R_{drift}(V_D, V_G)_{ext} - R_{drift}(V_D, V_G)_{sim}\right|}{R_{drift}(V_D, V_G)_{ext}} \cdot 100 \tag{3.15}$$

Calculated errors are reported respectively for n-channel XDMOS, p-channel XDMOS and n-channel LDMOS structures in Figs. 3.19 (a, b and c). It might be worthy to precise that Maximum and Mean error represent respectively the highest and average error values found for each V_G bias over the whole V_D range.

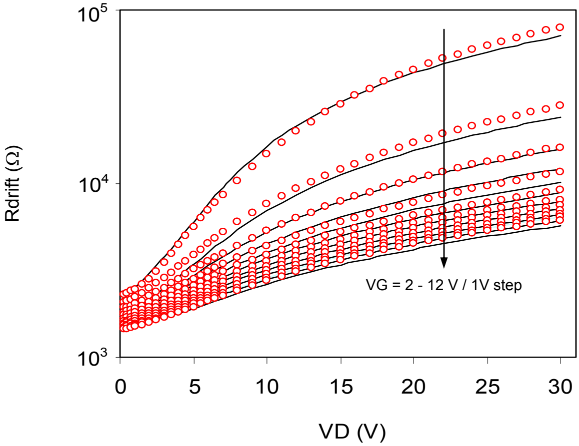


Fig. 3.16. Extracted drift-resistance characteristics at room-temperature from n-channel XDMOS MESDRIFT structure, in red, fitted with expression (3.12) in black.

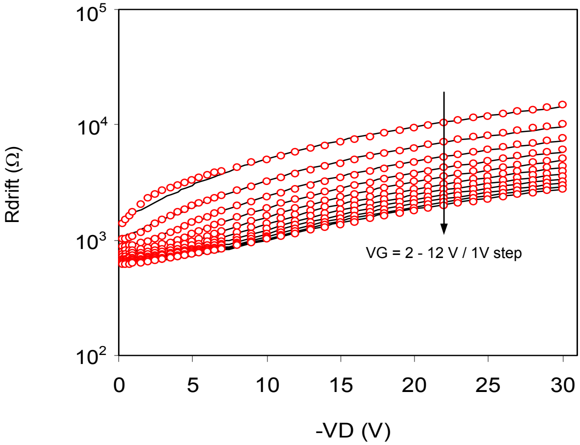


Fig. 3.17. Extracted drift-resistance characteristics at room-temperature from p-channel XDMOS MESDRIFT structure, in red, fitted with expression (3.12) in black.

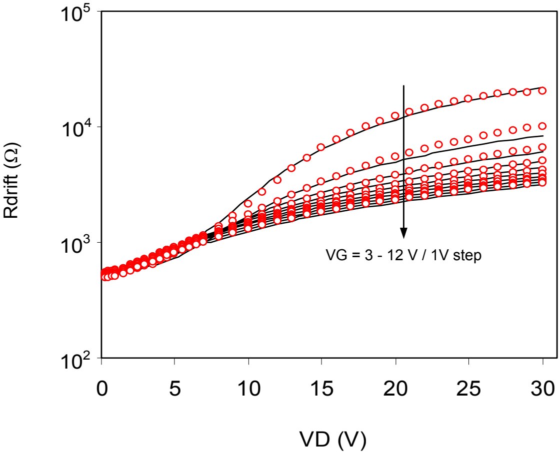
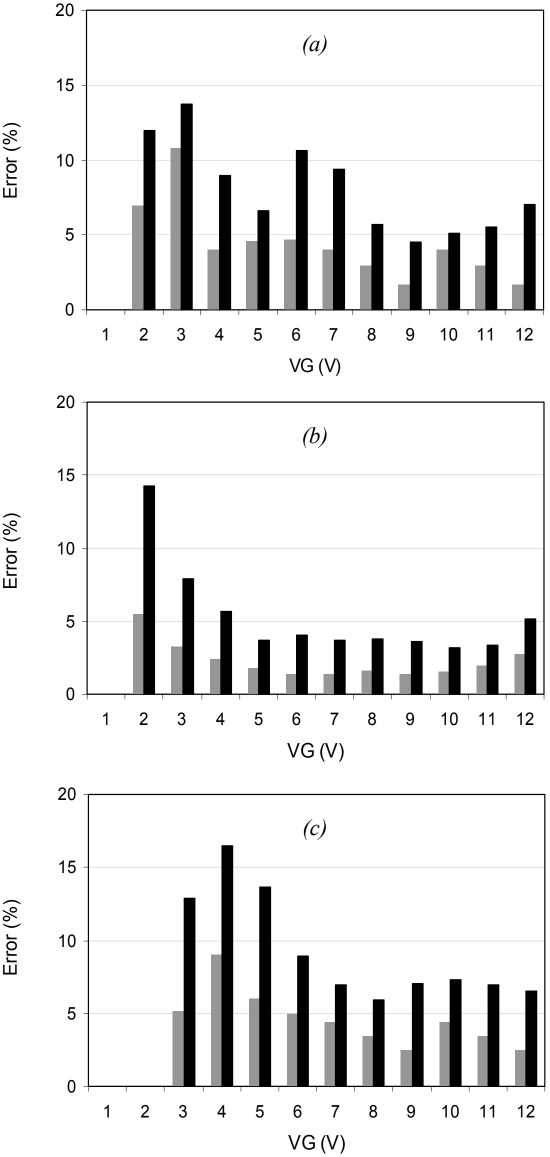


Fig. 3.18. Extracted drift-resistance characteristics at room-temperature from n-channel LDMOS MESDRIFT structure, in red, fitted with expression (3.12) in black.



Figs. 3.19. Calculated error percentages between experimentally extracted and fitted R_{drift} (V_D, V_G) characteristics at room temperature. Maximum error, in black, and Mean error, in grey, for: (a) n-channel XDMOS, (b) p-channel XDMOS and (c) n-channel LDMOS MESDRIFT architectures.

***(ii) Extracted vs. mathematically simulated drift-resistance over temperature*:** characterization of MESDRFIT structures have been performed in temperature up to 150°C only for n- and p-channel XDMOS architectures, while for n-channel LDMOS important leakage current has been observed when characterized at high temperature. Extracted characteristics and their corresponding fits are reported in Figs. 3.20 and 3.21.

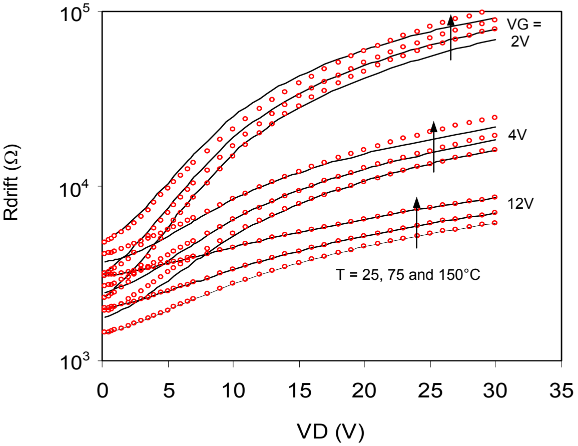


Fig. 3.20. Extracted drift-resistance characteristics in temperature (up to 150°C) from n-channel XDMOS MESDRIFT structure, in red, fitted with expression (3.14) in black.

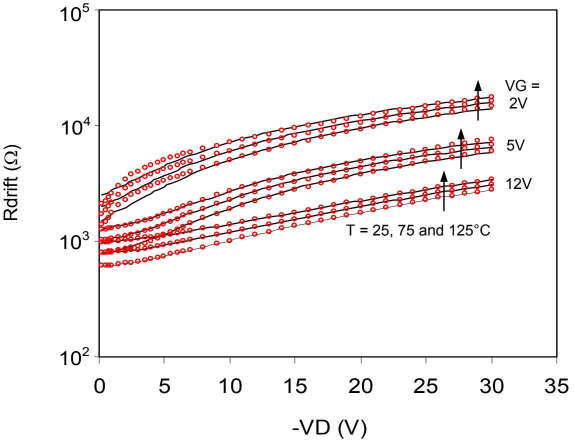
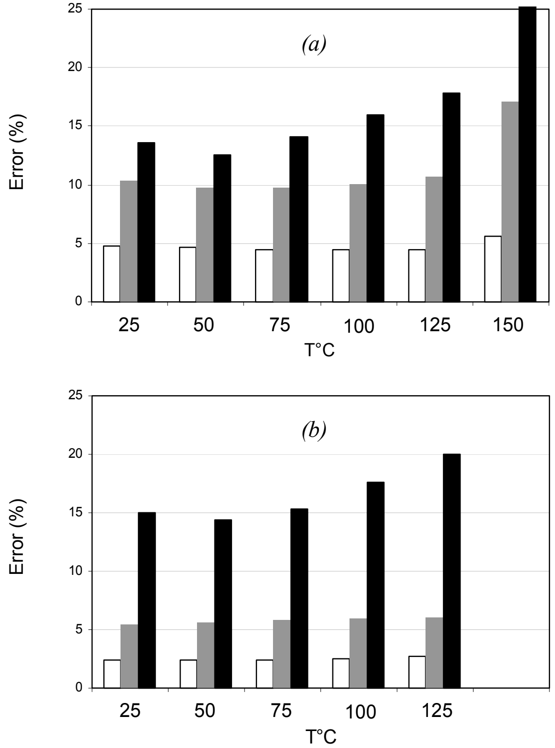


Fig. 3.21. Extracted drift- resistance characteristics in temperature (up to 125°C) from p-channel XDMOS MESDRIFT structure, in red, fitted with expression (3.14) in black.



Figs. 3. 22. Calculated error percentages between experimentally extracted and fitted R_D (V_D, V_G) characteristics in temperature. Maximum error, in black, Max-Mean error and in grey, Mean error in white for: MESDRIFT (a) n-channel and (b) p-channel XDMOS architectures.

In contrast with room-temperature notifications, here Maximum and Mean error respectively stand respectively for highest (in black) and average (in grey) error values found at each investigated temperature over the whole characterized V_D and V_G range. Max-mean error (in white) represents the highest average error depicted at each temperature. In case precise estimation of relative errors is needed, all calculated data illustrated in Figs. 3.19 and 3.22 are reported in tables 3.2 and 3.3.

Over the investigated V_D (0 to 30V) and V_G (±2 to ±12V) ranges at room temperature, Maximum and Mean errors found for investigated MESDRIFT architectures were respectively: 14.2% and 2.3% (p-channel XDMOS); 13.7% and 4.4% (n-channel XDMOS); 16.5% and 4.6% (n-channel LDMOS). Over the temperature range of interest (25 – 150C), the Maximum and Mean errors were respectively: 20% and 2.7% (p-channel XDMOS); 26.7% and 5.6% (n-channel XDMOS).

RELATIVE ERROR %							
	n-XDMOS		n-LDMOS			p-XDMOS	
V_G (V)	Max	Mean	Max	Mean	V_G (V)	Max	Mean
	V_D: 0 → 30V					V_D: 0 → -30V	
2	11.9	6.96	$V_G < V_T$		-2	14.2	5.51
3	13.7	10.8	12.87	5.13	-3	7.89	3.24
4	8.94	4.04	16.49	9.00	-4	5.70	2.42
5	6.60	4.60	13.69	5.98	-5	3.73	1.78
6	10.6	4.66	8.93	4.95	-6	4.01	1.38
7	9.39	4.00	6.97	4.41	-7	3.72	1.38
8	5.65	2.97	5.91	3.41	-8	3.81	1.65
9	4.56	1.67	7.05	2.53	-9	3.60	1.41
10	5.09	4.00	7.32	4.41	-10	3.22	1.55
11	5.48	2.97	6.98	3.41	-11	3.36	2.02
12	7.07	1.67	6.56	2.53	-12	5.14	2.74

Table 3.2. Relative Maximum and Mean errors, in percentage, between experimentally extracted $R_D (V_D, V_G)$ characteristics, at room temperature, and their corresponding fits for different MESDRIFT architectures: n-channel XDMOS, p-channel XDMOS and n-channel LDMOS.

T (°C)	RELATIVE ERROR %					
	n-XDMOS			p-XDMOS		
	V_D: 0 → 30V, V_G: 2 → 12V			V_D: 0 → -30V, V_G: -2 → -12V		
	Max	Max-Mean	Mean	Max	Max-Mean	Mean
25	13.61	10.36	4.82	15.05	5.45	2.43
50	12.54	9.75	4.66	14.41	5.63	2.35
75	14.16	9.74	4.50	15.28	5.85	2.4
100	15.95	10.05	4.50	17.56	5.97	2.55
125	17.81	10.73	4.47	20.05	6.00	2.67
150	26.70	17.10	5.60	Significant leakage current		

Table 3.3. Relative Maximum, Max-mean and Mean errors, in percentage, between experimentally extracted $R_D (V_D, V_G)$ characteristics, at various temperatures, and their corresponding fits for different MESDRIFT architectures: n-channel XDMOS and p-channel XDMOS.

As mentioned previously, the achieved accuracy necessitates the use of adequate coefficient values in both eq. (3.12) and (3.14). For such purpose, a fully optimized procedure to extract the optimum set of coefficient values, for all investigated architectures, has been implemented in a mathematical solver (MathCAD). It consists of a continuous iteration procedure which requests input initial guess-values and the desired error limit to be reached. The relative error is checked by the routine after each iteration and compared to the defined one. The procedure continues till the defined error tolerance is reached. The estimated time needed for the extraction of an optimized set of coefficients does not exceed the few minutes. It is expected that the overall accuracy can still be improved when global optimization, including BSIM parameters and drift-coefficients, is performed.

3. 3. DMOS TRANSISTOR MACRO-MODELING

After being going through the proposed experimental technique and mathematical approaches for the modeling of the bias-dependent drift-resistance in details and investigating their different aspects, the next step has been to evaluate the usefulness of both approaches for the modeling purposes of DMOS transistors using the Intrinsic-drain concept (V_K-concept). Fig. 3.23 illustrates the macro-model composites: (i) a Low-Voltage model (BSIM3v3), calibrated on DMOS intrinsic-MOSFET and (ii) bias-dependent drift-resistance represented by one of the reported approaches in this chapter.

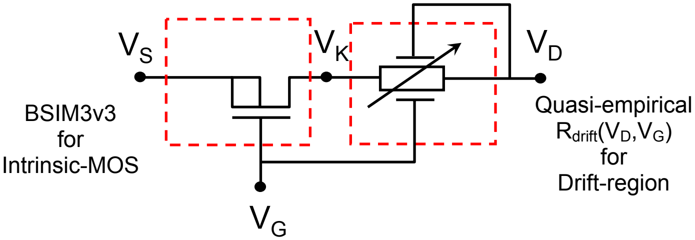


Fig. 3.23. Circuit representation of the HV-DMOS transistor macro-modeling.

3. 3. 1. DMOS Modeling Using Experimental R_{drift} Mathematical Expression:

Based on the experimental evaluation technique proposed in section (§ 3.2.1) and the reported experimental evaluation on n-channel LDMOS devices, a modeling strategy has been settled which can be summarized in the following steps:

Step-1: dividing the LDMOS transistor into significant parts: intrinsic-MOS part and drift part (see Fig. 2.4.a).
Step-2: evaluating experimentally the drift-resistance using the proposed technique and from which of the intrinsic $V_K\,(V_D,\,V_G)$ potential is calculated as follow:

$$V_K(V_D, V_G) = V_D - I_D \cdot R_{drift}(V_D, V_G) \qquad (3.16)$$

Step-3: approximating the $V_K(V_D,V_G)$ potential with an appropriate polynomial or non-linear approximation.
Step-4: setting-up the parameter extraction strategy: parameter extraction procedure for BSIM necessitates the experimental extraction of few parameters (e.g. V_T, μ_0, $\theta_{1,\,2}$, Swing).
Step-5: BSIM3v3 calibration on the intrinsic-MOS part (see § 3.1 and Fig. 3.1.a).
Step-6: macro-model build-up as illustrated in Fig. 3.23.

It is worth noting that each extracted drift-resistance value has a corresponding extrinsic V_D and V_G bias couple on an n-channel LDMOS I_D-V_D characteristic, therefore a separate simulation has to be run for each point value (i.e. time consuming process).

However, Macro-modeled I-V characteristics using experimentally and TCAD R_{drift} extracted values are in good agreements with measures characteristics [6] as it is illustrated in Fig. 3.24. It appears that extracted drift-resistance from TCAD structure (Fig. 3.9) provide a slight improved fitting more precisely in the linear-to-saturation transition region of the I_D-V_D characteristic (i.e. quasi-saturation region). This is essentially due to the reported noisy nature of the conductance characteristics, G_D-V_D, when derived from experimentally measure I_D-V_D curves (i.e. real device) in contrast with those derived from numerically simulated output characteristics (i.e. TCAD structures) and which are totally free of noise. All this obviously would differently impact the extracted drift-resistance, the calculated V_K-potential and thus the final macro-modeled characteristics.

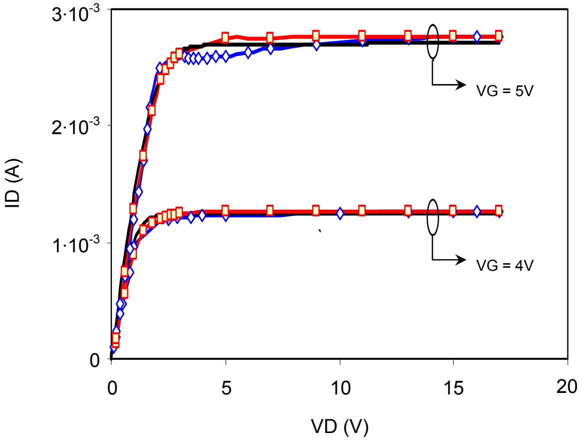


Fig. 3.24. n-channel LDMOS output characteristics: measured (in black), modeled using experimental R_{drift} (in blue) and modeled using TCAD extracted R_{drift} (in red).

The main advantages and draw-backs of this modeling approach can be resumed as following.

Advantages: **i-** Simple measurements and standard characterization equipments are needed.
ii- Do not depend on the drain architecture (i.e. suitable for any asymmetric MOS transistor).
iii- Easy to calibrate.
iv- Fast convergence.

Limitations: **i-** Despite to be a straightforward extraction technique, it is however, a lengthy and time-consuming procedure.
ii- Limited range of extraction on real devices (due to the noisy transconductance, G_D-V_D, characteristic in the saturation regime).
iii- Limited accuracy of the extraction technique in quasi-linear region.

3. 3. 2. DMOS Modeling Using Mathematical R_{drift} Modeling Approach:

The elaborated modeling strategy with the derived mathematical expression does not much differs from the settled one in section (§ 3.3.1). The MESDRIFT n-channel XDMOS structure has been selected to validate this modeling approach, since it has been intensively characterized and this up to 150°C. The strategy is summarized in the following steps:

Step-1: dividing the XDMOS transistor into significant parts: intrinsic-MOS part and drift part (see Fig. 2.4.b).
Step-2: extracting experimentally $R_{drift}(V_D,V_G)$ characteristics from the dedicated MESDRFIT architecture (Fig. 3.15) and from which $V_K(V_D,V_G)$ potential is estimated using eq. (3.16).
Step-3: fitting extracted characteristics with the appropriate derived mathematical expression: eq. (3.12) for fitting at room-temperature and eq. (3.14) for fitting over temperature.
Step-4: setting-up the parameter extraction strategy: parameter extraction procedure for BSIM necessitates the experimental extraction of few parameters (e.g. V_T, μ_0, $\theta_{1,2}$, Swing). Drift-expression coefficients are identified through a dedicated extraction routine implemented in the mathematical solver, MathCAD (§ 3.2.2.3.ii).
Step-5: BSIM3v3 model calibration on the intrinsic-MOS transistor using experimentally extracted I_D-V_K characteristics (Fig. 3.14).
Step-6: macro-model build-up as illustrated in Fig. 3.23.
Step-7: final model fitting: optimization of drift-coefficients together with BSIM3v3 parameters on global device characteristics, I_D-V_G and I_D-V_D.

3. 3. 2. 1. Extracted vs. modelled I-V characteristics at room-temperature: Transfer and output characteristics, measured from standard n-channel XDMOS transistor (without K-contact), have been fitted with the macro-model following the proposed modeling strategy detailed above. Typical model card with all optimized parameters are listed in table 3.4. Illustrated I_D-V_G characteristics in linear and log scale show good agreements between measured and modelled curves (Figs. 3.25 and 3.26) from weak-to-strong inversion; the subthreshold characteristics is precisely tracked as well as the threshold region as it can be seen from Fig. 3.26. The transconductance characteristic, g_m-V_G, is well reproduced despite the limited discrepancy at high V_G, where the severe attenuation due to self-heating effect (SHE) is not well tracked. However, the positive shift and rise of g_{max} with V_D is well estimated as seen in Fig. 3.7, a very important feature for circuit design. Output characteristics, I_D-V_D, are well modelled up to 65V (Fig. 3.28) on the drain and the different mode of saturation are reasonably reproduced; drift pinch-off at low V_G bias and quasi-saturation at high V_G (10V). Unfortunately, the negative slope of the saturated I_D for V_G = 4 and 6V (Fig. 3.28), induced by self-heating, cannot be reproduced since the macro-model does not account for such effect. Identically for the gm-V_G characteristics in Fig. 3.27, at high V_G (7-12V) and V_D (10-20V) the modelled curves (in black) overestimate the measured data. A very interesting issue for self-heating modeling has been lately reported [10,11] and which uses calibrated extrinsic thermal capacitance and resistor (C_{TH} and R_{TH}).Therefore it can be added as an independent module to any electrical circuit representing a DMOS structure. For more details reference [12] can be consulted. Conductance, g_{ds}-V_D, and on-resistance characteristics are correctly modelled as it can be seen from Figs. 3.29 and 3.30 (a and b) respectively. Calculated relative Maximum and Mean (average) errors according to eq. (3.15) reported in Figs. 3.31 and 3.32, respectively for I_D-V_G and I_D-V_D characteristics, reveal a Maximum error of 12% and a Mean error of 3-4% over the whole investigated bias range: V_G up to 12V and V_D up to 65V.

BSIM3v3 parameters

+ VTH0 = 1.15
+ K1 = 4.442E-16
+ K2 = -0.0186
+ K3 = 43.49
+ U0 = 530.5
+ UA = 1.0064E-10
+ UB = 1.E-21
+ UC = -0.001
+ VOFF = -6.661E-17
+ NFACTOR = 1.1
+ VBM = -5
+ RDSW = 502.652
+ VSAT = 3.81E+04
+ A0 = 1
+ AGS = -1
+ A1 = 0.1
+ A2 = 1
+ PCLM = 10
+ PDIBLC1 = 0.0005179
+ PDIBLC2 = 2.54545E-5
+ PDIBLCB = -1E-06
+ DROUT = 4.44E-16
+ PSCBE1 = 2.0192E+08
+ PSCBE2 = 1E-09
+ PVAG = 4.03436
+ PRWB = 0
+ PRWG = -0.001
+ WR = 1

BSIM3v3 temperature parameters

+ KT1 = -1.108
+ KT1L = 8.3E-08
+ KT2 = -0.1037
+ UTE = -1.0
+ UA1 = 1.0E-09
+ UB1 = -5.705E-18
+ UC1 = -0.1
+ AT = 5.4E+04
+ PRT = 2.22E-13
+ XTI = 3

Drift expression parameters

R0 = $1.73\cdot10^{3}\,\Omega$
R1 = $4.153\cdot10^{3}\,\Omega$
b_2 = 2.17674
b_3 = 0.0042
c_3 = 0.357
a_4 = 0.0294
b_4 = 0.519
c_4 = 3.042

m = 0.012
n = 0.473

Table 3.4. Model card parameters: most relevant BSIM3v3 parameters and drift-expression coefficients.

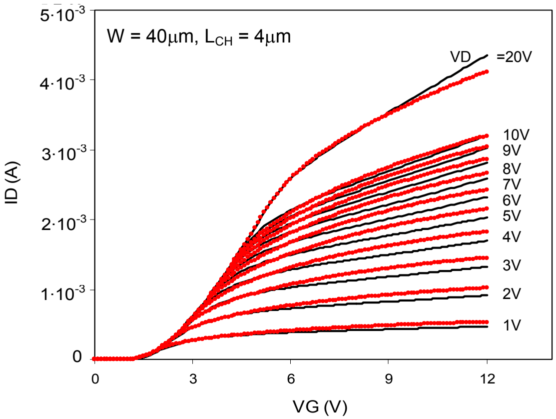


Fig. 3.25. n-channel XDMOS linear I_D-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

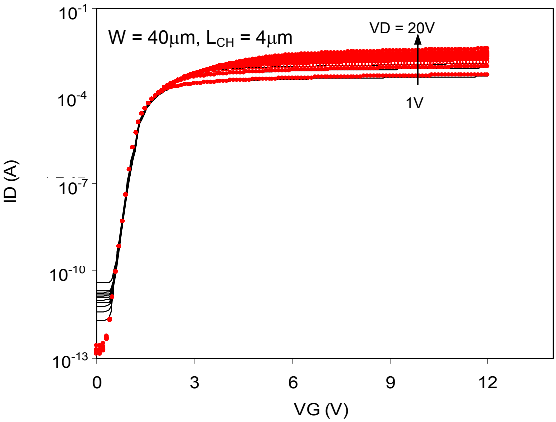


Fig. 3.26. n-channel XDMOS log I_D-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

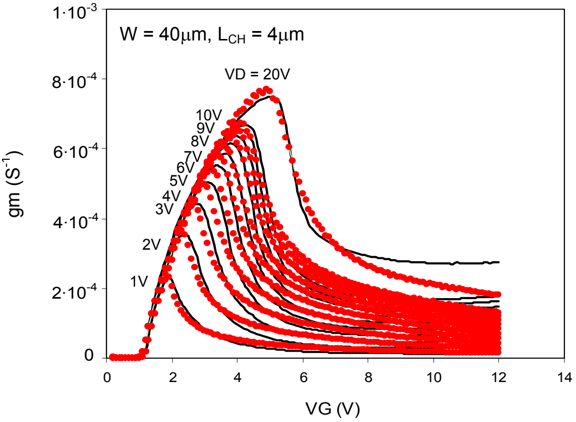


Fig. 3.27. n-channel XDMOS g_m-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

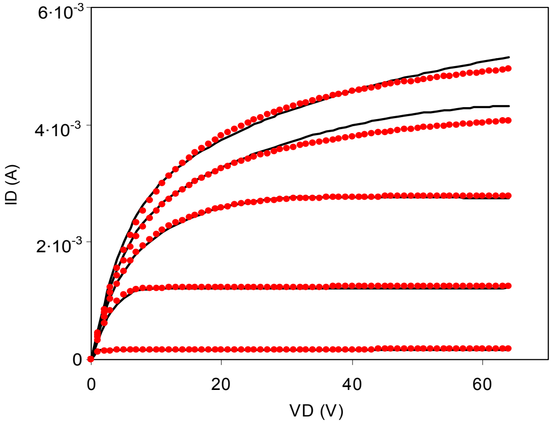


Fig. 3.28. n-channel XDMOS I_D-V_D characteristics at room-temperature: measured (in red) and modeled (in black).

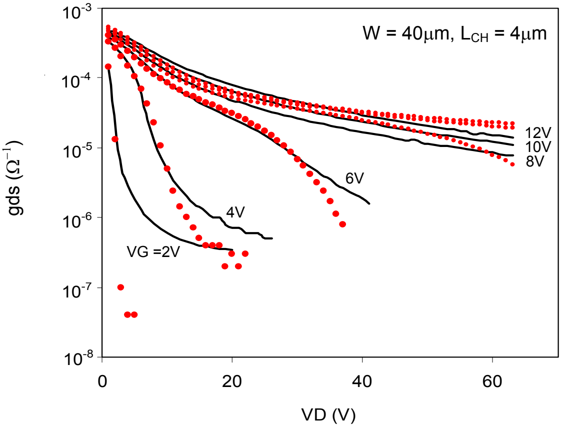


Fig. 3.29. n-channel XDMOS g_{ds}-V_D characteristics at room-temperature: measured (in red) and modeled (in black).

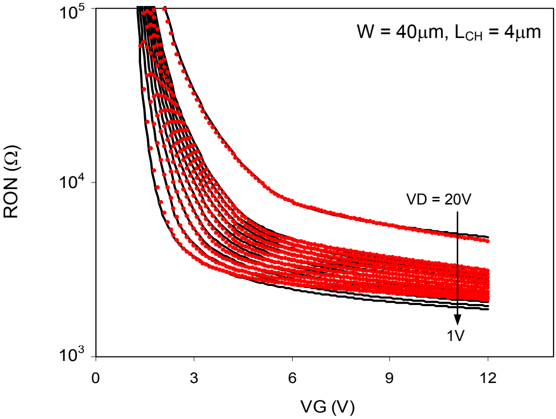


Fig. 3.30. n-channel XDMOS R_{ON}-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

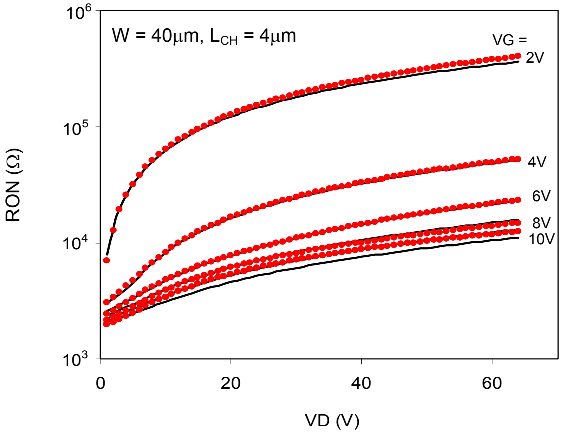


Fig. 3.30. n-channel XDMOS R_{ON}-V_D characteristics at room-temperature: measured (in red) and modeled (in black).

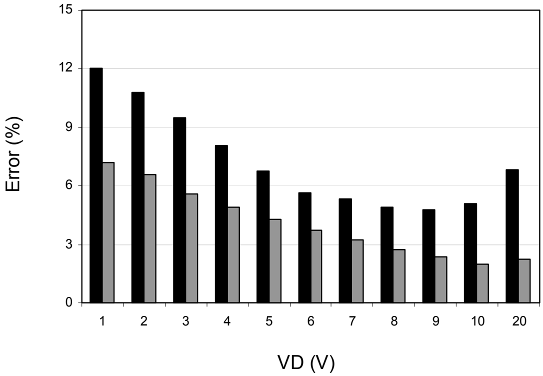


Fig. 3.31. Calculated error percentages between measured and modeled I_D–V_G characteristics with BSIM macro-approach at room-temperature: Maximum error (in black) Mean error and (in grey) for n-channel XDMOS device (data from Fig. 3.25).

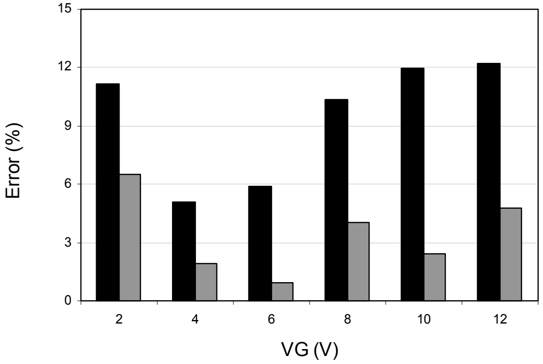


Fig. 3.32. Calculated error percentages between measured and modeled I_D -V_D characteristics with BSIM macro-approach at room-temperature: Maximum error (in black) Mean error and (in grey) for n-channel XDMOS device (data from Fig. 3.28).

3. 3. 2. 2. Extracted vs. modelled I-V characteristics over temperature: Fig. 3.33 reports on the good agreement between measured and modelled output, I_D-V_D, characteristics over the temperature range 25-125°C [7,8]. The model correctly reproduces saturated characteristics for moderate V_G bias (6V) and is still reasonably tracks the quasi-saturation signature on the characteristics for high V_G (12V). However, due to the fact that the model does not account for self-heating effect (SHE), the modelled output current is slightly overestimated as V_G and V_D biases become high and where SHE is more pronounced (Fig. 3.33, I_D -V_D curves at V_G = 12V).

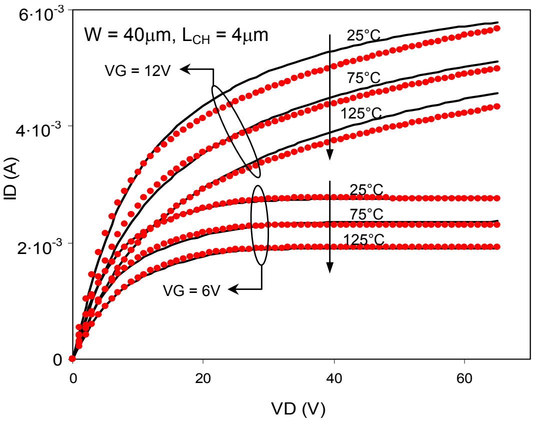


Fig. 3.33. n-channel XDMOS I_D-V_D characteristics over temperature: measured (in red) and modeled (in black).

3. 3. 2. 3. Model scalability: Reported measures in Figs. 3.25 – 3.33 have been performed on 40µm device width. In order the check the model scalability, further I-V measures have been performed over device widths ranging from 10µm to 250µm [7]. Measured transfer and output currents on n-channel XDMOS transistor featuring a 250µm channel width as well as extracted transconductance characteristics are illustrated in Figs. 3.34 - 3.37.

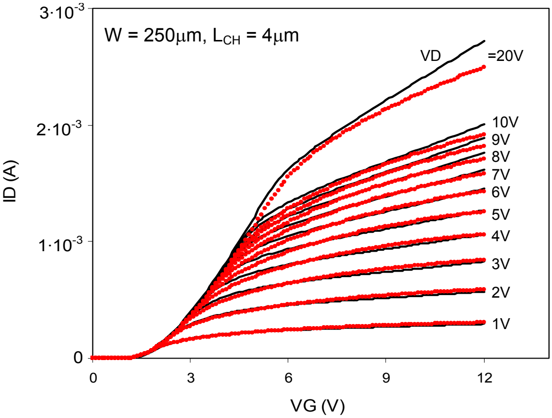


Fig. 3.34. n-channel XDMOS linear I_D-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

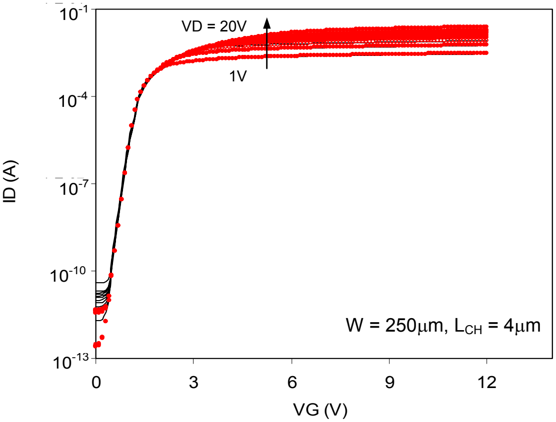


Fig. 3.35. n-channel XDMOS log I_D-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

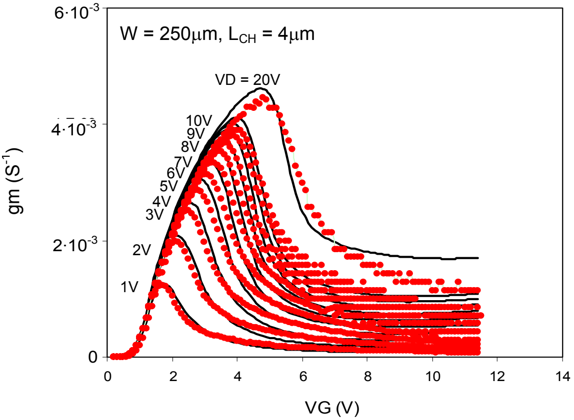


Fig. 3.36. n-channel XDMOS g_m-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

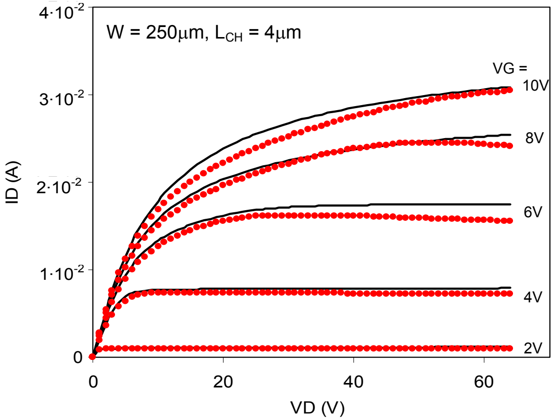


Fig. 3.37. n-channel XDMOS I_D-V_D characteristics at room-temperature: measured (in red) and modeled (in black).

In order to demonstrate the scalability of the model, the optimized parameters and coefficients on the 40µm n-channel XDMOS transistor have been used to model the 250µm device width; only the width parameters has been adjusted. As it can be seen from Fig. 3.34 the transfer characteristics are well fitted and in term of accuracy, no changes are depicted, where Maximum and Mean errors are found unchanged (i.e. Max ~ 12.2% and Mean ~ 4.3%). Subthreshold and threshold characteristics are precisely tracked (Fig. 3.35) and g_{max} evolution with V_D is correctly modeled (Fig. 3.36). Form the output characteristic in Fig. 3.37, the self-heating effect is more pronounced as it is proportional with the device width. Reported relative errors are slightly raised to 17.3% for Maximum error and 7% for Mean errors. However, still the model can fit the global output current trend with the exception of the negative slope of saturated currents as previously mentioned.

The proposed modeling strategy, which relies on a dedicated DMOS architecture (MESDRFIT) and the use of an adequate mathematical expression to describe its bias-dependent drift-resistance, revealed its interesting potential for HV-DMOS modeling purposes. The main advantages and limitations of such approach can be summarized as follow:

Advantages: **i**- At room temperature and with a total number of eight coefficients, R_{drift} (V_D, V_G) expression (eq. 3.12) is able to track the experimentally extracted drift resistance with a good accuracy.

ii- The drift-resistance evolution with temperature is physically modeled and only two extra coefficients are needed to model such dependence.

iii- The developed mathematical expression, eq. (3.14), is able to fit in temperature the three investigated MESDRFIT architectures, simply by properly tuning the coefficient values.

iii- The overall good accuracy of R_{drift} (V_D, V_G, T) expression is improved when combined with the standard LV-MOSFET model, BSIM3v3.

iv- fast and efficient modeling strategy

v- Specific phenomena like quasi-saturation are reasonably well reproduced by the model.

vi- Good model scalability.

vii- No convergence problems are experienced when implemented in circuit simulator like Smartspice.

Limitations: All experienced problems in the previous approach (§ 3.3.1) do not longer exist. The only limitations that can be eventually mentioned are:

i- The need of MESDRIFT architecture to monitor the intrinsic-drain potential: necessary for intrinsic-MOS BSIM calibration and bias-dependent drift resistance extraction.

ii- The large BSIM3v3 parameters number: 28 + 10 parameters for temperature modeling.

3. 4. DMOS TRANSISTOR COMPACT-MODELING

During the past ten years, important efforts have been made in the attempt to accurately model a variety of HV-DMOS architectures, with a particular focus on the lateral architecture, essentially due to its great compatibility with the existing CMOS and BiCMOS technologies, and thus its easy integration with a minimum added cost [13, 14].

According to literatures and published works, two main approaches appear for the modeling of HV DMOS transistors: (i) *macro*-modeling and (ii) *compact*-modeling. In brief, the macro approach consist of *discrete* elements or modules tied together to synthesize a new circuit element able to reproduce the electrical device properties. Generally, when a new device is to be modelled, such approach could appear as a good investigation tool. However, it is not always a successful solution when particular phenomena like quasi-saturation in HV-DMOS transistor is to be considered. Fig. 3.38 shows a qualitative representation of what could be lateral DMOS, if modelled with existing discrete elements. It is clear that as the number of elements rises (e.g. for accuracy purposes), the number of parameters to be extracted increases too and makes the extraction procedure more lengthy and complex. In addition, the circuit complexity rises (due to the increased number of internal nodes) and as a consequence, the simulation time increases and convergence problems might appear.

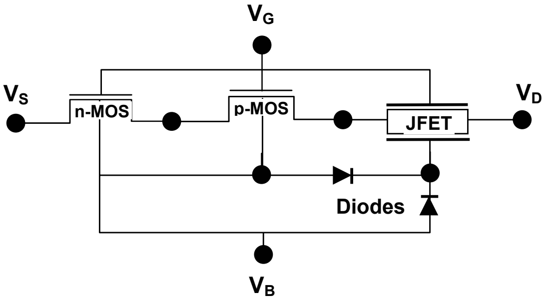


Fig. 3.38. HV-DMOS transistor macro-model using standard circuit elements.

In contrast, in the compact-modeling approach the device unity is preserved through a set of self-consistent and continuous expressions able to predict and reproduce the specific device phenomena. The approach appears to be not an easy task, but when successfully achieved, it delivers key features especially when implemented in simulators used for complex circuitry, where accuracy and robustness of model components becomes essential.

Among the more efficient and accurate compact-models for standard MOSFET's, the EKV model stands at the first position [15, 16]. It's continuous drain current expression, derived from classic MOSFET theory, introduces very few approximations. As a result, a robust, simple and accurate modeling for both hand calculation and numerical simulation is achieved in all regimes of operations (i.e. from weak-to-strong inversion, in linear and saturation regions) [16-18]. For HV-DMOS compact-modeling based on the V_K-concept, EKV appears as a very good candidate essentially due to: (i) its *limited number of parameter* compared to BSIM3v3 (i.e. 20 parameters for EKV, in contrast with ~70 parameters for BSIM3v3) simplify the intrinsic-MOS calibration and (ii) the *compact nature* of the EKV-expression allows the easy-integration of external modules like the derived mathematical drift-expression, eq. (3.12).

For evaluation purposes, a simplified version of EKV model (i.e. long-channel approximation) [15, 19, 20] is used; two basic assumptions are made: (i) short-channel effect is not considered and (ii) 2D field-effects on mobility is neglected (i.e. $\mu_{eff} = \mu_0$).

According to the intrinsic-drain concept (i.e. V_K-concept), subscripts "*K*" and "*D*" denote respectively any quantities associated to the "*intrinsic*" and "*extrinsic*" drain of the device (e.g. V_K and V_D or q_K and q_D).

3. 4. 1. DMOS Compact-Modeling Using EKV Simplified Expression:

According to the EKV long-channel approximation, the normalized drain current (*i*) can be expressed as the difference between the *forward* (i_f) and *reverse* (i_r) current:

$$i = \frac{I_D}{I_0} = i_f - i_r \tag{3.17}$$

$$\text{with } i_{f(r)} = q_{S(K)}{}^2 - q_{S(K)} \tag{3.18}$$

$$\text{and } I_0 = 2 \cdot n(V_P) \cdot C_{ox} \mu_0 U_t{}^2 \left(\frac{W}{L_{CH}} \right) \tag{3.19}$$

where, *"I_0"* stands for the EKV *specific current.*

In terms of potentials [17], $q_{S(K)}$ is given by:

$$q_{S(K)} = -\left(\frac{V_P - V_{S(K)}}{2U_t} - \frac{1}{2} \ln\left(- q_{S(K)}\right) \right) \tag{3.20}$$

where, *"V_P"* stands for the EKV *pinch-off voltage* and is defined as:

$$V_P = \frac{V_G - V_T}{n(V_P)} \tag{3.21}$$

When charge expression, eq. (3.20), is replaced in eq. (3.18), the current expression becomes:

$$i_{f(r)} = \left(\left(\frac{V_P - V_{S(K)}}{2U_t} - \frac{1}{2} \ln\left(- q_{S(K)}\right) \right) \right)^2 + \left(\frac{V_P - V_{S(K)}}{2U_t} - \frac{1}{2} \ln\left(- q_{S(K)}\right) \right) \tag{3.22}$$

The current expression, eq. (3.22), is valid from weak-to-strong inversion regions, but due to its implicit form, it can only be solved numerically.

However, in the case when only strong inversion is to be considered, eq. (3.22) can be simplified by neglecting the logarithmic term. Therefore, the charge expression, eq. (3.20), becomes:

$$q_{S(K)} \cong -\frac{V_P - V_{S(K)}}{2U_t} \tag{3.23}$$

an the current expression becomes:

$$i_{f(r)} \cong \left(\frac{V_P - V_{S(K)}}{2U_t}\right)^2 + \frac{V_P - V_{S(K)}}{2U_t} \tag{3.24}$$

where, “V_S” stands for the potential of the source terminal, “V_K” for the intrinsic-drain potential (i.e. intrinsic-channel end) and *“$n(V_P)$”* for EKV *slope factor*, which is defined as:

$$n(V_P) = 1 + \frac{\gamma}{2\sqrt{2\phi_F + V_P}} \tag{3.25}$$

with *“γ”*stands for EKV *body* or *substrate factor* and is defined as:

$$\gamma = \frac{\sqrt{2q \cdot \varepsilon_0 \varepsilon_{Si} N_{Sub}}}{C_{ox}} \tag{3.26}$$

where, *“N_{Sub}”* stands for the channel-region doping.

The intrinsic-drain potential, V_K, is estimated as follow:

$$V_K(V_D, V_G) = V_D - I_D \cdot R_{drift}(V_D, V_G) \tag{3.16}$$

When eq. (3.12), (317), (3.24), (3.25), (3.26) and (3.16), with $V_S = 0$, the drain current can be simply formulated as:

$$I_D \cong I_0\left(\left(\frac{V_P}{2U_t}\right)^2 + \left(\frac{V_P}{2U_t}\right) - \left(\frac{V_P - V_D + I_D \cdot R_{drift}(V_D, V_G)}{2U_t}\right)^2 - \left(\frac{V_P - V_D + I_D \cdot R_{drift}(V_D, V_G)}{2U_t}\right)\right) \tag{3.27}$$

where, R_{drift} (V_D, V_G) corresponds to the proposed mathematical drift-expression, eq. (3. 12).

In saturation (i.e. for $V_D \geq V_P$), the reverse current, i_r, becomes negligible compared to the forward current, i_f, (i.e. $i_f >> i_r$) and the drain current expression, eq. (3.27), simply reduces to the forward term [15]:

$$I_D sat \cong I_0\left(\left(\frac{V_P}{2U_t}\right)^2 + \left(\frac{V_P}{2U_t}\right)\right) \tag{3.28}$$

No impact on the model accuracy in strong inversion is expected when simplified $q_{S(K}$ expression is used to derive the current. This is demonstrated in Figs. 3.39 and 3.40 where no significant differences are depicted between modeled I-V characteristics with complete $q_{S(K)}$ expression, eq. (3.22), and its simplified form, eq (3.23).

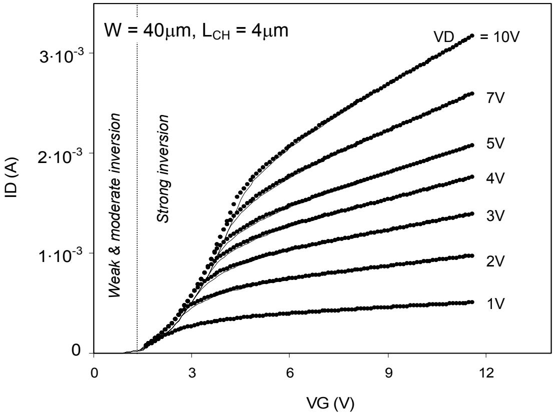


Fig. 3.39. Modelled n-channel XDMOS I_D-V_G characteristics at room-temperature: using the complete (eq. (3.22), symbols) and simplified (eq. (3.23), solid line) $q_{S(K)}$ expression.

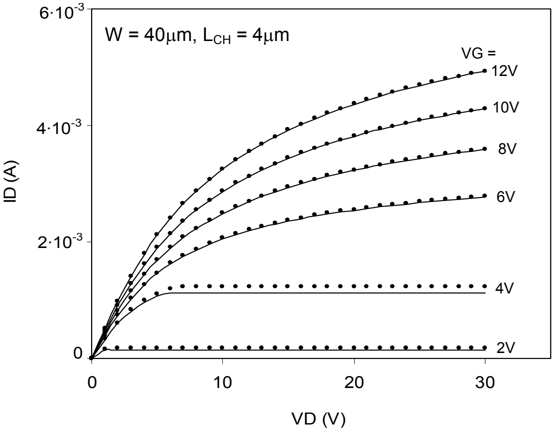


Fig. 3.40.. Modelled n-channel XDMOS I_D-V_G characteristics at room-temperature: using the complete (eq. (3.22), symbols) and simplified (eq. (3.23), solid line) $q_{S(K)}$ expression.

A smoothing function, "F_{trans}" has been introduced to current expression in order to allow in a controlled manner the transition from linear to saturation regime. The function is:

$$F_{trans} = \frac{\exp\left(\frac{I_D sat - I_D}{I_D + \delta} \cdot f_s\right)}{\exp\left(\frac{I_D sat - I_D}{I_D + \delta} \cdot f_s\right) + 1} \tag{3.29}$$

where, *"δ"* stands for a very small quantity, to avoid division by zero when I_D current is null, and "f_s" is a *smoothing factor*.

In reported fittings in (§ 3.4.2), δ and f_s corresponding values are:

Intrinsic-channel parameters

$VT = 1.05V$
$\mu 0 = 450$ cm/V·sec

Technological values

$Lch = 4\ \mu m$
$W = 40\ \mu m$
$tox = 17$ nm
$NSub = 17 \cdot 10^{16}\ cm^{-3}$

Smoothing Coefficients

$\delta = 5.7 \cdot 10^{-5} \equiv I_0 \times 10^6$ (calculated EKV specific current)
$f_s = 4 \equiv Lch \times 10^6$ (effective channel length)

Drift-expression parameters

$R0 = 1.487 \cdot 10^3\ \Omega$
$R1 = 1.979 \cdot 10^3\ \Omega$
$b2 = 0.75425$
$b3 = 0.014$
$c3 = 0.42$
$a4 = 0.042$
$b4 = -0.67$
$c4 = 3.3$

Table 3.5. Optimized set of parameters for the simplified EKV current expression used in the fitting of experimentally extracted I-V n-channel XDMOS characteristics.

3. 4. 2. Extracted vs. Modeling I-V Characteristics at Room-Temperature:

In order to fulfill the EKV long-channel approximation, final current expressions, eq. (3.27) and (3.28), have been validated on corresponding long-channel DMOS transistor (i.e. n channel XDMOS structure, $L_{Ch} \sim 4\mu m$ and $W = 40\mu m$) [21]. Figs. 3.41 – 3.43 and 3.45 - 3.48 report on the measured I-V characteristics at room-temperature and achieved fits using the simplified charge expression, eq. (3.23), to derive the drain current. From Figs. 3. 41 and 3.42, the I_D-V_G and g_{max} characteristics appear reasonably well fitted in the strong inversion region, equivalent to reported fits from macro-modeling with BSIM (see Fig. 3.25 and 3.27). However, the modelled g_m-V_G characteristics show an unusual behaviour (wave-like) as V_G rises. This is essentially due to the mathematical expression used to model the drift-resistance, which has been developed on a quasi-empirical basis. Note that the more important information (from design point of view) remains the g_{max} value and its evolution with external biases; such value is quite well reproduced as it can be seen in Fig. 3.42.

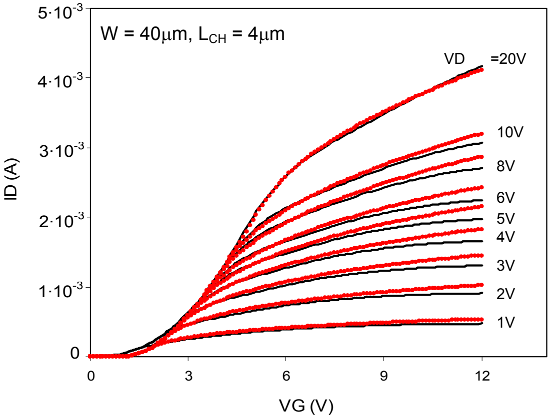


Fig. 3.41. n-channel XDMOS I_D-V_G characteristics at room-temperature: measured (in red) and modeled with simplified charge expression (in black).

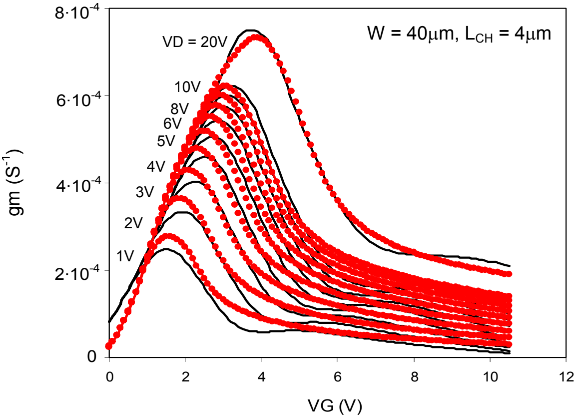


Fig. 3.42. n-channel XDMOS linear I_D-V_G characteristics at room-temperature: measured (in red) and modeled with simplified charge expression (in black).

As expected, in the weak-to-moderate inversions (i.e. $V_G < 2V$), large discrepancies appear in the I_D-V_G subthreshold characteristics between measured and modelled drain currents when simplified charge expression is used (see Fig. 3.43, dotted box). In contrast, when complete charge expression (eq. (3. 22)) is used to derive the drain current, a much less discrepancy with measures is reported in Fig 3.44, but still the fitting is not as accurate as the reported one in Figs. 3.26 and 3.35 (macro-modelled with BSIM). BSIM model dedicates two parameters (N_{FACTOR} and V_{OFFSET}) to fit the subthreshold characteristic, that is not the for the derived EKV model used in our investigation, which explain the error reported in this region.

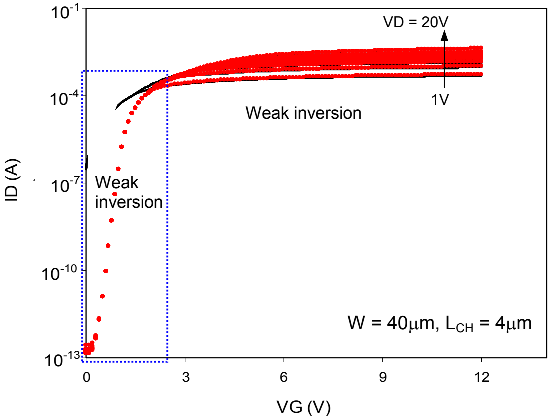


Fig. 3.43. n-channel XDMOS log scale I_D-V_G characteristics at room-temperature: measured (in red) and modeled with simplified charge expression (in black).

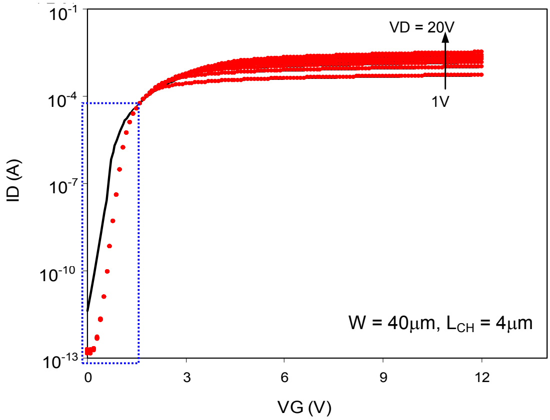


Fig. 3.44. n-channel XDMOS log scale I_D-V_G characteristics at room-temperature: measured (in red) and modeled with complete charge expression (in black).

Modelled output, I_D -V_D, characteristics show a good matching with measured data and as it can be seen from Fig. 3.45 the quasi-saturation signature (for V_G > 7V) is well reproduced. Over the equivalent V_D (up to 30V) and V_G (up to 12V) bias ranges, the fit is even slightly improved when compared to the reported fit in Fig. 3.28 for the BSIM macro-approach. The improved accuracy is confirmed in Fig. 3.46, where the EKV compact-expression shows a better ability to reproduce the g_{ds}-V_D characteristics than the reported fit in Fig. 3.29.

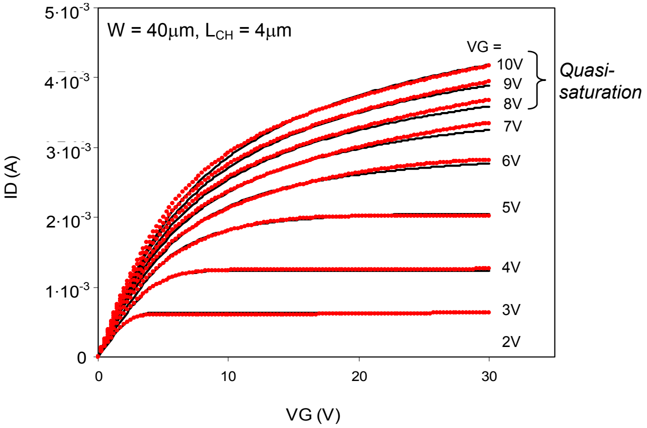


Fig. 3.45. n-channel XDMOS I_D-V_D characteristics at room-temperature: measured (in red) and modeled with simplified charge expression (in black).

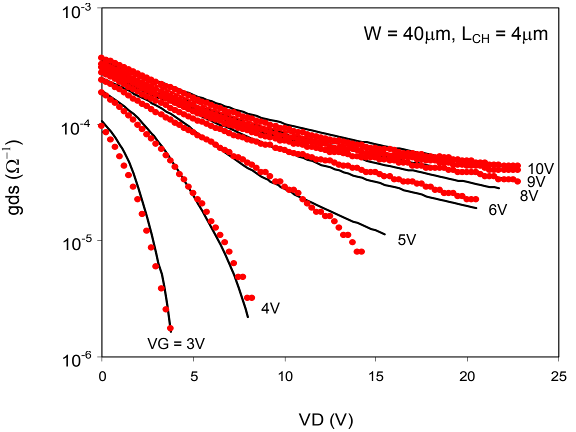


Fig. 3.46. n-channel XDMOS g_{ds}-V_D characteristics at room-temperature: measured (in red) and modeled with simplified charge expression (in black).

Measured R_{ON} characteristics are well predicted by the compact-model in strong inversion as it is seen from R_{ON}-V_G and R_{ON}-V_D characteristics, respectively illustrated in Figs. 3.47 and 3.48. For V_G biases within the weak-to-strong inversion region (i.e. $V_G < 2V$), model equations do not account for it, and thus, mismatches between measures and model within this region is expected in I-V characteristics, R_{ON} included (Figs. 3.47, doted box). This is not the case for macro-modelled curves with BSIM, where the weak and moderate inversions are well defined by model expressions.

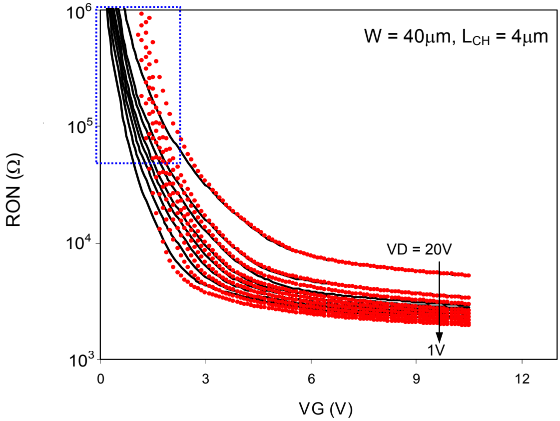


Fig. 3.47. n-channel XDMOS R_{ON}-V_G characteristics at room-temperature: measured (in red) and modeled (in black).

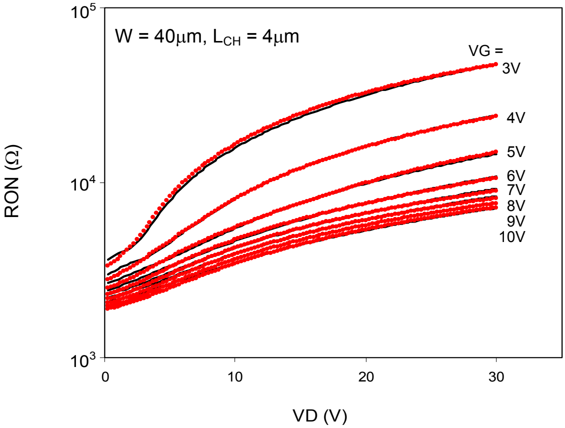
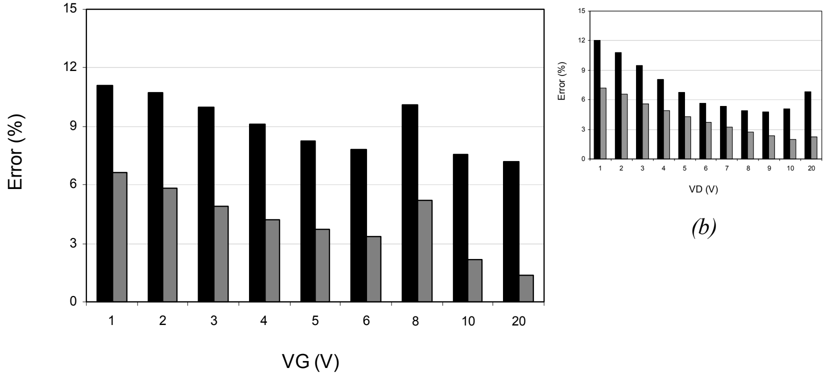


Fig. 3.48. n-channel XDMOS R_{ON}-V_D characteristics at room-temperature: measured (in red) and modeled (in black).

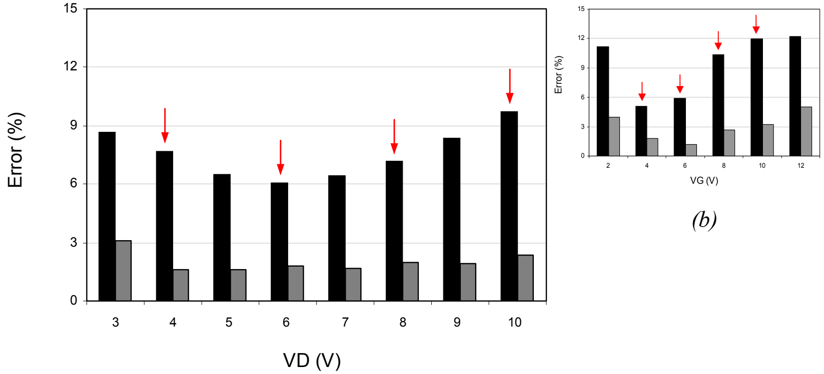
The reported model accuracy improvement in strong inversion is confirmed by plotted error percentages in Figs. 3.49 and 3.50, where the fitting improvement in term of numbers is estimated for I_D-V_G characteristics ~ 8% and for I_D-V_D characteristics ~ 12%.



(a)

(b)

Figs. 3.49. Calculated Maximum error (in black) and Mean error (in grey) between measured and modeled I_D-V_G XDMOS characteristics at room-temperature: (a) with EKV simplified current expression (data from Fig. 3.41) and (b) with BSIM macro-approach (data from Fig. 3.25).



(a)

(b)

Figs. 3.50. Calculated Maximum error (in black) and Mean error (in grey) between measured and modeled I_D-V_D XDMOS characteristics at room-temperature: (a) with EKV simplified current expression (data from Fig. 3.45) and (b) with BSIM macro-approach (data from Fig. 3.28).

3. 4. 3. Compact-Modeling Strategy

Here, the core strategy differs completely from the one reported for the macro-modeling approach with BSIM (§ 3.3.2). The proposed strategy relies essentially on the simplified and explicit form of the derived drain current expression, eq. (3.27), and which does only depend on external biasing voltages: V_S, V_D and V_G:

$$I_D = f_1\left(V_D, V_P(V_G), R_{drift}(V_D, V_G)\right) \tag{3.29}$$

From the current expression, it is possible to deduce the drift-resistance, where eq. (3.29) becomes:

$$R_{drift}(V_D, V_G) = f_2\left(V_D, V_P(V_G), I_D\right) \tag{3.30}$$

One can note that eq. (3.27) has the form of a 2nd order polynomial:

$$f(I_D) = a \cdot I_D^{\ 2} + b \cdot I_D + c \tag{3.31}$$

where, "*a*", "*b*" and "*c*" are constant terms for each combination of applied extrinsic voltages. Therefore, by considering I_D in eq. (3.30) a measured quantity (i.e. output characteristics), the current expression, eq. (3.27), can be re-formulated also in polynomial form of 2nd order:

$$f(R_{drift}) = A \cdot R_{drift}^{\ 2} + B \cdot R_{drift} + C \tag{3.32}$$

where, A, B and C depend on Known quantities: V_G, V_D and measured I_D, and thus, the bias-dependent drift-resistance can be *analytically* solved. The good agreements, illustrated in Fig. 3.51, between experimentally measured and analytically extracted R_{drift} (V_D, V_G) characteristics in terms of order of magnitude and bias dependence with V_G and V_D confirm the validity of the approach. The obtained set of drift parameters from eq. (3.32) are then re-injected in the current expression (eq. 3.29) as initial guess-values in order to perform a global fitting on the measured I-V curves.

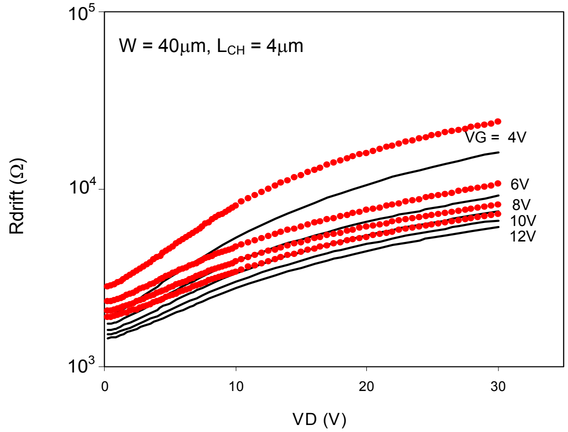


Fig. 3.51. n-channel XDMOS R_D (V_D, V_G) characteristics at room-temperature: extracted from MESDRFIT structure (in red) and modeled by eq. (3.33) (in black).

The compact-modeling strategy can be sequenced as follows:

Step-1: performing standard extrinsic I-V measurements on the HV-DMOS transistor over the desired range of investigation: I_D-V_G and I_D-V_D.

Step-2: extracting channel parameters: V_T and μ_0.

Step-3: calculating R_{drift} (V_D,V_G) characteristics according to eq. (3.33), which is the analytical solution of the 2nd order polynomial, eq. (3.32), for each couple of extrinsic V_D and V_G bias.

Step-4: fitting with the mathematical drift-expression, eq. (3.12), the calculated drift-resistance in step 3.

Step-5: injecting the drift-coefficients, together with extracted V_T and μ_0 values, in the simplified drain current expression, eq. (3.27) and final parameters optimization to fit the I-V device characteristics in strong inversion.

In case weak and moderate inversions are to be modeled, the complete "$q_{S(K)}$" expression, eq. (3.22) can be used to derive a more complex expression for the drain current. Even if complete and simplified charge expressions (eq. (3.22) and (3.23)) do not impact I-V characteristics in strong inversion as demonstrated in Figs. 3.39 and 3.40, still the optimized set of parameters from step 5 can be used as initial guess-values to extend the fit toward the subthreshold characteristic and cover all inversion regions (weak-to-strong). To keep in mind that such drain expression has an implicit form, and thus, can only be solved numerically. However, this is easily achievable in standard mathematical solvers like MathCAD, Mathematica or MatLab.

The main advantages and limitations of such approach can be summarized as follow:

Advantages: **i**- Applicable to any asymmetric MOSFET with any bias-dependent drift series resistance.

ii- Simple and fast extraction of channel parameters (only V_T and μ_0 are needed).

iii- Needs only few I_D-V_D measures at various V_G, as input values, to extract and fit the drift coefficients.

iv - A limited number of model parameters: ten in total for room-temperature model, including drift-expression coefficients.

v- Special test device with K-contact (i.e. MESDRIFT structure) is no longer needed.

vi- Able to adequately reproduces specific phenomena like quasi-saturation.

vii- To run simulations, no need to be implemented in a circuit simulator like Smartspice to run simulations; a mathematical solver is largely enough.

Limitations: Despites that all reported drawbacks for macro-modeling with BSIM have been solved: lake of accuracy in modeling the subthreshold characteristic remains the major limitation. The related term in the EKV-2.6 model for the subthreshold characteristic is the substrate factor, "γ" (eq. (3.26)), which account for the channel doping concentration, N_{Sub}. A re-adjustment from its physical value (probed from TCAD calibrated structure) could improve the fit in Fig. 3.44, but in such case, it is more appropriate to considered N_{Sub} as a tuning parameter rather than a constant technological value.

3. 5. CONCLUSION

This chapter demonstrates the usefulness of the intrinsic-drain concept (V_K-concept) for modeling purposes of high voltage devices, in general, by investigating its use in the elaboration of models for the bias-dependent drift series resistance.

Simple, yet universal **methodologies, dedicated to the experimental extraction of the drain series resistance in asymmetric HV-MOSFET's, independent on the extended drift-architecture, have been proposed and validated**.

We have particularly contributed to develop **two original approaches for the investigation and modeling of the drift series resistance of a DMOS transistor**:

(i) the first one consists in a **dedicated experimental method** that allows the extraction of a bias dependent series resistance
(ii) the second one uses a **dedicated test structure, MESDRIFT**, which enables the direct measurement of the drift series resistance, as well as **mathematical models able to fit the complex revealed dependence of R_{drift} on the gate and drain biases**.

Both methods have been validated by comparison between measured data and analytical/numerical simulations using the intrinsic drain voltage concept.

We have originally studied t**he experimental dependence of the drift series resistance in DMOS devices versus drain and gate biases** and found that R_{drift} can have very large non-linear variations (as high as four order of magnitude) depending on the values of the applied biases, which **explains why simple extensions of low voltage MOS models with constant series resistance are never able to accurately model HV devices**.

We **have developed a mathematical quasi-empirical model** using polynomial and log-exp functions for this drift resistance that is able to capture with high accuracy its evolution in various regimes of operations. **This R_{drift} elaborated model has been originally combined with a simplified version of the EKV model for the intrinsic MOS transistor** and **very accurate modeling results in terms of DC current and (trans)conductances have been obtained**. Related errors have been systematically reported.

Additional studies and modeling have involved **the temperature dependence of the drift series resistance that was successfully captured in our equations**. It is worth noting, that despite a relative low physical meaningfulness, the proposed mathematical formulation of R_{drift} offers excellent convergence and accuracy in all regions of operation being however a very interesting modeling alternative, especially in case of a single technology when scalability is not an issue.

REFERENCES

[1] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier, Y. Mourier, "*Investigation and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage,*" European Solid-State Device Research Conference (ESSDERC) 2001, pp.399 - 402.

[2] A. Ortiz-Conde, J.J. Liou, W. Wong and F.J. Garcia Sanchez, "*Simple Metod for Extracting the difference between the drain and source series resistance in MOAFETs*," Electronics Letters, Vol. 30, No. 12, 1994, p. 1013 – 1015.

[3] A. Blaum, J. Victory and C. C. McAndrew, "*A Simple Physical Extraction Method for R_D – R_S of Asymmetric MOSFETS*," International Conference on Microelectronic Test Structures (ICMTS), 1999, Vol. 12, pp. 141-146.

[4] Jan A. M. Otten and F. M. Klaassen, "*A Novel technique to Determine the Gate and Drain Bias Dependent Series Resistance in Drain Engineering MOSFET's Using One Single Device*," IEEE Transaction on Electron Device, 1996, Vol. 43, No. 9, p. 1478 - 1488.

[5] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, "*An Experimental Approach for Bias-Dependent Drain Series Resistances Evaluation in Asymmetric HV MOSFETs,*" European Solid-State Device Research Conference (ESSDERC), 2001, pp.403 - 406.

[6] C. Anghel, N. Hefyene, A.M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier and Y. Mourier, "*Physical Modelling Strategy for (Quasi-) Saturation Effects in Lateral DMOS Transistor Based on the Concept of Intrinsic Drain Voltage,*" International Semiconductor Conference (CAS), 2001, pp. 417 - 420.

[7] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, "*Bias-dependence Drift resistance Modeling for Accurate DC and AC Simulation of Asymmetric HV-MOSFET,*" International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2002, pp.203 - 206.

[8] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon and J. Rhayem, "*Universal Test Structure and Characterization Method for Bias-Dependent Drift Series Resistance of HV MOSFETs*," European Solid-State Device Research Conference (ESSDERC), 2002, pp. 247 - 250.

[9] C. Anghel, N. Hefyene, A.M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, "*Electrical Characterization of High Voltage MOSFETs Using MESDRIFT,*" International Semiconductor Conference (CAS), 2003, pp. 257 - 260.

[10] C. Anghel, A.M. Ionescu, N. Hefyene, and R. Gillon, "*New-Method for Temperature-Dependent Thermal Resistance and Capacitance Accurate Extraction in High-Voltage DMOS Transistors,*" International Electron Device Meeting (IEDM), 2003, pp. 133 – 136.

[11] C. Anghel, A.M. Ionescu, N. Hefyene, and R. Gillon, "*Self-Heating Characterization and Extraction Method for Thermal Resistance and Capacitance in High Voltage MOSFETs,*" European Solid-State Device Research Conference (ESSDERC) 2003, pp.449 – 452.

[12] C. Anghel, "*High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling*", Ph.D. Thesis No. 3116, Swiss Federal Institute of Technology, Lausanne (EPFL), Lausanne 2004.

[13] C. Y. Tsai et al., "*16-60V rated LDMOS Show Advanced Performance in a 0.72 μm Evolution BiCMOS Power Technology,*" Proceeding of Electron Devices Meeting (IEDM), 1997, pp. 367-370.

[14] T. Terashima et al., "*Multi-Voltage Device Integration technique for 0.5 μm BiCMOS and DMOS Process,*" Proceeding of the International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2000, pp. 331-334.

[15] M. Bucher, "*Analytical MOS Transistor Modeling for Analog Circuit Simulation*," Ph.D. Thesis No. 2114, Swiss Federal Institute of Technology, Lausanne (EPFL), 1999.

[16] http://legwww.epfl.ch/ekv

[17] J. M. Sallese and A. -S. Porret, "*A novel approach to charge-based non-quasi-static model of the MOS transistor valid in all modes of operation,*" Solid-State Electronics, 2002, Vol. 44, pp. 887 - 894.

[18] J. M. Sallese, M. Bucher, F. Krummenacher and P. Fazan, "*Inversion charge linearization in MOSFET modeling and rigorous derivation of the EKV compact model,*" Solid-State Electronics, Vol. 47, pp. 677 - 683, 2003.

[19] A-I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "*An Explicit Model for the Long-Channel MOS Transistor Including Small-Signal Parameters,*" Solid-State Electronics, 1995, Vol. 38, pp. 1945 - 1952.

[20] A-I. A. Cunha, M. C. Schneider and C. Galup-Montoro, "*An Explicit Model for the Long-Channel MOS Transistor Including Small-Signal Parameters,*" IEEE International Symposium on Circuits and Systems (ISCAS), 1997, pp. 1608 - 1911.

[21] N. Hefyene, J. M. Sallese, C. Anghel, A. Ionescu, S. Frere and R. Gillon, "*EKV Compact Modeling Extension for HV Lateral DMOS Transistors,*" International Conference on Advanced Semiconductor Devices and Microsystems (ASDAM), 2002, pp. 345 – 348.

CHAPTER 4

Drift resistance and AC modelling of DMOS transistor

4. 1. INTRINSIC-DRAIN VOLTAGE (V_K) CONCEPT FOR AC DMOS MODELING:

The AC modeling of HV-DMOS transistors is one the most difficult task to be achieved because of the drift-region and its contribution to the device charge control, resulting in bias-dependent capacitances. Moreover, specific phenomena related to the region, like quasi-saturation and drift pinch-off, largely contribute to raise the difficulty on capacitance modeling.

The reported analysis in chapter 2 (§ 2.3) revealed that the transition between conduction through high-resistance depleted area and conductive channel within the drift-region (see Figs. 2.11 and 2.13) is at the origin of depicted peaks from TCAD simulated intrinsic-drain voltage , V_K -V_G (Fig. 4.1), and gate-to-drain capacitance, C_{GD} -V_G (Fig 4.2), characteristics. As V_D increases, higher V_G bias is needed to compensate the depletion extends within the drift and accumulate electrons till the formation of a conductive channel beneath the gate oxide. When peak values of both characteristics are extracted and plotted together, Fig. 4.3, they show equal V_D dependence up to 60V and the slight shift between their corresponding V_G-peaks remains constant (0.75V).

This clearly confirms the strong correlation between the intrinsic potential of the DMOS transistor and its terminal capacitances (e.g. C_{GD}) and put in evidence the validity of the V_K-concept for AC modeling purposes. In this context, it becomes mandatory for the accurate modeling of device capacitances, the need of precise quantitative prediction of the V_K potential to properly estimate the drift-contribution to the total terminal capacitances. In such a way, the coherence of an over all model (DC and AC) based on the V_K-concept is maintained.

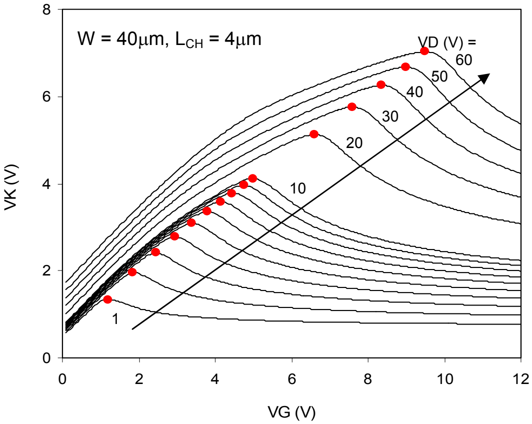


Fig. 4.1. Extracted V_K -V_G characteristics from numerically simulated n-channel XDMOS structure at various V_D biases: 1 - 10V (1V step) and 20 - 60V (10V step).

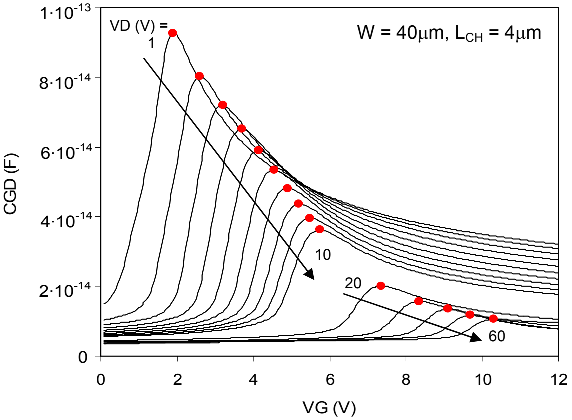


Fig. 4.2. Extracted C_{GD}-V_G characteristics from numerically simulated n-channel XDMOS structure at various V_D biases: 1 - 10V (1V step) and 20 - 60V (10V step).

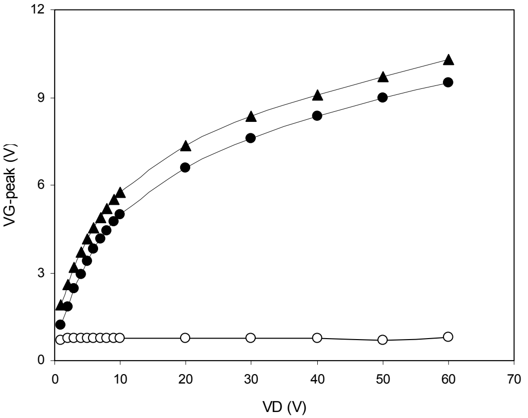


Fig. 4.3. Extracted corresponding gate biases (V_G-peak) to peak values depicted from numerically simulated n-channel XDMOS characteristics: V_K-V_G (sole circles) and C_{GD}-V_G (solid triangles). In open circles, the constant shift between both curves.

In principle, two approaches can be used for the AC modeling: (i) the *large signal* analysis (i.e. charge-partitioning approach) and (ii) the *small-signal* admittance analysis. The two approaches have been investigated through this chapter based on the monitoring of the intrinsic-drain potential, V_K. Each approach will be separately discussed in detail in the following sections.

4. 2. SMALL SIGNAL ANALYSIS:

Based on the DMOS small signal model proposed by Liu and Kuo [1] dedicated essentially to capture the quasi-saturation influence on DMOS capacitances and predict their specific peak characteristics, a simple first order model has been developed and its corresponding equivalent circuit is reported in Fig. 4.4. The principal assumption to be made is the dominance of the capacitance due to the drift-charge on the capacitance of the intrinsic-MOS drain, [1].

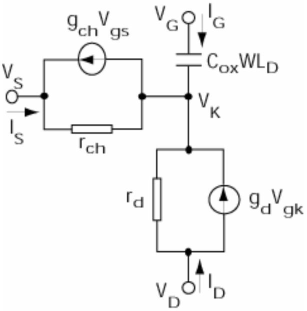


Fig. 4.4. Small signal equivalent circuit dedicated to DMOS transistor (after [1])

Such approach includes the possibility to relate reciprocal and non reciprocal gate-to-source and gate-to-drain capacitances, C_{GS}, C_{SG}, C_{GD} and C_{DG}, to intrinsic drain potential, V_K, and drift channel resistances, "r_d" and "r_{ch}". Accordingly, the following analytical expressions have been derived:

$$C_{GS} \cong \frac{\frac{r_d}{r_{ch}} + g_{ch}.r_d}{1+\left(\frac{r_d}{r_{ch}}\right)+g_d.r_d}\cdot C_{drift} \tag{4.1}$$

$$C_{GD} \cong \frac{1}{1+\left(\frac{r_d}{r_{ch}}\right)+g_d.r_d}\cdot C_{drift} \tag{4.2}$$

$$C_{SG} \cong \frac{\left(\frac{r_d}{r_{ch}}\right)\cdot\left(1+\frac{r_d}{r_{ch}}+g_{ch}.r_d\right)}{\left(1+\frac{r_d}{r_{ch}}+g_d.r_d\right)^2}\cdot C_{drift} \tag{4.3}$$

$$C_{DG} \cong \frac{(1 + g_d \cdot r_d)\cdot\left(1 + \frac{r_d}{r_{ch}} + g_{ch}.r_d\right)}{\left(1 + \frac{r_d}{r_{ch}} + g_d.r_d\right)^2}\cdot C_{drift} \qquad (4.4)$$

where,

$$r_d = \frac{V_D - V_K}{I_D} \qquad (4.5)$$

$$r_{ch} = \frac{V_K}{I_D} \qquad (4.6)$$

and “C_{drift}” is the oxide capacitance associated with the drift region (i.e. extension of the gate over drift). Since the field-plate gate electrode covers different oxide thicknesses ranging from 17nm for the gate oxide to ~ 500nm for the field oxide (LOCOS), it is important to precisely such variations. Fig. 4.5 illustrates the various oxide thicknesses to be considered for the accurate estimation of the total drift oxide capacitance term, C_{drift}.

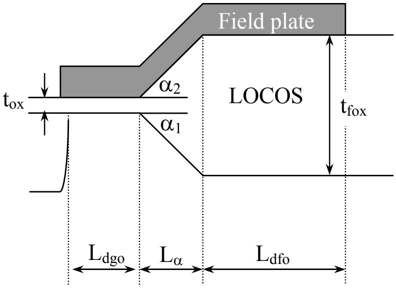


Fig. 4.5. Schematic illustration of the different oxide regions for accurate estimation of total drift oxide capacitance.

- gate oxide capacitance: $$C_{ox} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox}} \qquad (4.7)$$
- field oxide capacitance: $$C_{fox} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox} + L_\alpha \cdot (\tan(\alpha_1) + \tan(\alpha_2))} \qquad (4.8)$$
- ramped oxide capacitance: $$C_{rox} = \frac{\varepsilon_o \varepsilon_{ox}}{t_{ox} + \frac{L_\alpha}{2}(\tan(\alpha_1) + \tan(\alpha_2))} \qquad (4.9)$$

$$C_{drift} = W\left(C_{ox} \cdot L_{dgo} + C_{rox} \cdot L_\alpha + C_{fox} \cdot L_{dfo}\right) \qquad (4.10)$$

where, "L_{dgo}" is the drift length beneath the gate oxide, "L_{α}" is the drift length under the ramped gate oxide and "L_{dfp}" is the drift length beneath the field oxide (see Fig. 4.5).

The transconductance of the lateral channel-region (g_{ch}) and drift-region (g_d) are calculated as following:

$$g_{ch} = \frac{\partial I_D}{\partial V_{GS}} - \left(\frac{1}{r_{ch}}\right)\cdot\frac{\partial V_K}{\partial V_{GS}} \tag{4.11}$$

$$g_d = \left(\frac{\partial I_D}{\partial V_{GS}} + \left(\frac{1}{r_d}\right)\cdot\frac{\partial V_K}{\partial V_{GS}}\right)\cdot\left(1 - \frac{\partial V_K}{\partial V_{GS}}\right)^{-1} \tag{4.12}$$

Typical plots of the drift and intrinsic channel transconductances, g_d and g_{ch}, respectively, are reported in Fig. 4.6.

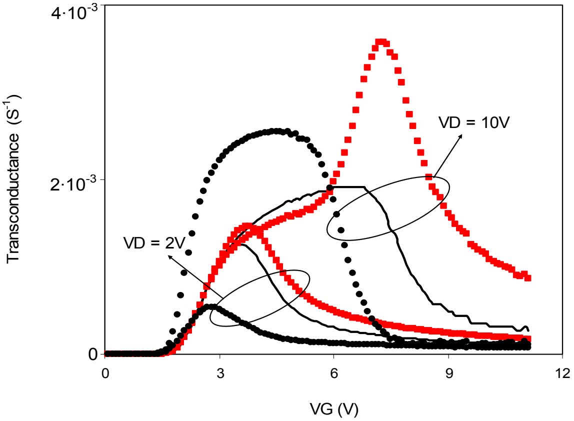


Fig. 4.6. Drift and intrinsic channel transconductances, g_d (black symbols) and g_{ch} (red symbols), calculated using eq. (4.11) and (4.12), respectively, for two different drain voltages, in case of XDMOS. Also reported in this figure: the (extrinsic) XDMOS transconductance, $g_m=dI_D/dV_G$ (solid line).

Systematic AC numerical simulations with the numerically simulated n-channel XDMOS TCAD structure have been conducted by applying a small signal on the gate electrode (10mV, 1MHz), in all the regions of operation described by static bias combinations (V_D, V_G). At each bias point, the C_{SG} and C_{DG} capacitances have been extracted by Silvaco's ATLAS simulator, [2]. From DC numerical simulations, the values of V_K potential and its first order derivative dV_K/dV_G, at each bias point (V_D, V_G), needed for r_d, g_d, r_{ch}, g_{ch} calculations in the small-signal model, have been directly probed near the intrinsic channel end, drift side. Calculated C_{SG}, C_{DG} capacitances are respectively reported in Figs. 4.7 and 4.8 and compared with extracted values from AC numerical simulations. The reasonable agreement between calculated capacitances with derived expressions, eq. (4.11) and (4.12), and numerical simulations supports the claim that, with the proposed capacitance model, it is possible to predict the peaks observed in HV-DMOS capacitances (which is the typical signature of the evolution of the drift depleted regions, onset of quasi-saturation and lateral doping profiles, [3]), as well as the capacitance evolution with V_D and V_G.

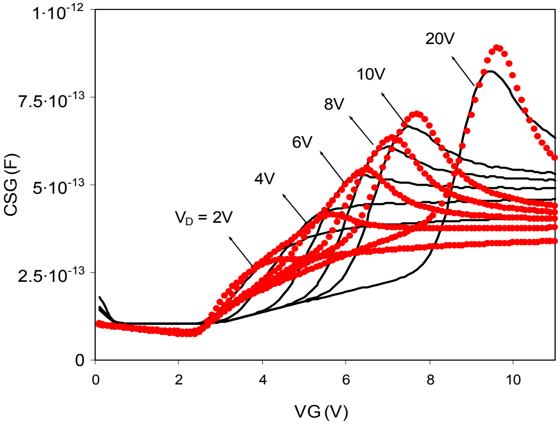


Fig. 4.7. n-channel XDMOS C_{SG}-V_G characteristic: numerically simulated (in red) and calculated with eq. (4.3) (in black).

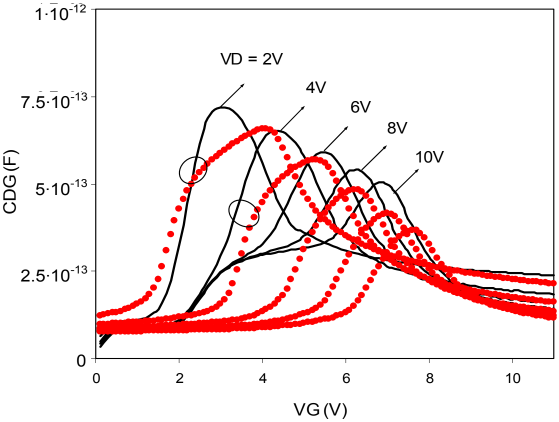


Fig. 4.8. n-channel XDMOS C_{DG}-V_G characteristic: numerically simulated (in red) and calculated with eq. (4.4) (in black).

4. 3. LARGE SIGNAL ANALYSIS:

The large signal analysis or charge partitioning is the most difficult because it necessitates precise estimation of the variable drift-controlled charge with V_G and V_D (see circuit model in Fig. 4.9). Therefore, accurate prediction of intrinsic-drain potential, V_K, is mandatory

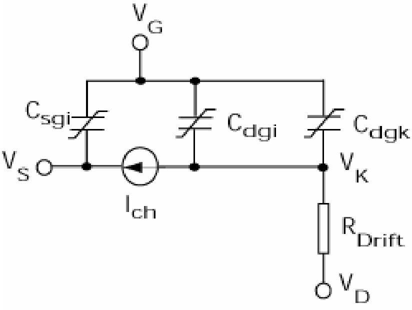


Fig. 4.9. Possible large signal circuit model for HV-DMOS device illustrating variable capacitances corresponding to charge partitioning (after [1]).

4. 3. 1. Drift-Region Modeling with Charge-based Approach:

The proposed model is based on a geometrical charge modeling approach, inspired by the reported modeling works in [4-6]. According to the applied couple of external biases (V_G and V_D), an accumulation layer takes place within the drift region, essentially localized beneath the gate oxide, while a fixed charge is induced by the depletion of the p-i-n diode (i.e. body-drift junction) and the combination of both charges consist the total charge of the drift region.

The description of the proposed charge-based model, in term of parameters, derived expressions and validation will be presented respectively as follow:

4. 3. 1. 1. Key constants and technological parameters: The most common physical constants used by model equations are:

- ε_o = 8.84×10^{-12} (F/cm)
- ε_{ox} = 3.9
- ε_{si} = 11.9
- **q** = 1.6×10^{-19} (C)
- **K** = 1.38×10^{-23} (J/K)
- **T** = 300 (K)
- n_i = 1.45×10^{10} (cm^{-3})

All technological and geometrical parameters related to the investigated DMOS structure and to be used as model inputs are listed in table 4.1.

Parameter name in Spice	Value	Unit	Description	Type of parameter
d_{NWELL}	5.34×10^{-6}	m	diffusion depth of drift region (n-well)	DC/AC
L_{dgo}	2×10^{-6}	m	drift length beneath the gate oxide	DC/AC
L_{α}	0.663×10^{-6}	m	drift length beneath the ramped oxide	DC/AC
L_{dfp}	2×10^{-6}	m	drift length beneath the **f**ield **p**late	AC
L_{dfo}	8.3×10^{-6}	m	drift length beneath the **f**ield **o**xide	DC/AC
W	40×10^{-6}	m	device width	DC/AC
t_{ox}	43×10^{-9}	m	gate oxide thickness	DC/AC
N_A	2×10^{-22}	cm^{-3}	body (channel) region doping	DC/AC
N_D	2.5×10^{-21}	cm^{-3}	drift region doping	DC/AC
$V_{FB\text{-}drift}$	-0.23866	V	flat-band potential of drift region	DC/AC
α_1	$\pi/7.2$	-	ramped oxide angle_1	DC/AC
α_2	$\pi/9$	-	ramped oxide angle_2	DC/AC

Table. 4.1. Geometrical and technological parameters used in the calculation of the HV-DMOS drift-charge.

4. 3. 1. 2. Fitting parameters: A limited number of fitting parameters have been introduced to the model equations in order to deliver a degree of flexibility and allowing fine tuning during parameter optimization step on reference data (measured or numerically simulated as it will be the case here). The fitting parameters are:

- θ: this term corresponds to the current *spreading angle* in the drift region beneath the gate oxide. It accounts for the physically monitored current path when living the channel region and entering the drift region. When channel accumulation beneath the gate oxide within the drift is formed, the current follows the interface and thus the spreading angle is expected to be close to zero. In contrast, when depletion is only presents, numerical simulation indicates that the current flow lines are not longer following the interface, but tend to flow across the drift-depletion. Here the spreading angle is to be considered.
  Typical range of values: $0 < \theta < \pi/3$.

- **F_{QD}**: it is the charge sharing factor, which accounts for the fact that the total depleted drift-charge is partially associated to the gate electrode.
  Typical range of values: $0 < F_{QD} < 1$.

- **n_a**: fitting parameter for *depleted area smoothing* functions, fa_1, fa_2 and fa_3.
  Typical range of values: $1 < n_a < 200$

- **n_s**: fitting parameter for the *charge transition smoothing* function, fs.
  Typical range of values: $1 < n_s < 10$

- **f_l**: fitting parameter for the *depletion charge modulation under the gate oxide*. It accounts essentially for the adjustment of the gate oxide length within the drift (L_{dgo}) and its associated charges. It could be considered as a geometrical tuning parameter.
  Typical range of values: $0 > f_l \geq 1$

Due to the non-uniform oxide thickness (see Fig. 4.5) within the drift-region, the associated oxide capacitance to each drift-sub-region is calculated according to eq. (4.7), (4.8) and (4.9) (see § 4.2).

4. 3. 1. 3. Drift-charges: Based on the analysis reported in chapter 2, it has been demonstrated the presence of an accumulation channel tends to form beneath the gate oxide (and to some extent under the ramped oxide) when the gate terminal is biased to high voltage values (typically around 9-12V). At low V_G values, the drift-region under the gate oxide is depleted at relatively low V_D bias (see Figs. 2.11.a and 2.13.a), and therefore, no accumulation is expected to takes place and the only charge present within the drift will be due to the depleted area.
The approach on which is based the drift-charge estimation can be summarized as follow: calculate separately each charge and define a boundary condition that determines the presence or not of each charge type. The boundary condition is defined by the *depletion boundary potential*, PHI_d, which corresponds to the potential at the end of the drift-depletion near interface, as illustrated in Figs. 4.10 – 4.13 (will be discussed in next section, § 4.3.1.4).

(i) *Accumulation drift-charge*: The derived expression to account for associated charge to the channel-accumulation beneath the drift gate oxide is:

$$Q_{drift-acc} = -W \cdot \left(V_G - V_{FB-drift} - PHI_d\right) \cdot \left(C_{ox} \cdot f_l \cdot L_{dgo} + C_{rox} \cdot L_{\alpha} + C_{fox} \cdot L_{dfo}\right) \quad (4.13)$$

(ii) *Depletion drift-charge***:** A drift-portion is associated to each oxide-region underneath the field plate (i.e. $A_1 \Rightarrow$ gate oxide, $A_2 \Rightarrow$ ramped oxide and $A_3 \Rightarrow$ field oxide) and the depletion charge of portion is individually calculated according to the extension of the depleted boundary (i.e. t_{dep} value) as illustrated in Figs. 4.10 – 4.13. The associated depleted areas to each oxide region are calculated according to the depletion boundary extension, which is calculated by the DC-model as follow:

$$t_{dep} = \sqrt{\frac{2\varepsilon_o\varepsilon_{si}}{q}\left[\frac{N_A}{N_D\left(N_A + N_D\right)}\right]\left[V_{bi} + PHI_d\right]} \quad (4.14)$$

where, "V_{bi}" is the *built-in potential* of the body-drift (p-n) junction and is calculated according to:

$$V_{bi} = \frac{K \cdot T}{q} \cdot \ln\left(\frac{N_A \cdot N_D}{n_i^2}\right) \tag{4.15}$$

According to the depletion boundary extension, t_{dep}, within the drift-region, different cases are considered:

Case (a)**:** when the depletion boundary covers partly the drift-region beneath the gate oxide (i.e. $t_{dep} \leq L_{dgo}$) as illustrated in Fig. 4.10.

$$A_{1\text{-}a} = \frac{1}{2} t_{dep} \cdot \left[2 \cdot d_{NWELL} - t_{dep} \cdot \tan(\theta)\right] + t_{dep} \cdot \left[f_1 \cdot L_{dgo} - t_{dep}\right] \tag{4.16}$$

$$A_{2\text{-}a} = L_\alpha \times t_{dep} \tag{4.17}$$

$$A_{3\text{-}a} = L_{dfo} \times t_{dep} \tag{4.18}$$

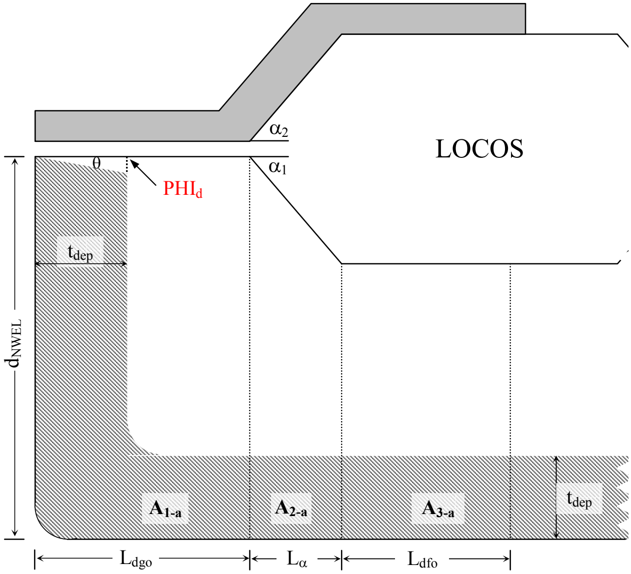


Fig. 4. 10. Schematic illustration of the drift-depletion extension depleted (assured area) under the boundary condition: $t_{dep} < L_{dgo}$

Case (b): when the depletion boundary covers completely the drift-region beneath the gate oxide and partly the region under the ramped gate oxide (i.e. $L_{dgo} < t_{dep} \leq (L_{dgo} + L_{\alpha})$) as illustrated in Fig. 4.11.

$$A_{1\text{-}b} = \frac{1}{2} f_1 \cdot L_{dgo} \times \left[2 \cdot d_{NWELL} - f_1 \cdot L_{dgo} \cdot \tan(\theta) \right] \tag{4.19}$$

$$\begin{aligned} A_{2\text{-}b} = {} & \frac{1}{2} \left[t_{dep} - f_1 \cdot L_{dgo} \right] \times \left[2 \cdot d_{NWELL} - 2 \cdot f_1 \cdot L_{dgo} \cdot \tan(\theta) - \left(t_{dep} - f_1 \cdot L_{dgo} \right) \cdot \tan(\alpha_1) \right] \\ & + \left[f_1 \cdot L_{dgo} + L_{\alpha} - t_{dep} \right] \times t_{dep} \end{aligned} \tag{4.20}$$

$$A_{3\text{-}b} = A_{3\text{-}a} = L_{dfo} \times t_{dep} \tag{4.21}$$

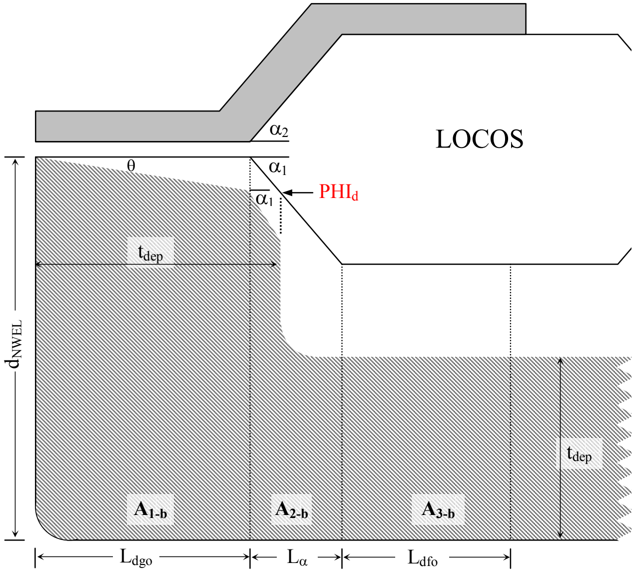


Fig. 4. 11. Schematic illustration of the drift-depletion extension depleted (assured area) under the boundary condition: $L_{dgo} < t_{dep} \leq (L_{dgo} + L_{\alpha})$.

Case (c)**:** when the depletion boundary extends within the drift-region beneath the field oxide (i.e. $(L_{dgo} + L_{\alpha}) < t_{dep} < (L_{dgo} + L + L_{dfo})$) as illustrated in Fig. 4.12

$$A_{1\text{-}c} = A_{1\text{-}b} = \frac{1}{2} f_1 \cdot L_{dgo} \times \left[2 \cdot d_{NWELL} - f_1 \cdot L_{dgo} \cdot \tan(\theta)\right] \tag{4.22}$$

$$A_{2\text{-}c} = \frac{1}{2} L_{\alpha} \times \left[2 \cdot d_{NWELL} - 2 \cdot f_1 \cdot L_{dgo} \cdot \tan(\theta) - L_{\alpha} \cdot \tan(\alpha_1)\right] \tag{4.23}$$

$$\begin{aligned} A_{3\text{-}c} = {} & \left[t_{dep} - f_1 \cdot L_{dgo} - L_{\alpha}\right] \times \left[d_{NWELL} - f_1 \cdot L_{dgo} \cdot \tan(\theta) - L_{\alpha} \cdot \tan(\alpha_1)\right] \\ & + \left[f_1 \cdot L_{dgo} + L_{dfo} - t_{dep}\right] \times t_{dep} \end{aligned} \tag{4.24}$$

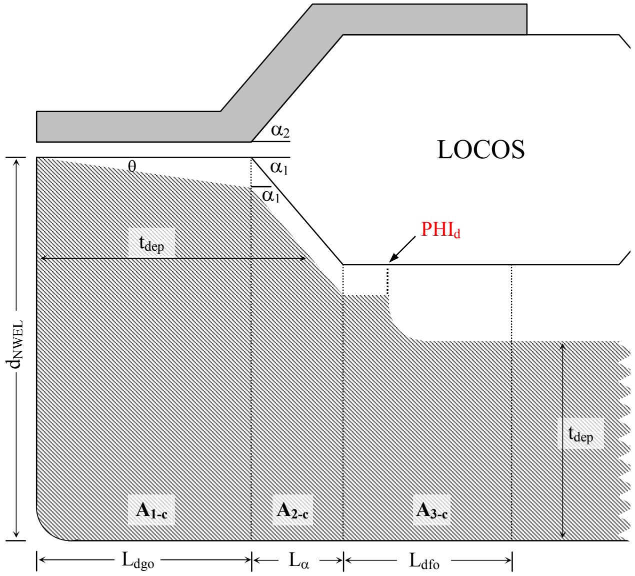


Fig. 4. 12. Schematic illustration of the drift-depletion extension depleted (assured area) under the boundary condition: $(L_{dgo} + L_{\alpha}) < t_{dep} < (L_{dgo} + L_{\alpha} + L_{dfo})$.

Case (d): when the depletion boundary covers the whole drift-region under the field-plate (i.e. $t_{dep} \geq (L_{dgo} + L_{\alpha} + L_{dfo})$) as illustrated in Fig. 4.13.

$$A_{1\text{-}d} = A_{1\text{-}b} = A_{1\text{-}c} = \frac{1}{2} f_1 \cdot L_{dgo} \times \left[2 \cdot d_{NWELL} - f_1 \cdot L_{dgo} \cdot \tan(\theta)\right] \tag{4.25}$$

$$A_{2\text{-}d} = A_{2\text{-}c} = \frac{1}{2} L_{\alpha} \times \left[2 \cdot d_{NWELL} - 2 \cdot f_1 \cdot L_{dgo} \cdot \tan(\theta) - L_{\alpha} \cdot \tan(\alpha_1)\right] \tag{4.26}$$

$$A_{3\text{-}d} = f_1 \cdot L_{dfo} \times \left[d_{NWELL} - f_1 \cdot L_{dgo} \cdot \tan(\theta) - L_{\alpha} \cdot \tan(\alpha_1)\right] \tag{4.27}$$

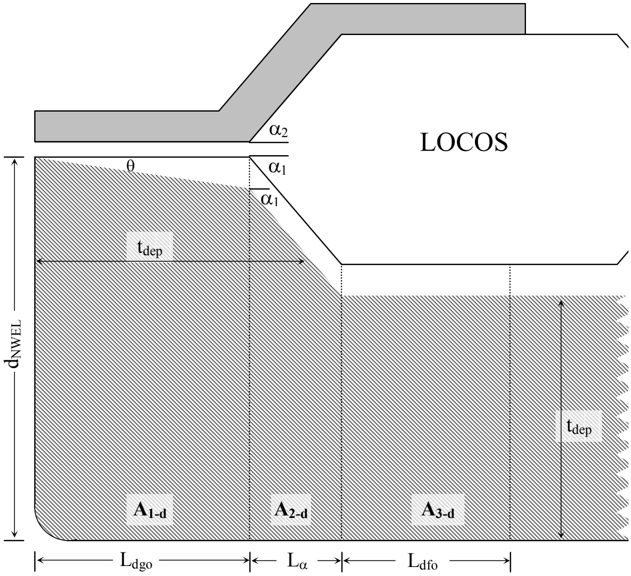


Fig. 4. 13. Schematic illustration of the drift-depletion extension depleted (assured area) under the boundary condition: $t_{dep} \geq (L_{dgo} + L_{\alpha} + L_{dfo})$.

In order to avoid any step-transition during at the different boundary conditions, a smoothing function is introduced at each defined boundary condition and resulting in three transition expressions, i.e. *fa₁*, *fa₂* and *fa₃*:

$$fa_1 = \frac{\exp\left(\frac{t_{dep} - f_1 \cdot L_{dgo}}{t_{dep} + 0.00001} \cdot n_a\right)}{\exp\left(\frac{t_{dep} - f_1 \cdot L_{dgo}}{t_{dep} + 0.00001} \cdot n_a\right) + 1} \tag{4.28}$$

$$fa_2 = \frac{\exp\left(\frac{t_{dep} - \left(f_1 \cdot L_{dgo} + L_\alpha\right)}{t_{dep} + 0.00001} \cdot n_a\right)}{\exp\left(\frac{t_{dep} - \left(f_1 \cdot L_{dgo} + L_\alpha\right)}{t_{dep} + 0.00001} \cdot n_a\right) + 1} \tag{4.29}$$

$$fa_3 = \frac{\exp\left(\frac{t_{dep} - \left(f_1 \cdot L_{dgo} + L_\alpha + L_{dfo}\right)}{t_{dep} + 0.00001} \cdot n_a\right)}{\exp\left(\frac{t_{dep} - \left(f_1 \cdot L_{dgo} + L_\alpha + L_{dfo}\right)}{t_{dep} + 0.00001} \cdot n_a\right) + 1} \tag{4.30}$$

When combining together with the different area expressions:

$$A_1 = \boldsymbol{fa_1} \cdot A_{1\text{-}b} + (1 - \boldsymbol{fa_1}) \cdot A_{1\text{-}a} \tag{4.31}$$

$$A_2 = \boldsymbol{fa_2} \cdot A_{2\text{-}c} + (1 - \boldsymbol{fa_2}) \cdot [\boldsymbol{fa_1} \cdot A_{2\text{-}b} + (1 - \boldsymbol{fa_1}) \cdot A_{2\text{-}a}] \tag{4.32}$$

$$A_3 = \boldsymbol{fa_3} \cdot A_{3\text{-}d} + (1 - \boldsymbol{fa_3}) \cdot [\boldsymbol{fa_2} \cdot A_{3\text{-}c} + (1 - \boldsymbol{fa_2}) \cdot A_{3\text{-}a}] \tag{4.33}$$

The sum of A_1, A_2 and A_3 constitutes the total depleted surface, from which is calculated the drift-depletion charge:

$$Q_{drift-dep} = W \cdot q \cdot N_D \cdot F_{QD} \cdot \left(A_1 + A_2 + A_3\right) \tag{4.34}$$

4. 3. 1. 4. Total drift charge: The total drift charge is calculated according to the defined boundary condition, PHI_d (depletion boundary potential), when compared to the surface potential ($V_G - V_{FB\text{-}drift}$) value.

(i) When $PHI_d < (V_G - V_{FB\text{-}drift})$, accumulation takes place beneath the gate oxide and because of the high density of the accumulated carriers ($>10^{18}$ cm^{-3}), the much smaller fixed charge due to the depleted surface can be neglected. Therefore, the total drift-charge is equivalent to the charge of the accumulated channel beneath the gate oxide.

$$Q_{\text{drift-tot}} = Q_{\text{drift-acc}} = -W \cdot (V_G - V_{FB-\text{drift}} - PHI_d) \times (C_{ox} \cdot f_l \cdot L_{dgo} + C_{rox} \cdot L_\alpha + C_{fox} \cdot L_{dfo}) \qquad (4.13)$$

(ii) When $PHI_d \geq (V_G - V_{FB\text{-drift}})$, accumulation channel beneath the gate oxide does not longer exist and the total drift-charge is only due to the fixed charge of the drift-extended depletion region.

$$Q_{\text{drift-tot}} = Q_{\text{drift-dep}} = W \cdot q \cdot N_D \cdot F_{QD} \cdot (A_1 + A_2 + A_3) \qquad (4.35)$$

In order to avoid any step-transition, the transition between the two regimes is achieved in a smooth way using a similar expression to the used one for the transition between the different depletion boundaries, eq. (4.28 - 4.30)).

$$f_s = \frac{\exp\left(\dfrac{PHI_d - (V_G - V_{FB\text{-drift}})}{PHI_d + 0.00001} \cdot n_s\right)}{\exp\left(\dfrac{PHI_d - (V_G - V_{FB\text{-drift}})}{PHI_d + 0.00001} \cdot ns\right) + 1} \qquad (4.36)$$

Combined with eq. (4. 16) and (4. 34), the final drift-charge expression in accumulation and depletion regimes is:

$$Q_{\text{drift-tot}} = f_s \cdot Q_{\text{drift-dep}} + (1 - f_s) \cdot Q_{\text{drift-acc}} \qquad (4.37)$$

4. 3. 2. AC DMOS Modeling with BSIM3v3:

The charges associated to each external node are obtained by putting together the calculated total drift charge and the intrinsic MOS charge, (calculated with BSIM) according to the charge conservation principles (see Fig. 4.14).

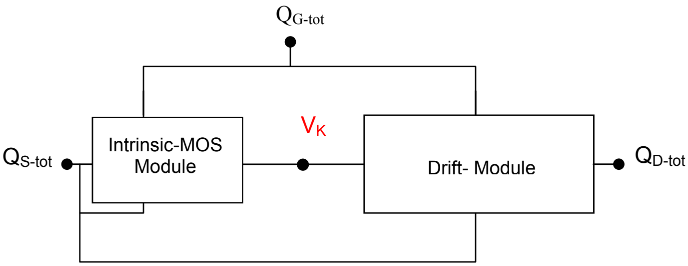


Fig. 4.14. Illustration of a possible large signal circuit model for HV-DMOS device.

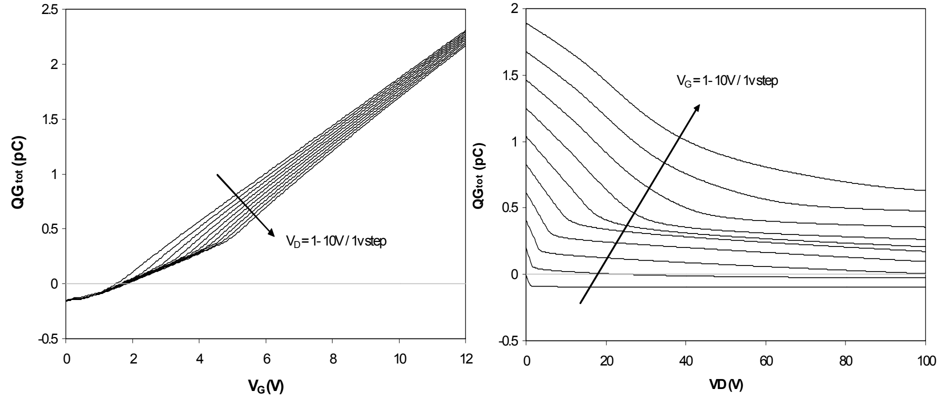
According to the charge conservation principle the total charges on the extrinsic gate, drain and source terminals are deduced as follow:

$$Q_{G\text{-}tot} = -\,Q_{drift} + Q_{Gi} = -\,Q_{drift} - Q_{Si} - Q_{Di} \tag{4.38}$$

$$Q_{D\text{-}tot} = Q_{Di} + Q_{drift} \tag{4.39}$$

$$Q_{S\text{-}tot} = Q_{Si} \tag{4.40}$$

where: "$Q_{G\text{-}tot}$" is the total extrinsic gate-node charge, "$Q_{D\text{-}tot}$" is the total extrinsic drain-node charge, "$Q_{S\text{-}tot}$" is the total extrinsic source-node charge, and "Q_{Si}" is the intrinsic MOS source charge (BSIM calculated) and "Q_{Di}" is the intrinsic MOS drain charge (BSIM calculated).



(a) (b)

Figs. 4. 15. Extrinsic gate charges calculated with eq. (4. 40): (a) Q_G-V_D @ # V_G and (b) Q_G-V_G @ # V_D and characteristics for an n-channel XDMOS device (W=40um).

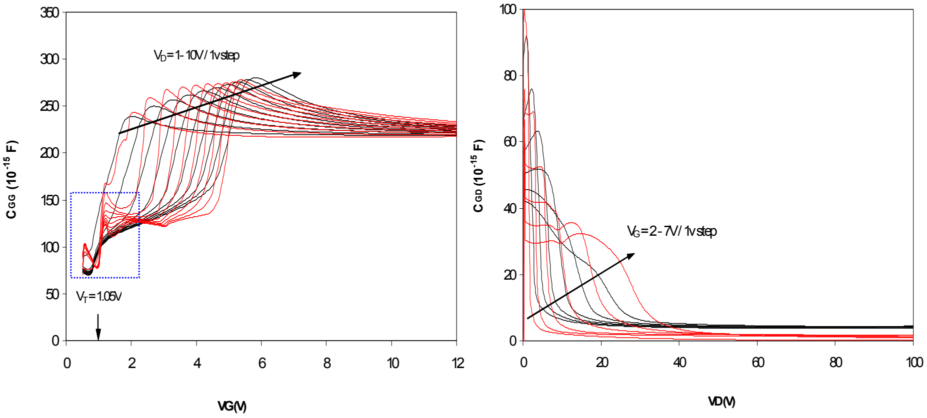
Figs. 4.15 (a and b) represent the modelled total charge seen from the gate electrode (i.e. on the gate node). As it can be seen from both characteristics, by increasing the V_G potential, the accumulation charge rises and the more negative it will be, the more positive will be the total charge seen from the gate side (i.e. Q_G rises with V_G). In the opposite, as V_D rises for a given V_G, the depletion boundary moves toward the drain and leads to an increased depletion charge. The more will it be, the more negative will be the total charge seen from the gate (i.e. Q_G drops with V_D).

Capacitances are numerically calculated according to the following definition:

$$C_{ij} = \begin{cases} \dfrac{-\partial Q_i}{\partial V_j} \rightarrow & i \neq j \\ \\ \dfrac{\partial Q_i}{\partial V_j} \rightarrow & i = j \end{cases} \tag{4. 41}$$

Derived AC model expressions have been implemented in the circuit Smart-spice simulator (using Verilog-A code) together with the developed accurate DC analytical model proposed by C. Anghel [4] in order to able the accurate prediction of intrinsic-drain potential (V_K) and depletion boundary potential (PHI_d).

A primary optimized set of parameters (see table 4.2) has been achieved in order to demonstrate the model capability to reasonably predict the capacitance behaviour of the investigated device (i.e. n-channel XDMOS transistor). 2D-numerically simulated capacitances have been performed and used to validate the implemented model expressions. Figs. 4.16 (a and b) represent respectively the gate-to-gate, C_{GG}-V_G, and gate-to-drain, C_{GD}-V_D, characteristics. Fig. 4.16 (a) illustrates the very good agreement obtained for C_{GG}-V_G characteristics, where the specific capacitance peak and its evolution with external biases is well reproduced. However, the model still needs further improvements in order to eliminate the *glitches* appearing in the weak inversion region (see doted box). This is possible by a more appropriate smoothing function (eq. 4.36) for the transition of the gate charge from accumulation-to-depletion inversion.



(a) (b)

Figs. 4.16. 2D-numerically Simulated (in black) and vs. model (in red) characteristics: (a) C_{GG}-V_G @ # V_D and (b) C_{GD}-V_D @ # V_G for an n-channel XDMOS device (W=40um).

Here are listed the intrinsic BSIM3v3 capacitance parameters and their corresponding values used to fit numerically simulated characteristics in Figs. 4.16 (a and b). Fig. 4.17 reports on the good matching between calculated (modeled) and the experimentally extracted C_{GD}-V_D characteristics at room temperature using a different set of optimized model parameters.

BSIM model	Value	AC model	Value	DC model	Value
CGS0	5×10^{-10} F/m	Theta	$\pi/8$	Tranz	9
CGD0	8.51×10^{-10} F/m	n_a	200	martor	25
CGB0	1×10^{-10} F/m	n_s	0.25		
CGSL	1×10^{-10} F/m	f_l	0.75		
CGDL	1×10^{-11} F/m	F_{QD}	0.7		
CF	1×10^{-11} F/m				
CJ	1×10^{-10} F/m				
CJSW	3.97×10^{-10} F/m				
CJSWG	5×10^{-10} F/m				

Table. 4.2. Set of parameters used to generate the different charge and capacitance characteristics in Figs. 4.15 and 4.16.

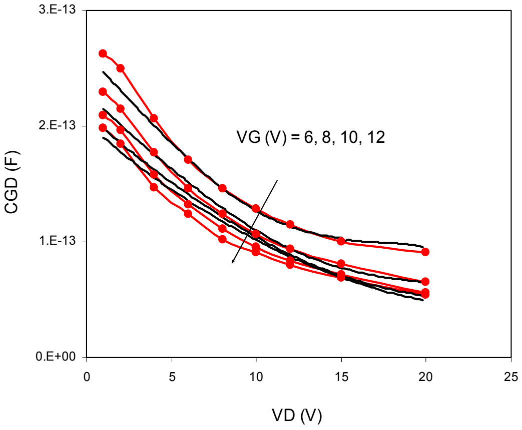


Fig. 4.17. C_{GD}-V_D @ # V_G: modelled with BSIM (in black) vs. measures (in red) for n-channel XDMOS device (W=40um).

4. 3. 3. AC DMOS Modeling with EKV (Long-Channel Approximation):

In this approach, the derived DC compact-expression for the drain current, eq. (3.17), has been used together with the proposed based-charge model expression (4.37). The intrinsic-drain potential, V_K has been predicted through the analytically extracted R_{drift} (V_D, V_G) characteristics, illustrated in Fig. 3.41.

Concerning the intrinsic-MOS (channel) charges, derived expressions in EKV 2.6 model [7, 8] has been used for the approximation of intrinsic source and drain charges, q_{Di} and q_{Si}. The exploited expressions are:

$$q_{Di} = -n(V_P)\cdot\left(\frac{4}{15}\cdot\frac{3\chi_r^3 + 6\chi_r^2\chi_f + 4\chi_f^2\chi_r + 2\chi_f^3}{(\chi_r + \chi_f)^2} - \frac{1}{2}\right) \tag{4.42}$$

$$q_{Si} = -n(V_P)\cdot\left(\frac{4}{15}\cdot\frac{3\chi_f^3 + 6\chi_f^2\chi_r + 4\chi_r^2\chi_f + 2\chi_r^3}{(\chi_r + \chi_f)^2} - \frac{1}{2}\right) \tag{4.43}$$

where, $$\chi_r = \sqrt{\frac{1}{4} + i_r} \tag{4.44}$$

and $$\chi_f = \sqrt{\frac{1}{4} + i_f} \tag{4.45}$$

and $n(V_P)$ is the slop factor as defined by eq. (3.25).

Following the same procedure as for BSIM, the estimated intrinsic-MOS charges are combined with calculated drift-charge according to expressions (3.42) and (3.43). By deriving the resulting total gate-charge with respect to the drain bias, dQ_G/dV_D, It has been possible to estimates the gate-to-drain capacitance, the most relevant capacitance characteristics in DMOS transistors.

Fig. 4.18, reports on the achieved fit on measured C_{GD}-V_D characteristics. The range of order and general trend are reasonably predicted; as V_G rises, the capacitance decreases as the measured curves. However, with V_D bias the model shows less dependence and tends to saturate around 12V, while the measured characteristics still drops. This is essentially due to the use of simplified intrinsic MOS charge expressions, where the main purpose here is to demonstrate the feasibility and validity of the approach using EKV; It is certain that accuracy can be improved using a complete EKV model for the intrinsic transistor. However, the use of the eq. (3.22) instead of eq. (3.23) (or a more advanced version of EKV) does not guarantee a full analytical compact model with explicit current expression.

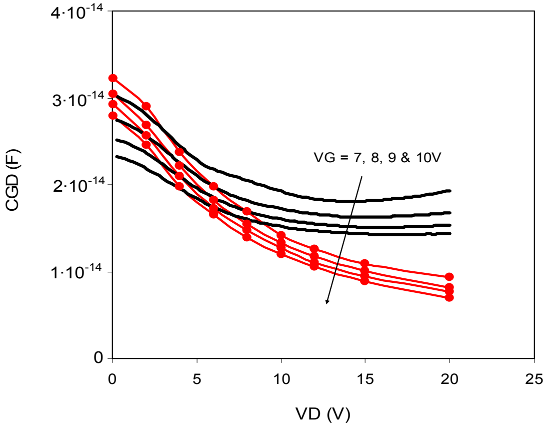


Fig. 4.18. C_{GD}-V_D @ # V_G: modelled with EKV (in black) vs. measures (in red) for n-channel XDMOS device (W=40um).

4. 4. CONCLUSION

This chapter was addressed to the AC modelling of HV DMOS transistors and demonstrate the validity of the intrinsic drain voltage concept. We reported on two approaches for AC modeling: **small signal** and **large signal** modeling.

For the small signal modeling, the derived model expressions revealed the following features:

- its capability **to reproduce the specific peak characteristic of the DMOS capacitance and acceptably predict its values and variation with extrinsic Biases (V_G, V_D)**.
- it is **free of fitting parameters** and do only necessitate the monitoring of few inputs (i.e. V_K, I_D, V_D and V_G).
- it clearly demonstrated **for asymmetric MOSFET's, that non-reciprocal capacitances differs from the reciprocal one**, and therefore, should be carefully considered.
- Simple and straight-forward.

For the large signal modeling, we proposed a geometrically charge-based approach for the modeling of the drift-charge, which accounts for channel-accumulation formation under the drift gate oxide and depletion extension within the drift region, where:

- in strong inversion, model expressions are able **to well reproduce the specific peak characteristics of the simulated DMOS capacitance and predict its variation with external biases**. This is valid also when compared to experimental data where a good matching is reported.
- a limited number of parameters are introduced and most of them have a physical origin.
- **the use of transition functions in the model build-up to that eliminated the use of IF-statements**, which could generate discontinuities and convergence problems.

The EKV compact-expression, when combined with the AC charge model for the drift, **demonstrated its ability to reproduce the general trend and range of order of the experimentally extracted gate-to-drain capacitance**, which confirms once more the potential of the approach toward accurate AC-DC modeling of HV-DMOS transistors.

Finally, **the coherence of an overall model based on the K-point is maintained, demonstrated and validated.**

REFERENCES

[1] C. M. Liu and J. B. Kuo, "*Quasi-Saturation Capacitance Behavior of a DMOS Device,*" IEEE Transaction on Electron Device, 1997, Vol. 44, No. 7, PP. 1117 – 1123.

[2] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, "*Bias-dependence Drift resistance Modeling for Accurate DC and AC Simulation of Asymmetric HV-MOSFET,*" International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 2002, pp.203 - 206.

[3] C. Anghel, N. Hefyene, A.M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier and Y. Mourier, "*Physical Modelling Strategy for (Quasi-) Saturation Effects in Lateral DMOS Transistor Based on the Concept of Intrinsic Drain Voltage,*" International Semiconductor Conference (CAS), 2001, pp. 417 - 420.

[4] C. Anghel, "*High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling*", Ph.D. Thesis No. 3116, Swiss Federal Institute of Technology, Lausanne (EPFL), Lausanne 2004.

[5] Y. Chung, "*Semi-Numerical Static Model for Nonplanar-Drift Lateral DMOS Transistor,*" IEE Circuit Devices Systems, 1999, Vol. 146, No. 3, pp. 139 – 147.

[6] Y. Chung, "LADSPICE-1.2: A *Nonplanar-Drift Lateral DMOS Transistor Model and its Application to Power IC TCAD,*" IEE Circuit Devices Systems, 2000, Vol. 147, No. 4, pp. 219 – 227.

[7] http://legwww.epfl.ch/ekv

[8] M. Bucher, "*Analytical MOS Transistor Modeling for Analog Circuit Simulation*," Ph.D. Thesis No. 2114, Swiss Federal Institute of Technology, Lausanne (EPFL), 1999.

CHAPTER 5

Hot Carrier Impact on the Capacitances of DMOS Transistors and Reliability Issues

5. 1 INTRODUCTION

The continuous improvements in HV DMOSFET's performances in terms of high-power and/or high-voltage capabilities allowed modern integrated circuits (IC's) issued from smart power technologies to provide real breakthrough in a variety of applications ranging from simple applications like dc-dc voltage converters to more complex utilities like power management, telecommunications (mobile phones), automotive safety equipments (like car airbags) or more recently multimedia products (like flat-panel displays) [1-4]. In such integrated circuits, Lateral DMOS transistors are so far the candidate of choice as driver transistors. This is due essentially to their compatibility and easy integration with standard and submicron CMOS processes, [5, 6].

The degradation of DMOS induced by Hot-Carriers (HC) remains a major concern in many applications. For example, in power management and RF-applications the LDMOS acts essentially as a switch between the On-state (high V_G and low V_D) and Off-state (low V_G and high V_D). During transient-state when both V_G and V_D meet at high values, HC degradation is expected to take place. Therefore, a gradual "wear-out" of the device is expected at frequent operations in the transient-state. Another example is in automotive applications where the blocking requirement is of primary concern. HV devices connected directly to the battery, must survive the load dump condition with it's transients of 40 to 60V, despite the nominal operating range of 12V, a condition which may force a device to breakdown or forward bias a junction and turning on a parasitic bipolar transistor. Both examples show that in practical HV transistors face critical situations under certain circumstances which exceed the normal working conditions and which might cause severe damages till total device failure. Here comes the importance of studying and experiment the effect of these "critical" conditions on the HV device and its electrical behaviour. Such specific investigations are so called *aging* or *stress* measurements, part of the *reliability* field, a well established science and of primary importance for the microelectronic industry.

Surprisingly, most of published works concerning HC effects are limited to the electrical static (DC) aspect of the device degradation, while the capacitive (AC) aspect has simply been ignored with the exception of few publications, and this is not only valid for HV DMOS transistors [7] but as well for standard MOSFET's, however some more exploration has been carried out for these last ones [8-12]. As a best proof, one could observe that the Safe-Operating-Area (SOA) concept, widely used by microelectronic manufacturers as reference guide for life-time estimation of their products, only relies on DC estimations [13-16] and no systematic importance is given to the AC part. We then believe that it is timely to dedicate a significant effort to the evaluation of HC on AC characteristics (capacitances) of HV devices, aspect which is detailed in this chapter, in close comparison with the conventional DC parameter degradation induced by DC stress.

The chapter presents a detailed investigation of different specific electrical stress conditions and their impacts on the electrical behaviours of an n-channel LDMOS transistor at ambient and elevated temperatures with a special focus on the terminal device capacitances. It is worth to note that of all terminal capacitances of a DMOS, the gate-to-drain, C_{GD}, is the most important one since it acts as a *Miller* capacitance during device operation. This capacitance becomes even more critical in applications where LDMOS transistors are used as fast switches at high-frequency and is the focus point of our work.

5. 2. DEVICE ARCHITECTURE

The structure under investigation is an n-channel Lateral DMOS transistors issued from the AMI Semiconductor 0.7µm CMOS compatible smart-power technology able to deliver a high-voltage capability of 100V on the drain. The gate oxide thickness is estimated to be 43 nm, which limits the maximum safe operating voltage on the gate to 12V. To ensure an accurate capacitance extraction, through S-parameter technique, a multi-finger RF-architecture is selected. The experimental device features six fingers and a channel length of 1µm with a total width of 240 (6×40) µm. The pitch distance between Aluminium contact pads is fixed to ~135 µm and all measured devices have shorted source and channel body as illustrated in Fig. 5.1.

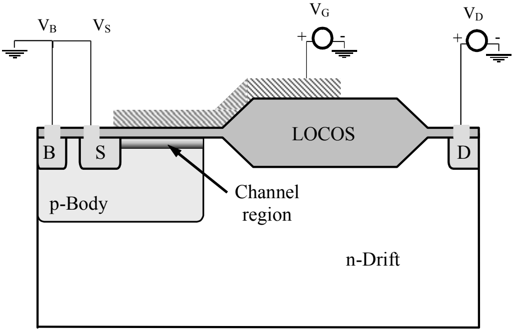


Fig. 5.1. Schematic illustration of the investigated n-channel Lateral DMOS structure.

5. 3. EXPERIMENTAL SETUP

The experiment has been carried out using a CASCADE probe station for On-wafer measurements, a parameter analyzer HP-4156 equipped with a pulse generator expansion unit HP-41501B, delivering high-voltage capabilities for stress analysis and electrical characterization and a VNA (Vector Network Analyser) HP-8719D for S-parameters acquisition. Tungsten RF probes with a GSG (Ground-Source-Ground) configuration are used to inject the mixed DC and AC signal to the device through a T-bias. Such configuration allows, with the same set-up connections, injecting either a DC voltage (sourced from the parameter analyser) for device stressing and DC characterization or a DC signal superposed by an AC signal (sourced from the VNA) when S-parameters measurement are performed. All equipments are computer controlled through a GPIB interface. Figs. 5.2 and 5.3 show respectively top-views of the RF and DC-probing configuration used in the proposed experimental work and a zooming on the RF-probes positioning with respect to a wafer-die under investigation.

5. 4. STRESS CONDITIONS

DC stressing as a HC characterization technique could be classified into two main categories according to the type of applied signal: (i) stressing at constant current or (ii) stressing at constant voltage biases. In our investigation we selected DC stress at constant voltage biases since it is so far the more commonly used one and very well documented in related literature.

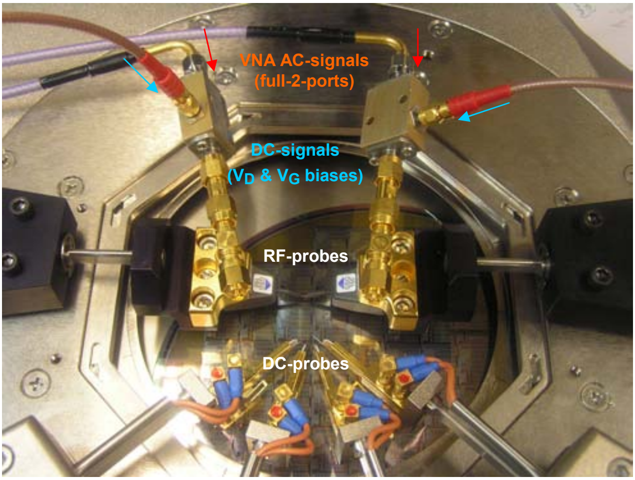


Fig. 5.2. Top-view of RF and DC-probes configuration used in the experimental investigation of n-channel LDMOS devices.

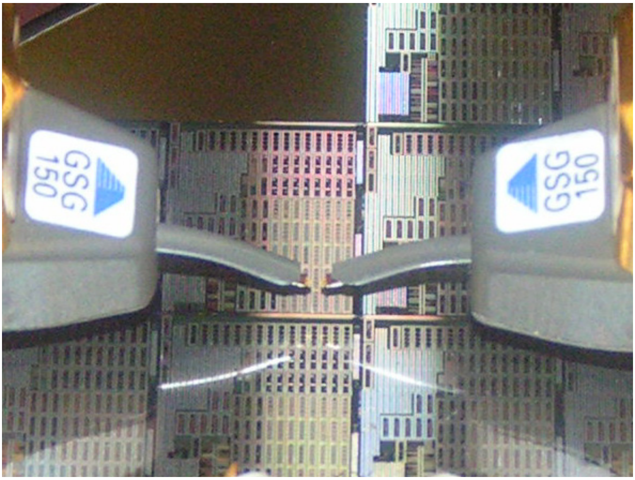


Fig. 5.3. Zoom on RF-probes during on-wafer characterization.

Referring to the state-of-the-art of Hot-carriers characterization in DMOS transistors [17-19] two different DC-stress voltage conditions were applied separately on identical devices.

5. 4. 1. Stress-A

Stress A is performed with **maximum drain voltage** and **gate voltage corresponding to the maximum body current** (see Fig. 5.2). This stress condition is commonly used in standard hot-carrier investigation for low-voltage MOSFET's [20-23], where the generated hot carriers are proportional to the body current (and then, maximized when it reaches its maximum) ; thus, this is the main source to create electrical damages and degradations under such conditions.

5. 4. 2. Stress-B

Stress B is performed with **maximum drain voltage and maximum gate voltage,** which corresponds to maximum device biases (restricted by design). Table 5.1 summarizes the two listed stress conditions corresponding to our devices.

Stress type	Node	Bias (V)	Stressing condition	T (°C)
A	V_D	100	Maximum drain biases ($V_{D\text{-}max}$)	25
	V_G	5.2	V_G @ maximum body current ($I_{B\text{-}max}$)	
B	V_D	100	Maximum drain bias ($V_{D\text{-}max}$)	
	V_G	12	Maximum gate bias ($V_{G\text{-}max}$)	

Table 5.1. Values of selected stress bias conditions.

5. 5. DC ANALYSIS OF HOT CARRIER DEGRADATION

DC analysis of effects induced by DC stress at room temperature has been performed before and after incremental series of stress cycles, typically 10Ksec/cycle. The analysis consists of recording the transfer characteristic I_D-V_G at low drain voltage and output characteristics I_D-V_D at various gate voltages before and after incremental series of stress cycles, typically 10Ksec per cycle, and from which are extracted the most relevant electrical parameters: threshold voltage V_T, sub-threshold slope S, interface states density D_{it}, low-field mobility μ_0, ON-resistance at V_G = 12V in linear (R_{ON}-*lin* , V_D = 100mV) and saturation (R_{ON}-*sat*, V_D = 50V) modes of operation. Table 5.2 summarizes quantitatively the bias conditions at which was performed the DC characterization as well as the extracted electrical parameters.

Measure	V_D (V)	V_G (V)	Extracted parameters	T (°C)
I_D-V_D	0 → 50	6, 12	R_{ON}-sat	25-100
I_D-V_G	0.1	0 → 12	V_T, μo, S, D_{it}, R_{ON}-lin	

Table 5.2. DC analysis, biasing values and most relevant electrical parameters extracted.

5. 6. AC ANALYSIS OF HOT CARRIER DEGRADATION

Following each incremental cycle of stress an AC analysis has been carried out, consisting of an S-parameters measurement at variable biases and covering a specific frequency range (RF). This technique was selected in order to allow a precise and accurate extraction of device capacitances. The most relevant DMOS capacitances are then extracted [5.5.a-d] through an implemented routine in a mathematical solver, Matlab. As mentioned in (§ 5.1) all devices featuring a multi-finger RF-architecture have shorted body to source, limiting the possible capacitances extraction to only $C_{GS}+C_{GB}$ and C_{GD}. However, this does not limit their usefulness in the achieved hot-carrier investigation as it will be demonstrated further in this chapter. Table 5.3 tabulates the measurement conditions at which S-parameters technique was achieved and the resultant extracted capacitances.

Measure	V_G (V)	V_D (V)	AC signal (mV)	Freq. (GHz)	Extracted Parameters	T (°C)
S -V_G	-6 → 10	0, 6, 20	10	0.5 – 2.5	C_{GD} $C_{GS}+C_{GB}$	25-100

Table 5.3. Measuring conditions of performed S-parameters evaluation and extracted device capacitances.

It is worth to mention that the device manufacturer, AMI Semiconductor Belgium, use identical techniques for capacitance extraction as part of its on-wafer electrical characterization procedure.

5. 7. PARAMETER EXTRACTION

We present in this section a short know-how on the extraction methodology used to obtain the different electrical parameters and characteristics listed in tables 5.2 and 5.3 respectively.

5. 7. 1. DC parameters:

The electrical parameters considered in our investigation are those usually used to evaluate electrically any field-effect transistor. The extraction methodology exploits the I_D-V_G characteristic performed at low V_D (100mV in our case) to ensure the extraction of the more significant device parameters in the linear regime. The parameters are: threshold voltage V_T, and low-field mobility μ_0, following the *Ghibaudo* technique [24] as well as subthreshold swing, S, from which is deduced the variation in the interface states density ΔD_{it}.

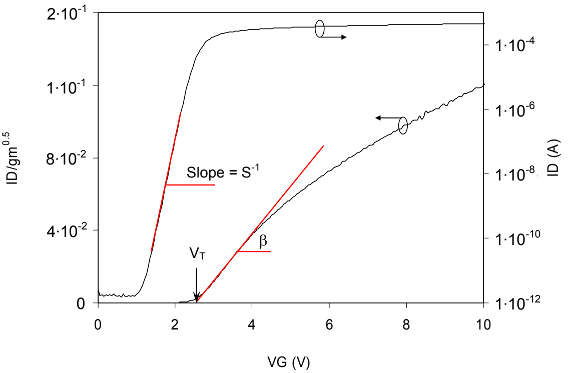


Fig. 5.4. Log I_D and $(I_D/gm^{0.5})$ vs. V_G characteristics used to extract the different electrical parameters.

The technique consists of plotting the ($I_D/gm^{0.5}$)-V_G characteristic as illustrated in Fig. 5.4. From the slope of the linear portion of the curve, the mobility is calculated using eq. (5.1) and from its intersection with the V_G-axis, the threshold voltage is obtained. This method minimizes first order source and drain series resistances and thus allows the extracting the intrinsic parameters values of the device, so-called channel parameters. The subthreshold swing *S* is determined from the inverse of the slope that covers at least two decades of the log I_D-V_G characteristic in the weak inversion region (see Fig. 5.4). From the extracted S value, D_{it} is straight forward calculated using eq. (5.2); however in term of relevance, ΔD_{it} appears more appropriate as it point-out any substantial generation of interface states due to electrical stressing. Therefore eq. (5.3) is rather useful than eq. (5.2).

$$\mu_0 = \frac{\beta^2}{\left(\frac{W}{L_{ch}}\right) \cdot V_D \cdot C_{ox}} \tag{5.1}$$

$$D_{it} = \left(\frac{S}{2.3\left(\frac{kT}{q}\right)} - \left(1 + \frac{C_{dep}}{C_{ox}}\right) \right) \frac{C_{ox}}{q} \tag{5.2}$$

$$\Delta D_{it} = \frac{\Delta S}{2.3\left(\frac{kT}{q}\right)} \cdot \frac{C_{ox}}{q} \tag{5.3}$$

where: $C_{Si} = \varepsilon_{Si}\varepsilon_0 / t_{dep}$, $C_{ox} = \varepsilon_{ox}\varepsilon_0 / t_{ox}$, $kT/q \approx 26\ \text{mV}$

and t_{dep} corresponds to the thickness of the depletion layer in strong inversion.

5. 7. 2. AC characteristics:

"AC characteristics" term denotes the device capacitances on which the AC analysis was essentially based. The, gate-to-drain, C_{GD}, and the gate-to-source coupled with gate-to-body, $C_{GS}+C_{GB}$, capacitances have been obtained through S-parameters measurement technique at the measurement conditions listed in table 5.3.

This paragraph details the procedure and the successive steps to be followed in order to extract capacitance characteristics from S-parameters data.

(i) **Experimental set-up check**: first of all and before performing any measurement, a routine check on the configured setup should be done to ensure that each apparatus delivers the correct output signal to the DUT and all equipments are able to communicate through the GPIB interface.

(ii) **Probe planarization**: Planarization could be defined as the ability to ensure all contacts to be at the same height. Probe tips planarity is verified through a simple visual inspection of the left marks on a *Contact Substrate*, a dedicated Alumina surface covered by a thin gold film.

(iii) **Full 2-port calibration**: In order to know precisely what is measured all errors up to the probe tips must be removed, including internal VNA errors and cables (see Fig. 5.5). This is achieved through a full 2-port calibration technique so-called *Line-Reflect-Reflect-Match (LRRM)* [25-27] implanted in WinCal® software from CASCADE Microtech® [28]. Multiple repeated patterns of short-load-thru standards are available on the *Impedance Standard Substrate (ISS)* calibration kit together with alignment marks for a proper probes separation setting [29]. The LRRM calibration has been performed over the frequency range of 50 MHz and up to 5 GHz to ensure a good stability phase during DUT measurements.

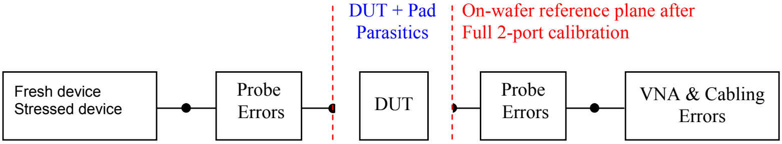


Fig. 5.5. Schematic illustration of the on-wafer reference plane after full 2-port calibration.

(iv) **De-embedding**: After calibration, the reference measurement plane is at probe tips. Therefore, the measured signal is the response of the device associated with the pad parasitics. For this purpose dummy structures are used in order to get rid of all parasitic elements [30-33]. In our case, all transistors have been be-embedded following the *Open Pad De-embedding (OPD)* technique [34], a simple and widely used method which consist of removing the dominant parasitic component (pad capacitances) using an Open dummy structure (see Fig. 5.6). This is confirmed by AMI Semiconductor, the LDMOS manufacturer, where de-embedded DMOS transistors using only Open dummy structures are comparable with those de-embedded with Open, Short and Thru dummy structures for frequencies bellow 5 GHz. Below Note that Open de-embedding is performed at $V_G = V_D = 0V$ [35].

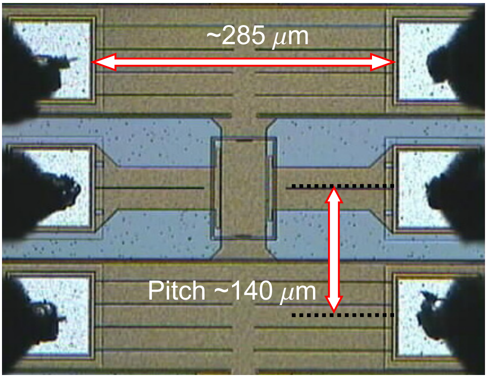


Fig. 5.6. Top-view of Open dummy structure used for the Open Pad De-embedding.

(v) **DUT measurement**: All LDMOS transistors have been measured over the frequency range of 0.5-1.5 GHz for each couple of V_G and V_D biases (see table 5.3), allowing extraction of device capacitances at different frequencies. The 1 GHz frequency was selected as an average range value. Fig. 5.7 shows a top view of a n-channel LDMOS transistor and its contact pads; as it can be seen the device failed during stress measurement (~60Ks of cumulative stress-time).

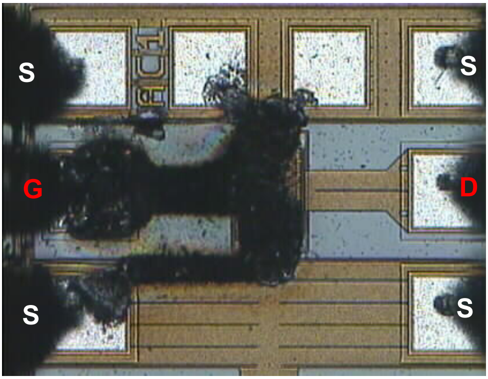


Fig. 5.7. Top view on characterized n-channel LDMOS transistor subject to failure.

(vi) **S- to Y-parameters**: In order to remove parasitics due to contact pads, Open dummy and device S-parameters are converted to Y-parameters through the set of expressions (5.4), (5.5), (5.6) and (5.7) [36]. Only then the open-dummy Y-parameters are subtracted from the total device Y-parameters, resulting to the DUT Y-parameters (see Fig. 5.7) as expressed in eq. (5.8).

$$Y_{11} = \frac{(1-S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}}{(1+S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}} \tag{5.4}$$

$$Y_{12} = \frac{-2\cdot S_{12}}{(1+S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}} \tag{5.5}$$

$$Y_{21} = \frac{-2\cdot S_{21}}{(1+S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}} \tag{5.6}$$

$$Y_{22} = \frac{(1+S_{11})\cdot(1-S_{22})+S_{12}\cdot S_{21}}{(1+S_{11})\cdot(1+S_{22})+S_{12}\cdot S_{21}} \tag{5.7}$$

$$Y_{DUT} = Y_{Total} - Y_{Open} \tag{5.8}$$

(vii) **Y_{DUT}-parameters to Device Capacitances**: Device capacitances are straight forward obtained from the de-embedded Y-parameters according to the following formula:

$$C_{GD} = -\frac{\mathrm{Im}(Y_{12})}{2\pi f} \tag{5.9}$$

$$C_{GS} + C_{GB} = -\frac{1}{2\pi f \cdot \mathrm{Im}\left(\frac{1}{Y_{11} + Y_{12}}\right)} \tag{5.10}$$

with $f = 0.7\times10^9$ Hz

Fig. 5.8 illustrates the complete flowchart of the capacitance extraction procedure used in our investigation.

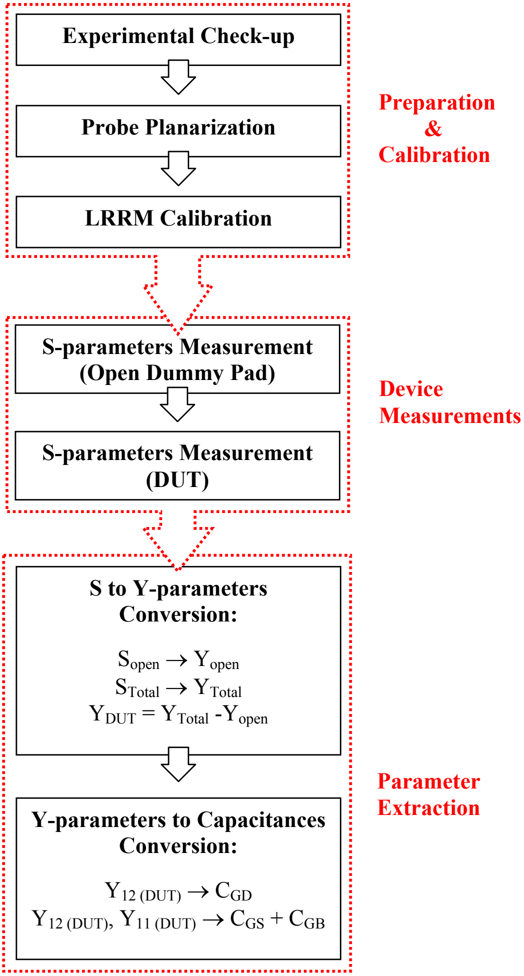


Fig. 5.8. Flowchart of the capacitance extraction procedure used in our work.

5. 8. DMOS GATE CAPACITANCES

Before any discussion related to the hot-carrier impact on the DMOS capacitances, it would be more useful to first have a close view on the atypical characteristics of the n-channel LDMOS subject to our investigation. As mentioned several times all devices have shorted source and body terminals, therefore only coupled C_{GS} and C_{GB} (C_{GS}+C_{GB}) and C_{GD} characteristics could be extracted.

5. 8. 1. Gate Capacitance at $V_D = 0V$:

The typical DMOS capacitances C_{GS}+C_{GB} and C_{GD} characteristics versus V_G extracted at V_D = 0V are shown in Fig. 5.9. For clarity, three main regions are indicated:

In ***region (A)***, where $V_G > V_{FB}$, a hole layer is formed in the intrinsic channel due to accumulation and in the drift region beneath the gate oxide due to inversion oxide as its flat-band voltage is negative ($V_{FB\text{-}Drift}$ ~ -0.5V, extracted from numerical simulated structure calibrated on real device). As for standard CMOS transistors, this is typically characterized by a plateau appearing at negative gate bias on the C_{GB} or C_{GS}+C_{GB} characteristic.

In ***region (B)***, where $V_{FB\text{-}Ch} < V_G$ (> V_T), the non-uniform lateral doping profile of the channel induced by the double-diffusion process shows a maximum near source side of ~7.7×10^{16} cm^{-3} and gradually drops along the channel to reach at its end ~1.2×10^{15} cm^{-3} near the body-drift junction (see Fig. 5.10).

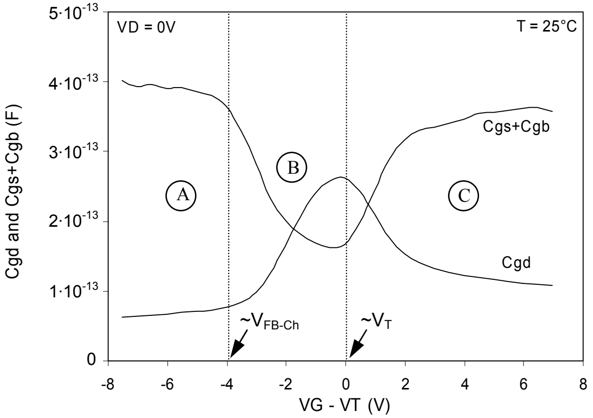


Fig. 5.9. Measured C_{GD} and C_{GS}+C_{GB} vs. V_G-V_T characteristics for an n-channel LDMOS transistor at zero drain bias.

Such configuration causes a gradual V_T along the channel where the portion near its end goes to inversion before the portion near the source side. It is important to notify that the V_T of the device is the one at which the channel is completely inverted, and therefore it is determined by the highest local V_T (near source-side).

As V_G rises, the channel goes from hole-accumulation to depletion and $C_{GS}+C_{GB}$ capacitances drops from its plateau value as it can be seen in Fig. 5.9 while, the drift part turns to accumulation and gives rise to an electron layer beneath the gate oxide since $V_{FB\text{-}Drift}$ is negative. This is depicted by the sharp increase in C_{GD} which accounts only for the electron charge of the drift zone as most of the channel is in depletion. However, in the sub-threshold region even if less sharp, C_{GD} keeps rising despite the complete formation of the electron layer in the drift due to accumulation. This is explained by the fact that when V_G increases the channel is progressively inverted starting from the low-threshold region at the channel-end.

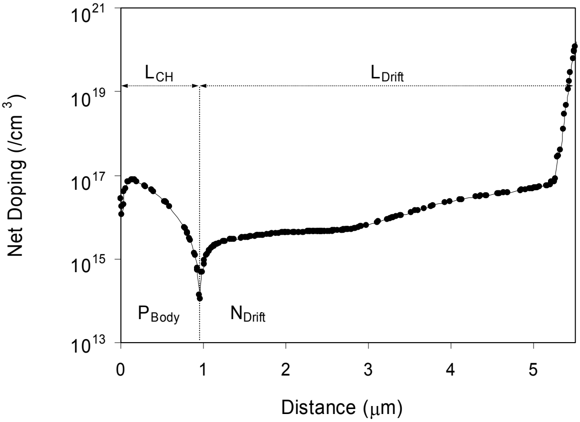


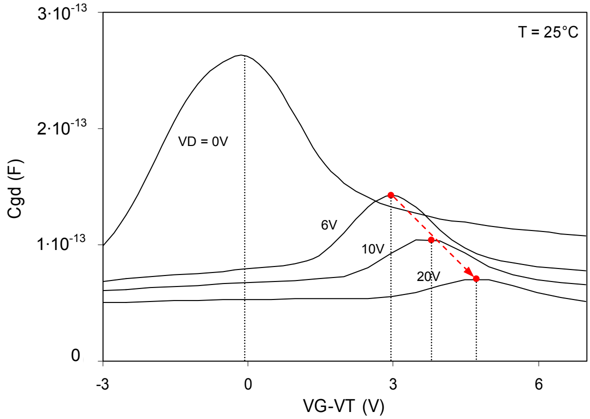
Fig.5. 10. Net doping profile distribution beneath the Si/SiO$_2$ interface extracted from 2D numerical simulation of n-channel LDMOS structure calibrated on real device.

Due to its intimate adjacency to the accumulated drift layer, the rising charge of the channel-end with V_G contributes to the total charge amount of the drift [37-39]. At this point there is no charge transfer between the source and drain terminals and C_{GD} accounts essentially for the accumulated electron charge in the drift as well as the inverted portion of the channel-end. C_{GD} exhibits a well defined maximum when $V_G = V_T$, indicating the entire channel is inverted.

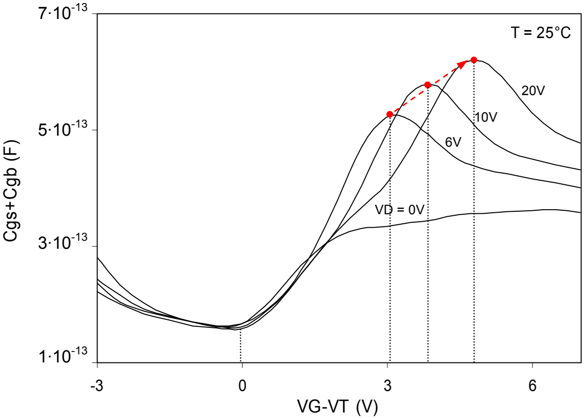
In ***region (C)***, where $V_G > V_T$, the whole channel is in strong inversion, $C_{GS}+C_{GB}$ rises, while C_{GD} drops as the source terminal starts providing a substantial share of the charge to the device channel.

5. 8. 2. Gate Capacitance at $V_D > 0V$:

As the drain voltage moves from the zero bias to higher values, a unique and specific phenomenon proper to DMOS transistors is observed. First, the $C_{GS}+C_{GB}$ versus V_G characteristic exhibits a peak well above the plateau level for $V_D = 0V$ (Fig. 5.11.a), which coincide with those depicted from the C_{GD} versus V_G curves (Fig. 54.11.b); second, as V_D increases, both $C_{GS}+C_{GB}$ and C_{GD} maximums shift positively respectively to higher and lower values (Figs. 5.11, red symbols). It is explained by the fact that as V_D is raised, a higher gate bias is needed to compensate the extended depletion within the drift and accumulate electrons till the formation of a conductive channel beneath the gate oxide.



(a)



(b)

Figs. 5.11. Measured gate capacitances characteristics at room-temperature for an n-channel LDMOS transistor at different V_D biases ranging from zero to 20V, (a) C_{GS} +C_{GB} vs. V_G-V_T; (b) C_{GD} vs. V_G-V_T.

5. 9. HOT-CARRIER DEGRADATION AT ROOM TEMPERATURE

In this section, the degradation of the DC and AC characteristics of post-stressing n-channel Lateral DMOS transistors at room temperature and their correlation with the biases conditions (see table 5.1) will be reported and discussed. It is worth to mention that the presented results and analysis have been performed over a number of twenty dies. Fig. 5.12 illustrates the position of each investigate die as well as its location in the wafer.

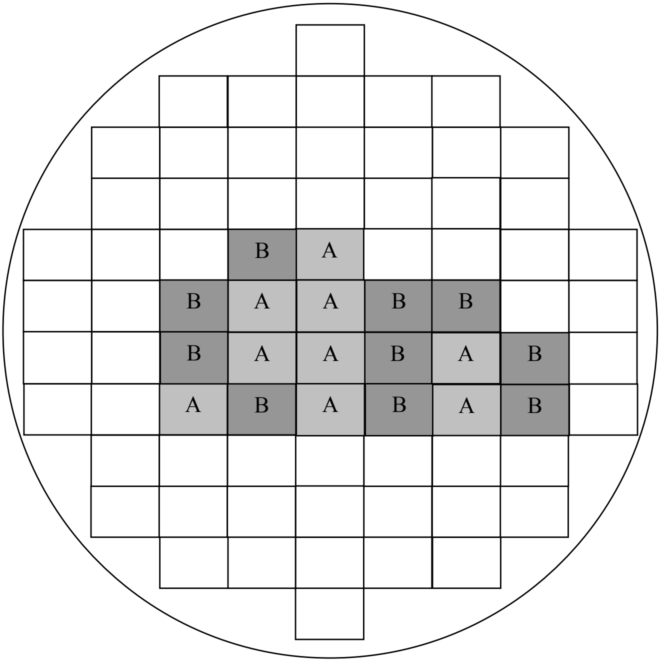


Fig. 4.12. Wafer mapping of stressed dies at room-temperature and the bias conditions applied to each one of them; stress-A: $V_G = 5.2V$ & $V_D = 100V$ and stress-B: $V_G = 12V$ & $V_D = 100V$.

5. 9. 1. DC HC-degradation Analysis at Room Temperature:

As detailed previously (§ 5.3), two different stress conditions have been selected in our investigation according to the state-of-the-art in hot-carrier characterization, where **stress-A** ($V_G = 5.2V$ and $V_D = 100V$) stands for V_G at which the maximum body current I_B is generated for V_D maximum (Fig. 5.13) and **stress-B** ($V_G = 12V$ and $V_D = 100V$) stands for the maximum V_G and V_D biases allowed by design. Fig. 5.13 shows the $I_{B\text{-max}}$ characteristic versus V_G at various V_D and to avoid eventual device failure near breakdown (V_{BR} ~104V), the applied drain voltage has been limited up to 80 volts.

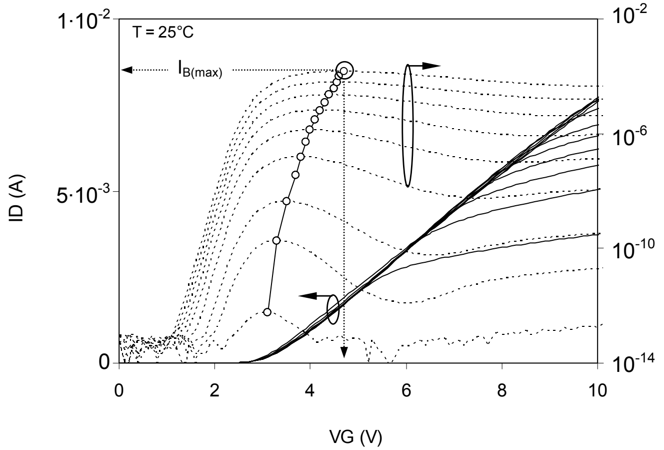


Fig. 5.13. Measured I_B and I_D vs. V_G characteristics for different V_D (up-to 80V). The solid symbols shows $I_{B(max)}$ values and their corresponding gate voltage, V_G-$I_{B(max)}$.

The induced degradation by applying **stress-A** up to 50Ks on the transfer (I_D-V_G and g_m-V_G) and output (I_D-V_D and R_{ON}-V_D) characteristics are presented respectively in Fig. 5.14 and 5.15. Only a slight drop in the maximum transconductance g_{max} and transfer and output drain current level can be depicted, as well for the sub-threshold characteristics (log I_D-V_G, Fig. 5.14) and the ON-resistance (log R_{ON}-V_D, Fig. 5.15) remain almost unchanged.

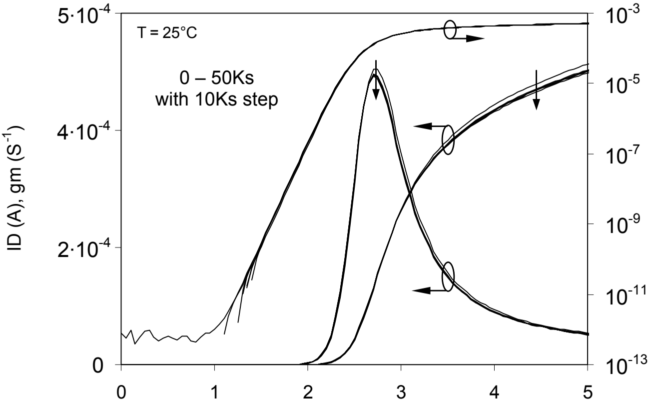


Fig. 5.14. Room temperature g_m and I_D vs. V_G characteristics measured at low V_D (100mV) in linear and log scales for a 50Ks stress-A (V_G = 5.2V & V_D = 100V) duration at 10Ks stress intervals.

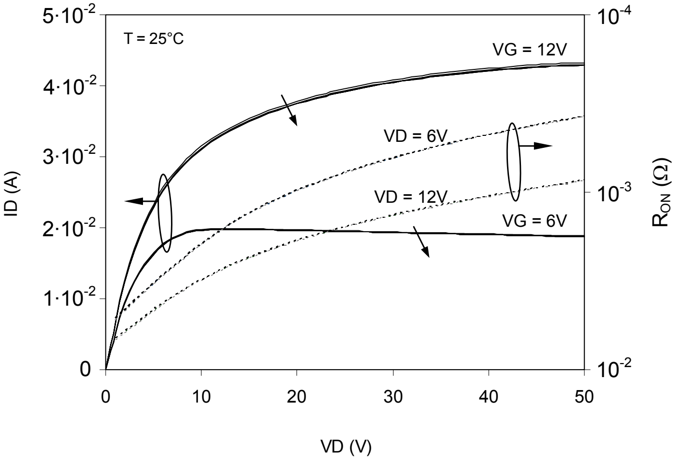


Fig. 5.15. Room temperature I_D-V_D (solid line) and R_{ON}-V_D (dashed line) measured characteristics for V_G = 6 and 12V for a 50Ks stress-A (V_G = 5.2V & V_D = 100V) duration at 10Ks stress intervals.

In the opposite when stress-B is applied for an equal cumulated stress-time, a positive shift in the subthreshold characteristic as well as a net drop in g_{max} and transfer characteristics are depicted from Fig. 5.16. The monitoring of I-V suggests a major degradation *within the early stage* of stress-B, where after the first 10Ks of stressing a large degradation is already taking place in both transfer and output characteristics.

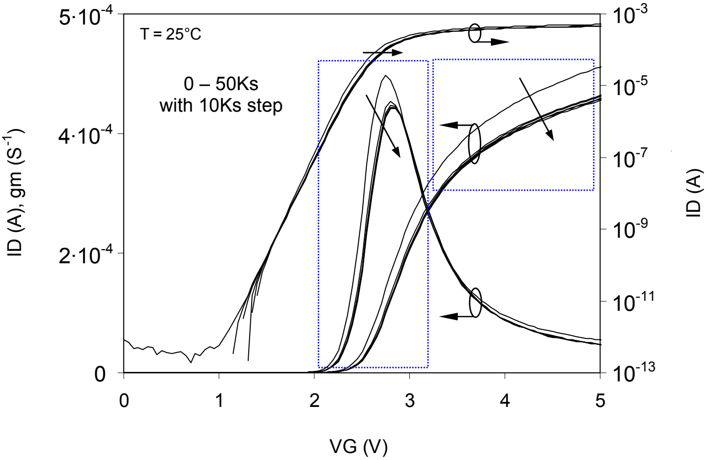
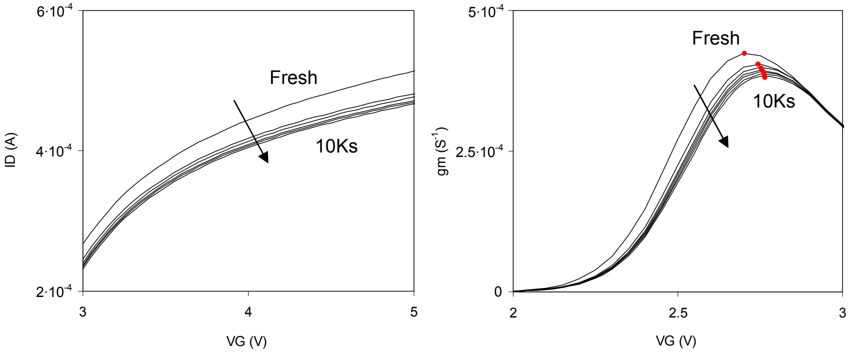


Fig. 5.16. Room temperature measured characteristics; g_m and I_D vs. V_G at low V_D (100mV) in linear and log scales for a 50Ks stress-B (V_G = 12V & V_D = 100V) duration at 10Ks stress intervals.

The smaller stress intervals carried out over 10Ks stress duration confirm this finding; after only 1.25Ks of stress-B a clear decrease in the drain current (Fig. 5.17.a) and a positive-shift-and-drop in the g_{max} denoted by the red symbols in Fig. 5.17.b are observed.



(a) *(b)*

Figs. 5.17. Zoom of inset dashed areas in Fig. 4.16; (a) I_D-V_G and (b) g_m-V_G at low V_D (100mV) for a 10Ks stress-B (V_G = 12V & V_D = 100V) duration at 1.25Ks stress intervals.

The output current and on-resistance curves seen in Fig. 5.18 consolidate our suggestion; degradations induced by the first 10Ks of stressing largely overpass those induced over the remaining 10-50Ks period.

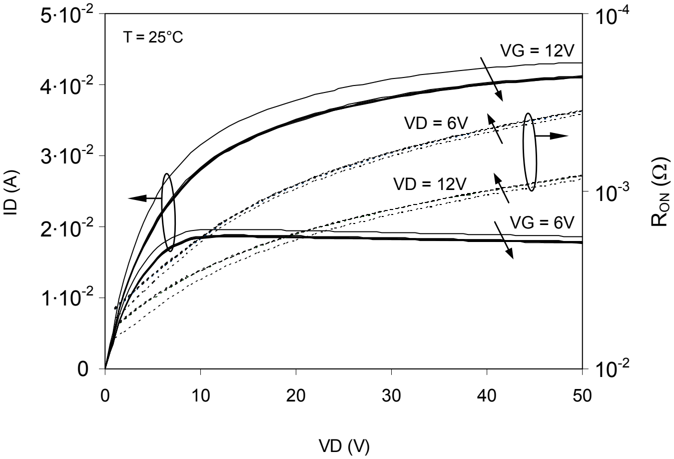


Fig. 5.18. Room temperature I_D-V_D (solid line) and R_{ON}-V_D (dashed line) measured characteristics for V_G = 6 and 12V for a 50Ks stress-B (V_G = 12V & V_D = 100V) duration at 10Ks stress intervals.

The variations in the relevant LDMOS channel parameters extracted at all intervals of accumulated time of stress-A and stress–B are plotted together for comparison in order to have a better view on the induced impact degradation of both stressing conditions. Figs. 5.19 (a and b) stand for threshold voltage and low-field mobility (ΔV_T, $\Delta\mu_{eff}$), Figs. 5.20 for sub-threshold Swing and increment in interface states density (ΔS, ΔD_{it}) and Figs. 22 for the ON-resistance at V_G = 12V in linear (V_D = 100mV) and saturation (V_D = 50V) mode of operations (R_{ON}-lin, R_{ON}-sat). The reported results reveal minor degradation of the electrical parameters for devices subject to stress-A conditions over 50Ks of cumulated stress-time. Degradation tends to saturate after the first 10Ks of stressing around 0.4-0.5% for threshold voltage (Fig. 5.19.a) and mobility (Fig. 5.19.b) and 1.2% for subthreshold Swing (Fig. 5.20.a). The on-resistance follows the same trend with stagnation at ~0.6% and ~2.2% increment for linear and saturation mode of operations (Figs. 5.21 (a and b)). In the opposite, at stress-B conditions the DC parameters are significantly altered and this in the very early stages, where extracted data after 10Ks stress-time show about 70-90% of the total induced degradation (50Ks); ΔV_T rises by 2.5%, $\Delta\mu_{eff}$ by 5.2%, ΔS by almost 5%, ΔR_{ON}-lin by ~16% and ΔR_{ON}-sat by ~5%.

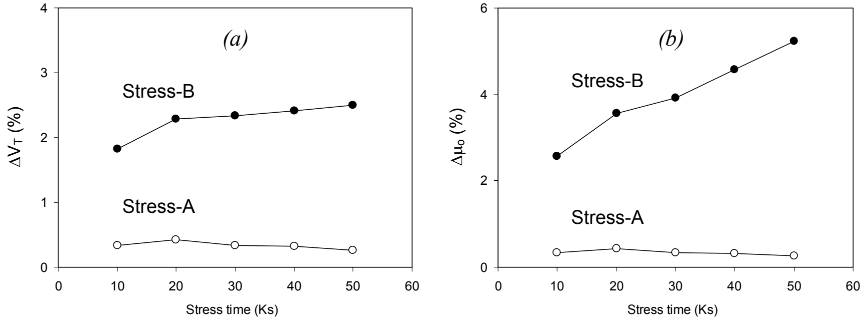


Fig. 5.19. Extracted (a) VT and (b) and low field mobility changes versus cumulated stress-time for stress-A: V_G=5.2 & V_D=100V (open symbols) and stress-B: V_G=12 & V_D=100V (solid symbols) at room temperature.

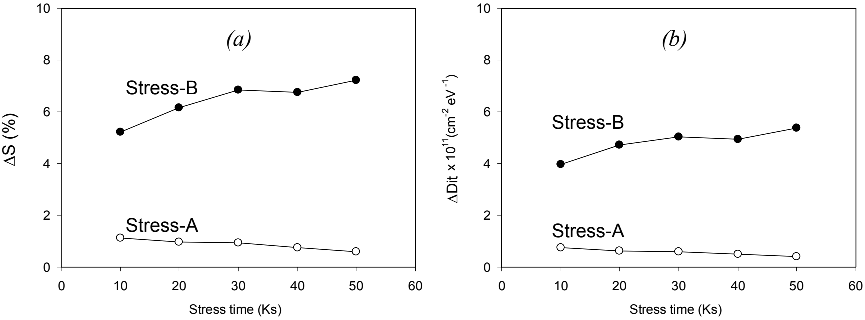


Fig. 5.20. Extracted (a) Subthreshold degradation and (b) ΔD_{it} increment versus cumulated stress- time for stress-A: V_G=5.2 & V_D=100V (open symbols) and stress-B: V_G=12 & V_D=100V (solid symbols) at room temperature.

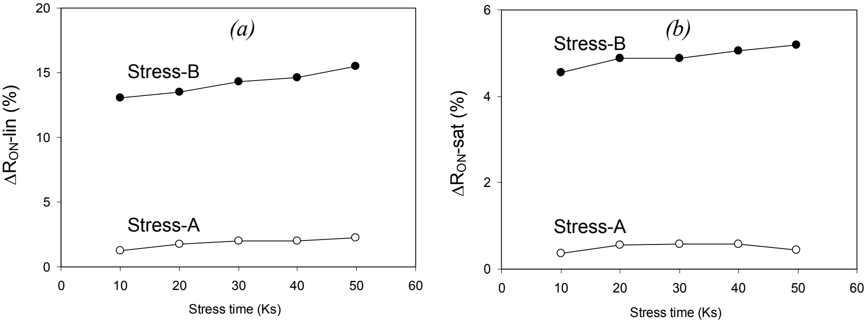


Fig. 5.21. (a) R_{ON}-lin and (b) R_{ON}-sat deterioration versus cumulated stress- time for stress-A: V_G=5.2 & V_D=100V (open symbols) and stress-B: V_G=12 & V_D=100V (solid symbols) at room-temperature.

As it can be noticed, ΔR$_{ON}$-lin overpasses the symbolic 10% the Safe-Operating-Area (SOA) at the very-early stage of stress-B (~ 13% after 10Ks, Fig. 5.21.a) and reaches ~16% after 50Ks stress-time. However, even if changes in mobility (~5%) and V_T (~2.5%) still remains within the 10% limit, the sharp rate at which mobility degrades under stress-B should be considered with care since it is a parameter of primary importance on which the device performance relies.

5. 9. 2. Capacitance HC Degradation Analysis at Room Temperature:

For both stress-A and B configurations, a systematic gate capacitances extraction from S-parameters measurement is performed before stressing the device and after each 10Ks (§ 5.5). As for the reported DC characteristics and channel parameters, under stress-A biases (V_G = 5.2 and V_D = 100V) only a limited degradation in C_{GD} characteristics (see Fig. 5.22) is detected with accumulated stress-time.

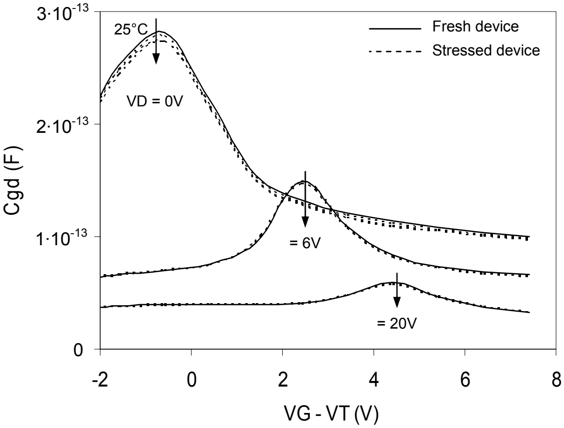


Fig. 5.22. Extracted LDMOS C_{GD} vs. V_G-V_T characteristics at room temperature under stress-A condition for V_D= 0, 6 and 20V before (solid lines) and after at 10, 30 and 60Ksstress intervals (dashed lines).

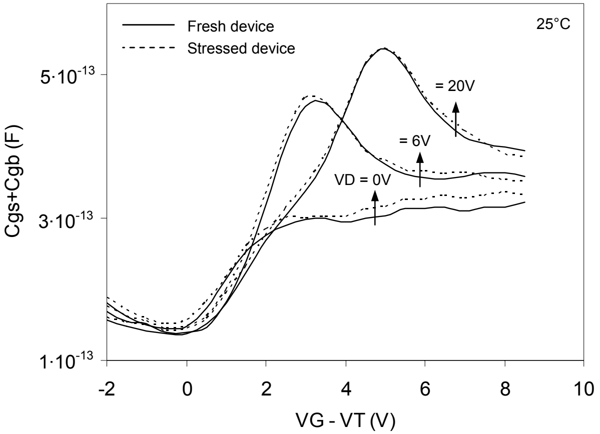
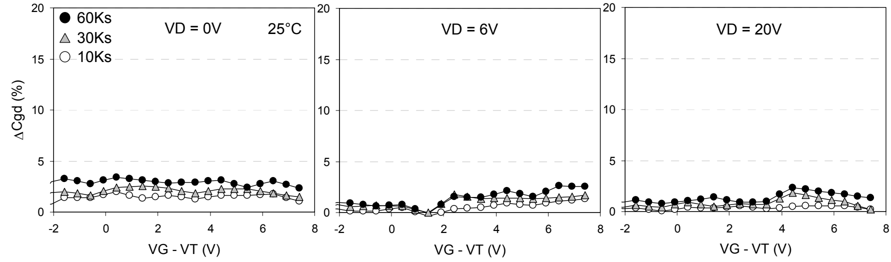


Fig.5. 23. Extracted LDMOS (C_{GS}+C_{GB}) vs. V_G-V_T characteristics at room-temperature under stress-A condition for V_D= 0, 6 and 20V before (solid lines) and after 60Ks cumulated stress (dashed lines).



(a) *(b)* *(c)*

Fig. 5.24. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at room temperature from device under stress-A biases at several stress-time intervals (10, 30 and 60Ks) for V_D = 0V (a), 6V (b) and 20V (c).

In term of quantitative degradation, after 50Ks of stress-A an average 3.4% variation in C_{GD} is observed at low V_D (0V), while for higher values (20V) the variation diminishes to around 1.7% (see Fig. 5.24, (a, b and c), black symbols). The same tendency is depicted from extracted C_{GS}+C_{GB} characteristics in Fig. 5.23 after 60Ks stress time, where at V_D = 20V, fresh and stressed measures are almost identical. In contrast, device subject to stress-B conditions shows with accumulated stress-time a more pronounced deterioration of the C_{GD} and C_{GS}+C_{GB} characteristics at all range of V_D biases (Figs. 5.25 and 5.26). More concretely, around 8-10%

variations in capacitance are observed after the first 10Ks of stressing and with a peak value of ~15-17% after 60Ks (see Figs. 5.27 (a, b and c), black symbols).

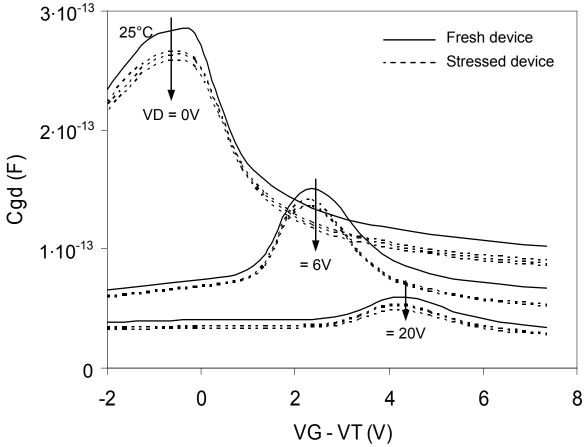


Fig. 5.25. Extracted LDMOS C_{GD} vs. V_G-V_T characteristics at room temperature under stress-B condition for V_D= 0, 6 and 20V before (solid lines) and after at 10, 30 and 60Ks stress intervals (dashed lines).

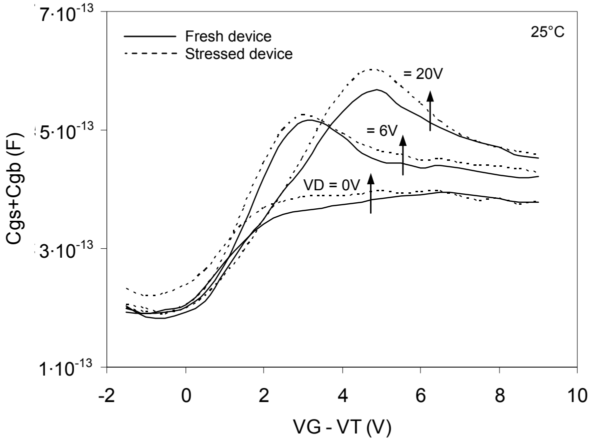
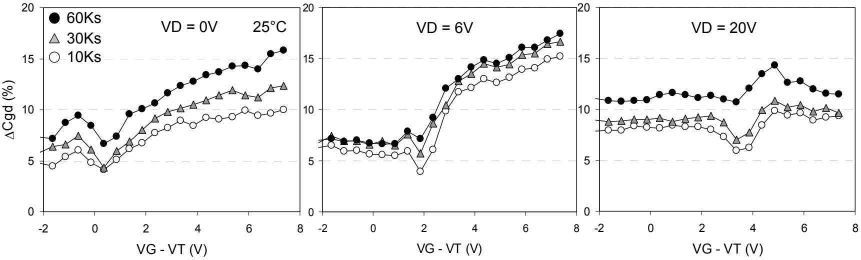


Fig. 5.26. Extracted LDMOS (C_{GS}+C_{GB}) vs. V_G-V_T characteristics at room temperature under stress-B condition for V_D= 0, 6 and 20V before (solid lines) and after 60Ks cumulated stress (dashed lines).



(a) *(b)* *(c)*

Fig. 5.27. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at room temperature from device under stress-B biases at several stress-time intervals (10, 20 and 60Ks) for V_D = 0V (a), 6V (b) and 20V (c).

Furthermore, measurements at negative V_G bias have been performed in order to investigate the impact of DC-stress on device capacitances in the depletion-to-accumulation regime (Fig. 5.9, regions A and B) with a particular focus on the $C_{GS}+C_{GB}$ characteristic, from which the device $V_{FB\text{-}Ch}$ (channel region) is extracted. Figs. 5.28 and 5.29 illustrate alteration in DMOS capacitances at zero drain bias respectively for stress-A and -B. As it can be seen, device subject to stress-A (V_G = 5.2V and V_D = 100V) shows no significant changes in capacitances despite a 50Ksec of cumulated stress time. Minor changes appear only after rising stress-time up to 80Ksec with peak values not exceeding 3% for ΔC_{GD} and 9% for $\Delta(C_{GB}+C_{GS})$. In contrast, device subject to stress-B (V_G = 12 and V_D = 100V) shows important changes in capacitance at the early stage of stress. Fig. 5.30 originally illustrates how drastically could be the impact on LDMOS capacitances with variations in characteristics reaching ~45% for C_{GD} and ~75% for $C_{GB}+C_{GS}$ are found after 80Ksec.

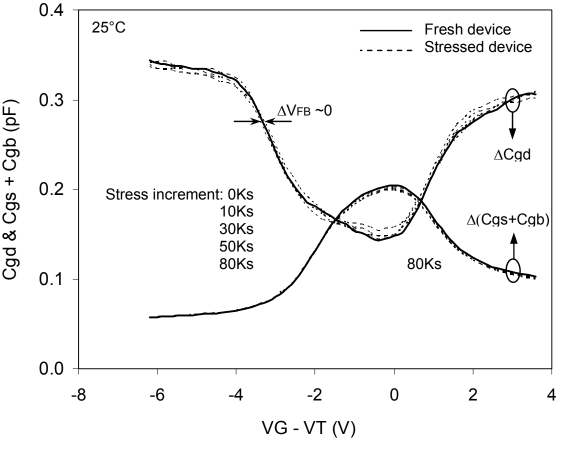


Fig. 5.28. Extracted LDMOS C_{GD} and (C_{GS}+C_{GB}) vs. V_G-V_T characteristics at room temperature under stress-A condition at V_D= 0V before (solid line) and after 10, 30, 50 and 80Ks stress-time (dashed lines).

This will be an added value in the up-coming argumentation and discussion concerning the degradation *mechanism*, at the origin of the induced DC/AC alterations seen in Figs.5.14 - 5.30, and its physical *location* within the LDMOS device; channel or drift region.

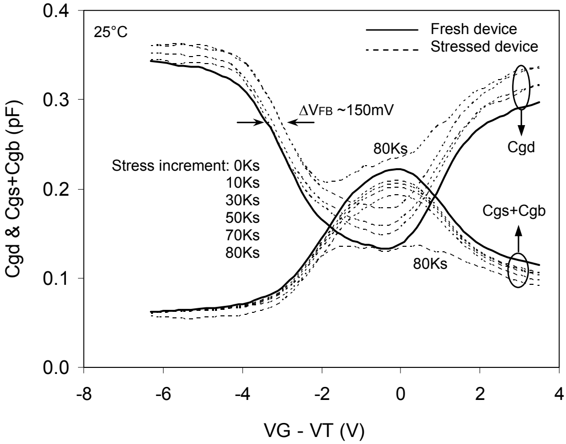


Fig. 5.29. Extracted LDMOS C_{GD} and (C_{GS}+C_{GB}) versus V_G-V_T characteristics at room temperature under stress-B condition at V_D= 0V before (solid line) and after 10, 30, 50, 70 and 80Ks stress-time (dashed lines).

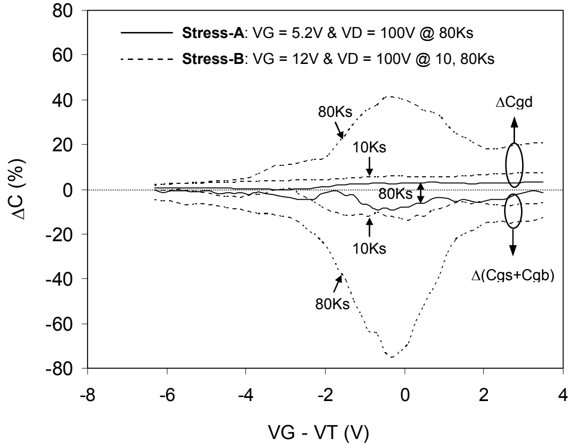


Fig. 5.30. Change in capacitances versus V_G-V_T for stress-A after 80Ks (solid lines) and stress-B after 10 and 80Ks (dashed lines).

5. 9. 3. Discussion at Room-Temperature

5. 9. 3. 1. *Discussion of stress effect at maximum body current (stress-A)*

In case of applied stress-A, DC and AC analysis have revealed very limited degradations in electrical parameters and characteristics regardless to the cumulative stress-time of 60Ks (Figs. 5.14, 5.15, 5.19-5.21). The negligible change in V_T (<1%, see Fig. 5.19. a) and sub-threshold Swing (<0.5%, see Fig 5.20.a) as well as the almost unchanged ΔD_{it} (saturates $\sim 0.7\times10^{11}$ cm^{-2} eV^{-1}, see Fig. 5.20.b) suggest that stress-A conditions do not induce significant hot-carrier damages within the *gate-oxide/channel-region* to alter its flat band voltage, $V_{FB\text{-}Ch}$. This is confirmed by the (C_{GS}+C_{GB}) characteristics illustrated in Fig.5.28, where all curves tend to overlay in the depletion-to-accumulation region, and from which the $V_{FB\text{-}Ch}$ value is conventionally determined. Despite the very long applied stress-time of 80Ks, nor significant shift can be depicted or extracted from the characteristic even with an incremental V_G step as low as 50mV (i.e. $\Delta V_{FB\text{-}Ch} \sim$ null).

An interesting finding is reported in Figs. 5.22 and 5.23, that suggest *smaller changes in gate capacitances as drain bias increases*); extracted ΔC_{GD} after 60Ks of stressing (black symbols, Figs. 5.24 (a, b and c)) drops from ~3.8% to ~2.5% to ~1.7% variations as V_D rise from 0 to 6 to 20V respectively. In order to explain this phenomenon, a close look on data plotted in Fig. 5.31 can provide some help. It shows the distribution of the electrical field along the Si/SiO$_2$ interface for stress-A and -B biases extracted from a numerical 2D-structure calibrated on real n-channel LDMOS devices, identical to those used in our investigation. The corresponding curve to stress-A (open circle) shows two peak values with a *lower-maximum* ($\sim 2.3\times10^5$ V/cm) near the source-side of the channel and an *upper-maximum* ($\sim 3.6\times10^5$ V/cm) at the bird's beak area. In correlation with the almost 0 extracted $V_{FB\text{-}Ch}$ and negligible change in V_T, it becomes clear that the intrinsic channel region is much less affected by the stress-A conditions and that the most susceptible location subject to degradation would be within the drift region, more precisely where the maximum electrical-field points, i.e. at the *bird's beak region*. The well detailed works and studies [16-19] demonstrated that under equivalent stress-A conditions (i.e. V_G at I_{Bmax} and V_{Dmax}), for n-channel LDMOS transistors, the degradation mechanism is mainly due to *hot-hole injection in the oxide* and *acceptor-like traps formation near the interface*. When the transistor is turned-On, flowing electrons from source-to-drain near the interface tend to fill those created traps, leading to a negative charge builds-up in this oxide with the accumulated stress-time, which in turn compensate "locally" the positive charge at the gate, and thus reduces by a limited amount the On-state current flowing near the interface at low V_D. This explains the limited drop observed in the I_D-V_G characteristic (see Fig. 5.14) and the increase in $\Delta R_{ON\text{-}Lin}$ with stress-time in Fig. 5.21.a (dashed curve).

As V_D increases, the current path is no longer following the interface but tends to flow deep in the drift volume far from bird's beak and becomes no more affected by the charges trapped in the oxide at high V_D voltages. This is well illustrated in Figs.5.32 by the 2D-numerical simulations of the current flow-lines (red contours) travelling from source-to-drain within the n-channel LDMOS structure for V_G at maximum body current (5.2V). At low V_D (Fig. 5.32.a, 100mV) the electron path keeps very close to the interface when passing near the bird's beak region, while at higher V_D (Fig. 5.32.b, 20V) electrons flow deep in the structure as they leave the channel-end. When V_G is raised to its maximum (12V), the current flow lines at low V_D are even more confined to the interface in the bird's beak area, while at higher V_D electrons are not any more going deep in the structure as they leave the channel; they keep close to the interface but much less confined then at lower V_D as it can be seen in Figs. 5.33 (a and b, Inset zooms).

Therefore, only a slight increase in capacitance degradation would be expected when compared at lower V_G as it is seen in Fig. 5.24.b (curves at 10 and 30Ks), where a slight progressive rises in ΔC_{GD} can be depicted with V_G. This clearly confirms that the proposed degradation mechanism proposed under stress-A conditions originates *within the drift region near the bird's beak* [16, 19].

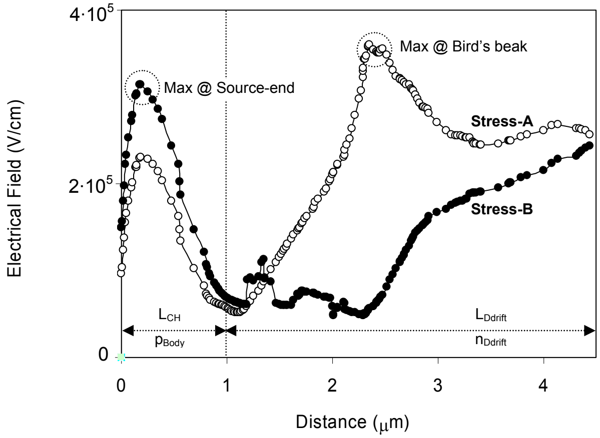
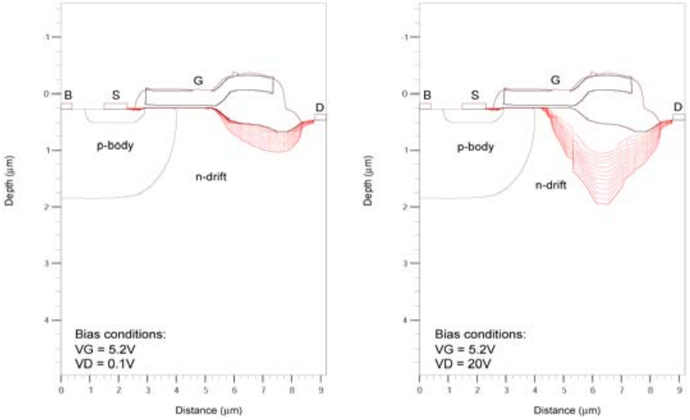
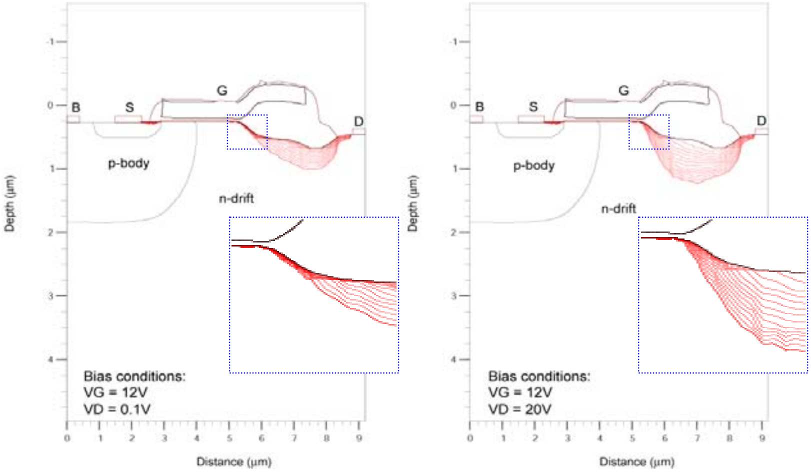


Fig. 5.31. Electrical-field distribution extracted near the Si/SiO2 interface beneath the field-plate oxide for stress-A (solid circles) and stress-B (open circles) conditions.



(a) *(b)*

Figs. 5.32. 2D-numerical simulations of current flow-lines distribution within n-channel LDMOS structure for V_G = 5.2V and (a) V_D = 0.1V and (b) V_D = 20V.



(a) *(b)*

Figs. 5.33. 2D-numerical simulations of current flow-lines distribution within an LDMOS structure biased at $V_G = 12V$ and (a) $V_D = 0.1V$ and (b) $V_D = 20V$.

5. 9. 3. 2. *Discussion of stress effect at maximum gate voltage (stress-B)*

The AC and DC analysis of stress-B reveals very significant degradations of the electrical parameters at the very early stages of stressing. For instance, C_{GD} drops by around 10-17% in strong-inversion after 60Ks of stressing (Fig. 5.25) and about half of its initial value after 80Ks stress-time in the weak-to-strong inversion region as it can be seen in Fig. 5.29. The significant change in V_T (~2.5%, Fig. 5.19.a) and ΔS (~5%, Fig. 5.20.a) after 60Ks suggests alteration in the channel flat-band voltage, $V_{FB\text{-}Ch}$, and thus a probable alteration within the intrinsic channel-region. If any HC induced effect takes place within the channel, it will be reflected by the (C_{GS}+C_{GB}) characteristic when biased toward accumulation. Fig. 5.29 shows a continuous positive-shift with stress-time equivalent to a $\Delta V_{FB} \approx 150mV$ extracted after a total cumulative stress-time of 80Ks, which clearly confirms that degradation occurs at the device channel and causes the V_{FB} shift, V_T increase and mobility reduction ($\Delta\mu_{eff}$ ~5%, Fig. 5.19.b) and their combined effect contributes to the important current drops seen in Figs. 5.16 – 5.18. The degradation mechanism is similar to stress-A, i.e. traps formation, electron-trapping and negative charge builds-up with cumulated stress-time. The maximum electrical-field depicted in Fig. 5.31 for stress-B points at the channel source-end of the device, which is a clear indication that the channel source-end is the more plausible location for degradation occurrence [7, 40]. This has no equivalent in conventional MOSFET's where most of HC-degradation and hot-carriers injection takes place at drain-side [9-11], explained by the channel doping uniformity leading to an electrical-field maximum pointing at the peak of the channel-potential, V_{CH}, physically located at the channel-end of MOSFET's. Note that extracted ΔD_{it} from sub-threshold characteristics (Fig. 5.20.b) consolidate our analysis where changes induced by stress-B after 60Ks of stressing (5.3×10^{11} cm^{-2} eV^{-1}) exceeds 10 times those induced by stress-A (0.4×10^{11} cm^{-2} eV^{-1}).

5. 9. 4. Conclusion: HC degradation at room temperature

The HC experimental investigation at room temperature based on the two selected stressing conditions (called Stress-A and B) and the complete analysis of post-stress data is synthesized by the following comments:

- **Capacitance degradation monitoring appears as a much more sensitive method to quantify and distinguish between various types of stresses** at least compared with DC monitoring;
- Proposed analysis of capacitance degradation after stress-A and B at room-temperature reveals completely different locations of degradation in both cases: drift region and channel region respectively;
- For **stress-A induced degradation takes place at LOCOS bird's beak area**;
- For **stress-B induced degradation takes place at source-end gate oxide region**;
- Analysis indicates **hot-hole injection in the oxide and acceptor-like traps formation near the interface** as the most probable degradation mechanism for investigated LDMOS device architecture.
- Analysis of Stress-A and B systematically reveals **higher alteration in device capacitances than in DC electrical parameters**;
- **Stress-B is identified as the worst-case** induced degradation for investigated LDMOS device.

The proposed original investigation demonstrates that experimental monitoring of the hot-carrier capacitance degradation in DMOS transistors is not only a complementary analysis to the more standard evaluation of the DC characteristics but can delivers unique insights in HC cases when DC parameter degradation offers only limited information. From the reported work, one should note that while some DC parameters are still within the SOA limits, the AC characteristics appear largely altered and over pass the symbolic 10% variation. This open the debate about the importance or not of considering the capacitive aspect in standard reliability tests, where only the DC degradation aspect accounts and from which the device SAO limits are defined.

5. 10. HOT-CARRIER DEGRADATION AS FUNCTION OF TEMPERATURE

As mentioned earlier in this chapter, due to the high-voltages and/or high-current capability of HV DMOS related to their various applications, tens of Watts are dissipated, and consequently, in the on-state regime they operate near the 100°C temperature range. At our best knowledge, mainly HC damage in low voltage MOSFET's as function of temperature has been investigated in detail over the past 15 years [41-46], while much less work has been dedicated to HV transistors despite the fact that these devices are the most concerned. In this context, an experimental investigation able to *quantify* the HC/temperature coupling and its *impact* on the capacitance characteristics of the n-channel LDMOS transistor is proposed in this section. For the relevance of the work a systematic comparison with a standard DC parameter degradation for same applied stresses is reported.

As a continuity of the reported analysis at room temperature (§ 5.8) and for delivering a consistent analysis over the full 25-100°C range, the same measuring sequences and parameter extraction procedures have been kept (see tables table 5.2). Concerning stressing conditions, minor modifications on applied V_G and V_D stress biases have been introduced in order to account for the temperature effect. This will be detailed in the next paragraph.

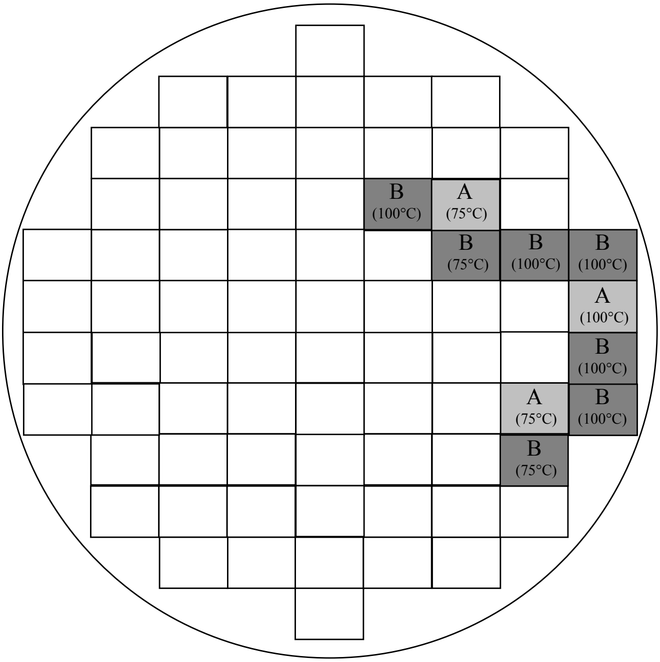


Fig. 5.34. Wafer mapping of stressed dies over temperature (75 and 100°C).

5. 10. 1. Applied Stress Biases Over Temperature

As the temperature of a HV MOSFET device increases, its characteristics and extracted electrical parameters are affected in different ways (e.g. drain current decreases, mobility drops, on-resistance rises, threshold voltage shifts … etc.), therefore it is important to account for *the temperature impact on the applied stressing conditions*. In order to ensure equivalent electrical stressing conditions to those performed at room-temperature (reference value at which stress biases have been selected) and thus *allowing equivalent transversal and lateral electrical-field conditions over temperature*, stress-A and –B bias conditions have been verified over the investigated range of temperature 25-100°C based on the following criteria:

(i) for drain-stress bias: $V_{D\,(stress\text{-}A)} = V_{D\,(stress\text{-}B)} = V_{BD\,(T°)} - 4V$

(ii) for gate-stress biases: $V_{G\,(stress\text{-}A)} = V_G$ at $I_{B\text{-}max\,(T°)}$

$$V_{G\,(stress\text{-}B} = V_{G\text{-}max\,(25°)} - \Delta V_{T\,(T°)}$$

$$= 12V - \Delta V_{T\,(T°)}$$

Accordingly, series of I_D-V_G at low V_D (100mV) and I_B vs. (V_G-V_T) measures at high V_D biases (60-80V) have been performed over temperature and the resulting characteristics are respectively illustrated in Figs. 5.35 and 5.36. Also the proportionality between generated body and drain currents (I_B/I_D vs. V_G-V_T) and $I_{B\text{-}max}$ vs. V_D characteristics for various stress-temperatures have been extracted and plotted in Figs. 5.37 and 5.38 respectively. Drain-to-source breakdown voltage (V_{BD}) has been extracted only for 25 and 100°C and extrapolated for the temperature values in between. This can be justified by the limited numbers of available devices and the destructive nature of such measurements, which generally conducts the devices under test toward failure.

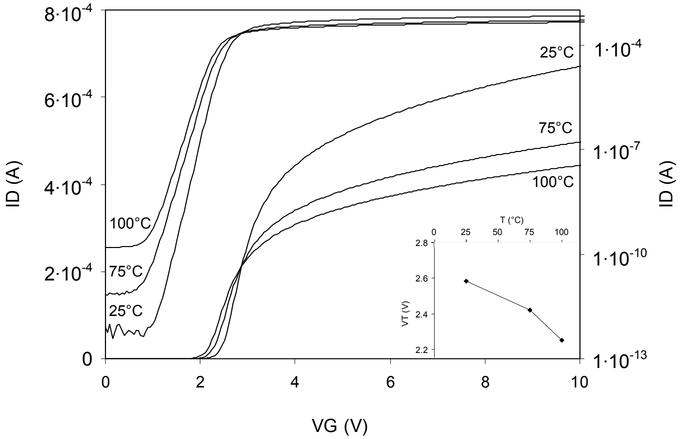


Fig. 5.35. Measured I_D -V_G characteristics over temperature (25, 75 and 100°C) at low V_D bias (100mV); inset: extracted V_T values for each temperature.

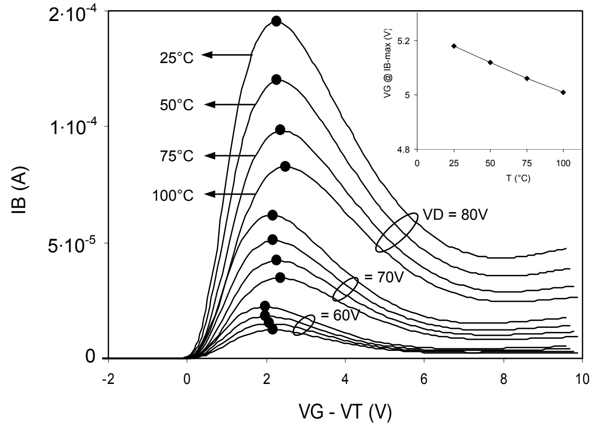


Fig. 5.36. Measured I_B vs. (V_G-V_T) characteristics at 25, 50, 70 and 100°C for different V_D biases (60, 70 and 80V) and their $I_{B\text{-}max}$ values denoted by solid symbols. Inset graph; V_G values for $I_{B\text{-}max\ (T°)}$ at V_D = 100V.

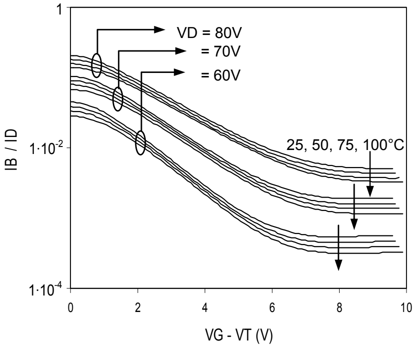


Fig. 5.37. Measured I_B/I_D vs. (V_G-V_T) characteristics at 25, 50, 70 and 100°C for different V_D biases (60, 70 and 80V).

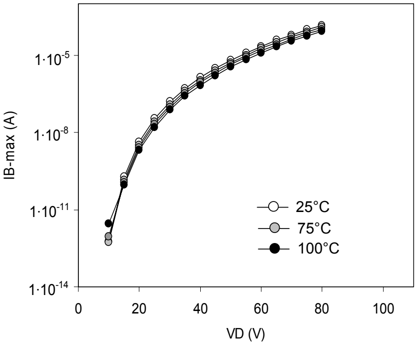


Fig. 5.38. Extracted $I_{B\text{-}max}$ vs. V_D characteristics from I_B-V_G curves at various V_D and stress-temperatures (25, 75 and 100°C).

Extracted shifts in V_T values over temperature (Fig. 5.35. inset graph) show: $\Delta V_{T\ (75°)}$ ~170mV and $\Delta V_{T\ (100°)}$ ~ 330mV, while the measured shift in V_{BD} with temperature indicates ΔV_G at $I_{B\text{-max}\ (75°)}$ ~ 100mV, ΔV_G at $I_{B\text{-max}\ (100°)}$ ~ 150mV and $\Delta V_{BD\ (100°)}$ ~ 2V.

The corresponding V_G values at maximum $I_{B\text{- max}\ (T°)}$ for V_D = 100V (Fig. 5.36. inset graph) are extracted from equivalent values at lower drain biases (60-80V) and from which the linear-extrapolation feasibility has been verified over temperature as it can be seen in Fig. 5.39. This is explained by the fact that device architecture on which are performed I_B-V_G measures has much smaller width dimension (~ 40μm) compared to those subject to stressing (~ 6×40μm).

Such devices are more sensitive to current crowding and exhibit a reduced heat-dissipation capability at high current levels, which make them more susceptible to device heat-up and/or premature device burning. One could ask why such a smaller device width is then used. The reason is the specific architecture of such device which promotes among all available LDMOS transistors a separate source and body contact, primordial for body current measurements and thus precise $I_{B\text{-}max}$ extraction.

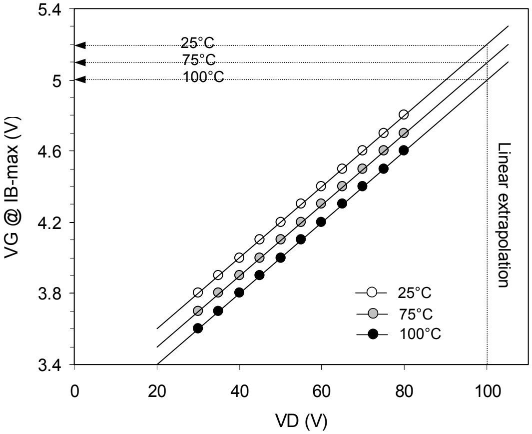


Fig. 5.39. Corresponding V_G values of $I_{B\text{-}max}$ over 25, 75 and 100°C from which are extrapolated (linearly) V_G at $I_{B\text{-}max\,(T°)}$ values for $V_D = 100V$.

Accordingly, stress-A and B biases have been adjusted for each corresponding stress-temperature following the listed criteria in previous section (§ 5.9.1) and are summarized in table 5.4.

Stress type	T (°C)	V_G (V)	V_D (V)	Stressing condition
A	25 75 100	5.2 5.1 5.0	100 98 98	Maximum drain bias ($V_{D\text{-}max}$) & V_G @ maximum body current ($I_{B\text{-}max}$)
B	25 75 100	12 11.8 11.5	100 90 90	Maximum drain bias ($V_{D\text{-}max}$) & Maximum gate bias ($V_{G\text{-}max}$)

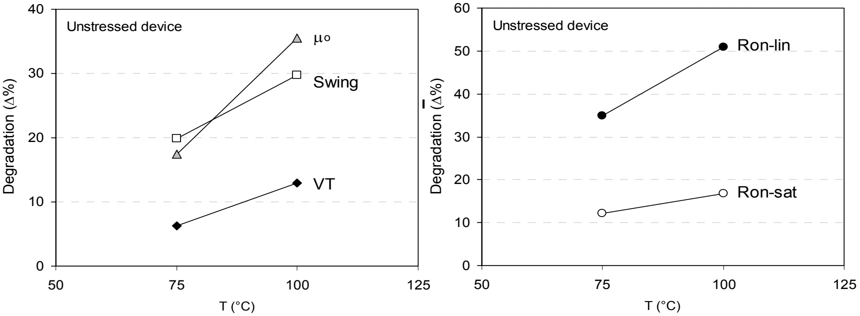
Table 5.4. Values of adjusted stress bias conditions correlated with stressing-temperature.

As it can be noticed for stress-B conditions over temperature, V_D bias has been lowered to 90V for stress-temperatures 75°C and 100°C. This is justified by the experimental founding during stress-B measurements where devices stressed at V_D = 98V fail (i.e. burn) after exceeding 20Ks stress-time at 75°C and only ~ 11-13Ks at 100°C; *a clear indication on the sever alterations within the devices, most probable cause of their premature break-down.*

5. 10. 2. DC HC-degradation Analysis over Temperature:

Reported experimental data and extracted parameters over temperature are compared to those obtained at room temperature, in order to provide an effective view on the impact of temperature up on device characteristics and most relevant electrical parameters. However, to separate and well distinguish between alterations in device performances which are due to the impact of temperature and those induced by electrical stressing over temperature, the most relevant electrical parameters (i.e. V_T, Swing, μ_0, R_{ON}-lin and R_{ON}-sat) have been extracted over temperature for *unstressed* LDMOS device and plotted in Figs. 5.40, while changes induced only to electrical stressing are separately illustrated respectively in Figs. 5.41 and 5.42 for stress-A and Figs. 5.43 and 5.44 for stress-B.

Extracted parameters from device prior to stress in Fig. 5.40, illustrate the strong negative impact exerted by temperature a on the device performance; mobility drop severely, V_T shifts, Swing rises considerably and on-resistance becomes higher. In term of numbers, increasing temperature from 25 to 75°C ($\Delta T_{25\text{-}75} = 50$°C) gives rise to a $\Delta\mu_0 \sim 17.4\%$, and from 25 to 100°C ($\Delta T_{75\text{-}100} = 25$°C) to $\Delta\mu_0 \sim 35.5\%$. By a simple subtraction, it appears that the temperature rise $\Delta T_{25\text{-}75}$ (25°C) degrades channel mobility as much as those induced by the temperature increase $\Delta T_{75\text{-}100}$ (25°C), revealing an *inverse power-low dependence* with temperature. [47] Demonstrates experimentally a $T^{-2.5}$ DMOS channel mobility dependence, which is significantly more severe than the $T^{-1.5}$ commonly observed for conventional CMOS transistors [48,49]. Measured V_T over temperature (25-100°C) show a threshold voltage variation ΔVT of ~ -5mV/°C, more severe than those observed for standard MOSFET's and very close to the change (-5.2mV/°C) revealed for DMOS devices in [47]. The on-resistance indicates a *quasi-linear dependence* with temperature and shows a more severe variation in linear (~ 51%) than in saturation regime (~17%) as well as a faster deterioration (i.e. ΔR_{ON}-lin rises twice faster than ΔR_{ON}-sat). The plotted data show a ΔS changes of ~ 0.3mV/decade/°C and with a ~ 30% degradation at 100°C, which is quite considerable.



(a) *(b)*

Figs. 5.40. Extracted (a) V_T, S and μ_0 and (b) R_{ON}-lin and R_{ON}-sat alteration (Δ%) with temperature from unstressed n-channel LDMOS device.

Figs. 5.41 and 5.42 present degradations induced by **stress-A** (i.e. at maximum body current, $I_{B\text{-max}}$) cumulated over a period of 60Ks over temperature (T = 25, 75 and 100°C) respectively on the transfer (I_D-V_G and g_m-V_G) and output (I_D-V_D). As expected, a global shift in

I-V characteristics with temperature is monitored, while for each temperature the sub-threshold characteristics (log I_D-V_G, Fig. 5.41) remain unchanged and only a slight decrease in g_{max} and the transfer and output current level can be noticed. One interesting observation is depicted from these measured characteristics over temperature; transfer and output currents show a slight enhanced degradation at 100°C when compare to those at room-temperature especially in the linear and quasi-linear regimes (Figs. 5.41 and 5.42, doted boxes).

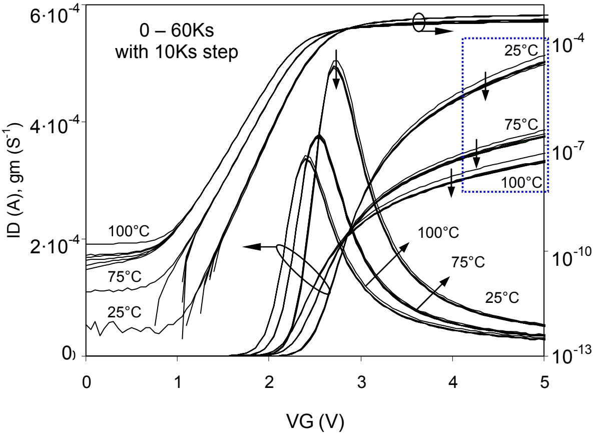


Fig. 5.41. Measured g_m and I_D-V_G characteristics subject to stress-A in linear and log scales before and after incremental 10Ks stress intervals, up to 60Ks accumulated stress, for T = 25, 75 and 100°C.

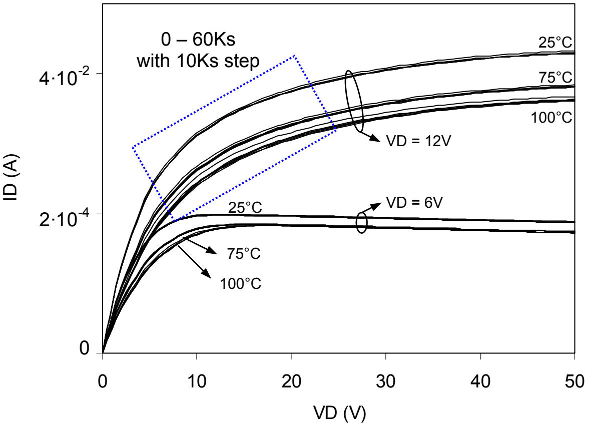


Fig. 4.42. Measured I_D-V_D characteristics subject to stress-A before and after incremental stress intervals of 10Ks, up to 60Ks accumulated stress for T = 25, 75 and 100°C.

Figs. 5.43 and 5.44 show degradations induced by **stress-B** (i.e. at maximum gate voltage, $V_{G\text{-max}}$) over a period of a cumulated stress-time of 50Ks for temperatures T = 25 and 75°C and up to 30Ks for T = 100°C respectively on the transfer (I_D-V_G and g_m-V_G) and output (I_D-V_D). DC measurements at 100°C have been interrupted after few kilo seconds of a 30Ks cumulative stress-time due to device failure and this despite the reduced $V_{D(\text{stress-B})}$ from 98 to 90V (see table 5.4). The major portion of drops in I-V and g_m curves shift of the V_T and sub-threshold characteristics occurs within the first 10Ks of stressing, which confirms over temperature the severe degradation reported for room-temperature at the very-early stage of stress-B conditions (§ 5.8.1).

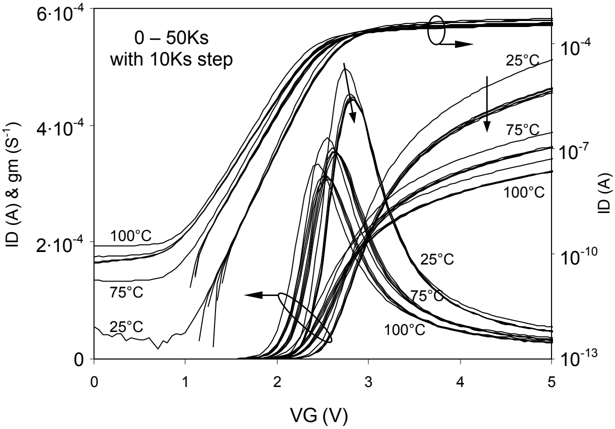


Fig. 5.43. Measured g_m and I_D-V_G characteristics subject to stress-B in linear and log scales before and after incremental 10Ks stress intervals, up to 50Ks accumulated stress at T = 25 and 75°C and up to 30Ks at T = 100°C.

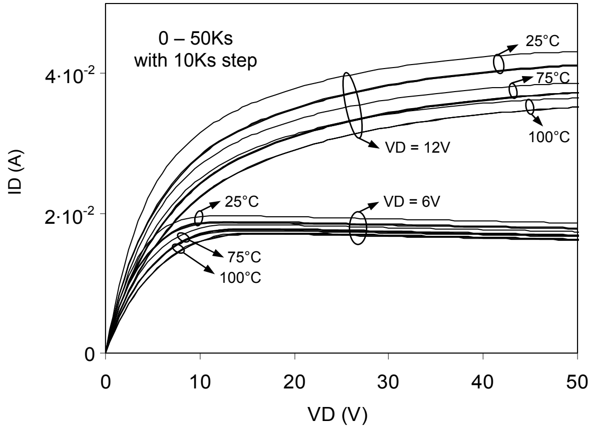
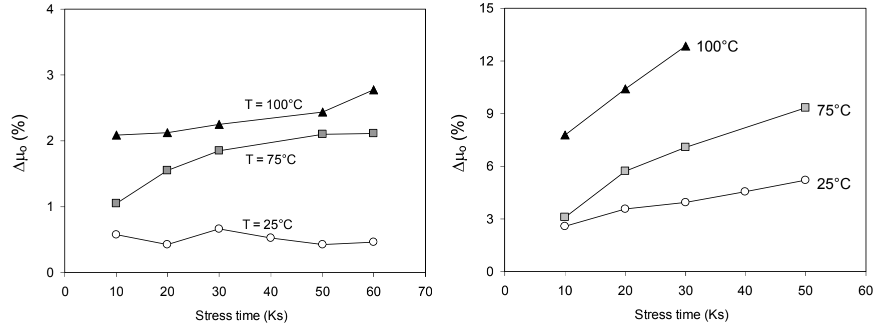


Fig. 5.44. Measured I_D-V_D characteristics subject to stress-B before and after incremental 10Ks stress intervals, up to 50Ks accumulated stress at T = 25 and 75°C and up to 30Ks at T = 100°C.

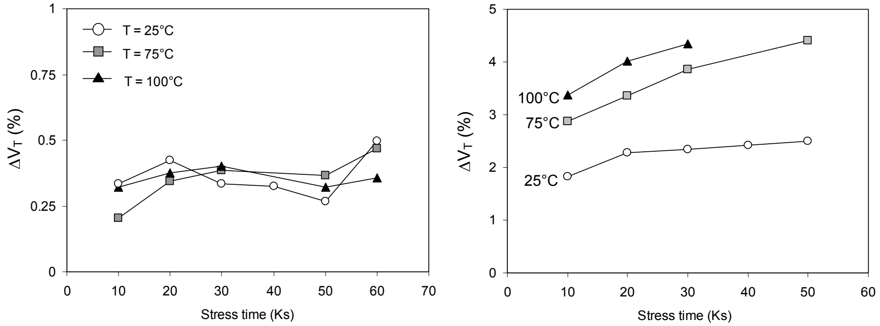
Extracted mobility from devices subject to stress-A and B indicates a net increased alteration with temperature. Under stress-A biases; at room-temperature $\Delta\mu_0$ stagnates around 0.5% over the 60Ks cumulated stress-time, while at higher temperatures $\Delta\mu_0$ shows a progressive raise with stress-time and stress-temperature to reaches after 60Ks of stressing ~2% at 75°C and ~3% at 100°C (see Fig. 5.45.a). For stress-B conditions mobility changes keep rising with stress-time at all measured temperatures; after 30Ks of cumulative stressing, changes in mobility are found equal to ~13%, ~7% and ~4% respectively for T = 25, 75 and 100°C (see Fig. 5.45.b). However a net difference in the rate at which mobility degradation rises with stress-time over temperature under stress-B when compared to stress-A biases is clearly depicted from Figs. 5.45 (a and b).



(a) *(b)*

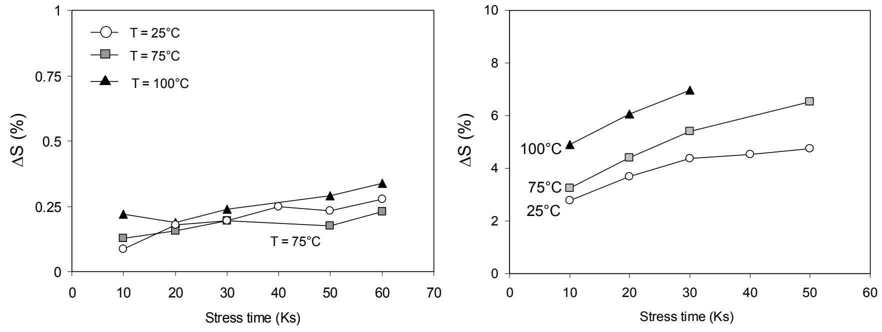
Figs. 5.45. Extracted low field mobility changes versus cumulated stress-time for (a) stress-A and (b) stress-B at various stress-temperatures: 25, 75 and 100°C.

Under stress-A biases, threshold and sub-threshold characteristics indicate no significant changes with temperature after a total stress-time of 60Ks; ΔV_T stagnates between 0.2-0.4% (see Fig. 5.46.a) and ΔS remains within the 0.1-0.3% boundaries (see Fig. 5.47.a).



(a) *(b)*

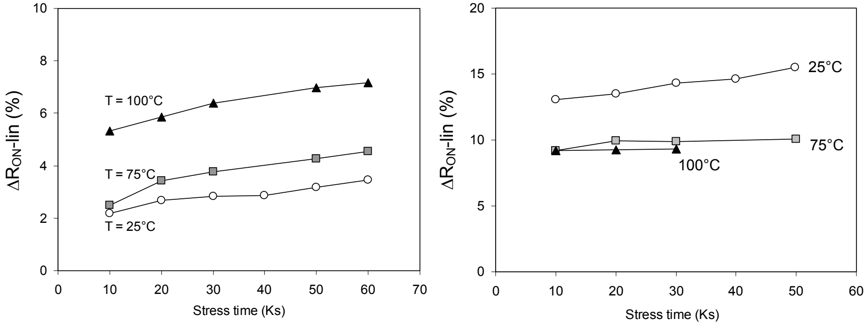
Figs. 5.46. Extracted V_T changes vs. cumulated stress-time for (a) stress-A and (b) stress-B at various stress-temperatures: 25, 75 and 100°C.



(a) *(b)*

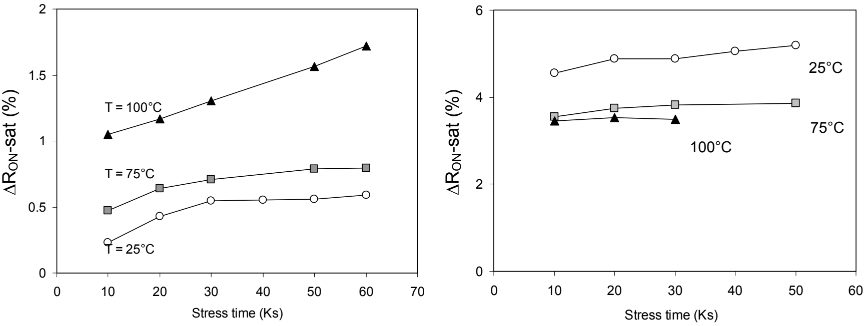
Figs. 5.47. Extracted subthreshold degradation versus cumulated stress- time for (a) stress-A and (b) stress-B at various stress-temperatures: 25, 75 and 100°C.

In contrast, under stress-B biases, a clear increase with temperature is observed for extracted threshold and sub-threshold characteristics; after 30Ks stress-time extracted ΔV_T = 2.3%, 3.9% and 4.4% (Fig. 5.46.b) and ΔS = 3.4%, 4.4% and 7% (Fig. 5.47.b) respectively for T = 25, 75 and 100°C. The observed increasing rate of degradation with temperature for mobility under stress-B biases is also depicted for extracted ΔV_T and ΔS as it can be seen from extracted values at 25 and 75°C (see Figs. 5.46.b and 5.47.b). Extracted on-resistance in linear and saturation regimes from device subject to stress-A shows a progressive increase with both stress-time and stress-temperature; after a 60Ks stress-time, ΔR_{ON}-lin is doubled, from 3.5% at 25°C to 7.2% at 100°C (Fig. 5.48.a), and ΔR_{ON}-sat almost tripled, from 0.6% at 25°C to 1.72% at 100°C (Fig. 5. 49.a). For stress-B, a *reverse dependence* with temperature is depicted in both linear and saturation regimes; after a cumulated 30Ks of stressing ΔR_{ON}-lin drops from 14.3% at 25°C to 9.9% at 75°C and 9.3% at 100°C (see Fig. 5.48.b), while ΔR_{ON}-sat drops from 4.9% at 25°C to 3.8% at 75°C and 3.5% at 100°C (see Fig. 5.49.b).



(a) *(b)*

Figs. 5.48. Extracted R_{ON}-lin deterioration versus cumulated stress- time for (a) stress-A and (b) stress-B at various stress-temperatures: 25, 75 and 100°C.



(a) *(b)*

Figs. 5.49. Extracted R_{ON}-sat deterioration versus cumulated stress- time for (a) stress-A and (b) stress-B at various stress-temperatures: 25, 75 and 100°C.

5. 10. 3. Capacitance HC-degradation Analysis over Temperature

Reported I-V characteristics and extracted channel parameters from device prior to stress respectively in Figs. 36 and 43 show how drastically the impact of temperature on the LDMOS transistor is. This is also confirmed from device capacitances measured over temperature and illustrated in Fig. 5.50. C_{GD} curves show a drop by ~ 15% at 75°C and by ~20% at 100°C, while C_{GS}+C_{GB} capacitance shows an increase together with a positive shift in characteristics and giving rise to a $\Delta V_{FB\text{-}Ch}$ estimated to ~200-300mV over the temperature range 25-100°C (extracted $\Delta V_{T(25\text{-}100°C)}$ = 330mV for unstressed device).

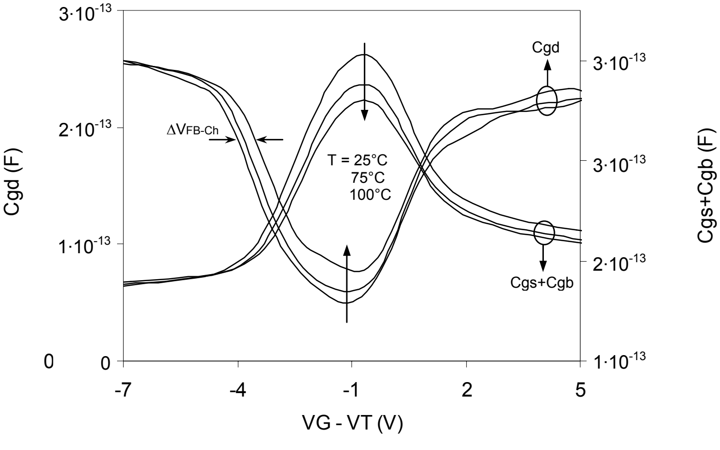
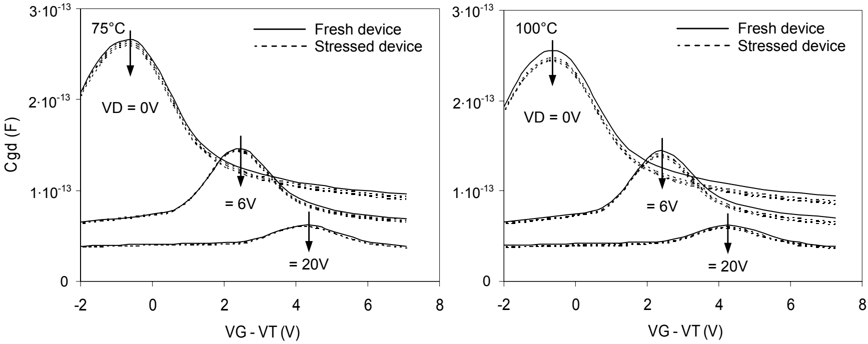


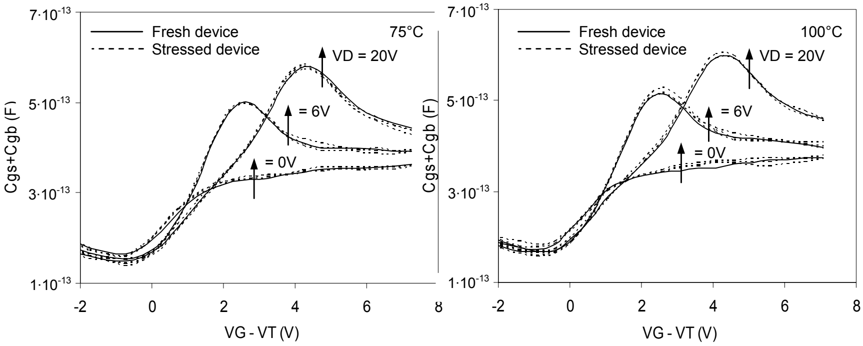
Fig. 5.50. Extracted LDMOS C_{GD} and (C_{GS}+C_{GB}) versus V_G -V_T characteristics prior to stress for V_D= 0V at stress-temperature: 25, 75 and 100°C

As for the DC characteristics and channel parameters reported over temperature, under stress-A biases only a limited degradation in C_{GD} and $C_{GS}+C_{GB}$ characteristics (see Figs. 5.51 and 5.52) is detected with accumulated stress-time. However, a progressive rise in capacitance degradation with temperature is depicted from extracted changes gate-to-drain capacitance characteristics illustrated respectively in Figs. 5.53 – 5.55; at low V_D (0V) extracted ΔC_{GD} at 25° after 60Ks stressing – denoted by black circles - do not exceed 3.8%, while extracted changes at 75° and 100°C for equivalent stress-time reach respectively 5.3% (see Figs. 5.53.a, 5.54.a and 5.55.a) and 8.1%. Identically at higher V_D (20V) ΔC_{GD} at 25° after 60Ks stress-time is at maximum 2%, while extracted changes at 75° and 100°C for equivalent stress-time reach respectively 3.3% and 6% (see Figs. 5.53.c, 5.54.c and 5.55.c). This confirms over temperature the reported tendency for room-temperature (§ 5.8.2): *ΔC_{GD} diminishing with raised drain bias for device subject to stress-A*.



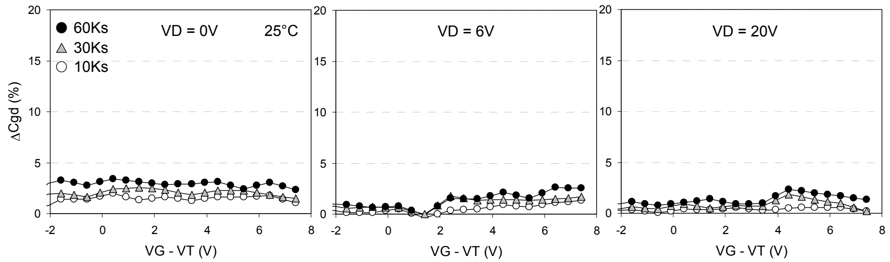
(a) *(b)*

Figs. 5.51. Extracted C_{GD} vs. V_G-V_T characteristics under stress-A biases for V_D= 0, 6 and 20V before (solid lines) and after at 10, 30 and 60Ks stress intervals (dashed lines) at stress-temperatures: (a) 75°C and (b) 100°C.



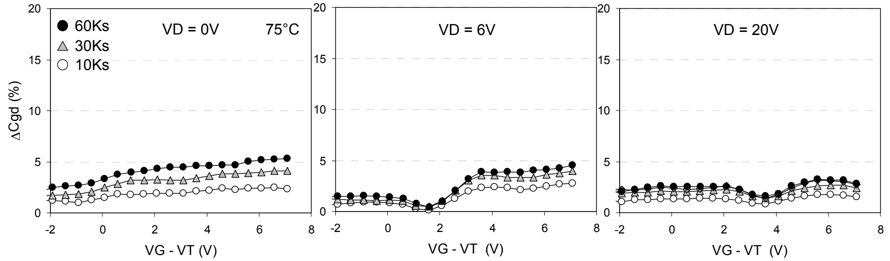
(a) *(b)*

Figs. 5.52. Extracted $C_{GS}+C_{GB}$ versus V_G-V_T characteristics under stress-A biases for V_D= 0, 6 and 20V before (solid lines) and after at 10, 30 and 60Ks stress intervals (dashed lines) at stress-temperatures: (a) 75°C and (b) 100°C.



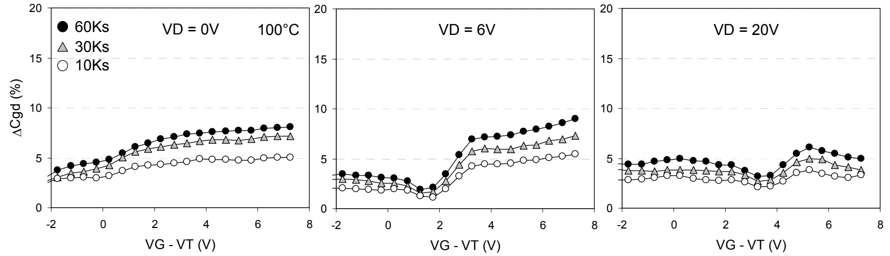
(a) (b) (c)

Figs. 5.53. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at room temperature from device under stress-A biases at several stress-time intervals (10, 30 and 60Ks) for $V_D = 0V$ (a), 6V (b) and 20V (c).



(a) (b) (c)

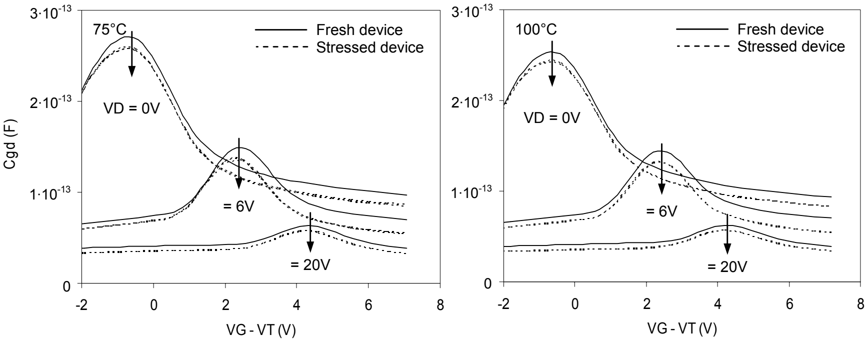
Figs. 5.54. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at 75°C from device under stress-A biases at several stress-time intervals (10, 30 and 60Ks) for $V_D = 0V$ (a), 6V (b) and 20V (c).



(a) (b) (c)

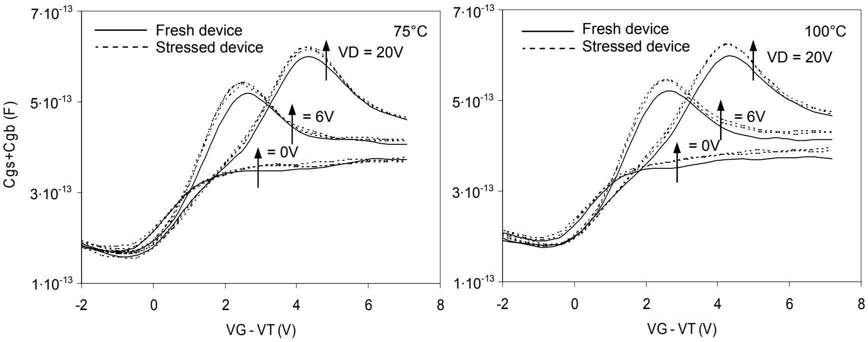
Figs. 5.55. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at 100°C from device under stress-A biases at several stress-time intervals (10,30 and 60Ks) for $V_D = 0V$ (a), 6V (b) and 20V (c).

When compared to stress-A conditions, devices subject to stress-B show with accumulated stress-time more important deteriorations of C_{GD} and $C_{GS}+C_{GB}$ capacitances measured at all stress-temperatures and V_D biases (Figs. 5.56 and 5.57). Referring to the maximum cumulated stress-time over temperature (30Ks at T = 100°C); extracted ΔC_{GD} at stress-temperatures 25, 75 and 100°C - denoted by grey triangles - indicates respectively for low V_D (0V) alterations around 13%, 10% and 9% (Figs. 5.58.a, 5.59.a and 5.60.a) and for high V_D (20V) variation between 9-10% (Figs. 5.58.c, 5.58.c and 5.69.c), while for intermediate V_D (6V) it shows at all temperatures a 16-17% change (Figs. 5.58.b, 5.59.b and 5.60.b).



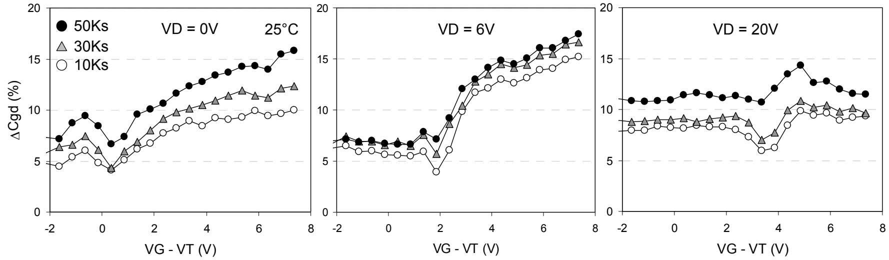
(a) *(b)*

Figs. 5.56. Extracted C_{GD} versus V_G-V_T characteristics under stress-B conditions for V_D= 0, 6 and 20V before (solid lines) and after (dashed lines) stressing at stress-temperatures: (a) 75°C (10, 30 and 50Ks stress-time) and (b) 100°C (10 and 30Ks stress-time).



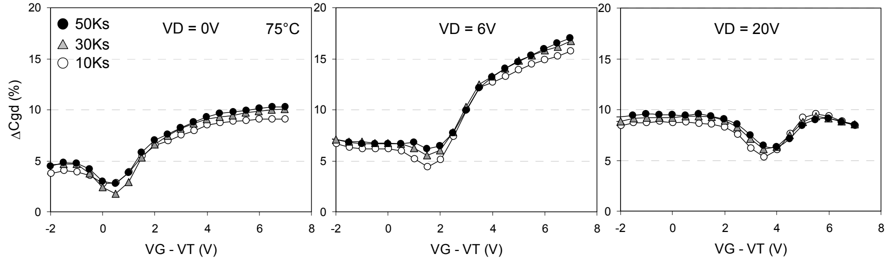
(a) *(b)*

Figs. 5.57. Extracted $C_{GS}+C_{GB}$ versus V_G-V_T characteristics under stress-B conditions for V_D= 0, 6 and 20V before (solid lines) and after (dashed lines) stressing at stress-temperatures: (a) 75°C (10, 30 and 50Ks stress-time) and (b) 100°C (10 and 30Ks stress-time).



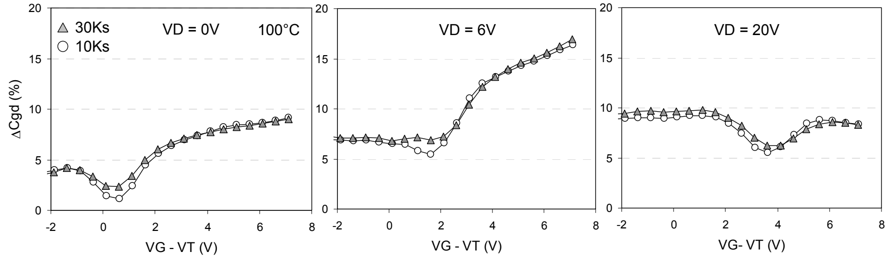
(a) *(b)* *(c)*

Fig. 5.58. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at room temperature from device under stress-B biases at several stress-time intervals (10, 30 and 50Ks) for V_D = 0V (a), 6V (b) and 20V (c).



(a) *(b)* *(c)*

Fig. 5.59. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at 75°C from device under stress-B biases at several stress-time intervals (10, 30 and 50Ks) for V_D = 0V (a), 6V (b) and 20V (c).



(a) *(b)* *(c)*

Fig. 5.60. Extracted ΔC_{GD} vs. V_G-V_T degradation characteristics at 100°C from device under stress-B biases at several stress-time intervals (10 and 30Ks) for V_D = 0V (a), 6V (b) and 20V (c).

5. 10. 4. Discussion of Hot Carrier Degradation Function of Temperature

5. 10. 4. 1. *Discussion of stress effect at maximum body current (stress-A)*

As reported previously for room-temperature (§ 5.9.3.a) stress-A biases show negligible effects on n-channel LDMOS DC and AC characteristics. However at higher temperatures some device deterioration becomes more visible and a temperature enhancement effect on device degradations experienced. For instance, extracted channel parameters have revealed a progressive deterioration in terms of mobility and on-resistance in all mode of operation (i.e. linear and saturation regimes (see Figs. 5.47.a, 5.48.a and 5.49.a), while the threshold and sub-threshold characteristics remains almost unchanged, confirming that the channel region is not affected by stress-A conditions at all investigated stress-temperatures. Change in capacitance measures (Figs. 5.53 – 5.55) maintain over temperature ΔC_{GD} tendency to vanish as V_D is raised, which confirms over temperature the drain bias control on the current path displacement within the drift volume; at high V_D electrons exit the channel-end and goes deep into the n-drift region, avoiding the bird's beak rich-defect area (see Fig. 5.32.b), while at low V_D electrons flow along the interface till the bird's beak end because of the dominant transversal electrical-field (see Figs. 5.32.a and 5.33.a).

From performed I_B-V_G measures over temperature (Fig. 5.36), I_B/I_D vs. V_G and $I_{B\text{-max}}$ vs. V_D at each stress-temperature are extracted and plotted in Figs. 5.37 and 5.38 respectively; the first out-coming observation is the reverse I_B-temperature dependence with respect to drain current I_D, which means for equivalent drain current I_D less body current I_B is generated as temperature rises. This is explained by the fact that less drain current is flowing within the structure as temperature rise up and therefore less hot-carrier are generated (source of I_B current). Considering the body current I_B and $I_{B\text{-max}}$ decreases with temperature (Figs. 5.36 – 5.38), less degradation, due to hot-holes-injection, would be expected when moving from 25°C to 100°C. This seems in contrast with increased capacitance degradation by a factor of four (×4) at higher temperature; as it can be noted from Figs. 5.53 – 5.55, for low $V_D = 0V$ extracted ΔC_{GD} at 25° after 60Ks stressing is equivalent to extracted ΔC_{GD} at 75° after only 10Ks; in turn after 60Ks stress-time ΔC_{GD} at 75° after 60Ks is almost equal to ΔC_{GD} extracted at 100° after 10Ks and this is thru for intermediate (6V) and higher V_D (20). This suggests that HC degradation is strongly enhanced by temperature; most probably by (i) *activating a larger amount of defects* at the bird's beak region despite the reduced number of generated hot-carriers, where positives activation energies of fast-interface-traps-formation is demonstrated to decrease with temperature [50], which suggests a thermally activated process assisting interface-trap-generation by hot-carriers at the interface or (ii) an enhancement of hydrogen related bond-breaking and diffusion processes, a probable source of D_{it}-generation [50]; released positive hydrogen species migrate under positive gate bias toward Si-SiO_2 interface and generate interface-traps upon their arrival at the interface [51]. In fact both interface-defect formations are temperature-enhanced mechanisms; their combinations are probable and thus could be a plausible explanation for reported HC-degradation enhanced by temperature.

5. 10. 4. 2. *Discussion of stress effect at maximum gate voltage (stress-B)*

Capacitance and DC analysis of stress-B over temperature shows severe degradations of the electrical parameters at the very early stage of stressing; after 10Ks of cumulative stress-time more than 80% of the total degradation is depicted from transfer and output characteristics and this at all investigated stress-temperature combinations. Mobility indicates a severe deterioration when temperature is raised from 25 to 100°C; after 30Ks stressing at 100°C mobility reaches ~13% alteration, which is the double and triple, for equivalent stress-time, for 75 and 25°C, respectively (Fig. 5.45.b). V_T shows more pronounced shifts with temperature; rising from ~2.2% at 25°C to double its value after only 30Ks stressing at 100°C (~4.4%, Fig. 5.46.b). Identically ΔS already altered by ~4% at 25°C rises to ~7% changes after a cumulative stress-time of 30Ks at 100°C (Fig. 5.47.b).

The surprised and unexpected parameter change is the on-resistance where for both linear and saturation regimes a reverse-dependence tendency is observed. ΔR_{ON}-lin and ΔR_{ON}-sat decrease as temperature rises. The stress impact on R_{ON} parameter is confirmed at each temperature but the change in the value of the parameter (ΔR_{ON}) appears less affected by applied stress at higher temperatures. In fact, the decrease in ΔR_{ON} tends to saturate with both stress-temperature and stress-time as it can be seen in Figs. 5.48.b and 5.49.b. Extracted gate-to-drain capacitances over temperature indicate a limited reduction observed for ΔC_{GD} when passing from 25 to 100°C. Figs. 5.58.a and 5.60.a show, after 30Ks stressing for $V_D = 0V$, a drop from ~12% (at 25°C) to ~9% (at 100°) and, for $V_D = 20V$, drops from ~11% at 25°C to ~9% at 100°C. It is very probable that the reported similarity in ΔR_{ON} and ΔC_{GD} have the same origin; however we have not been in measure to identify a clear physical explanation for such behaviour. As such observation is reported on DMOS transistors for the first time (as well as the presented capacitance degradation study over temperature) it was also impossible to correlate our findings with other published reports. This suggests the need of some additional experiments using various devices to confirm this effect and any correlations with the device geometry.

5. 11. CONCLUSION

In this chapter we have reported on the hot carrier impact on the DC and AC characteristics of DMOS transistor. Essentially, two stress conditions were selected and experimentally studied: (i) stress A, with a maximum drain voltage and a gate voltage corresponding to the maximum body current, and (ii) stress B, with maximum gate and drain voltages. We have found that for stress-A **the induced degradation takes place at LOCOS bird's beak area** and for stress-B **the induced degradation is at source-end gate oxide region**. In conclusion, the most relevant conditions of stress fro high-voltage devices could distinctively degrade the intrinsic channel or the drift region, highly depending on the operation conditions of the devices.

The same study allowed us to demonstrate, for the first time, that **the DMOS capacitance monitoring could be a much more sensitive tool that the pure DC parameter degradation induced by hot carriers**, at least for the conditions studied in this work. We believe that, in practice, the best method is to combine DC and AC measurements after cycles and applied stresses, which is the unique way to draw realistic conclusions about the main mechanisms of hot carrier degradation.

Finally, we have **originally studied the combined effect of stress and temperature of DMOS DC and AC characteristics**. In general, it is found that the temperature could significantly reinforce the effect of the applied stress (in conditions of similar applied electrical fields). However, in some particular cases we have been not able to fully explain some of the observed very complex trends, which necessitate further investigations. However, even in this very complex analysis, **only the measurement of the capacitance shift with applied stress and temperature combined with the DC parameters degradation**, allowed to draw some of the preliminary conclusions.

REFERENCES

[1] P. Perugupalli, M. Trividi, M. Kshnai and S. K. Leong, "*Modeling and Characterization of an 80V Silicon LDMOSFET for Emerging RFIC Applications,*" IEEE Transaction on Electron Devices, 1998, Vol. 45, pp. 1468 - 1478.

[2] G. Ma, W. Burger, C. Dragon and T. Gillenwater, "*High Efficiency LDMOS Power FET for low Voltage Wireless Communications,*" International Electron Device Meeting (IEDM), 1996, pp. 91 - 94.

[3] A. Wood, C. Dragon and W. Burger, "*High Performance Silicon LDMOS Technology for 2-GHz RF Power Amplifier Applications,*" International Electron Device Meeting (IEDM), 1996, pp. 87 - 90.

[4] M. S. Shekar, M. Cornell, R. K. Williams and M. Darwish, "*Optimization of 60V integrated Freewheeling Diode for Automotive 0.8 um BiCMOS/DMOS Technology,*" 10th International Symposium on Power Semiconductor Devices and ICs (ISPSD), 1998, pp. 62 – 72.

[5] C. Y. Tsai et al., "*16-60V rated LDMOS Show Advanced Performance in a 0.72 μm Evolution BiCMOS Power Technology,*" Proceeding of Electron Devices Meeting (IEDM), 1997, pp. 367-370.

[6] T. Terashima et al., "*Multi-Voltage Device Integration technique for 0.5 μm BiCMOS and DMOS Process,*" Proceeding of the International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2000, pp. 331-334.

[7] A. Pieracci and B. Ricco, "*A New Characterization Method for Hot-Carrier Degradation in DMOS Transistors,*" IEEE Transaction on Electron Device, 1998, Vol. 45, No. 8, pp. 1855 - 1998.

[8] C. T. Yao, M. Peckerar, D. Friedman and H. Hughes, "*On the Effect for Hot-Carrier Stressing on MOSFET Terminal Capacitances,*" IEEE Transaction on Electron Device, 1988, Vol. 35, No. 3, pp. 384 - 386.

[9] Y. T. Yeow, H. Ling and L. K. Ah, "*Observation of MOSFET Degradation Due to Electrical Stressing Through Gate-to-Source and Gate-to-Drain Capacitance Measurement,*" IEEE Electron Device Letters, 1991, Vol. 12, No. 7, pp. 366 - 368.

[10] R. Ghodsi, Y. T. Yeow, C. H. Ling and M. K. Alam, "*Arriving at a Unified Model for Hot-Carrier Degradation in MOSFET's Through Gate-to-Drain Capacitance Measurement,*" IEEE Transaction on Electron Device, 1994, Vol. 41, No. 12, pp. 2423 - 2429.

[11] C. H. Ling, S. E. Tan and D. S. Ang, "*A Study of Hot-Carrier Degradation in MOSFET'sby Gate Capacitacnes and Charge Pumping Current,*" IEEE Transaction on Electron Device, 1995, Vol. 42, No. 7, pp. 1321 - 1328.

[12] D. Esseni, A. Pieracci, M. Manrico and B. Ricco, "*Hot-Carrier-Induced Alterations of MOSFET Capacitances: A Quantitative Monitor for Electrical Degradation,*" IEEE Transaction on Electron Device, 1995, Vol. 45, No. 11, pp. 2319 - 2328.

[13] R. Versari, A. Pieracci, S. Manzini and B. Ricco, "*Hot-Carrier Reliability in Submicrometer LDMOS Transistors,*" International Electron Device Meeting (IEDM), 1997, pp. 371 - 374.

[14] V. O'Donovan, S. Whiston, A. Deignan and C. N. Chleirigh, "*Hot-Carrier Reliability of Lateral DMOS Transistors,*" 38th Anunual International Reliability Physics Symposium (IRPS), 2000, pp. 174 - 179.

[15] P. Moens, M. Tack, R. Degraeve and G. Groeseneken, "*A Novel Hot-Hole Injection Degradation Model for Lateral nDMOS Transistor,*" Proceeding of the International Electron Device Meeting (IEDM), 2001, pp. 877 - 880.

[16] D. Brisbin, A. Strachan and P. Chaparala, "*Hot Carrier Reliability of N-LDMOS Transistor Arrays for Power BiCMOS Applications,*" Proceeding of the 40t Annual International Reliability Physics Symposium (IRPS), 2002, pp. 105 - 110.

[17] P. Moens, M. Tack, R. Degraeve and G. Groeseneken, "*A Novel Hot-Hole Injection Degradation Model for Lateral nDMOS Transistor,*" International Electron Device Meeting (IEDM), 2201, pp. 877-880.

[18] P. Moens, G. Van den bosch and G. Groeseneken, "*Hot Carrier Degradation Phenomena in Lateral and Vertical DMOS Transistor,*" IEEE Transaction on Electron Device, 2004, Vol. 51, No. 4, pp. 623 - 628.

[19] P. Moens, G. Van den bosch and G. Groeseneken, "*Competing Hot Carrier Degradation Mechanisms in Lateral n-Type DMOS Transistor,*" Proceeding of the 41t Annual International Reliability Physics Symposium (IRPS), 2003, pp. 214 - 221.

[20] C. H. Ling, Y. T. Yeow and L.K.Ah, "*Characterization of Charge Trapping in Submicrometer NMSOFET's by Gate Capacitance Measurements,*" ," IEEE Transaction on Electronic Device, November 1992, Vol. 13, No. 11 pp. 587-589.

[21] F. gamiz, J. A. Lopez, J. Banqueri and J. E. Carceller, "*Influence of the Oxide-Charge Distribution Profile on Electron Mobility in MOSFET's,*" ," IEEE Transaction on Electronic Device, November 1992, Vol. 42, No. 5, pp. 999-1004.

[22] R. Ghodi and Y. T. Yeow, "*Hot-Carrier Induced Trapped Carriers and Interface in MOSFET0s Observed by Gate-to-Drain Capacitance Measurement,*" International Conference on Microelectronics and VLSI , 1995, pp. 242 – 245.

[23] C. H. Ling, B. P. Seah and C. H. Gan, "*Characterization of Charge Trapping in Submicrometer NMSOFET's by Gate Capacitance Measurements,*" ," IEEE Transaction on Electronic Device, May 1995, Vol. 42, No. 5, pp. 928-934.

[24] G. Ghibaudo, "*New Method for the Extraction of MOSFET Parameters*", Electronics Letter, Vol. 24, p.543, 1988.

[25] E. Strid, "*On-Wafer Calibration, Device Measurements and Modelling,*" Measurement Techniques for Microwave Device Characterization and Modelling, 1990, pp. 98 – 108.

[26] D. Williams, J. Pence and A Davidson, "*Comparison of On-Wafer Calibration,*" Conference Digest of 38th Automatic RF Techniques Group, December 1991.

[27] J. Pence, "*Verification of LRRM Calibration with Load Inductance Compensation for CPW Measurements on GaAs Substrates,*" Conference Digest of 42nd Automatic RF Techniques Group, November 1993.

[28] http://www.cascademicrotech.com/pubs/WINCAL-DS.pdf

[29] Cascade Microtech ISS product guide (P/N DS-803)

[30] J. jang, O. Tornblad, T. Arnborg, Q. Chen, K. Banerjee and Z. Yu, "*RF LDMOS Characterization and Its Compact Modeling*," IEEE MTT-S International Microwave Symposium Digest, 2001, pp. 967-970.

[31] T. E. Kolding, "*A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements,*" IEEE Transaction on Electronic Device, March 2000, Vol. 47, No. 4, pp. 734-740.

[32] S-S. Lu, C-C. Meng, T-W. Chen and H-C. Chen, "*A novel Interpretation of Transistor S-Parameters by Poles and Zeros for RF IC Circuit Design,*" IEEE Transactions on Microwave Theory and Techniques, February 2001, Vol. 49, No. 2, pp. 406-409.

[33] C. F. Campbell and S. A. Brown, "*An Analytical Method to Determine GaAs FET Parasitic Inductances and Drain Resistance Under Active Bias Conditions,*" IEEE Transactions on Microwave Theory and Techniques, 2001, Vol. 49, No. 7, pp. 1241-1247.

[34] T. E. Kolding, "*On-Wafer Calibration Techniques for Giga-Hertz CMOS Measurements,*" Proceeding of the International Conference on Microthecnic test Structures (ICMTS), 1999, Vol. 12, pp. 105-110.

[35] D. Lovelace, J. Costa and N. Camilleri, "*Extracting Small-Signal Model Parameters of Silicon MOSFET Transistors*," IEEE MTT-S International Microwave Symposium Digest, 1994, pp. 865-868.

[36] http://www.rfcafe.com/references/electrical/s-h-y-z.htm

[37] A pieracci, M. Lanzoni, P. Galbiati, S. Manzini, C. Contiero and B. Riccò, "*Extraction of Channel Doping Profile in DMOS Transistors,*" Technical Digest of Electron Devices Meeting (IEDM), 1996, pp. 485-488.

[38] N. V. D'halleweyn, L. F. tiemeijer, J. bensin and W. redman-White, "*Charge Model for SOI LDMOSFET with Lateral Doping Gradient,*" Proceeding of 2001 International Symposium on Power Semiconductor Devices and ICs (ISPSD), 2001, pp. 291-294.

[39] C. Anghel, "*High Voltage Devices for Standard MOS Technologies – Characterisation and Modelling*", Ph.D. Thesis No. 3116, Swiss Federal Institute of Technology, Lausanne (EPFL), Lausanne 2004.

[40] S. Aresu, W. De Ceuninck, G. Van den bosch, G. Groeseneken, P. Moens, J. Manca, D. Wojciechowski and P. Gassot, "*Evidence for source side injection hot carrier effects on Lateral DMOS transistors,*"

[41] P. Heremans, G. Van Den Bosch, R. Bellens, G. Groeseneken and H. E. Maes, "*Temperature Dependence of the Channel Hot-Carrier Degradation of n-Channel MOSFET's,*" IEEE Transaction on Electron Device, 1990, Vol. 37, No. 4, pp. 980 - 993.

[42] H. Hwang, J-S. Goo, H. Kwon and H. Shin, "*Anomalous Hot Carrier Degradation of nMOSFET's at Elevated Temperatures,*" IEEE Electron Device Letters, 1995, Vol. 16, No. 4, pp. 148 - 150.

[43] P. Aminzadeh, M. Alavi and D. Scharfetter, "*Temperature Dependence of Substrate Current and Hot Carrier-Induced Degradation at Low Drain Bias,*" Symposium on VLSI Technology Digest, 1998, pp. 178-179.

[44] E. Li, E. Rosenbaum, L. F. Register, J. Tao and P. Fang, "*Hot Carrier Degradation in Deep Submicron MOSFETs at 100°C,*" Proceeding of the 38th Annual International Reliability Physics Symposium (IRPS), 2000, pp. 103 - 107.

[45] W-K. Yeh, W-H. Wang, Y-K. Fang and F-L. Yang, "*Temperature Dependence of Hot-Carrier-Induced Degradation in 0.1μm SOI nMOSFETs With Thin Oxide,*" IEEE Electron Device Letters, 2002, Vol. 23, No. 7, pp. 425 - 427.

[46] W-K. Yeh, W-H. Wang, Y-K. Fang and F-L. Yang, "*Temperature Dependence of Hot-Carrier Degradation in Silicon-on-Insulator Dynamic Threshold Voltage MOS Transistors,*" IEEE Electron Device Letters, 2002, Vol. 23, No. 11, pp. 673 - 675.

[47] G. M. Dolny, G. E. Nostrand and K. E. Hill, *"The Effect of Temperature on Lateral DMOS Transistors in a Power IC Technology,"* IEEE Transactions of Electron Devices, 1992, Vol. 38, No. 4, pp. 990 - 995.

[48] N. D. Arora and G. Sh. Gildenblat, *"A Semi-Empirical Model of the MOSFET Inversion Layer Mobility for Low-Temperature Operation,"* IEEE Transactions of Electron Devices, 1987, Vol. ED-34, pp. 89 - 93.

[49] G. Baccarini, A. M. Mazzoni and C. Monradi, *"The Diffused Scattering Model of Effective Mobility in the Strongly Inverted Layer of MOS Transistors,"* Solid-States Electronics, 1974, Vol. 17, pp. 785 - 788.

[50] C. –H. Hsu, D. –S. Wen, M. R. Wordeman, Y. Taur and H. Ning, *"A Comprehensive Study of Hot-Carrier Instability in P- and N-Type Poly-SI Gateed MOSFET's,"* IEEE Transactions of Electron Devices, 1994, Vol. 38, No. 4, pp. 675 - 680.

[51] P. Aminzafeh, M. Alavi and D. Scharfetter, *"Temperature dependence of Substrate Current and Hot Carrier-Induced Degradation at Low Drain Bias,"* IEEE Technical Digest of VLSI Symposium, 1998, pp. 178 - 179.

Final Conclusion

With the work reported in this manuscript we have essentially contributed to the electrical characterization and modelling of high voltage MOSFETs, more particularly DMOS architectures such as X-DMOS and L-DMOS able to sustain voltages ranging from 30V to 100V. The technology information and the investigated devices have been kindly provided by AMIS, Belgium (former Alcatel Microelectronics).

In general, all the initial defined targets in term of the orientation of our work, as defined in the introduction chapter, have been maintain along the progress of the work. However, sometimes, based on the obtained results we have decided to pay more attention to some less explored topics such as the hot carrier impact of DMOS capacitances and the combine effect of stress and temperature, which initially were not among the planned activities.

We believe that we have contributed to some of the planned targets, as following:

- In Chapter 2, the extensive investigation of the equivalent numerically simulated (TCAD) DMOS structures was at the origin **of the intrinsic-drain voltage concept**, which revealed a good basis of analysis of the most significant bias dependent characteristics and phenomena related to HV-DMOS architectures.
- In Chapter 3, we **experimentally validated the concept of intrinsic drain voltage** (or K-point) proposed in Chapter 2 **and its use for the DC and AC modelling of HV devices using the MESDRIFT structure** provided by our industrial partner. In fact, despite the limitations associated with a non-ideal probe contact of this structure, in some of the investigated regimes (such as accumulation in the drift), the agreement between numerical simulation and measurement was very good for V_K. The importance of this concept overpasses the frame of our work, being usable for many other types of devices.
- In the same Chapter 3 we proposed an **original mathematical yet quasi-empirical formulation for the bias-dependent drift series resistance of DMOS transistor, which is very accurate for modelling all the regimes of operation of the high voltage device**. We combined for the first time such a model with EKV low voltage MOSFET model developed at EPFL.
- In Chapter 4, we have proposed **models for the capacitances of high voltage devices** at two levels: **equivalent circuits for small signal operation based on VK-concept** and **large signal charge-based models**. These models capture the main physical charge distribution in the device but they are less adapted for fast circuit simulation and still remain subject to further improvement. It is more appropriate to consider them as initial basis for DMOS capacitance modelling.
- In Chapter 5 we have **originally contributed to the investigation of hot carrier effects on DC and AC characteristics of DMOS transistors**, with **key emphasis on the degradation of transistor capacitances and the influence of the temperature**. At our knowledge, our work reported in this chapter is among the first reports existing in this field. We have essentially shown that the monitoring of capacitance degradation if mandatory for a deep understanding of the degradation mechanisms and, in conjunction with DC parameter degradation, could offer correct insights for reliability issues. Even more**, we have shown situations (by comparing two fundamental types of stresses) when the capacitance degradation method by HC is much more sensitive than DC parameter degradation method**. Of course, some of the combined stress-temperature investigations were too complex to find very coherent explications for all the observed effect, knowing that in the most recent literature very few works related to the topic are available. However, our works

stress out the interest and significance of such an approach for defining the SOA of high voltage devices, in general.

Overall, our work can be considered as placed at the interface between electrical characterization and modelling of high voltage devices emerging from conventional low voltage CMOS technology, continuing the research tradition in the field established at the Electronics laboratory (LEG) of EPF Lausanne.

APPENDIX

List of Publications

1. N. Hefyene, C. Anghel, R. Gillon and A. M. Ionescu, “Hot Carrier Degradation of Lateral DMOS transistor Capacitance and reliability Issues”, International Reliability Symposium (IRPS), 2005, to be published.
2. A. M. Ionescu, D. Munteanu, N. Hefyene, C. Anghel, “Compact Modeling of Weak Inversion Generation Transients in SOI MOSFETs”, J. of The Electrochemical Society, Vol. 151, No. 6, pp. G396-G401, 2004.
3. C. Anghel, N. Hefyene, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, A.M. Ionescu, “Electrical characterisation of high voltage MOSFETs using MESDRIFT”, International Semiconductor Conference, CAS, Vol. 2, pp. 257 – 260, 2003.
4. C. Anghel, N. Hefyene, S.F. Frère, R. Gillon, J. Rhayem, A. Ionescu, "Universal Test Structure and Characterization Method for Bias-Dependent Drift Series Resistance of HV MOSFETs", Proc. of European Solid-State Device Research Conf., ESSDERC, pp. 247 – 250, 2002.
5. N. Hefyene, E. Vestiel, B. Bakeroot, C. Anghel, S. Frere, A.M. Ionescu, R. Gillon, “Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HVMOSFET”, Proc of Int. Conf. on Simulation of Semiconductor Processes and Devices, SISPAD, pp. 203 – 206, 2002.
6. N. Hefyene, J.M. Sallese, C. Anghel, A.M. Ionescu, S.F. Frere, R. Gillon, “EKV compact model extension for HV lateral DMOS transistors”, Proc. of Int. Conf. on Advanced Semiconductor Devices and Microsystems, ASDAM, pp. 345 – 348, 2002.
7. C. Anghel, N. Hefyene, A.M. Ionescu, M. Vermandel, B. Bakeroot, J. Doutreloigne, R. Gillon, S. Frere, C. Maier, Y. Mourier, "Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage", Proc. of European Solid-State Device Research Conf., ESSDERC, pp. 399 – 402, 2001.
8. N. Hefyene, C. Anghel, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot, J. Doutreloigne, "An Experimantal Approach for Bias-Dependent Drain Series Resistances Evaluation in Asymmetric HV MOSFETs", Proc. of European Solid-State Device Research Conf., ESSDERC, pp. 403 – 406, 2001.
9. C. Anghel, N. Hefyene, A. M. Ionescu, M. Declercq, J. W. Tringe, J. D. Plummer, "Pseudo-MOS Operation of Ultra-Narrow Polysilicon Wires: Electrical Characterisation and Memory Effects", Proc. of Materials Research Society, MRS, F12.4, 2000.

Nasser Hefyene

Material and Microelectronic Engineer

Av. Recordon 44, CH-1004 Lausanne

+41 21 693 39 71 (Office)
+41 21 693 36 40 (Fax)

naser.hefyene@epfl.ch

CITIZENSHIP AND LANGUAGES

- Libyan Citizen
- French: Native Tongue
- Arabic: Mother Tongue
- English: Fluent

FIELD OF INTEREST

- Microelectronics and Nanotechnologies
- Material physics

RESEARCH EXPERIENCE

- **Experimental evaluation of Nano-scale MOSFET transistors** 2004-2005
  NESTOR European project with Phillips, Enfineon and ST-Microelectronics
  Contact: Prof. Adrian M. Ionescu; EPFL, Adrian.Ionescu@epfl.ch

- **Characterization and Modelling of High-Voltage MOSFET transistors** 09/00-01/04
  AUTOMACS European project with AMIS, BOSCH and SILVACO
  Contact: Prof. Adrian M. Ionescu; EPFL, Adrian.Ionescu@epfl.ch

- **High-temperature evaluation and BSIM Modelling of Lateral DMOS transistor** 03/00-09/04
  Mandated by ALCATEL
  Contact: Prof. Adrian M. Ionescu; EPFL, Adrian.Ionescu@epfl.ch

- **Characterization of Ultra-thin SOS (Silicon-On-Sapphire) material** 09/99-03/00
  Mandated by ASAHI-KASEI Chemical, Japan
  Contact: Dr. Sorin Cristoloveanu; LPCS, ENSERG; sorin@enserg.fr

- **Experimental evaluation of SOI (Silicon-On-Insulator) Unibond@ material and Ultra-thin SOI-MOSFET transistors** 03/99-09/99
  Master graduation project
  Contact: Dr. Sorin Cristoloveanu; LPCS, ENSERG; sorin@enserg.fr

- **Feasibility study of micro surface-alloying of the Al-Cu system with Nd-Yag Laser** 03/95-05/96
  College (B.S) graduation project

- **Dental materials and alloys** 03/94-07/94
  Under-graduation project; Material selection and Economy course

TECHNICAL SKILLS

- Testing laboratory: Micro-device characterization (e.g. I-V, C-V, S-parameters techniques, charge pumping, stress and aging).

INDUSTRIAL EXPERIENCE

- **Junior Field Engineer training** 05/96-12/97
  SCHLUMBERGER Overseas Ltd., Wireline & Testing division, Italy, Lybia, Gabon and UK

TEACHING EXPERIENCE

- **Lab and Exercise assistance,** 2000-2004
  EPFL, STI-IMM-LEG, Lausanne, Switzerland

COMPUTER AND GRAPHICS EXPERIENCE

- **Mathematical Solvers;** Mathematica, Mathcad, Matlab
  Graphics Solvers; Adobe Illustrator, Photoshop

EDUCATION

- **Ph.D.**
  Solid state physics and devices: "*Electrical Characterization and Modelling of Lateral DMOS transistor – Investigation of Capacitance and Hot Carrier Impact* 2001-2005
  EPFL, STI-IMM-LEG, Lausanne, Switzerland

- **M.S.**
  Solid state physics
  Joseph Fourier University/INPG, Grenoble, France 1998-1999

- **B.S.**
  Material Science Department, Engineer Faculty,
  El-Fatah University, Tripoli, Libya 1991-1996

PERSONAL

- **Sports:** Fitness, Tennis, Tennis table
- **Arts:** Photography, Drawing, Design, Event Organization