# INVESTIGATION AND CONTROL OF A HYBRID ASYMMETRIC MULTI-LEVEL INVERTER FOR MEDIUM-VOLTAGE APPLICATIONS

THÈSE N$^{O}$ 2846 (2003)

PRÉSENTÉE À LA FACULTÉ SCIENCES ET TECHNIQUES DE L'INGÉNIEUR

Institut des sciences de l'énergie

SECTION D'ÉLECTRICITÉ

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES TECHNIQUES

PAR

Martin VEENSTRA

Master of Science in Electrical Engineering, Delft University of Technology, Pays-Bas
et de nationalité néerlandaise

acceptée sur proposition du jury:

Prof. A.-Ch. Rufer, directeur de thèse
Prof. R. Lorenz, rapporteur
Dr T. Meynard, rapporteur
Prof. J.-J. Simond, rapporteur
Dr P. Steimer, rapporteur

Lausanne, EPFL
2003

# Preface

In the final phase of my studies at Delft University of Technology, I performed 4 months practical work at ABB Corporate Research, which led to my employment as a Research Engineer in the same company immediately after my graduation in 1995. During the following 3 years, I gained a lot of industrial experience from my colleagues and the variety of projects we worked on, all in the field of high-power drives for traction or industrial applications. A job rotation at ABB Industry resulted in the proposal for an industrial Ph.D. research topic, which I eagerly accepted.

This dissertation has been carried out in the years 1998 through 2003 during my employment as Assistant-Doctorant under Prof. Alfred Rufer, director of the Laboratoire d'Électronique Industrielle at the École Polytechnique Fédérale de Lausanne. The topic of this thesis is a collaboration with ABB Industry as industrial partner.

I sincerely thank Prof. Alfred Rufer for accepting me as doctoral student. His strict confidence, availability and full support throughout the whole period of my research work, towards me personally and in managing the laboratory as a whole, together with his openness to new ideas, created the nutritious environment in which the obtained results could grow.

Special thanks go to Dr. Peter Steimer of ABB Industry for supporting this research project. His proposal of the subject and financial contribution were the basis for this dissertation, and our fruitful collaboration resulted in a patent.

I wish to thank the President of the Board of Examiners Prof. Juan Mosig and its Members Prof. Alfred Rufer, Prof. Jean-Jaques Simond, Prof. Robert Lorenz, Dr. Peter Steimer and Dr. Thierry Meynard for their valuable participation in the exam.

My thanks are equally addressed to all the members of the Laboratoire d'Électronique Industrielle for their support and the pleasant atmosphere they create in the lab. The administrative and technical assistance of Fabienne Vionnet, Roberto Zoia and Yves Birbaum form a great and appreciated relief

in the daily work. Special thanks go to Sébastien Mariéthoz for our exhaustive and instructive discussions on a wide range of technical topics and the fruitful collaboration in the realization of hardware for our laboratory prototypes. I also wish to thank Dr. Philippe Barrade for reading the manuscript and commenting it with valuable remarks in an incredibly short time.

Finally, I address my sincere thanks to my parents and my friends, whether living around the corner or hundreds of kilometers away. Their constant support and their encouragement in difficult moments has been an important contribution in the realization of this work. Their presence for writing, talking or undertaking social activities and mountain tours gave me the energy to finish this project as it is.

September 2003,
Martin Veenstra

# Abstract

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. However, the existing solutions suffer from some important drawbacks.

Hybrid asymmetric multi-level inverters promise significant improvements for medium-voltage applications. This dissertation investigates such a hybrid inverter. To simplify the topology, some inverter parts are deprived of their feeding from the net and can only supply reactive power. The non-supplied intermediate-circuit capacitor voltages are inherently unstable and require a suitable control method for converter operation, preferably without influence on the load. Apart from normal operation, also converter start-up is an issue to consider, for which it is desirable to limit additional equipment.

In this dissertation, we investigate the behaviour of this new inverter, and develop methods to obtain its reliable operation for the considered applications. These methods include modulation, voltage stabilization and start-up. We establish suitable models for their foundation.

The principle achievement of this work is the development of a control method to stabilize a multitude of capacitor voltages which have no equilibrium state. Power balancing is performed by varying the common-mode output voltage, using a non-linear model-predictive controller. This method, which is new to power electronics, is applied to our hybrid asymmetric nine-level inverter driving an asynchronous motor. Computer simulations and measurements on an experimental drive system demonstrate stable behaviour in steady-state and during transients over the whole operating range. The obtained results prove the possible implementation of such a complex control algorithm for fast real-time operation.

As second important accomplishment, this thesis proposes a start-up method that charges the non-supplied intermediate-circuit capacitors in parallel with the supplied ones, without additional equipment. Measurements show its successful application in the investigated drive system.

# Résumé

Les onduleurs de l'électronique de puissance gagnent en popularité pour diverses applications d'entraînements industriels. Au cours des dernières années, des applications moyenne tension de forte puissance ont également été installées. Cependant, les solutions existantes souffrent de certains inconvénients majeurs.

Les onduleurs multiniveaux asymmétriques hybrides promettent des améliorations considérables pour les applications moyenne tension. Cette thèse examine un tel onduleur hybride. Afin de simplifier la topologie, certaines parties de l'onduleur sont privées de leur alimentation réseau, et ne peuvent fournir que de la puissance réactive. Les tensions des condensateurs aux circuits-intermédiaires non-alimentés sont instables et requièrent une méthode de contrôle adéquate afin de permettre le fonctionnement du convertisseur, de préférence sans influence sur la charge. Indépendament du fonctionnement normal, le démarrage du convertisseur est également un sujet à étudier, pour lequel on souhaite limiter les équipements supplémentaires.

Dans cette thèse, nous étudions le comportement de ce nouvel onduleur, et nous développons des méthodes afin d'obtenir un fonctionnement fiable pour les applications envisagées. Ces méthodes incluent la modulation, la stabilisation des tensions et le démarrage. Nous établissons des modèles appropriés pour leur fondement.

Le résultat principal de ce travail est le développement d'une méthode de réglage pour stabiliser une multitude de tensions de condensateur n'ayant pas d'état d'équilibre. L'équilibrage des puissances est effectué par la variation de la composante homopolaire des tensions de sortie, en utilisant un régulateur prédictif non-linéaire. Cette méthode, qui est nouvelle dans le domaine de l'électronique de puissance, est appliquée à notre onduleur neuf-niveaux asymmétrique hybride entraînant un moteur asynchrone. Des simulations sur ordinateur ainsi que des mesures sur un système d'entraînement expérimental démontrent un comportement stable sur toute la plage de fonctionnement, aussi bien en régime stationnaire qu'en régime transitoire. Les résultats obte-

nus prouvent l'implémantation possible en temps réel rapide d'un algorithme fort complexe.

Comme deuxième résultat important, cette thèse propose une méthode de démarrage qui pré-charge les condensateurs aux circuits-intermédiaires non-alimentés en parallèle avec ceux alimentés, sans équipement supplémentaire. Des mesures montrent sa mise en oeuvre réussie sur le système d'entraînement étudié.

# Zusammenfassung

Leistungselektronische Umrichter gewinnen an Beliebtheit für verschiedenste industrielle Antriebe. In den letzten Jahren wurden ebenfalls Hochleistungs- und Mittelspannungsantriebe installiert. Die bestehenden Lösungen leiden jedoch unter einige wichtige Nachteile.

Hybride asymmetrische Mehrstufenumrichter versprechen wichtige Verbesserungen für Mittelspannungsanwendungen. Diese Dissertation untersucht einen solchen Hybridumrichter. Um den Leistungsteil zu vereinfachen werden einige Umrichterteile von ihren Netzspeisungen beraubt, weswegen sie nur noch Blindleistung liefern können. Die Spannungen der nichtgespiesenen Zwischenkreiskondensatoren sind unstabil und verlangen ein geeignetes Regelungsverfahren für den Umrichterbetrieb, vorzugsweise ohne Einfluss auf die Last. Neben dem Normalbetrieb ist auch der Aufstart des Umrichters ein wichtiges Thema, wofür zusätzliche Ausrüstung beschränkt werden sollte.

In dieser Dissertation untersuchen wir das Verhalten dieses neuen Umrichters und entwickeln ein Verfahren zwecks Ermöglichung seines zuverlässigen Betriebs für die betrachteten Anwendungen. Diese Verfahren beinhalten Modulierung, Spannungsstabilisierung und Aufstart. Wir leiten geeignete Modelle zu deren Fundierung her.

Das wichtigste ergebnis dieser Arbeit ist die Entwicklung eines Regelungsverfahrens zwecks Stabilisierung einer Mehrzahl von Kondensatorspannungen die keinen Gleichgewichtszustand haben. Der Leistungsausgleich wird erreicht durch variieren der Homopolarspannungskomponente am Umrichterausgang, unter Verwendung eines nichtlinearen Vorhersagereglers. Dieses Verfahren, das neu ist in der Leistungselektronik, wird auf unserem hybriden asymmetrischen Neunstufenumrichter angewand, der einen Asynchronmotor antreibt. Computersimulationen und Messungen an einem experimentellen Antriebssystem demonstrieren ein stabiles Verhalten im ganzen Drehzahlbereich, sowohl im stationären wie im transienten Betrieb. Die erzielten Ergebnisse beweisen die mögliche Implementierung solch ein komplexes Regelverfahren für schnellen Echtzeitbetrieb.

Als zweites wichtiges Ergebnis schlägt diese Abhandlung ein Aufstartverfahren vor, das die nichtgespiesenen Zwischenkreiskondensatorspannungen parallel zu den gespiesenen auflädt, ohne zusätzliche Ausrüstung. Messungen zeigen seine erfolgreiche Anwendung auf das untersuchte Antriebssystem.

# Contents

# Chapter 1

# Introduction

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed [1, 2]. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years [3–6]. However, the increasing number of devices tends to reduce the overall reliability and efficiency of the power converter. On the other hand, solutions with a low number of devices either need a rather large and expensive $LC$ output filter to limit the motor-winding insulation stress, or can only be used with motors that do withstand such stress.

## 1.1 Asymmetric and Hybrid Multi-Level Inverters

Asymmetric multi-level inverters use different intermediate-circuit capacitor voltages in various parts of the inverter. By addition and subtraction of these voltages, more different output-voltage levels can be generated with the same number of components, compared to a symmetric multi-level inverter [7–9]. Higher output quality can be obtained with smaller circuit and control complexity, and output filters can be remarkably shrunk or even eliminated.

The various parts of an asymmetric multi-level inverter execute different functions in the power conversion. Equipped with several different semiconductor devices, a hybrid converter exploits their individual advantages and

strengths [10–13]. The main power is supplied with high reliability and low losses by one device, the output harmonic content is reduced by an other. By using state-of-the-art semiconductor devices, this can lead to a better overall design for medium-voltage drives.

In order to further simplify the power part and increase the efficiency of such a converter, we can remove some of the power supplies and let those parts of the converter supply only reactive power [14–16]. We obtain a very interesting solution in terms of power quality, efficiency, reliability and cost.

However, the resulting system is unstable, and without control the non-supplied intermediate-circuit capacitor voltages will quickly run away from their nominal values. An appropriate converter control method is needed to stabilize those voltages, preferably without deteriorating the output voltage. In general, this can not be done instantaneously by lack of an equilibrium state, but only on an average in time. Apart from normal operation, also the pre-charging of the non-supplied intermediate-circuit capacitors upon converter start-up is an issue to consider.

## 1.2 Subject of the Dissertation

This dissertation investigates a hybrid asymmetric multi-level inverter which promises significant improvements for medium-voltage drives. It consists of a three-phase three-level IGCT inverter (main inverter), with a two-phase two-level IGBT inverter (sub inverter) in series with each phase (see Figure 1.1) [14–16]. Integrated gate-commutated thyristors (IGCT) with a high voltage-blocking capability are used to provide the main power with high reliability and low losses [17–19], insulated-gate bipolar transistors (IGBT) with a higher switching-frequency capability are used to reduce the output harmonic content. We will use a ratio of 3 between the intermediate-circuit capacitor voltages of the main and the sub inverter to obtain a maximum of output-voltage levels. By addition and subtraction of these voltages, nine different output-voltage levels can be generated.

The main inverter is fed from the net by a twelve-pulse transformer and diode rectifier. As an alternative, a back-to-back configuration with a second hybrid inverter, serving as active rectifier, is possible as well [14].

To keep the power part simple and the efficiency high, the sub inverters have *no* feeding from the net. They can only supply reactive power, which *must* be assured by appropriate converter control. Moreover, also the main-inverter neutral-point, which lacks supply by a power source too, must be kept balanced.

To avoid additional cost and reduced reliability, additional pre-charging

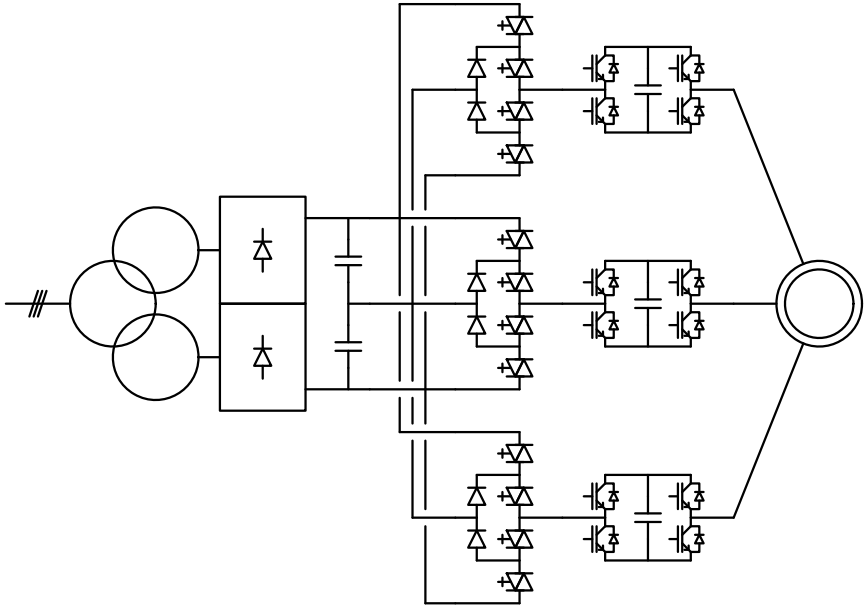


Figure 1.1: Circuit diagram of the hybrid inverter in a medium-voltage drive application. The three sub-inverter intermediate circuits are *not* supplied by a power source.

equipment should be kept minimal. The main inverter can be pre-charged in a usual way, using a set of pre-charge resistors along with a bypass switch on the AC or the DC side of the transformer and rectifiers. Pre-charging of the sub inverters can not be accomplished in such a manner. It is, however, desirable to avoid additional equipment and to dispose of an other method to perform this task.

The main goals of this dissertation are a thorough understanding of the behaviour of this new inverter, and the development of methods to obtain its reliable operation for the considered applications. The principle topics to be studied are described in the following section.

## 1.3 Outline of the Dissertation

In Chapter 2, we will take a brief look at existing inverter topologies and new research fields. We will discuss the main advantages and disadvantages of

those solutions. Based on this, the power-part topology of a hybrid asymmetric multi-level inverter for medium-voltage industrial drives will be synthesized. It promises to be a simple and reliable circuit with a good output quality and high efficiency.

Different modulation methods exist to generate appropriate output voltages with a voltage-source inverter. We will investigate the widely used and well-known pulse-width modulation (PWM) methods in Chapter 3. Many variants exist, especially for multi-level inverters. We will discuss some properties and choose a modulator for our hybrid asymmetric multi-level inverter.

In Chapter 4, we will study the common mode and the differential mode of voltages and currents in three-phase power systems. As we will see in the following chapters, these aspects are of great importance to our system. We will define a transform matrix to change between phase quantities and their corresponding common and differential modes. As an illustration, we will apply the transform to some relevant signals of a nine-level inverter: the inverter output-states voltages, and the reference and output signals of its pulse-width modulator. Finally, for the purpose of our future control, we will investigate varying common mode at fixed differential mode.

In order to properly control an inverter, we must thoroughly understand its behavior. Especially the switched-mode behavior of power-electronic inverters can make its modeling difficult. Chapter 5 starts with an exact description of ideal switches. Based on this, we will derive an approximate switch model under PWM control, neglecting the switching behavior and taking only average values over a switching interval into account. Using such switch models, we will construct a model of our hybrid asymmetric multi-level inverter. Especially the intermediate-circuit capacitor voltages will be of our interest, since we need a control algorithm to stabilize them. We will focus at the influence of the possible common-mode voltages, because—as we will learn in Chapter 6—this stabilization can be done by adding an appropriate common-mode component to the output voltage.

Since the main-inverter neutral point and the three sub-inverter intermediate circuits are not supplied by a power source, their capacitor voltages have to be stabilized by an appropriate control algorithm, preferably without deteriorating the output voltage. This system is unstable, and without control the non-supplied intermediate-circuit capacitor voltages will quickly run away from their nominal values. Chapter 6 describes methods to affect the capacitor voltages without influence on the load, and analyzes their properties. Based on these insights, we propose a strategy to accomplish the desired control. We will show how this strategy can be applied to stabilize the capacitor voltages in our hybrid inverter.

For the development of the models, methods and strategies proposed in the

previous chapters, extensive use of computer calculations and simulations has been employed. In order to validate the obtained results, a low-voltage laboratory prototype of a hybrid-inverter drive system has been built and tested. Chapter 7 describes the design of our hybrid inverter in a drive application. We will discuss its implementation in a simulation model, together with the obtained results. The realization of a laboratory prototype required adaptations in the controller design, which we will comment. The prototype has been subjected to extensive tests, whose results are presented and discussed.

In Chapter 8, we will propose a special pre-charge method for our hybrid inverter. The main inverter (NPC topology) is pre-charged in a usual way via a set of pre-charge resistors along with a bypass contactor, either on the AC or the DC side of the transformer and rectifiers. The sub-inverter intermediate-circuit capacitors are charged in parallel to and together with those of the main inverter, by exploiting certain inverter switching configurations. Measurements show its successful application in the proposed drive system.

# Chapter 2

# Power-Part Topology

Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed [1, 2]. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years [3–6]. However, the increasing number of devices tends to reduce the overall reliability and efficiency of the power converter. On the other hand, solutions with a low number of devices either need a rather large and expensive $LC$ output filter to limit the motor-winding insulation stress, or can only be used with motors that do withstand such stress.

In this chapter, we will take a brief look at existing inverter topologies and new research fields. We will discuss the main advantages and disadvantages of those solutions. Based on this, the power-part topology of a hybrid asymmetric multi-level inverter for medium-voltage industrial drives will be synthesized. It promises to be a simple and reliable circuit with a good output quality and high efficiency.

## 2.1 Multi-Level Inverters

In this section, we will discuss the most important multi-level inverter topologies and their properties. First, we will look at the well-known symmetric multi-level inverter topologies. Second, we will regard the emerging field of asymmetric multi-level inverters.

### 2.1.1 Symmetric Multi-Level Inverters

Multi-level inverters are known since several decades [3]. The well-known circuit topologies are:

- series-connected H-bridges inverter (SHB);
- neutral-points clamped inverter (NPC);
- imbricated-cells inverter (IC).

Their properties are briefly discussed in the following. A generalized multi-level topology, which combines the topologies of NPC and IC inverters, is described in [6].

Multi-level inverters are characterized by the number of different output-voltage levels that can be generated by the inverter. Any inverter that generates more than two output-voltage levels is called a multi-level inverter. Although mostly an odd number of levels is chosen, even numbers are possible as well.

The classical solutions are called symmetric multi-level inverters, because they have the same voltage on each of the intermediate-circuit capacitors, and all the power semiconductors have to be capable to block this same voltage in their 'off' state. A value corresponding to the chosen technology is used. Series connection of components is needed where multiples of this voltage occur. This is the case for NPC and IC converters of more than three levels. As can be deduced from the generalized topology [6], series connection of equivalent diodes or capacitors is related to their clamping of multiple switches.

#### Series-Connected H-Bridges Inverter

Figure 2.1 shows the circuit diagram of a 5-level series-connected H-bridges inverter [1, 5, 20, 21]. For clarity, only one phase is drawn. The power semiconductors form H-bridges, which are connected in series. The number of active semiconductors is proportional to the number of levels.

Each H-bridge has its own intermediate-circuit capacitor, which are at different and varying potentials. As a consequence, the circuit needs an isolated

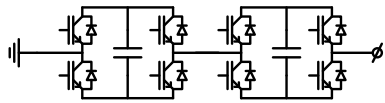


Figure 2.1: Phase circuit diagram of a 5-level SHB inverter.

power supply for each DC link. The number of intermediate-circuit capacitors, and thus of independent power supplies, is proportional to the number of levels.

The ground symbol shows a common (for all phases) reference point, where the phases are connected together. Each H-bridge can generate a positive, a negative or a zero voltage. The total output voltage is the sum of the individual H-bridge voltages. The possible output voltages are thus symmetric around zero, and zero voltage can be generated as well. The number of output-voltage level is therefore always odd.

The high number of isolated power supplies, using either low- or medium-frequency transformers, tend to make the circuit rather complex. Since the converter consists basically of three independent single-phase converters, no (reactive) power can be directly exchanged between the phases. It must either be stored in the intermediate circuits—which increases their capacitor size—, or exchanged via active rectifiers and the transformer—which increases losses.

A similar converter is obtained by parallel connection of the H-bridges on their DC side and a series connection via independent transformer windings on their AC side [22,23]. In this case, a single power supply feeds the common DC link.

### Neutral-Points Clamped Inverter

Figure 2.2 shows the circuit diagram of a 5-level neutral-points clamped inverter [4,24]. For clarity, only one phase is drawn. The power semiconductors are connected in series. The intermediate circuit is divided into several parts, whose so called neutral points can be connected to the output via the clamp-

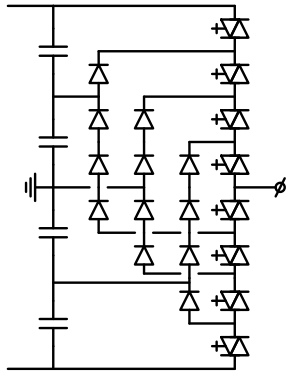


Figure 2.2: Phase circuit diagram of a 5-level NPC inverter.

ing diodes. Series connection of clamping diodes is necessary, assumed they have the same voltage-blocking capability as the power semiconductors. The number of active semiconductors is proportional to the number of levels, the number of clamping diodes, however, is proportional to its square.

The intermediate-circuit capacitors are common for all phases. As a consequence, the circuit needs only one power supply for the total DC link. Moreover, (reactive) power can be freely exchanged between the phases without additional losses. The number of intermediate-circuit capacitors is proportional to the number of levels.

The ground symbol shows a common (for all phases) reference point in the middle of the DC link. The possible output voltages are thus symmetric around zero. In case the circuit has an even number of levels, and thus an odd number of intermediate-circuit capacitors, this reference point must be artificially constructed.

Component load is not equally distributed within the converter, both for the semiconductors and the capacitors, which complicates converter design. The stabilization of the capacitor voltages is problematic. Although a new approach proposes to overcome this problem [25], it rises new issues which limit its application.

### Imbricated-Cells Inverter

Figure 2.3 shows the circuit diagram of a 5-level imbricated-cells inverter [26, 27]. For clarity, only one phase is drawn. The power semiconductors are connected in series. Their connection points are clamped by additional ca-

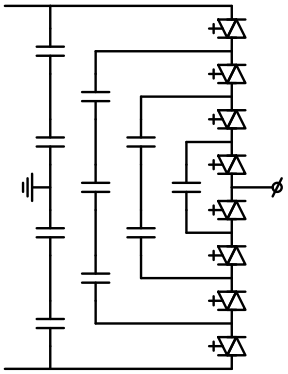


Figure 2.3: Phase circuit diagram of a 5-level IC inverter.

pacitors. Series connection of clamping capacitors is necessary, assumed they have the same voltage rating as the power semiconductors. The number of active semiconductors is proportional to the number of levels, the number of clamping capacitors, however, is proportional to its square.

The intermediate-circuit capacitors (not the clamping capacitors!) are common for all phases. As a consequence, the circuit needs only one power supply for the total DC link. Moreover, (reactive) power can be freely exchanged between the phases without additional losses. The number of intermediate-circuit capacitors is proportional to the number of levels.

The ground symbol shows a common (for all phases) reference point in the middle of the DC link. The possible output voltages are thus symmetric around zero. In case the circuit has an even number of levels, and thus an odd number of intermediate-circuit capacitors, this reference point must be artificially constructed.

The high number of clamping capacitors are rather voluminous and costly. Their voltage stabilization requires appropriate control and a high number of measurements.

The concept of the IC inverter has been further developed, resulting in the stacked multi-cell (SMC) inverter [28, 29]. It promises a reduction of the energy stored in the converter and thus of the clamping-capacitors size.

### 2.1.2 Asymmetric Multi-Level Inverters

In the past few years, the idea has risen to use different voltages on the various intermediate-circuit capacitors of a multi-level inverter. These inverters are called asymmetric multi-level inverters. Up to now, mainly asymmetric SHB inverters have been investigated [7–9, 12, 13, 16, 30–35], although the concept can be applied to other circuit topologies as well: NPC [33, 36], IC [37], and combinations of basic structures [9–11, 14–16].

*Asymmetric* multi-level inverters have exactly the same circuit topology as *symmetric* multi-level inverters. They differ only in the used *capacitor voltages*. The properties of asymmetric multi-level inverters are however quite different from those of their symmetric versions. Especially the number of output-voltage levels can be dramatically increased.

Instead of increasing the number of levels, one can also choose to reduce the number of cells. This is an interesting possibility to increase the reliability of a converter, while keeping the same output quality. As an example, we will compare a symmetric with an asymmetric nine-level inverter (Figure 2.4 and 2.5). The asymmetric version is only one possible solution out of several [8, 9].

We will first take a look at the inverter states and the corresponding output voltages of both inverters. Based on this, we will briefly discus the voltage,

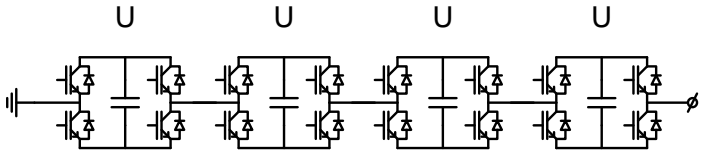



Figure 2.4: Phase circuit diagram of a symmetric 9-level SHB inverter.

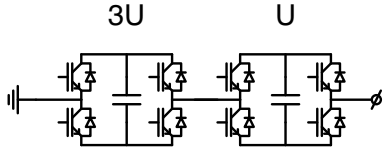



Figure 2.5: Phase circuit diagram of an asymmetric 9-level SHB inverter.

power and switching frequency of the different cells.

**Inverter States and Output Voltages**

Each H-bridge cell has four possible switching states, of which two result in the same output voltage. The output voltages are 'plus the capacitor voltage', 'minus the capacitor voltage' and 'zero voltage' (two times). We will only take the three states with different output voltages into account, and forget about the internal redundancy for now. The voltage of the $k^{\text{th}}$ cell $u_k$ is thus

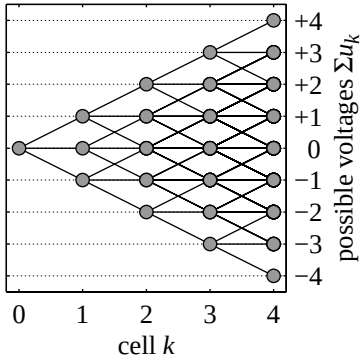
$$u_k = s_k u_{C_k} \quad \text{with } s_k \in \{-1, 0, +1\}, \tag{2.1}$$

where $s_k$ is the switching state and $u_{C_k}$ is the capacitor voltage of this cell. After $k$ cells in the inverter, we have the voltage $u_{k0}$ relative to the reference point

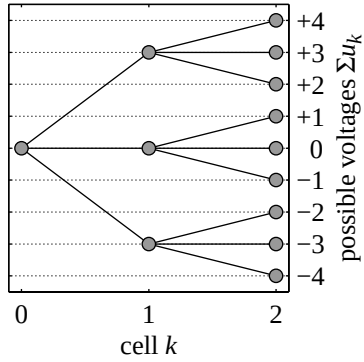
$$u_{k0} = \sum_{i=1}^{k} u_i. \tag{2.2}$$

The phase output voltage is, of course, obtained by summing over all cells.

We can now construct a tree of possible cell and output voltages. We start at the reference point, which has zero voltage per definition. From this point, three branches are drawn, corresponding to the three possible voltages of the first cell. At each of these three values, we have the three possible voltages of the second cell. So at each point of the first cell, we draw the three branches




(a) Symmetric 9-level SHB inverter shown in Figure 2.4.




(b) Asymmetric 9-level SHB inverter shown in Figure 2.5.

Figure 2.6: Inverter states and output voltages (one phase) of two different 9-level SHB inverters.

of the second cell. And we go on in a similar manner until the last cell to complete the tree. Figure 2.6 shows such trees for our two inverters.

Each branch in the tree corresponds to a switching state of an H-bridge cell. So each path in the tree (a sequence of branches) corresponds to a switching state of the inverter. Different paths can result in the same output voltage. If so, the inverter has redundant switching states. As can be clearly seen in Figure 2.6(a), the symmetric solution has many redundant states. The presented asymmetric solution of Figure 2.6(b), however, has no redundant states.

### Cell Voltage, Power and Switching Frequency

The cells in the symmetric inverter all have the same voltage. Normally, the controller is designed in such a way that the delivered active power and the switching frequency are the same as well. This is done by properly alternating the redundant states.

In the asymmetric inverter, the cells have different voltages. This also has consequences for the delivered power and the switching frequency [9, 15, 16]. 'Big cells', which have a big voltage, deliver mainly active power, and are operated with a low switching frequency. 'Small cells', which have a small voltage, deliver mainly reactive power, and are operated with a high switching frequency.

## 2.2 Medium-Voltage Drives

Power-electronic converters have been successfully implemented for medium-voltage drive applications. The most important and widely-used solutions are:

- series-connected H-bridges inverter (SHB);
- neutral-point clamped inverter (NPC);
- current-source inverter (CSI);
- load-commutated inverter (LCI);
- cyclo converter (CC).

The first two solutions are multi-level voltage-source converters, both of which have been successfully implemented as standard products for medium-voltage industrial drives. Their aspects will be treated in more detail in this section. The other converters are current-source or direct converters. They will not be regarded in this dissertation.

### 2.2.1 Series-Connected H-Bridges Inverter

The series-connected H-bridges inverter is an emerging inverter for medium-voltage drive applications [1,20]. A state-of-the-art realization with three cells per phase is shown in Figure 2.7, higher cell numbers are common though. An input transformer feeds each of the cells via its own three-phase winding and diode rectifier. To obtain a high pulse number at the primary side, secondary transformer windings in star, delta, zig-zag and combinations are used. The SHB inverter uses insulated-gate bipolar transistors (IGBT) with a low voltage-blocking but a high switching-frequency capability. IGBT require only rather simple gate drivers.

This inverter has excellent input-current and output-voltage waveforms. The output-voltage steps are steep but limited in magnitude. Therefore no output filter is needed even for retro-fit applications. Due to the small voltage steps of this inverter, also the common-mode voltage can be kept small enough to be of no further concern.

The drawback of this inverter is the high number of components for the rectifier, the inverter, as well as the control equipment, and the complexity of the input transformer. All this has a negative influence on the efficiency, reliability and cost of such a drive.

For applications where energy recuperation is desired, the diode rectifiers can be replaced by three-phase IGBT inverter bridges. This solution implies a different topology and control on the net and the motor side. A so called common DC bus application, where several inverters are connected to the same intermediate circuit, can not be realized.

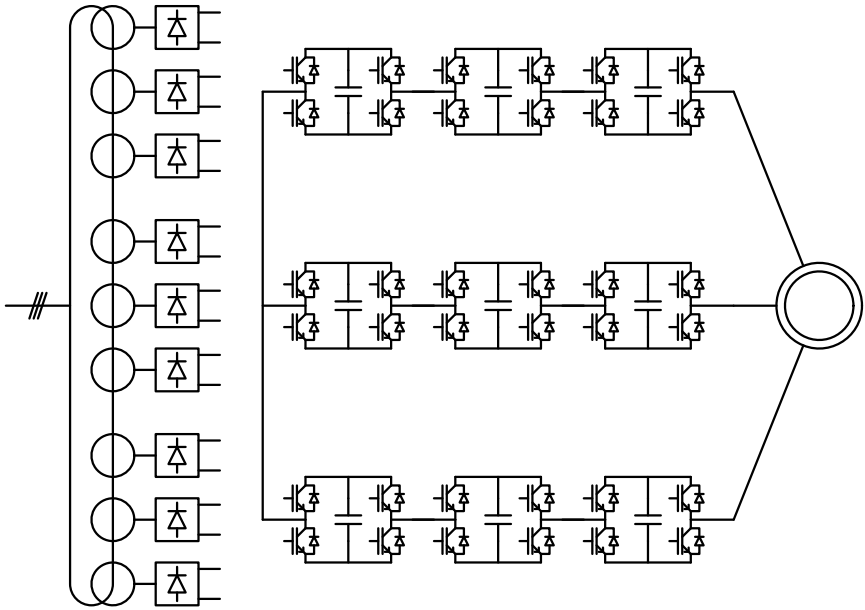


Figure 2.7: Circuit diagram of an SHB inverter in a medium-voltage drive application.

### 2.2.2 Neutral-Point Clamped Inverter

The three-level neutral-point clamped inverter is a widely used inverter for medium-voltage drive applications [2, 14, 38, 39]. A state-of-the-art realization with output filter is shown in Figure 2.8. A twelve-pulse input transformer and diode rectifier feeds the common intermediate circuit (a higher pulse number is possible for special cases). The NPC inverter uses integrated gate-commutated thyristors (IGCT) with a high voltage-blocking but a low switching-frequency capability. IGCT are highly reliable components with rather low losses.

The NPC inverter has a simple circuit, but generates big and steep voltage steps which can damage the winding insulation of standard motors. For retrofit applications, where an existing motor is subsequently equipped with an inverter, an $LC$ output filter is needed in order to smooth the inverter voltage. Such a filter is rather heavy and expensive. Since passive damping would cause too big losses, an active damping algorithm must be added to the controller. In case of a fault, self-excitation between motor and filter capacitors can occur. A special protection concept must prevent this and potential damage caused

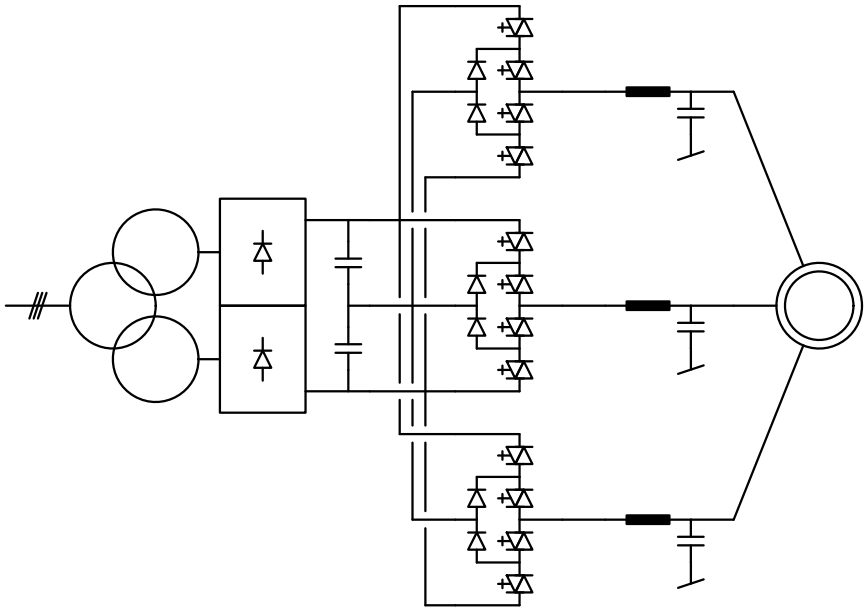


Figure 2.8: Circuit diagram of an NPC inverter in a medium-voltage drive application.

by its increasing voltages.

As most power-electronic converters, also the NPC inverter generates a common-mode voltage. In order to keep it away from the motor, the *LC* filter star point is connected to the ground. As a result, the full common-mode voltage will be seen on the transformer side. To prevent big common-mode currents in case of long transformer cables (big parasitic capacities), a common-mode filter must be added to the circuit (e.g. in the intermediate circuit between rectifier and capacitors).

For applications where energy recuperation is desired, a simple back-to-back connection of two inverters can be realized. The transformer and rectifier are thus replaced by a second NPC inverter with its *LC* filter. A so called common DC bus application, where several inverters are connected to the same intermediate circuit, is possible as well.

## 2.3 Hybrid Inverter

In the previous sections, we have regarded existing medium-voltage drives and the concept of asymmetric multi-level inverters. We have briefly discussed their main properties. In this section, we will combine the advantages of those different solutions and synthesize the power-part topology of a hybrid asymmetric multi-level inverter for medium-voltage industrial drives. It promises to be a simple and reliable circuit with a good output quality and high efficiency.

### 2.3.1 Topology Synthesis

As we have seen in the previous section, two multi-level inverter topologies have been successfully implemented as standard products for medium-voltage industrial drives: the SHB and the three-level NPC inverter.

In spite of their success, both topologies suffer from a principle drawback: the trade-off between power quality—both on the grid and the motor side—and circuit complexity—which translates in efficiency, reliability and cost. The SHB inverter has excellent input-current and output-voltage waveforms, at the cost of a complex input transformer and a high number of semiconductor devices, along with their control equipment. The NPC inverter, on the other hand, has a simple circuit, but needs a large $LC$ output filter to drive standard motors.

This trade-off can be tackled by using an asymmetric multi-level inverter. Applying this approach to the SHB topology allows to reduce the number of H-bridge cells while maintaining the number of output-voltage levels. However, the need for a, although somewhat simplified, complex input transformer remains.

As a consequence of choosing an asymmetric multi-level inverter, also the power semiconductors have to be capable to block these different cell voltages in their 'off' state. If we have cell voltages with a ratio of 3 or even more, it is not recommended to use the same power semiconductors all over the inverter. It is better to use different elements which suit the different requirements best [9–16, 33, 34].

On the one hand, 'big cells', which have a big voltage, deliver mainly active power, and are operated with a low switching frequency. These are ideal operating conditions for IGCT, which are very reliable elements providing a high blocking voltage together with low on-state losses [17–19].

On the other hand, 'small cells', which have a small voltage, deliver mainly reactive power, and are operated with a high switching frequency. These are ideal operating conditions for IGBT, which allow higher switching frequencies and have good performance at lower voltages.

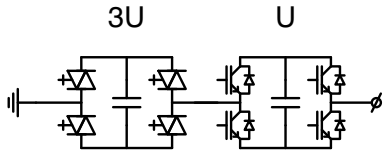



Figure 2.9: Phase circuit diagram of a hybrid asymmetric 9-level SHB inverter, combining two power-semiconductor technologies.

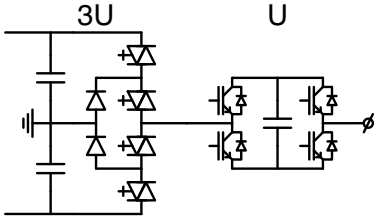



Figure 2.10: Phase circuit diagram of a hybrid asymmetric 9-level NPC/SHB inverter, reducing the feeding complexity.

By combining IGBT and IGCT in a hybrid asymmetric SHB inverter, we take advantage of their individual qualities and strength [12, 13, 34]. We call it a hybrid inverter because it unites two power-semiconductor technologies. The resulting topology is shown in Figure 2.9.

In this topology, the problem of the complex feeding of the cells remains. So we will look for a solution to improve this. As we have seen, the H-bridge cells generate three different voltages each. But a three-level inverter would do the same! So, instead of using three H-bridges (one for each output phase), we can use one three-phase three-level inverter [10, 11]. This works, of course, only for those cells which are directly connected to each other (the 'big cells'), and not for the floating ones (the 'small cells'). The NPC inverter has only one common intermediate circuit for all three phases, instead of separate ones for each H-bridge it replaces. This leads to a further simplification of the feeding transformer and rectifiers. The resulting topology, which combines the SHB with the NPC inverter, is shown in Figure 2.10.

In this topology, we have reduced the feeding to one 'big' DC link, which is common for all three phases, and three floating 'small' DC links. But we have seen that 'big cells' deliver mainly active power, whereas 'small cells' deliver mainly reactive power. This rises the idea to remove the feeding of

the latter completely and let them produce reactive power only [14–16]. By eliminating those power supplies, we considerably reduce the complexity of the feeding transformer and rectifiers: only that of the NPC inverter remains. This reduces the inverter cost and increases its reliability. At the same time, converter efficiency is increased by elimination of related power-supply losses.

However, ensuring zero active power for the non-supplied cells is not an easy task. This is required to keep their capacitor voltages stabilized. We will see how this can be achieved by an appropriate inverter control method in the following chapters.

Figure 2.11 shows the resulting circuit diagram of our hybrid asymmetric multi-level inverter for medium-voltage drive applications [14–16]. It consists of a three-phase three-level IGCT inverter (main inverter), with a two-phase two-level IGBT inverter (sub inverter) in series with each phase. IGCT with a high voltage-blocking capability are used to provide the main power with high reliability and low losses, IGBT with a higher switching-frequency capability are used to reduce the output harmonic content. We will use a ratio of 3 between the capacitor voltages of the main and the sub inverter to obtain a maximum of output-voltage levels. By addition and subtraction of these voltages, nine different output-voltage levels can be generated.

### 2.3.2 Properties

The power-part topology of our hybrid asymmetric nine-level inverter for medium-voltage drive applications is a merger of the well-known IGCT NPC inverter, the well-known IGBT SHB inverter, and the new concept of asymmetric multi-level inverters. The power is supplied from the net by an input transformer and twelve pulse rectifier (higher pulse number in special cases). The robust IGCT NPC inverter delivers the active power with a poor waveform but low losses. The series-connected IGBT H-bridge cells improve the output quality to a nine-level waveform. The whole circuit remains very efficient, simple and reliable.

The output-voltage steps are steep but limited in magnitude. Therefore no output filter is needed even for retro-fit applications. Due to the small voltage steps of this inverter, also the high-frequency common-mode voltage is small enough to be of no further concern.

For applications where energy recuperation is desired, a simple back-to-back connection of two inverters can be realized. The transformer and rectifier are thus replaced by a second hybrid inverter [14]. A so called common DC bus application, where several inverters are connected to the same intermediate circuit, is possible as well.

The main problem of this inverter lies in the control part. Since there is no

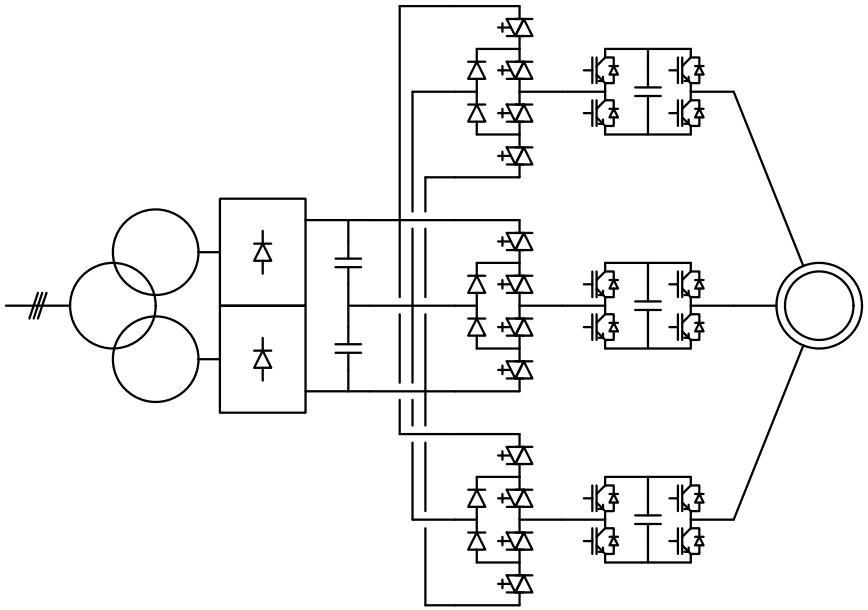


Figure 2.11: Circuit diagram of a hybrid asymmetric nine-level inverter in a medium-voltage drive application. The three sub-inverter intermediate circuits are *not* supplied by a power source.

feeding of the three floating H-bridge cells, we need a control method to keep their capacitor voltages stable. At the same time, this control method must assure a stable neutral-point voltage of the NPC inverter part as well.

Ensuring zero active power for the non-supplied cells is not an easy task. The resulting system is unstable, and without control the non-supplied intermediate-circuit capacitor voltages will quickly run away from their nominal values. An appropriate converter control method is needed to stabilize those voltages, preferably without deteriorating the output voltage. In general, this can not be done instantaneously by lack of an equilibrium state, but only on an average in time.

As we will see in the following chapters, we can solve this problem by adding a common-mode voltage to the output ($3^{\text{rd}}$, $9^{\text{th}}$ or $15^{\text{th}}$ harmonic). The amplitude and the absolute frequency of this common-mode voltage will always stay small enough not to harm the driven motor. The additional common-mode voltage will be very small around the nominal operating point (output voltage and frequency). This especially means that an eventual line-side inverter will

never need and generate big common-mode voltages.

Apart from normal operation, also the pre-charging of the intermediate-circuit capacitors is an issue to consider. To avoid additional cost and reduced reliability, additional equipment should be kept minimal. Usually a set of pre-charge resistors along with a bypass contactor on the AC or the DC side of the transformer and rectifiers is used. This enables to benefit from the anyhow existing feeding circuit. The solution on the AC side is more economical for multiple independent DC links (e.g. SHB), the one on the DC side is attractive in case of a single intermediate circuit (e.g. NPC).

Pre-charging of the sub inverters in our hybrid topology can not be accomplished in such a manner. However, additional equipment is not required, by charging their intermediate-circuit capacitors in parallel to and together with those of the main inverter. The latter is pre-charged in a usual way. The switching configuration used for this purpose is explained in Chapter 8.

### 2.3.3 Variants

The proposed power-part topology of our hybrid asymmetric nine-level inverter is not the only viable solution. Within the same concept, other variants are possible as well. Some of these possibilities are given in the following, which can be used alone or in combination. This dissertation does not further study their properties, but its theory can be extended and applied to them as well.

Instead of using a ratio of 3 between the capacitor voltages of the main and the sub inverter, we can choose a ratio of 2 as well.[1] In this case, we obtain a seven-level inverter with some redundant states. These redundancies can be used either to reduce the switching frequency of the semiconductor components, or to influence the capacitor loading of the floating H-bridge cells [9, 15, 16].

As in general concepts for symmetric and asymmetric multi-level inverters, we can of course increase the number of floating cells per phase beyond one. They can have all the same or (partly) different capacitor voltages, and (partial) feeding is possible as well [9–11, 15, 16]. A higher number of output-voltage levels can be obtained, with or without redundant states. However, an increasing number of non-fed intermediate-circuit capacitors will increase control complexity and might limit the operating range.

The floating cells are not limited to two-level H-bridges, but can be more complex structures as well [9, 35]. Mainly three-level or combined two/three-level H-bridges are of practical interest [10, 11, 15]. Similarly, the main inverter

[1] With a ratio of 1, the multi-level inverter is symmetric [40]. With ratios of 1, 2 or 3, the multi-level inverter has a uniform step (voltage difference between two adjacent output-voltage levels); its step is non-uniform with other values [9].

is not limited to a three-level NPC topology. As an alternative, the classical two-level inverter is of practical interest as well [9–11, 15, 16].

# Chapter 3

# Pulse-Width Modulation

Voltage-source inverters—two-level and multi-level—have a finite number of possible output voltages. For most applications, especially motor drives and net inverters, sinusoidal output voltages are desired. Different modulation methods exist to generate appropriate output voltages, taking the inverter limitations and required output quality into account.

In this chapter, we will investigate the widely used and well-known pulse-width modulation (PWM) methods [41–46]. Many variants exist, especially for multi-level inverters [9,47–52]. We will discuss some properties and choose a modulator for our hybrid asymmetric multi-level inverter.

In the following sections, we will define all inverter voltages relative to the (equivalent) intermediate-circuit midpoint. For all inverters—two-level or multi-level—the minimum value of the output phase voltage will be normalized equal to $-1$, and the maximum value equal to $+1$. For two-level inverters only those two output states exist. Multi-level inverters have additional states in between, which are usually equally distributed between those limits. With an equal distribution, the multi-level inverter has a uniform step (voltage difference between two adjacent output-voltage levels); its step is non-uniform with other values [9].

We will define the modulation index as the ratio of the fundamental phase-voltage amplitude and the maximum inverter phase output voltage. With the normalized inverter voltages defined above, the modulation index equals the fundamental phase-voltage amplitude.

## 3.1 Two-Level PWM Strategies

Two-level pulse-width modulation is well-known and widely used in power electronics. We will explain its principle and variants in this section.

### 3.1.1 Basic Principle

Within a switching interval $t_s$, an average output voltage $\bar{u}$ is generated by switching the two output-state voltages $u_1$ and $u_2$ for appropriate times $t_1$ and $t_2$:

$$t_1 u_1 + t_2 u_2 = t_s \bar{u}, \quad \text{with } t_1 + t_2 = t_s. \tag{3.1}$$

We can solve this equation with respect to the switching times:

$$t_1 = \frac{\bar{u} - u_2}{u_1 - u_2} t_s, \quad t_2 = \frac{\bar{u} - u_1}{u_2 - u_1} t_s. \tag{3.2}$$

We see a linear relationship between the switching times $t_k$ and the average output voltage $\bar{u}$.

The previous equations can also be written in terms of the duty cycles $d_k$, which are the conduction times $t_k$ relative to the switching interval $t_s$:

$$d_k = \frac{t_k}{t_s}, \quad k = 1, 2; \tag{3.3}$$

$$d_1 u_1 + d_2 u_2 = \bar{u}, \quad \text{with } d_1 + d_2 = 1; \tag{3.4}$$

$$d_1 = \frac{\bar{u} - u_2}{u_1 - u_2}, \quad d_2 = \frac{\bar{u} - u_1}{u_2 - u_1}. \tag{3.5}$$

From (3.5), we see that the duty cycles can also be interpreted as normalized average voltages. The duty cycle $d_2$ corresponds to the average voltage $\bar{u}$ for the mapping $[u_1, u_2] \rightarrow [0, 1]$.

For practical realization, we must determine the switching moments, when we switch from one output state to the other. We can either calculate the switching times according to (3.2) and use a timer to detect the switching moments. Or we can use the linearity of (3.2) and compare the desired output voltage with a linear ramp signal in each switching interval, as illustrated in Figure 3.1.

The ramp can either be raising or falling, in both cases the higher output-voltage level is chosen if the desired voltage is bigger than the ramp, and the lower output-voltage level is chosen if the desired voltage is smaller than the ramp. The raising and/or falling ramps of all the consecutive switching intervals form the carrier signal of the pulse-width modulation method.

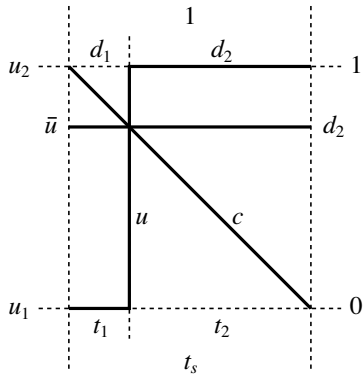



Figure 3.1: Determining the PWM switching moment, where we switch the output voltage $u$ between the two output-states voltages $u_1$ and $u_2$, by comparing the (desired) average output voltage $\bar{u}$ (or a duty cycle $d_k$) with a linear ramp signal $c$ in a switching interval $t_s$. This diagram corresponds to (3.2), (3.3) and (3.5), as can be seen by checking congruent triangles.

### 3.1.2 Variants

Based on this principle, there are several different ways to generate the modulation signals for an inverter [41–46]. But they can all be represented by similar graphical diagrams: a reference signal is compared to a carrier signal, and the output state is chosen according to which of the two signals is the biggest. It is especially mentioned here again, that also methods which only use calculated switching times, like the well-known space-vector PWM, have a corresponding graphical representation [42–46].

The main differences are in the choice of the carrier and reference signals. The possibilities are listed below.

- The carrier is usually a symmetrical triangular signal, but a saw tooth, or even irregular mixtures, can be used as well. The symmetrical signal produces less harmonics [41].
- If the inverter has several branches (H-bridge, three-phase inverter), a reference signal for each branch (phase) is needed. For each reference either the same carrier or phase-shifted carriers can be used. The same carrier is normally chosen, because it produces less harmonics in the branch-to-branch (phase-to-phase) voltages [41].
- In the case of multiple phases (branches), a common signal can be added to each of their references. This does not change the phase-to-phase

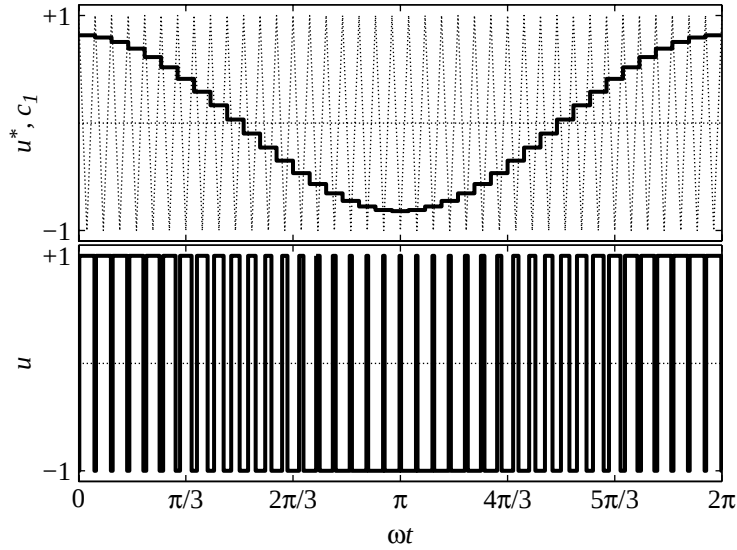



Figure 3.2: Reference signal $u^*$, triangular carrier $c_1$ and output voltage $u$ of a two-level inverter.

(branch-to-branch) reference signal, but does change the modulation pattern. It can of course only be done if the mid or star point of the load is not connected. This is often used to optimize the switching pattern with respect to generated harmonics or device switching frequency [43–46].

- The reference signals can be continuous or sampled synchronously to the carrier signal [52, 53]. The latter method generally produces less current harmonics [52]. Since digital controllers are used anyway nowadays and it is of no use to have a controller which is much faster than the modulator, this method is the preferred choice. Having the whole controller sampled this way also has the advantage of eliminating the switching-frequency content in the current measurements [53].

An example of a two-level pulse-width modulation is given in Figure 3.2.

## 3.2 Multi-Level PWM Strategies

Multi-level pulse-width modulation is an extension of the two-level PWM principles. We will discuss its variants in this section.

### 3.2.1 Basic Principle

As for the two-level PWM, an average output voltage $\bar{u}$ is generated by switching several (or even all) of the output-state voltages $u_{1\ldots n}$ for appropriate times within a switching interval $t_s$ [25]. Normally, only the two closest states with voltages directly below and above the desired output voltage are used. The adjacent output-states voltages form modulation bands. Modulating only within such bands requires the fewest switching actions and produces the smallest harmonic content [52].

As for the two-level PWM, we can use carrier signals to determine the switching moments. Similarly to Figure 3.1, we will need one carrier per modulation band (pair of adjacent output-states voltages). For an inverter with $n$ phase output levels, we have $n-1$ modulation bands, and we thus need $n-1$ carrier signals [51].

### 3.2.2 Variants

As for the two-level PWM, there are several different ways to generate the modulation signals. Additional to the possibilities listed in Section 3.1, the multiple carrier signals can have some phase shifts relative to each other [48, 49, 51, 52], or carriers with different waveforms can be used [50, 52]. The most used arrangements are equal triangular signals, which are either in-phase or alternated opposite-phase. Examples of a five- and a nine-level pulse-width modulation are given in Figure 3.3 and 3.4, where equal and in-phase carrier waveforms are used.

Carrier arrangements other than in adjacent-voltage modulation bands exist as well, such as the often used arrangement with horizontally distributed triangular signals (with a magnitude which reaches from the lowest ($-1$) to the highest ($+1$) state voltage) [48]. Actually, this method generates exactly the same output voltage as the alternated opposite-phase one, since the carrier line segments cover each other exactly.

Depending on the hardware realization of the multi-level inverter (series-connected H-bridges SHB, neutral-points clamped NPC, imbricated cells IC, ...), a control function is needed to associate the output state command to the individual switch commands. This function should also handle possible redundant states, for example by cycling through them. For certain hardware/-modulator combinations a direct relation between the carrier signals and the individual switch commands exists (NPC with vertically distributed carriers, SHB and IC with horizontally distributed carriers) and therefore no additional function is needed. These combinations are often used in multi-level applications [4, 5, 20, 23, 26].

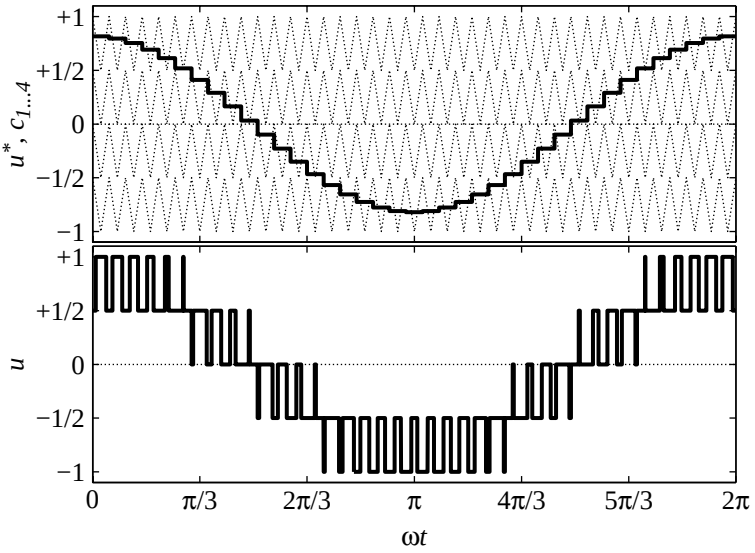



Figure 3.3: Reference signal $u^*$, triangular carriers $c_{1...4}$ and output voltage $u$ of a five-level inverter.

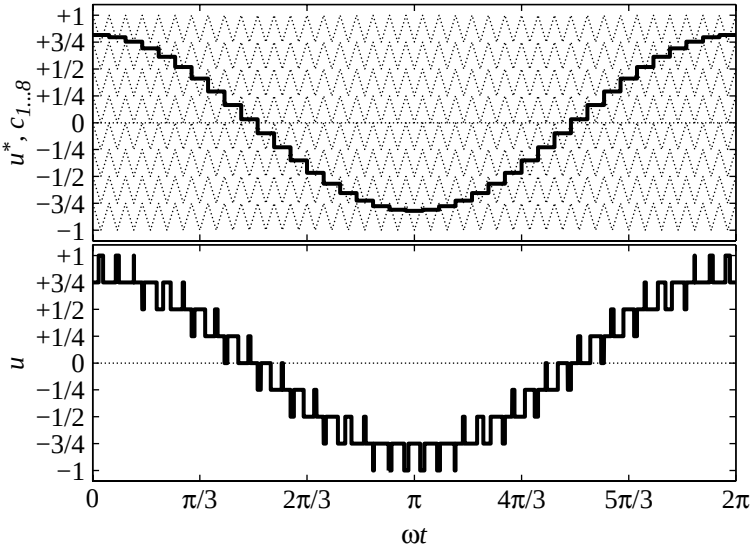



Figure 3.4: Reference signal $u^*$, triangular carriers $c_{1...8}$ and output voltage $u$ of a nine-level inverter.

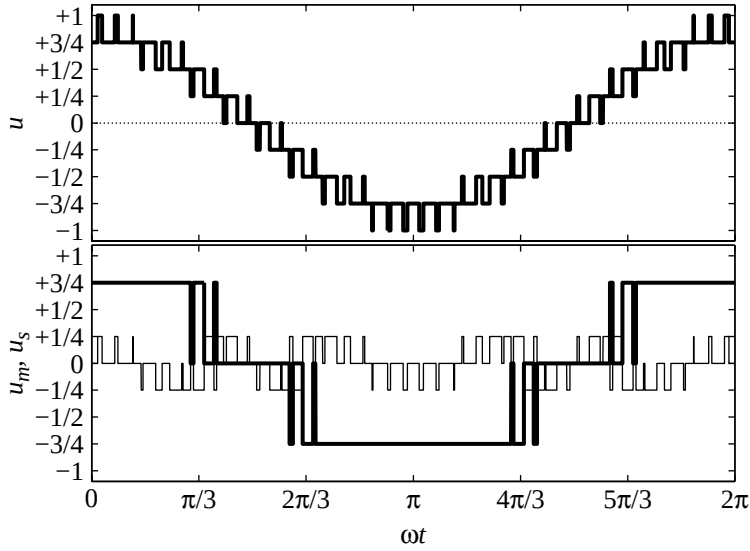



Figure 3.5: Output voltage $u$ and cell voltages $u_m$, $u_s$ of an asymmetric nine-level inverter.

Since there are no redundant output states in a two-cell asymmetric nine-level inverter (see also Figure 2.6(b)), the relation between the output and the cell states is unique. The same is true for our hybrid nine-level inverter. As an example, the main- and sub-inverter output voltages are shown in Figure 3.5, for the same pulse-width modulation signals as in Figure 3.4.

### 3.2.3 Chosen Variant

In the following, we will use the vertically distributed in-phase triangular carrier signals, because it is the most interesting solution—regarding the harmonic content—for three-phase loads *without* the neutral connected [48,52]. We will use a digital controller for our drive system, sampled synchronously to the carrier signal, and the reference signals will thus be regularly sampled as well. As an example, reference signals for a modulation index $m = 1.15$ are shown in Figure 3.6, the generated output phase voltages in Figure 3.7. A common-mode signal has been added to each of the references, to enable a modulation index bigger than unity. As can be seen in Figure 3.8, the resulting line-to-line output voltages modulate locally only between two adjacent states, which is not the case for other carrier arrangements.

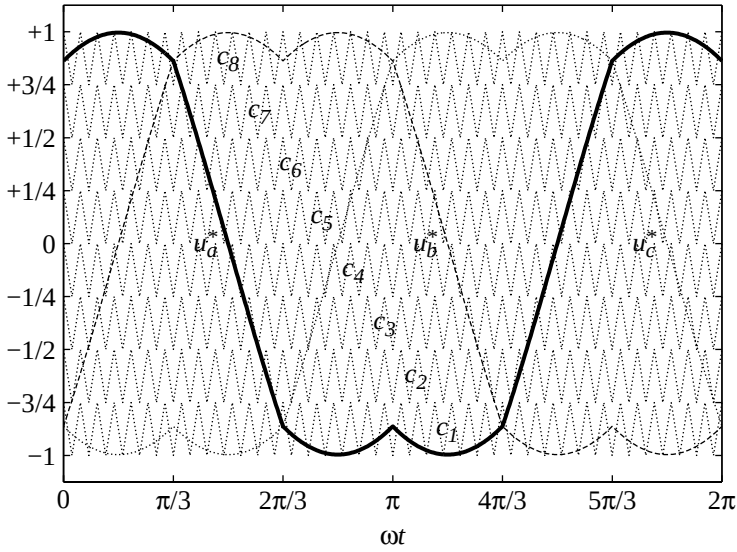



Figure 3.6: Reference signals $u^*_{a\ldots c}$ and triangular carriers $c_{1\ldots 8}$ of a nine-level inverter, with $m = 1.15$.

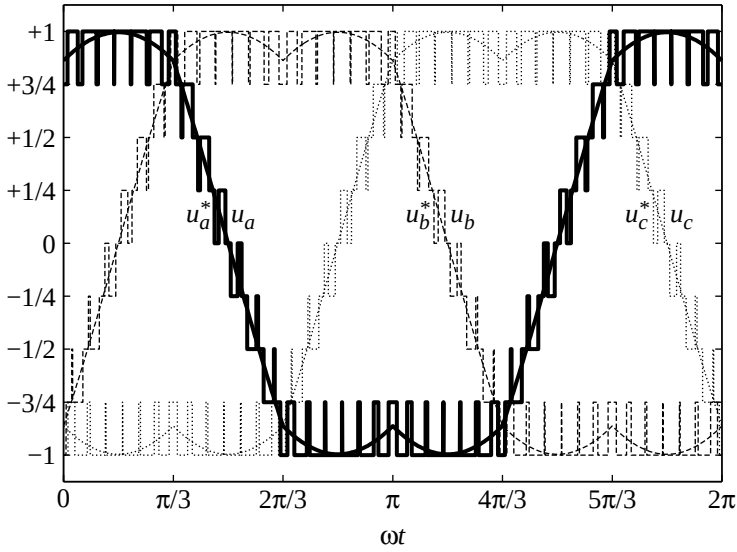



Figure 3.7: Reference signals $u^*_{a\ldots c}$ and generated output voltages $u_{a\ldots c}$ of a nine-level inverter, with $m = 1.15$.

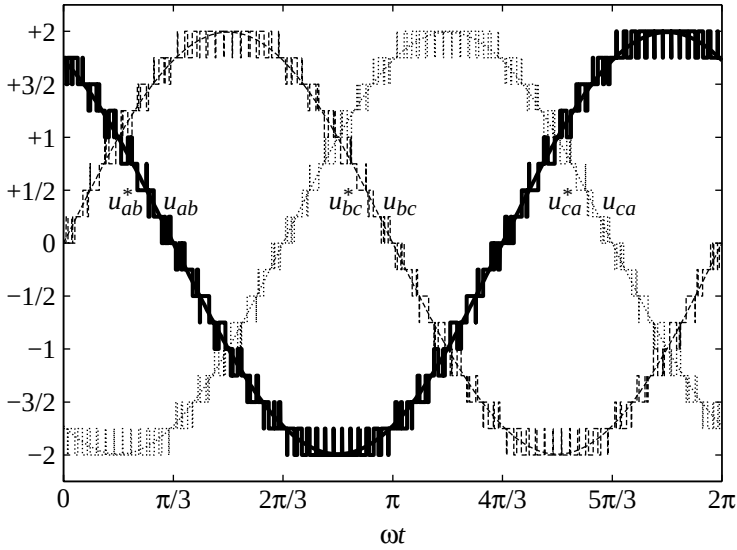



Figure 3.8: Phase-to-phase reference signals $u^*_{ab...ca}$ and generated output voltages $u_{ab...ca}$ of a nine-level inverter, with $m = 1.15$.

### 3.2.4 Modified Representation

Since all carrier signals are in fact composed of the same basic triangular signal plus a (different) constant offset, we can subtract this basic triangular signal from all carriers and all reference signals. This will not change the intersection points of the reference and the carrier signals, and therefore the generated output voltages will be the same. The original carrier signals are now reduced to their constant offset levels, whereas the reference signals are modified by the basic carrier. This is illustrated in Figure 3.9.

The carrier signals now function as comparison levels, located exactly in the middle between two adjacent output-states voltages (see Figure 3.9). In this representation, the behaviour of the modulator is like that of an A/D converter: the state closest to the reference signal is selected. Since the resolution of this A/D converter is quite bad (only nine possible digital values for a nine-level inverter), the quality of the output voltage can be improved by the addition of the carrier to the reference signals. This results in the well-known pulse-width modulation between adjacent discrete states. The peak-to-peak amplitude of the carrier signal is equal to the A/D-converter step.

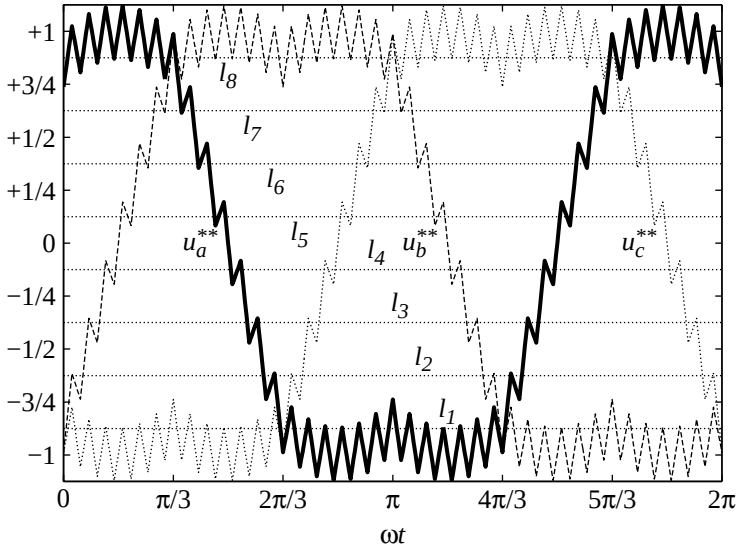



Figure 3.9: Modified reference signals $u_{a...c}^{**}$ and comparison levels $l_{1...8}$ of a nine-level inverter, with $m = 1.15$. The phase output states are located at $u_{a...c} \in \{-1, -\frac{3}{4}, -\frac{1}{2}, -\frac{1}{4}, 0, +\frac{1}{4}, +\frac{1}{2}, +\frac{3}{4}, +1\}$.

## 3.3 Varying Output-Voltage Levels

The pulse-width modulation methods described in the previous sections assume constant inverter output-state voltages. This assumption can be considered true, if the voltage sources feeding the various intermediate circuits are strong enough and the intermediate-circuit capacitors are big enough to compensate for the (rapid) power fluctuations due to converter switching.

An inverter is normally designed for the latter condition. But usually, the DC input voltages depend somewhat on the supplied power, and also variations due to net voltage fluctuations can be observed. However, if the distribution of the output-state voltages can be kept uniform between the minimum and the maximum possible output voltage, these generally slow variations can easily be taken into account by a scaling factor.

As we have discussed in Chapter 2, our hybrid inverter will have no feeding of the series-connected H-bridge cells, and no feeding of the NPC-inverter neutral point as well. As we will see in the following chapters, important power fluctuations must be accepted in their intermediate-circuit capacitors. A capacitor design capable of handling those power fluctuations would be too

big and too expensive. As a consequence, we will have to accept considerable variations in the output-voltage levels, resulting in non-uniform distributions.

With a conventional PWM method, variations in the output-voltage levels will create distortions of the output voltages. To prevent this, the modulator must take the variations in the output-voltage levels into account. This section will explain how this can be accomplished, assuming that the levels do not significantly change within a switching interval $t_s$.

### 3.3.1 Basic Principle

As we have seen in the previous sections, we can create a modulator either by calculating the switching times according to (3.2) each switching interval, or by comparing the desired output voltage with a linear ramp as illustrated in Figure 3.1. But both methods already take the values of the two used output-states voltages into account! We just have to use the actual, measured values instead of the ideal, constant ones. The resulting waveforms are illustrated in Figure 3.10, which shows an example of a nine-level pulse-width modulation with varying levels.

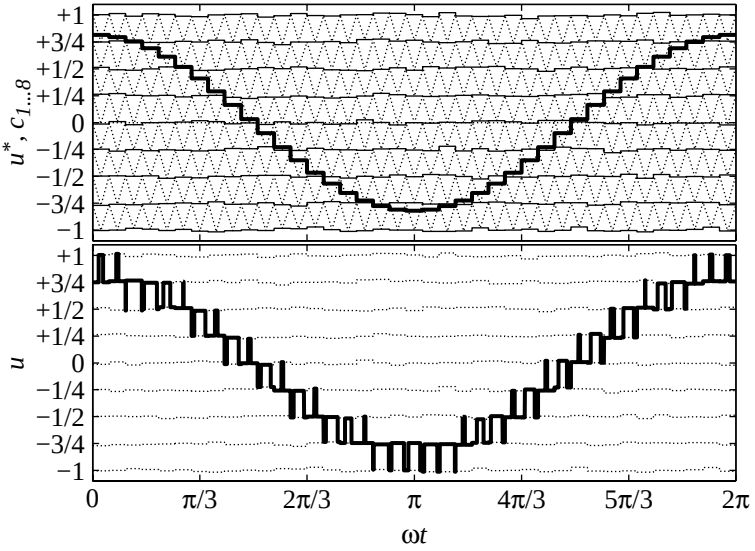



Figure 3.10: Reference signal $u^*$, triangular carriers $c_{1...8}$ and output voltage $u$ of a nine-level inverter with varying levels.

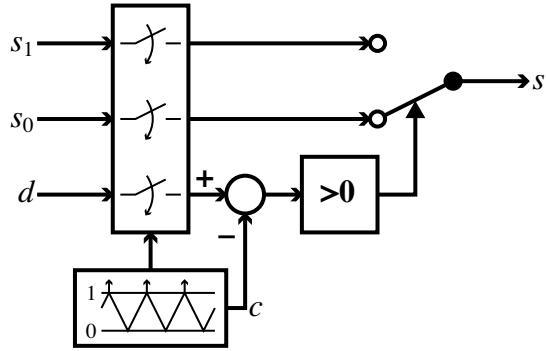



Figure 3.11: Digital implementation of a multi-level pulse-width modulator, corresponding to the input signals of (3.6) or (3.9).

### 3.3.2 Modulator Implementation

For an implementation of such a PWM method, it is not practical to determine all the carriers, especially if they are varying as in Figure 3.10. It is of course sufficient to determine only the carrier in the modulation band where the desired output voltage is situated. And by calculating the duty cycles according to (3.5), only one normalized carrier in the band $[0, 1]$ (see also Figure 3.1) is needed for al phases, which is easily implemented. Because this modulator only modulates between two states, we must specify which switching states are to be used [9]. Thus, the following information must be provided as input to the modulator:

$$\text{if } u_k \le u^* \le u_{k+1} \quad \begin{cases} s_0 = s_k, \\ s_1 = s_{k+1}, \\ d = \dfrac{u^* - u_k}{u_{k+1} - u_k}. \end{cases} \tag{3.6}$$

The corresponding modulator block diagram is shown in Figure 3.11. The varying voltage levels and the desired output voltage are all accounted for in the band selection and the duty cycle, as long as the actual measured values are used.

In case of an inverter with a uniform step, (3.6) can be further simplified. With a (positive) step $\Delta u$, the output-voltage levels $u_{1\ldots n}$ of our $n$-level inverter are:

$$u_k = u_0 + k\Delta u, \quad k = 1 \ldots n, \tag{3.7}$$

defined relative to some voltage $u_0$. Substitution in (3.6) leads to:

$$\text{if } k \leq \frac{u^* - u_0}{\Delta u} \leq k+1 \quad \begin{cases} s_0 = s_k, \\ s_1 = s_{k+1}, \\ d = \dfrac{u^* - u_0}{\Delta u} - k. \end{cases} \tag{3.8}$$

Instead of searching the modulation band by multiple comparisons, we can find it by a straight-forward calculation, which can be easily implemented and rapidly calculated on a digital signal processor (DSP) [54]:

$$u^{**} = \frac{1}{\Delta u}(u^* - u_0), \quad k = \text{trunc}(u^{**}) \quad \begin{cases} s_0 = s[k], \\ s_1 = s[k+1], \\ d = u^{**} - k. \end{cases} \tag{3.9}$$

The switching states are stored in a table $s[\cdot]$ and are addressed by the pointer $k$. The time-consuming division can even be omitted in case of non-varying output-voltage levels and thus of a constant step, by storing and using the latter's reciprocal value.

# Chapter 4

# Common Mode and Differential Mode

For any multi-wire system, we can distinguish the common mode and the differential mode of signal quantities. This is an important, although often neglected, issue in power systems as well. In two-wire systems, e.g. a symmetric signal transmission line, the modes are easily distinguished and their effects understood. In three-phase power systems however, the modes are less easily distinguished, represented and understood. As we will see in the following chapters, these aspects are of great importance to our system.

In this chapter, we will study the common mode and the differential mode of voltages and currents in three-phase power systems. We will define a transform matrix to change between phase quantities and their corresponding common and differential modes. As an illustration, we will apply the transform to some relevant signals of a nine-level inverter: the inverter output-states voltages, and the reference and output signals of its pulse-width modulator. Finally, for the purpose of our future control, we will investigate varying common mode at fixed differential mode.

## 4.1 Properties of Signal Modes

Common-mode and differential-mode parts of three-phase quantities have completely different influences on a system. In most cases, common-mode impedances are different from differential-mode impedances, and the common-mode system has totally different voltage and current requirements and constraints. We will discuss the main properties of these signal modes in this section, with

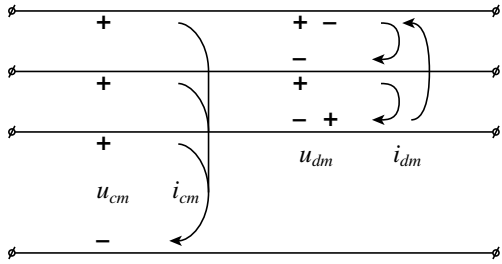



Figure 4.1: Common-mode and differential-mode voltages and currents in a three-phase system.

focus on three-phase power systems.

### 4.1.1 Common Mode

The common-mode part of a three-phase quantity is, as suggests its name, common to all three phase quantities. It can be a current flowing in each of the three wires, or a voltage difference between all three phases and the neutral or the ground, as illustrated in Figure 4.1.

The common-mode current $i_{cm}$ flows in all three wires in the same direction, and it can only return to its source via an other path like the neutral or the ground, possibly via parasitic elements. The common-mode voltage $u_{cm}$ represents the offset of the whole three-phase system relative to the neutral or the ground.

In three-phase loads such as electric machines, common-mode voltages and currents do not produce the desired phenomena like magnetic fields and electromagnetic torque (except for non-ideal effects or non-linear couplings like saturation). Since this mode seems to have no influence, its presence is often accepted or even ignored. However, common-mode currents and voltages can cause negative side effects, such as additional losses, bearing currents, insulation stress, magnetic saturation, et cetera. Common-mode quantities should be kept constrained in order to limit these effects.

Contrary to electric machines, power-electronic converters can strongly be affected by common-mode voltages and currents. For example, a common-mode voltage can change the load sharing between converter parts, and a common-mode current can influence the charge state of intermediate-circuit capacitors.

### 4.1.2 Differential Mode

The differential-mode part of a three-phase quantity is, as suggests its name, different for all three phase quantities. It can be the currents circulating in the three wires, or the voltage differences between the three phases, as illustrated in Figure 4.1.

The differential-mode currents $i_{dm}$ circulate in the three wires, in different directions in each wire, and they form closed circuits without return via other paths. The differential-mode voltages $u_{dm}$ represent the voltages within the three-phase system, without any relation to other objects.

In three-phase loads such as electric machines, it's the differential-mode voltages and currents that do produce the desired phenomena like magnetic fields and electro-magnetic torque. Proper equipment functioning depends on the appropriate establishment of this mode. For this purpose, power-electronic converters are designed to function mainly with differential-mode voltages and currents as well.

## 4.2 Transforming Three-Phase Quantities

In this section, we will discuss the transforms we can use to get the common- and differential-mode parts of a three-phase quantity. First, we will look at the widely used formula to obtain the space-vector representation of a quantity (differential-mode part). Besides this, we have a separate formula to calculate the zero-sequence, or homopolar, component of a quantity (common-mode part). Second, we will combine the two formulas into one transform matrix, with a slightly different scaling as in the separate formulas. Finally, we will apply the transform to the output-states voltages of a three-phase inverter and to the pulse-width modulation signals of such an inverter.

### 4.2.1 Separate Transforms

Three-phase quantities are usually transformed into the space-vector representation, because it simplifies the analysis of the investigated systems. The three independent phase quantities $u_a$, $u_b$ and $u_c$ are transformed into a two-dimensional space vector $\underline{u}$, which is often defined using complex numbers [55]:

$$\underline{u} = \frac{2}{3}\left(u_a e^{j0} + u_b e^{j\frac{2\pi}{3}} + u_c e^{j\frac{4\pi}{3}}\right). \tag{4.1}$$

This space vector represents the differential mode of the original three-phase quantity. For a symmetric sinusoidal system, the space vector rotates along a circle through the complex plane. By choosing 2/3 as the scaling factor, the

length of the space vector (radius of the circle) corresponds to the amplitude of the phase quantities. The differential mode of the original phase quantities can be reconstructed by geometrical projection of the space vector on the corresponding phase axes $\underline{e}_a = e^{j0}$, $\underline{e}_b = e^{j\frac{2\pi}{3}}$ and $\underline{e}_c = e^{j\frac{4\pi}{3}}$, which are rotated by 120° relative to each other.

The zero-sequence, or homopolar, component of three-phase quantities—which represents the common mode—is usually omitted or treated separately, because it has a completely different influence on the system. In most cases common-mode impedances are different from differential-mode impedances, and the common-mode system has totally different voltage and current requirements and constraints. Usually the average value of the three phase quantities is used [55]:

$$u_{hom} = \frac{1}{3}(u_a + u_b + u_c), \tag{4.2}$$

which corresponds to the voltage difference between the (real or artificial) neutral points of the source and the load, under the assumption that both are symmetric.

### 4.2.2 Combined Transforms

The differential- and the common-mode transforms (4.1) and (4.2) can be combined into one single transform [51, 56–58]. The transform can be described by a 3-by-3 matrix: the input vector contains the three phase quantities as three independent dimensions ($abc$-space), the output vector contains the transformed values, again as three independent dimensions ($xyz$-space, also known as $\alpha\beta 0$-space). The differential-mode part is found in the $xy$-plane, the common-mode part along the $z$-axis.

We will define the transformation matrix $\mathbf{A}$ as a real unitary matrix [51, 56–58]:

$$\mathbf{A} = \sqrt{\frac{2}{3}} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix}, \tag{4.3}$$

and the following relation holds:

$$\mathbf{A}^{-1} = \mathbf{A}^T. \tag{4.4}$$

With this definition, transformed objects will only be rotated in three-dimensional space and not be deformed or scaled. The transformed vector $\vec{u}^{\,xyz}$,

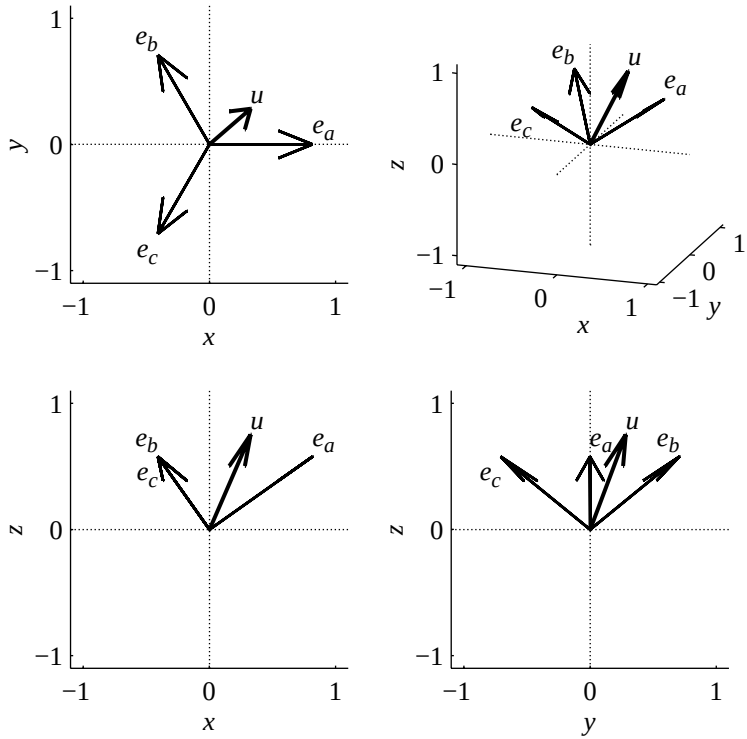



Figure 4.2: Transformed voltage vector $\vec{u}$ and phase axes $\vec{e}_a$, $\vec{e}_b$, $\vec{e}_c$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

which is obtained as

$$\vec{u}^{\,xyz} = \mathbf{A}\vec{u}^{\,abc}, \tag{4.5}$$

$$\text{with } \vec{u}^{\,abc} = \begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix}, \quad \vec{u}^{\,xyz} = \begin{pmatrix} u_x \\ u_y \\ u_z \end{pmatrix},$$

is a rotation of the original vector $\vec{u}^{\,abc}$ with the same length. The same holds for the three phase axes $\vec{e}_a$, $\vec{e}_b$ and $\vec{e}_c$: after transformation they will still be perpendicular to each other. An example of a transformed voltage vector and phase axes are shown in Figure 4.2. We can easily recognize the well-known 120°-rotated phase axes in the $xy$-plane (usually referred to as $\alpha\beta$-plane).

The scaling of the transform in (4.3) is different from the usual definition

in (4.1) and (4.2). By using a unitary transform matrix, the equations for the electrical-system instantaneous power (active and reactive) will be conserved [51, 56–58]. For the currents and voltages of a three-phase system, the instantaneous active power $p$ can be expressed as:

$$\begin{aligned} p &= \vec{u} \cdot \vec{i} \\ &= u_a i_a + u_b i_b + u_c i_c \\ &= u_x i_x + u_y i_y + u_z i_z. \end{aligned} \tag{4.6}$$

For the instantaneous reactive power $q$ we can write:

$$\begin{aligned} q &= \vec{e}_z \cdot \left( \vec{u} \times \vec{i} \right) \\ &= \frac{1}{\sqrt{3}} [(u_b i_c - u_c i_b) + (u_c i_a - u_a i_c) + (u_a i_b - u_b i_a)] \\ &= (u_x i_y - u_y i_x). \end{aligned} \tag{4.7}$$

Here, the vector $\vec{e}_z$ is the unit vector in the $z$-direction, either in $xyz$- or in $abc$-space:

$$\vec{e}_z^{\,xyz} = \begin{pmatrix} 0 \\ 0 \\ 1 \end{pmatrix}, \quad \vec{e}_z^{\,abc} = \frac{1}{\sqrt{3}} \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix}. \tag{4.8}$$

In an extended theory of instantaneous power, all three dimensions of the reactive-power cross product $\vec{q} = \vec{u} \times \vec{i}$ have a meaning, and the definition should not be limited to its $z$-axis component [58].

### 4.2.3 Application to Inverter States

As in Chapter 3, we will define all inverter voltages relative to the (equivalent) intermediate-circuit midpoint. For all inverters—two-level or multi-level—the minimum value of the output phase voltage will be normalized equal to $-1$, and the maximum value equal to $+1$. For two-level inverters only those two output states exist. Multi-level inverters have additional states in between, which are usually equally distributed between those limits.

The output states of a three-phase inverter form a cube in the three-dimensional $abc$-space. For a two-level inverter, the $2^3 = 8$ states form the eight corners of the 'basic' cube as shown in Table 4.1. The application of the transform (4.3) to the inverter states results in a rotation of the cube into $xyz$-space, as shown in Figure 4.3. We can easily recognize the well-known space-vector hexagon of inverter states in the $xy$-plane (usually referred to as $\alpha\beta$-plane).

Table 4.1: The output-states voltages of a two-level inverter.

| state number | voltage vector in $abc$-space $(u_a, u_b, u_c)$ | voltage vector in $xyz$-space $(u_x, u_y, u_z)$ |
|---|---|---|
| 0 | $(-1,-1,-1)$ | $(0, 0, -\sqrt{3})$ |
| 1 | $(+1,-1,-1)$ | $(+\frac{2\sqrt{2}}{\sqrt{3}}, 0, -\frac{1}{\sqrt{3}})$ |
| 2 | $(+1,+1,-1)$ | $(+\frac{\sqrt{2}}{\sqrt{3}}, +\sqrt{2}, +\frac{1}{\sqrt{3}})$ |
| 3 | $(-1,+1,-1)$ | $(-\frac{\sqrt{2}}{\sqrt{3}}, +\sqrt{2}, -\frac{1}{\sqrt{3}})$ |
| 4 | $(-1,+1,+1)$ | $(-\frac{2\sqrt{2}}{\sqrt{3}}, 0, +\frac{1}{\sqrt{3}})$ |
| 5 | $(-1,-1,+1)$ | $(-\frac{\sqrt{2}}{\sqrt{3}}, -\sqrt{2}, -\frac{1}{\sqrt{3}})$ |
| 6 | $(+1,-1,+1)$ | $(+\frac{\sqrt{2}}{\sqrt{3}}, -\sqrt{2}, +\frac{1}{\sqrt{3}})$ |
| 7 | $(+1,+1,+1)$ | $(0, 0, +\sqrt{3})$ |

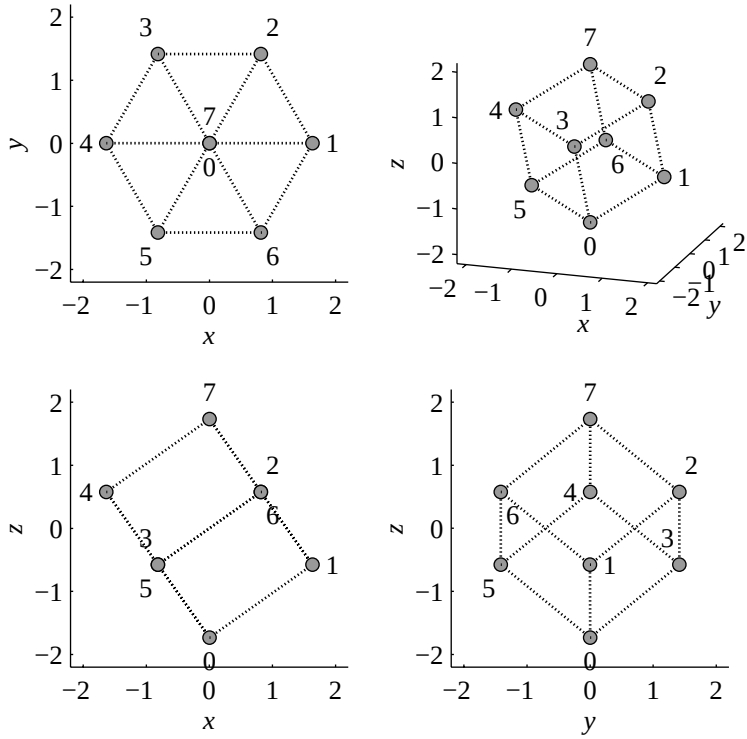



Figure 4.3: Transformed states of a two-level inverter. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

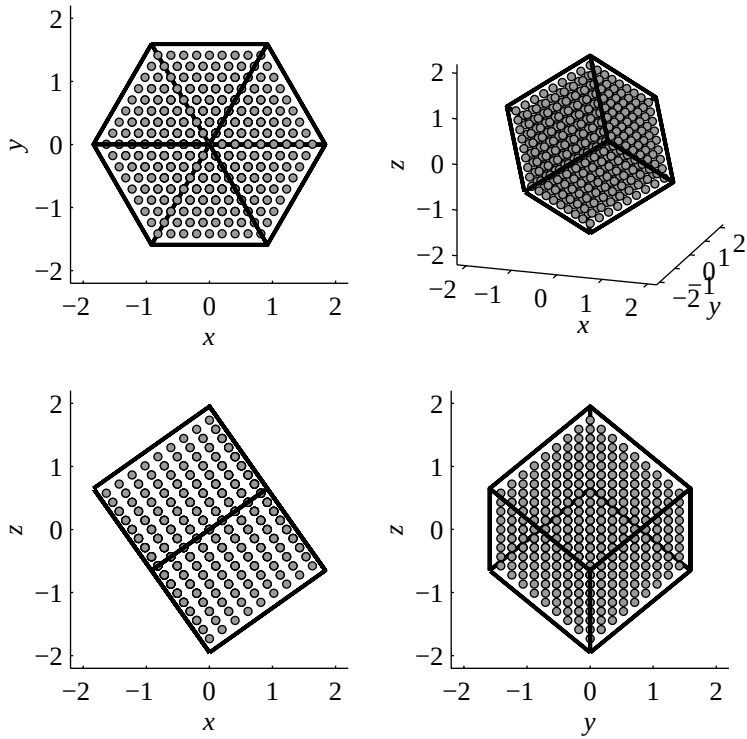



Figure 4.4: Transformed states of a nine-level inverter. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

For an $n$-level inverter, the cube is filled with additional (regularly) distributed points. The $n^3$ states form a (regular) grid within the 'basic' cube. Again, the application of the transform to the inverter states results in a rotation of the grid cube into $xyz$-space. Figure 4.4 shows the transformed states of a nine-level inverter.

### 4.2.4 Application to PWM Signals

In Section 3.2, we have seen a modified representation of the multi-level pulse-width modulation method. We subtracted the basic triangular signal from all carriers and all reference signals. The original carrier signals were reduced to their constant offset levels, whereas the reference signals were modified by the basic carrier (see Figure 3.9).

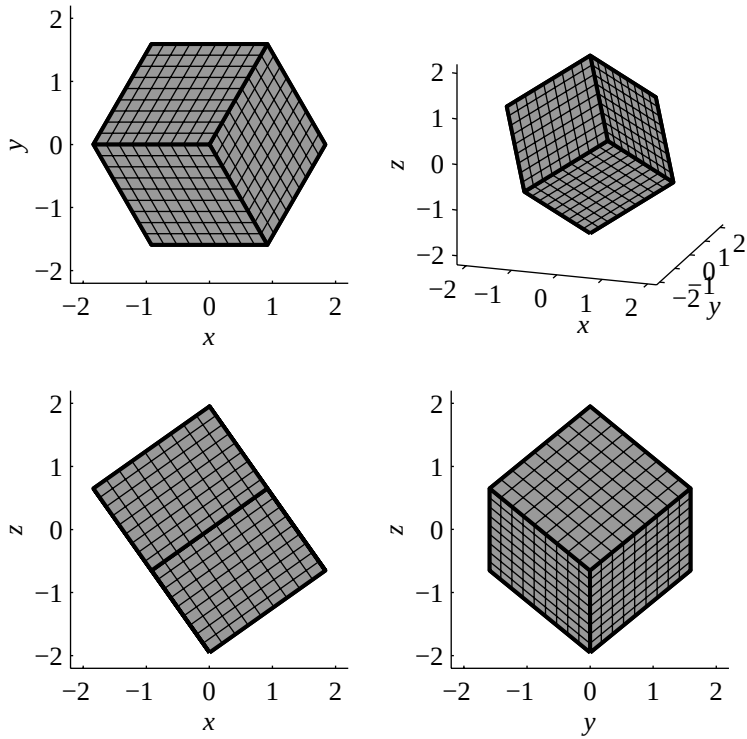



Figure 4.5: Transformed comparison levels of a nine-level inverter. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

In $abc$-space, the constant PWM comparison levels for phase $a$ are planes parallel to the $bc$-plane ($a$ = constant). Similarly, the levels for phase $b$ and $c$ are parallel to the $ac$- and the $ab$-plane respectively. Together, those planes form little cubes around all the inverter states, creating a three-dimensional A/D converter. If the reference signal vector is somewhere in a comparison cube, the corresponding inverter state (in its center) will be selected. Again, the application of the transform (4.3) to the comparison cubes results in a rotation of the cubes into $xyz$-space, as shown in Figure 4.5.

We now apply the transform (4.3) to the three modified phase reference signals. Because the carrier added to the reference signals is the same for all three phases, it represents a common-mode component. If the original reference signals form a symmetric sinusoidal three-phase system with constant

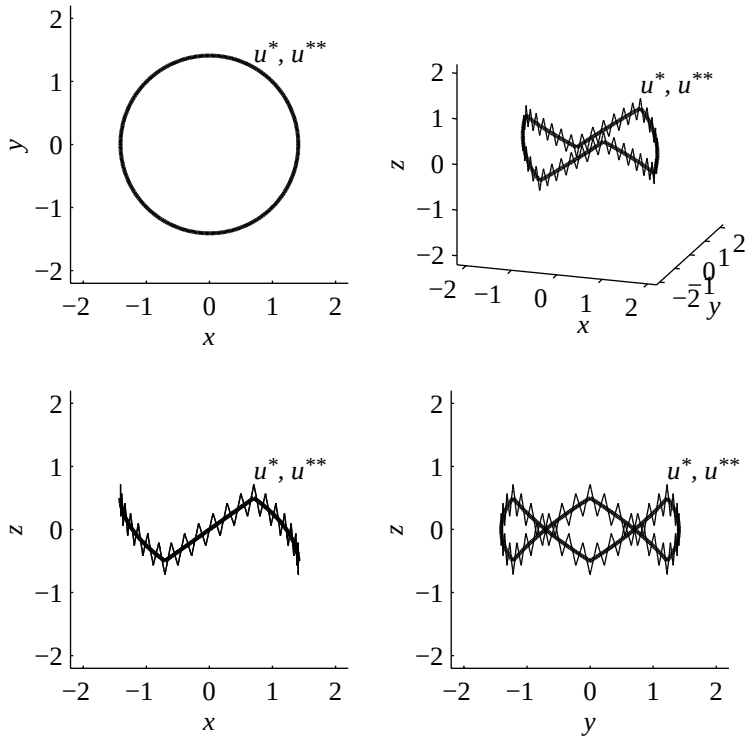



Figure 4.6: Transformed original $\vec{u}^*$ and modified $\vec{u}^{**}$ reference vector of a nine-level inverter, with $m = 1.15$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

amplitude and frequency, its vector representation will describe a circle parallel to the $xy$-plane in $xyz$-space. A possible common-mode component will displace it along the $z$-direction. The modified reference vector will have the triangular carrier added to this in the $z$-direction. As an example, the transformed original and modified reference vectors are shown in Figure 4.6, for the same pulse-width modulation signals as in Figure 3.9. The corresponding generated output voltage vector is shown in Figure 4.7.

The pulse-width modulation process in vector space can now be described as follows. The reference vector is describing its orbit through the A/D converter cube, moving up and down with the carrier frequency all the time (intersection of Figure 4.6 with Figure 4.5). It will go through several different comparison cubes on its way, and the corresponding output states will be

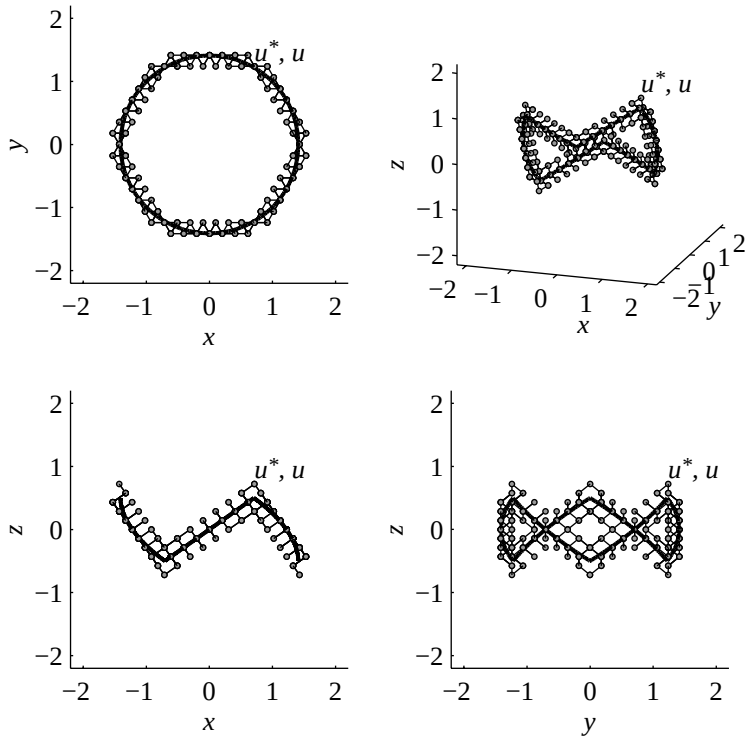



Figure 4.7: Transformed reference vector $\vec{u}^*$ and generated output voltage vector $\vec{u}$ of a nine-level inverter, with $m = 1.15$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

selected.

If the original reference vector is sampled synchronously to the carrier, the modified reference vector can touch maximally four comparison cubes each sampling period. Seen along the $z$-axis (classical space-vector view), the modulator will sequentially select those states for a certain time, that form a triangle around the space-vector tip. Two of those four states are redundant in the $xy$-plane, like the well-known zero states $\vec{u}^{\,abc} = (-1, -1, -1)$ and $\vec{u}^{\,abc} = (+1, +1, +1)$. This method results basically in the same modulation pattern as with the well-known classical space-vector modulation procedure. By choosing appropriate values for the common-mode part of the reference signals, the desired time sharing for the redundant—for differential-mode—output states can be easily controlled (see also Chapter 3).

## 4.3 Varying Common Mode at Fixed Differential Mode

In purely three-phase power systems (without any single-phase loads), the neutral is usually not connected. AC drives belong to this category: neither at the supply nor at the motor side the neutral is connected. As a consequence, the common-mode part of the inverter voltage can—within constraints to limit negative side effects—be considered as a degree of freedom. It is often used to optimize the switching pattern [43–45, 47, 49].

However, the common-mode voltage does affect power-electronic converters. Multi-level inverters usually have several power supplies and intermediate-circuit capacitors, of which equivalent load sharing and voltage stabilization is an important issue. Common-mode voltages and currents have an important influence on this.

To understand the influence of the possible common-mode output voltages on inverter behaviour of interest (e.g. the voltages of intermediate-circuit capacitors in multi-level inverters), we can analyze the inverter behaviour for reference vector orbits with all possible common-mode components.

The inverter output voltage is limited to a cube in three-dimensional *abc*- or *xyz*-space. The inverter behaviour of interest is a function (or are several functions) of the output voltage, so it is a function (several functions) defined on this cube.

Since the differential mode controls the desired load behaviour, we will consider this as a given quantity, which we are not allowed to change. We will only modify the common-mode part to control the inverter behaviour of interest.

A symmetric sinusoidal three-phase system with constant amplitude and frequency is represented by a vector that describes a circle parallel to the $xy$-plane. Since the common-mode component will displace it along the $z$-direction, a cylinder parallel to the $z$-axis is obtained for all possible common-mode values.

To visualize and to optimize the influence of the possible common-mode output voltages on the inverter, we must intersect this cylinder with the inverter function cube. This results in the inverter behavior as a function of the output voltage phase angle and common-mode component.

Figure 4.8 shows the inverter output-voltage cube and a reference-voltage cylinder. The part of the cylinder that remains after intersection of the two is shown in Figure 4.9. In this example, no function is defined on the cube. A function could be visualized using color or gray-scale. An example of this method will be given in Chapter 5.

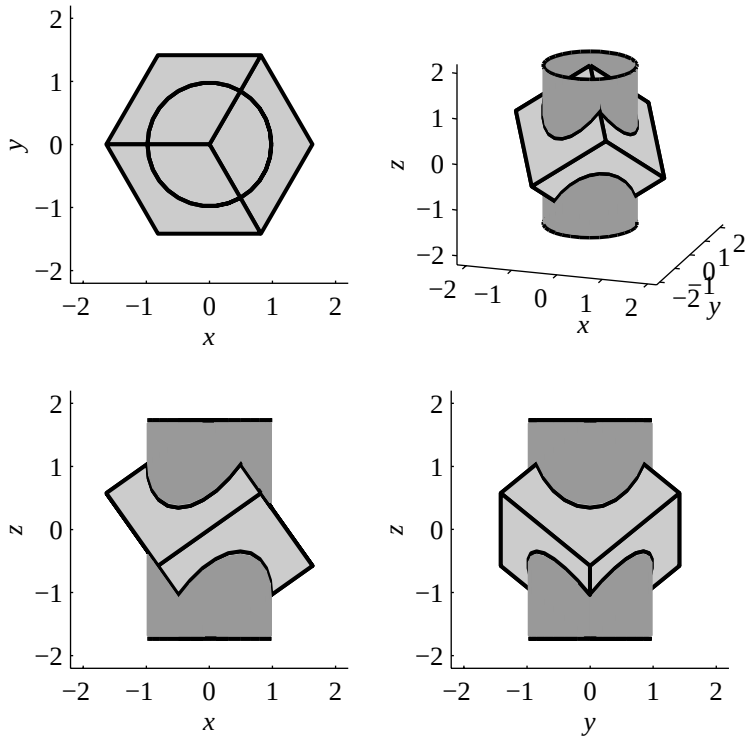



Figure 4.8: Transformed inverter output-voltage cube and reference-voltage cylinder, with $m = 0.8$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

The cylinder surface can be flattened to a two-dimensional graph, and possible common-mode paths can be drawn on top of it. This is shown in Figure 4.10 for different operating points. As can be clearly seen, the possibilities to select the common-mode component are reduced for increasing output voltage. Especially, a non-zero common-mode component is needed for a modulation index $m > 1$. The cylinder surface vanishes for $m > \frac{2}{\sqrt{3}} \approx 1.15$, which indicates that pulse-width modulation is no longer possible.

The curved boarders of the cylinder originate from the tilted states-cube faces. These boarders correspond to the minimum and maximum possible common-mode component. They are equal to the difference between the maximum (minimum) possible inverter output voltage and the maximum (mini-

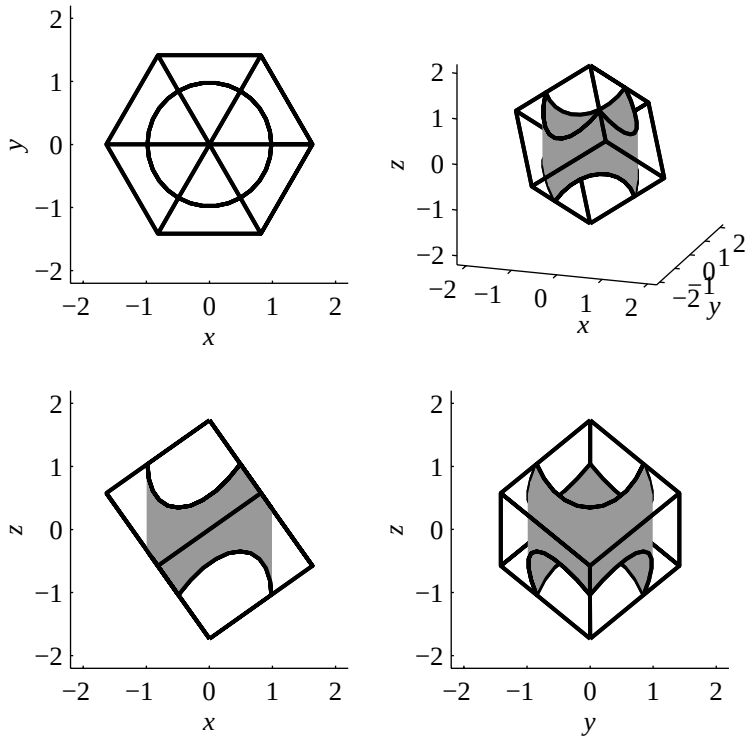



Figure 4.9: Transformed intersection of inverter output-voltage cube and reference-voltage cylinder, with $m = 0.8$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

mum) value of the differential-mode voltages:

$$\begin{aligned} u_{cm,max} &= u_{inv,max} - \max(\vec{u}_{dm}), \\ u_{cm,min} &= u_{inv,min} - \min(\vec{u}_{dm}). \end{aligned} \tag{4.9}$$

The different (two-level) PWM methods frequently described in the literature also have corresponding characteristic common-mode voltages [44–46]. It can be verified that they always remain within the intersected cylinder surface derived in this chapter. Especially the curved boarders can be recognized in the so-called discontinuous modulation methods, where a phase is kept clamped to the minimum or maximum possible inverter voltage for certain times. This corresponds to using the minimum respectively maximum possible common-mode voltage.

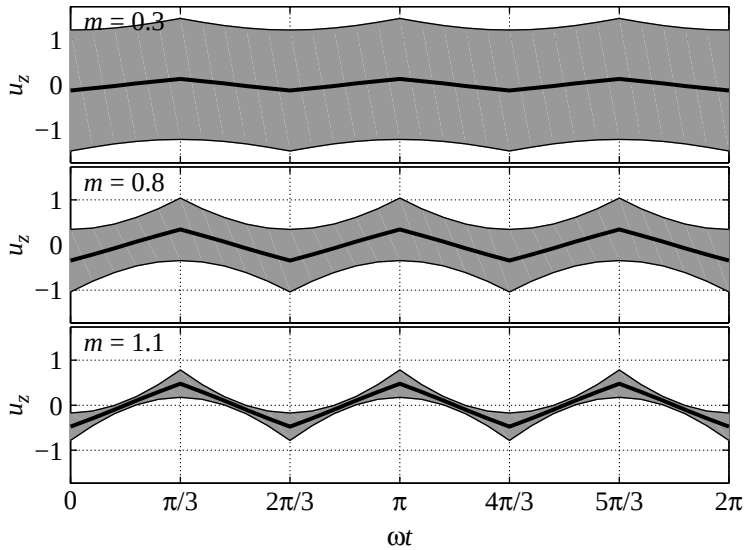



Figure 4.10: Flattened reference-voltage cylinder surface after intersection with the inverter output-voltage cube, for three different operating points. Possible common-mode paths are drawn on top of it.

# Chapter 5

# Inverter Modeling

In order to properly control an inverter, we must thoroughly understand its behavior. Power-electronic inverters are, among other components, build up of switches. Especially the switched-mode behavior can make inverter modeling difficult. We will control our inverter by the pulse-width modulation (PWM) method described in Chapter 3, and we need an appropriate inverter model for this control method.

In this chapter, we will start with an exact description of ideal switches. Based on this, we will derive an approximate switch model under PWM control. This approximate model neglects the switching behavior and takes only average values over a switching interval into account. Using such switch models, we can construct a model of our hybrid asymmetric multi-level inverter. Especially the intermediate-circuit capacitor voltages will be of our interest, because we need a control algorithm to stabilize them. As we will see in Chapter 6, this stabilization can be done by adding an appropriate common-mode voltage to the output. Therefore, we will focus at the influence of the possible common-mode voltages.

## 5.1 PWM-Controlled Ideal Switch

Power-electronic inverters are, among other components, build up of switches. Often, single-pole switches are used in circuit diagrams. However, in voltage-source inverters a current path is always ensured by free-wheeling diodes or switch command rules. As a consequence, an equivalent circuit diagram can be drawn using multi-pole switches. A multi-pole switch has no ‘open’ state, but is always connected to one of its poles.

In this section, we will mathematically model ideal multi-pole switches. An approximate averaged model under PWM control is derived from its exact continuous-time model.

### 5.1.1 Continuous-Time Model

An ideal $n$-pole switch consists of a throttle, which will be connected to either one of the $n$ poles. We will associate a switching function $s_k$ to each of the poles, which is equal to 1 if the throttle is connected to the corresponding pole, and 0 otherwise. Since the throttle is always connected to exactly one pole, the sum of the switching functions is always equal to 1:

$$\sum_{k=1}^{n} s_k = 1, \quad s_k \in \{0, 1\}. \tag{5.1}$$

An ideal switch has zero resistance between the throttle and a pole in the connected state, and infinite resistance in the unconnected state. Thus, the throttle voltage $u$ equals the voltage of the connected pole, which can be expressed as follows:

$$u = \sum_{k=1}^{n} s_k u_k. \tag{5.2}$$

The pole currents $i_k$ equal the throttle current $i$ in the connected state, and zero current otherwise:

$$i_k = s_k i, \quad k = 1 \ldots n. \tag{5.3}$$

Since the switch cannot produce, store or consume any energy, the power on both sides of the switch must always be equal:

$$ui = \sum_{k=1}^{n} u_k i_k. \tag{5.4}$$

That this relation holds, can be easily verified by substituting (5.2) and (5.3) into (5.4).

As an illustration, the following set of equations describes a two-pole switch:

$$u = s_1 u_1 + s_2 u_2; \tag{5.5}$$

$$i_1 = s_1 i, \quad i_2 = s_2 i; \tag{5.6}$$

$$\text{with } s_1 + s_2 = 1, \quad s_{1,2} \in \{0, 1\}. \tag{5.7}$$

### 5.1.2 PWM-Controlled Average Model

In voltage-source inverters, the intermediate circuit is capacitive with the character of a voltage source. The possible output-voltage levels are thus about constant (at least for a short time interval). To prevent very big currents, the load cannot be of a voltage-source type. It is usually inductive with the character of a current source. The output current is thus about constant (at least for a short time interval).

If the switching frequency is sufficiently high, the output currents and intermediate-circuit voltages have only small variations (ripple) within a switching interval $t_s$. We will neglect this ripple in the following and assume their values constant on this time scale. As a consequence, the pulsating character of the capacitor currents and inductance voltages can be neglected as well. We will only take their average values over a switching interval $t_s$ into account.

We will first determine the average pole switching functions $\bar{s}_k$ of our $n$-pole switch. Since the switching functions $s_k$ are equal to 1 for the times $t_k$, during which the throttle is connected to the $k^{\text{th}}$ pole, and equal to 0 for the rest of the switching interval $t_s$, their average values are:

$$t_s \bar{s}_k = t_k 1 + (t_s - t_k)0, \quad k = 1 \dots n. \tag{5.8}$$

Solving for the average pole switching functions leads to:

$$\bar{s}_k = \frac{t_k}{t_s}, \quad k = 1 \dots n. \tag{5.9}$$

We note that they are equal to the pole duty cycles. Since the throttle is always connected to exactly one pole, the sum of the pole connection times is equal to the switching interval:

$$\sum_{k=1}^{n} t_k = t_s. \tag{5.10}$$

As a consequence, the sum of the average switching functions is equal to 1, equivalent to (5.1):

$$\sum_{k=1}^{n} \bar{s}_k = 1, \quad \bar{s}_k \in [0, 1]. \tag{5.11}$$

Similarly, we can determine the average throttle voltage $\bar{u}$ and pole currents $\bar{i}_k$:

$$t_s \bar{u} = \sum_{k=1}^{n} t_k u_k; \tag{5.12}$$

$$t_s \bar{i}_k = t_k i + (t_s - t_k)0, \quad k = 1 \dots n. \tag{5.13}$$

Solving for the average throttle voltage $\bar{u}$ and pole currents $\bar{i}_k$ using (5.9) leads to:

$$\bar{u} = \sum_{k=1}^{n} \bar{s}_k u_k; \tag{5.14}$$

$$\bar{i}_k = \bar{s}_k i, \quad k = 1 \ldots n. \tag{5.15}$$

This is equivalent to (5.2) and (5.3).

As in (5.4), the power on both sides of the switch is always equal:

$$\bar{u} i = \sum_{k=1}^{n} u_k \bar{i}_k, \tag{5.16}$$

which can be easily verified by substituting (5.14) and (5.15) into (5.16).

As an illustration, the following set of equations describes an averaged PWM-controlled two-pole switch:

$$\bar{u} = \bar{s}_1 u_1 + \bar{s}_2 u_2; \tag{5.17}$$

$$\bar{i}_1 = \bar{s}_1 i, \quad \bar{i}_2 = \bar{s}_2 i; \tag{5.18}$$

$$\text{with } \bar{s}_1 + \bar{s}_2 = 1, \quad \bar{s}_{1,2} \in [0, 1]. \tag{5.19}$$

If we compare the equations of the average switch model with those of the exact model, we see that they are in fact the same! So, as long as the switching frequency is sufficiently high, we can always use the same equations, without bothering about the time scale we are looking at. Therefore, we will omit the bar over symbols, indicating average values, in the following.

## 5.2 PWM-Controlled Hybrid Inverter

The hybrid asymmetric multi-level inverter consists of several switches. In the previous section, we have modeled an ideal switch under pulse-width modulation.

In this section, we will model our hybrid inverter based on the ideal switch models. Especially the intermediate-circuit capacitor voltages and currents will be of our interest.

The power-part topology of our hybrid inverter was presented in Chapter 2, and the circuit diagram shown in Figure 2.11. The idealized circuit diagram for one phase leg of the hybrid inverter is shown in Figure 5.1. Each phase is a series connection of a main and a sub inverter, which are equipped with ideal switches.

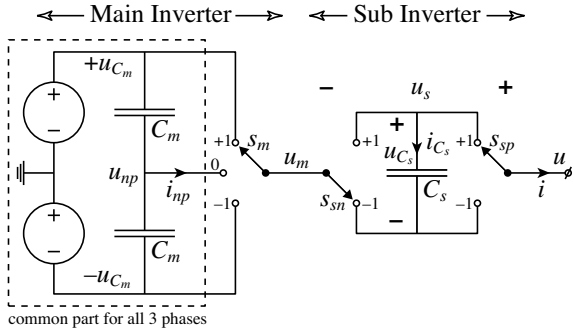



Figure 5.1: Idealized circuit diagram for one phase leg.

### 5.2.1 Main Inverter

The main inverter is a three-level neutral-point-clamped (NPC) inverter. It consists of two intermediate-circuit capacitors $C_m$, which are common for all three phases, and a three-pole switch for each phase.

An equivalent circuit diagram for the main-inverter neutral point can be seen in Figure 5.2. The equivalent neutral-point capacitor $C_{np}$ is the parallel connection of the two intermediate-circuit capacitors $C_m$:

$$C_{np} = 2C_m. \tag{5.20}$$

With this equivalent circuit, the behavior of the neutral point voltage can be better understood. Of course, the equivalent neutral-point capacitor is also common for all three phases.

The voltage reference point (ground) is chosen to be the (artificial) midpoint of the main-inverter supply-voltage source. The source supplies twice the ideal intermediate-circuit capacitor voltage $u_{C_m}$, once negative and once positive according to the choice of the reference point. The real capacitor voltages differ from this ideal voltage by the neutral-point capacitor voltage $u_{C_{np}}$.

For convenience, we will label the three switch poles '$m-$' for the negative supply, '$np$' for the neutral point, and '$m+$' for the positive supply. Using the switch model of the previous section, the main-inverter output voltage is:

$$u_m = (s_{m+} - s_{m-})u_{C_m} + s_{np}u_{C_{np}}. \tag{5.21}$$

We can define one single switching function $s_m$ for the main-inverter three-pole switch, which will be equal to $-1$ if connected to the negative supply, 0

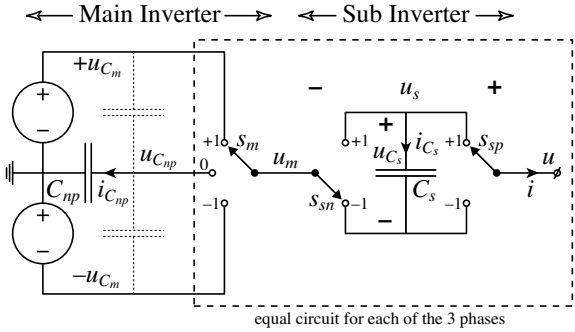



Figure 5.2: Equivalent idealized neutral-point circuit diagram.

if connected to the neutral point, and +1 if connected to the positive supply:

$$s_m = s_{m+} - s_{m-}. \tag{5.22}$$

With this definition, the main inverter output voltage is:

$$u_m = s_m u_{C_m} + s_{np} u_{C_{np}}. \tag{5.23}$$

The neutral-point switching function can be expressed in terms of the main switching function:

$$s_{np} = 1 - |s_m|. \tag{5.24}$$

For averaged switching functions, this relation is only valid if we modulate only between adjacent states within a PWM switching interval, and never directly between the '+' and the '−' states. Since this is the PWM method we will use, the above equation can be used for our model.

Similar to the voltages, we can deal with the currents. Using the switch model of the previous section, the main-inverter switch currents are:

$$i_{m+} = s_{m+} i, \quad i_{np} = s_{np} i, \quad i_{m-} = s_{m-} i. \tag{5.25}$$

Concerning the intermediate-circuit currents, we are especially interested in the neutral-point current. The neutral-point capacitor current is defined in the opposite sense of the switch current. Since the main-inverter intermediate circuit is common for all three phases, we have to sum the three neutral-point phase currents to find the total neutral-point capacitor current:

$$i_{C_{np}} = -\sum_{ph=a,b,c} i_{np,ph} = -\sum_{ph=a,b,c} s_{np,ph} i_{ph}. \tag{5.26}$$

The subscript $ph$ refers to the considered phase and can take the values $a$, $b$ or $c$. The corresponding capacitor voltage is obtained by integration of its current:

$$u_{C_{np}} = \frac{1}{C_{np}} \int i_{C_{np}} \mathrm{d}t. \tag{5.27}$$

### 5.2.2 Sub Inverter

The sub inverter is a floating H-bridge, which is separate for each phase. It consists of an intermediate-circuit capacitor $C_s$ and two two-pole switches.

To start, we will refer all voltages to the (artificial) midpoint of the intermediate circuit, which has a voltage $u_{s0}$ relative to the ground. The intermediate-circuit capacitor has a voltage $u_{C_s}$, and its two connections thus minus and plus half this value relative to the midpoint.

For convenience, we will label the two switches '$n$' (negative) for the first and '$p$' (positive) for the second switch, and for each we will label the two switch poles '$-$' for the negative connection and '$+$' for the positive connection. Using the switch model of the previous section, the sub-inverter branch voltages are:

$$\begin{aligned} u_{sp} &= (s_{sp+} - s_{sp-}) \frac{u_{C_s}}{2} + u_{s0}, \\ u_{sn} &= (s_{sn+} - s_{sn-}) \frac{u_{C_s}}{2} + u_{s0}. \end{aligned} \tag{5.28}$$

The sub-inverter output voltage is the difference between the two branch voltages:

$$u_s = u_{sp} - u_{sn} = ((s_{sp+} - s_{sp-}) - (s_{sn+} - s_{sn-})) \frac{u_{C_s}}{2}. \tag{5.29}$$

We can define one single switching function $s_{sn}$ and $s_{sp}$ for each of the two sub-inverter switches, which will be equal to $-1$ if connected to the negative connection and $+1$ if connected to the positive connection:

$$\begin{aligned} s_{sp} &= s_{sp+} - s_{sp-}, \\ s_{sn} &= s_{sn+} - s_{sn-}. \end{aligned} \tag{5.30}$$

There are four different switching states for the entire sub inverter, but the resultant switching function $s_s$ has only three possible values:

$$s_s = \frac{s_{sp} - s_{sn}}{2}. \tag{5.31}$$

It can be seen in Table 5.1 that the zero-state is redundant, which means that it can be realized in two different ways. With the above definitions, the sub inverter output voltage is:

$$u_s = s_s u_{C_s}. \tag{5.32}$$

Table 5.1: Sub inverter switching states.

| $s_{sp}$ | $s_{sn}$ | $s_s$ |
|---|---|---|
| +1 | −1 | +1 |
| +1 | +1 | 0 |
| −1 | −1 | 0 |
| −1 | +1 | −1 |

Similar to the voltages, we can deal with the currents. Using the switch model of the previous section, the sub-inverter switch currents are:

$$\begin{aligned} i_{sp+} &= +s_{sp+}i, \quad i_{sp-} = +s_{sp-}i, \\ i_{sn+} &= -s_{sn+}i, \quad i_{sn-} = -s_{sn-}i. \end{aligned} \tag{5.33}$$

The intermediate-circuit capacitor current is the sum of the two switch currents. It is the positive sum on the negative connection, and the negative sum on the positive connection, because of the current sense definitions:

$$\begin{aligned} i_{C_s} &= -(i_{sp+} + i_{sn+}) \quad = +(i_{sp-} + i_{sn-}) \\ &= -(s_{sp+} - s_{sn+})i = +(s_{sp-} - s_{sn-})i. \end{aligned} \tag{5.34}$$

Using (5.30) and (5.31), this can be written as:

$$i_{C_s} = -s_s i. \tag{5.35}$$

The corresponding capacitor voltage is obtained by integration of its current:

$$u_{C_s} = \frac{1}{C_s} \int i_{C_s} \mathrm{d}t. \tag{5.36}$$

### 5.2.3 Hybrid Inverter

The main and sub inverters are connected in series. The total phase output voltage $u$ is the sum of the main- and the sub-inverter voltages (5.23) and (5.32):

$$u = u_m + u_s = s_m u_{C_m} + s_{np} u_{C_{np}} + s_s u_{C_s}. \tag{5.37}$$

The maximum value this can take is the sum of both intermediate-circuit capacitor voltages $u_{C_m}$ and $u_{C_s}$. We will call this the equivalent total intermediate-circuit voltage $u_C$:

$$u_C = u_{C_m} + u_{C_s}. \tag{5.38}$$

We note that, because of our reference-point definition, the minimum value the phase output voltage can take is $-u_C$.

Table 5.2: Phase switching states and voltages of the hybrid asymmetric nine-level inverter. Nominal capacitor voltages $u_C = 1$, $u_{C_m} = 0.75$, $u_{C_s} = 0.25$, $u_{C_{np}} = 0$.

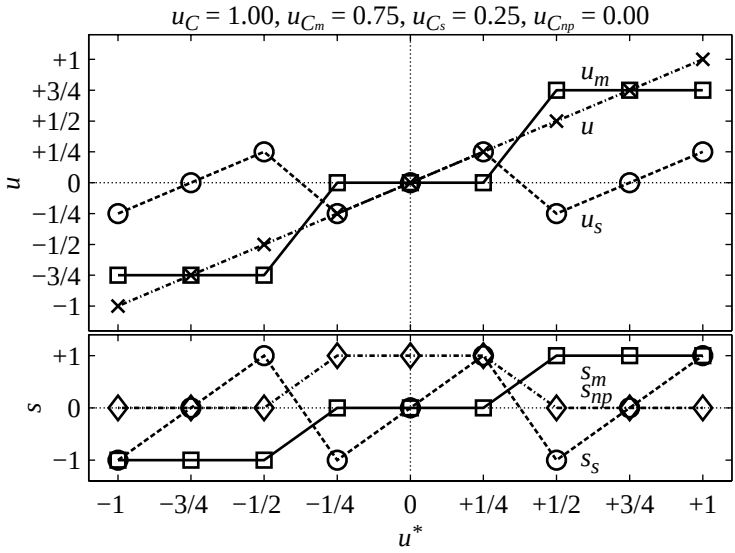
| $s_m$ | $s_s$ | $u_m$ | $u_s$ | $u$ |
|---|---|---|---|---|
| +1 | +1 | +0.75 | +0.25 | +1 |
| +1 | 0 | +0.75 | 0 | +0.75 |
| +1 | −1 | +0.75 | −0.25 | +0.5 |
| 0 | +1 | 0 | +0.25 | +0.25 |
| 0 | 0 | 0 | 0 | 0 |
| 0 | −1 | 0 | −0.25 | −0.25 |
| −1 | +1 | −0.75 | +0.25 | −0.5 |
| −1 | 0 | −0.75 | 0 | −0.75 |
| −1 | −1 | −0.75 | −0.25 | −1 |

The voltages for all possible switching states can be found in Table 5.2, where the total intermediate-circuit voltage is normalized to 1. In order to get a uniform-step nine-level inverter, the ratio of the main and the sub intermediate-circuit capacitor voltages is equal to 3 (see also Chapter 2 and Figure 2.6(b)).

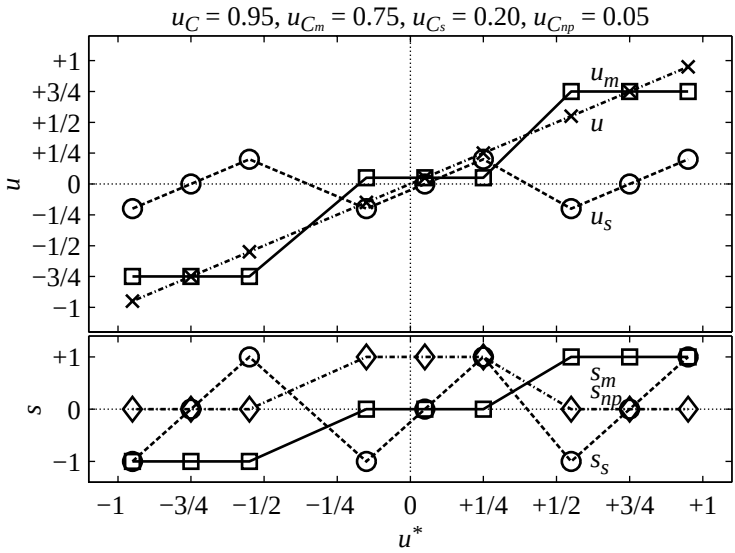
We will operate our hybrid inverter using the pulse-width modulator of Chapter 3, which switches between the two nearest adjacent states. As we have seen in this and the previous section, we can linearly interpolate between the discrete states to obtain a continuous model.

Using the inverter states of Table 5.2 and the modulation method according to (3.6), we can now draw the partial and total phase voltages as a function of the desired (reference) voltage. The result is shown in Figure 5.3(a), along with the corresponding switching functions. The states of Table 5.2 are specially marked. As expected, the total output voltage equals its reference, according to the corresponding line in the diagram.

Figure 5.3(a) shows the inverter voltages and switching functions for the ideal case of nominal intermediate-circuit capacitor voltages. However, we will have rather big fluctuations of these capacitor voltages in our hybrid inverter. To illustrate what happens in such a case, the inverter voltage characteristic is drawn again in Figure 5.3(b). The sub-inverter capacitor voltage is now 20% smaller than its ideal value, and the neutral-point voltage is an equal amount bigger.




(a) Nominal capacitor voltages.




(b) Non-nominal capacitor voltages.

Figure 5.3: Partial and total phase output voltages $u_m$, $u_s$, $u$ and switching functions $s_m$, $s_{np}$, $s_s$ of the hybrid asymmetric nine-level inverter as a function of the reference voltage $u^*$: states (markers) and linear interpolation (lines).

## 5.3 Influence of Common Mode on Capacitor Voltages

As we have seen in Chapter 4, the common-mode part of the inverter output voltage can often be considered as a degree of freedom for the load. But it has an important influence on the intermediate-circuit capacitor currents and voltages.

In this section, we will analyze the influence of a variable common-mode voltage on the intermediate-circuit capacitors, using the inverter model of the previous sections. First, we will analyze the neutral-point voltage of a three-level NPC inverter. Second, we will analyze the three sub-inverter capacitor voltages and the main-inverter neutral-point voltage of our hybrid inverter.

### 5.3.1 Neutral-Point Voltage of NPC Inverter

In a neutral-points-clamped (NPC) inverter (see also Figure 2.2 and 2.8), the neutral-point voltages are usually not fixed from the supply side. An active control method is needed to stabilize these voltage levels [4, 25, 47, 51, 59, 60]. In some operating points large oscillations of the voltages can be observed. To understand these phenomena and to be able to design a stabilization controller, we will investigate the behaviour of the neutral-point voltage of a three-level NPC inverter.

As we have seen for the main inverter in the previous section, the output voltage of a three-level NPC inverter can be expressed in terms of its switching function according to (5.23). In the following, we will assume that the neutral-point voltage remains rather small compared to the total intermediate-circuit voltage. Neglecting the neutral-point voltage, we get:

$$u_{ph} = s_{m,ph} u_{C_m}. \tag{5.39}$$

The subscript $ph$ refers to the considered phase and can take the values $a$, $b$ or $c$. We can separate the phase voltages in a differential- and a common-mode part:

$$u_{ph} = u_{dm,ph} + u_{cm}. \tag{5.40}$$

As in (5.24), the neutral-point switching functions can be expressed as:

$$s_{np,ph} = 1 - |s_{m,ph}|. \tag{5.41}$$

According to (5.26), the neutral-point capacitor current equals:

$$i_{C_{np}} = -\sum_{ph=a,b,c} s_{np,ph} i_{ph}. \tag{5.42}$$

Using (5.41), (5.39) and (5.40), we get:

$$i_{C_{np}} = \sum_{ph=a,b,c} \left( \left| \frac{u_{dm,ph} + u_{cm}}{u_{C_m}} \right| - 1 \right) i_{ph}. \tag{5.43}$$

The corresponding capacitor voltage is obtained by integration of its current:

$$u_{C_{np}} = \frac{1}{C_{np}} \int i_{C_{np}} \mathrm{d}t. \tag{5.44}$$

The main purpose of the inverter is to supply a load. It usually requires symmetrical sinusoidal three-phase voltages. Similar currents are drawn from the inverter. This function should of course not be changed. So, the output currents and *differential*-mode voltages are given quantities for our analysis. There are of course different operating points, where those quantities take different values. For our analysis, only the *common*-mode voltage is variable.

So, as described in Section 4.3 and illustrated in Figure 4.8, 4.9 and 4.10, we will visualize the influence of a possible common-mode output voltage on the neutral-point capacitor current. The function (5.43) is calculated on the reference-voltage cylinder. Figure 5.4 shows the result for a modulation index $m = 0.8$ and a load-current angle $\cos(\varphi) = 0.71$. Dark zones mean a big and light zones a small neutral-point capacitor current.

The cylinder surface can be flattened to a two-dimensional graph, which shows the capacitor current as a function of the output-voltage phase angle and common-mode component. Possible common-mode paths can be drawn on top of it. To find the resulting neutral-point voltage, the current must be integrated along a chosen common-mode path. The graph is different for each output voltage and output current combination. Some examples of capacitor currents and common-mode paths for different operating points are given in Figure 5.5. Dark zones mean a big and light zones a small neutral-point capacitor current, whereas positive and negative zones are indicated with plus and minus signs respectively.

It is interesting to see that the capacitor current is very small along the indicated common-mode paths if the output current is in phase with the output voltage ($\cos(\varphi) = 1$), which means little oscillations in the neutral-point voltage as well. However, the capacitor current (and thus the voltage itself) increasingly oscillates with the third harmonic frequency if the output-current phase angle increases ($\cos(\varphi) \to 0$). For some operating points a common-mode path for zero neutral-point capacitor currents can be found, for others voltage oscillations are unavoidable. By integrating the neutral-point capacitor current along a chosen common-mode path, the amplitude of the oscillations can be calculated.

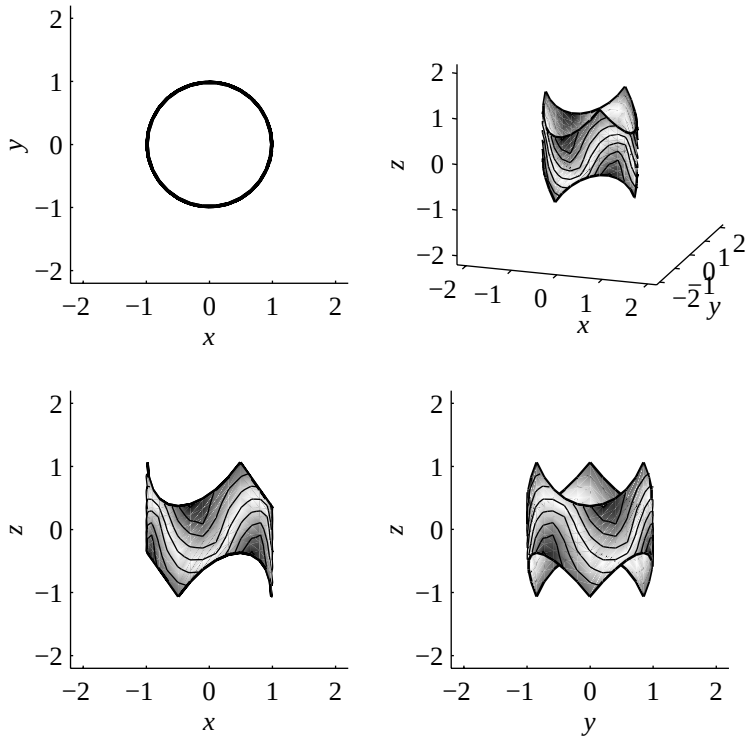



Figure 5.4: Neutral-point capacitor current of a three-level NPC inverter as a function of time and common-mode voltage, with $m = 0.8$, $\cos(\varphi) = 0.7$. Three-dimensional view and the projections on the $xy$-, $xz$- and $yz$-planes respectively.

### 5.3.2 Capacitor Voltages of Hybrid Inverter

In our hybrid inverter (see also Figure 2.11), the main-inverter neutral-point and the sub-inverter intermediate circuits are not connected to a power supply. An active control method is needed to stabilize their voltages. To be able to design a stabilization controller, we will investigate the behaviour of these voltages. We can analyze the capacitor-voltage variations of our hybrid inverter in a similar manner as done for the neutral-point voltage of an NPC inverter.

As we have seen in the previous section, the output voltage of the hybrid inverter can be expressed in terms of its switching functions according to (5.37). The inverse functions, however, can not easily be expressed. They are very

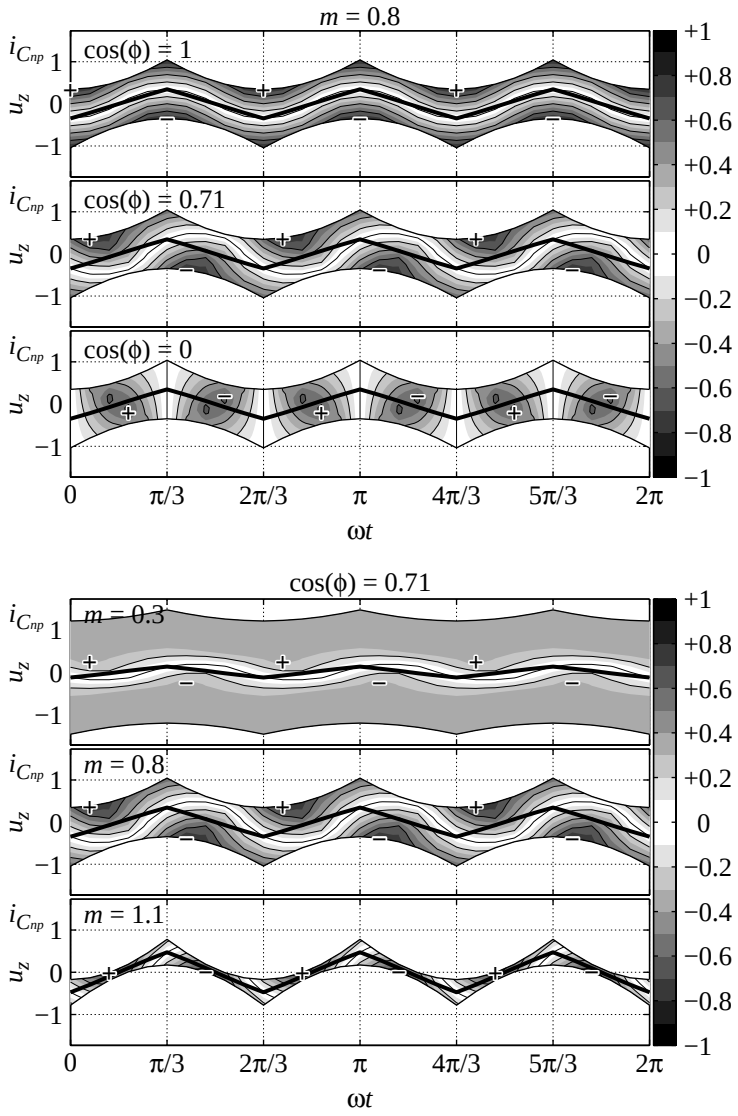



Figure 5.5: Neutral-point capacitor current of a three-level NPC inverter as a function of time and common-mode voltage, for six different operating points. Possible common-mode paths are drawn on top of it.

non-linear functions as can be seen in Figure 5.3.

As we have seen in (5.26), (5.27), (5.35) and (5.36), the capacitor currents and voltages directly depend on these non-linear switching functions:

$$i_{C_{np}} = -\sum_{ph=a,b,c} s_{np,ph}(u_{dm,ph} + u_{cm})i_{ph}, \tag{5.45}$$

$$i_{C_s,ph} = -s_{s,ph}(u_{dm,ph} + u_{cm})i_{ph}. \tag{5.46}$$

The subscript $ph$ refers to the considered phase and can take the values $a$, $b$ or $c$. The corresponding capacitor voltages are obtained by integration of their currents:

$$u_{C_{np}} = \frac{1}{C_{np}} \int i_{C_{np}} \mathrm{d}t, \tag{5.47}$$

$$u_{C_s,ph} = \frac{1}{C_s} \int i_{C_s,ph} \mathrm{d}t. \tag{5.48}$$

As in (5.40), we separated the phase voltages in a differential- and a common-mode part.

The main purpose of the inverter is to supply a load. It usually requires symmetrical sinusoidal three-phase voltages. Similar currents are drawn from the inverter. This function should of course not be changed. So, the output currents and *differential*-mode voltages are given quantities for our analysis. There are of course different operating points, where those quantities take different values. For our analysis, only the *common*-mode voltage is variable.

So, as described in Section 4.3 and illustrated in Figure 4.8, 4.9 and 4.10, we will visualize the influence of a possible common-mode output voltage on the capacitor currents. The functions (5.45) and (5.46) are calculated on the reference-voltage cylinder.

We now have four functions for each operating point, corresponding to the four capacitor currents. For symmetric output voltages and currents, also the sub-inverter capacitor currents and voltages will be symmetric. They will be phase-shifted by 120° from one phase to another, and it is of course sufficient to visualize only one of them. However, since the main problem of our hybrid inverter is to keep the three sub-inverter capacitor voltages charged, it is very instructive to look at the average (common-mode, homopolar) value of their three currents and voltages as well:

$$i_{C_s,h} = \frac{1}{3} \sum_{ph=a,b,c} i_{C_s,ph}. \tag{5.49}$$

$$u_{C_s,h} = \frac{1}{C_s} \int i_{C_s,h} \mathrm{d}t. \tag{5.50}$$

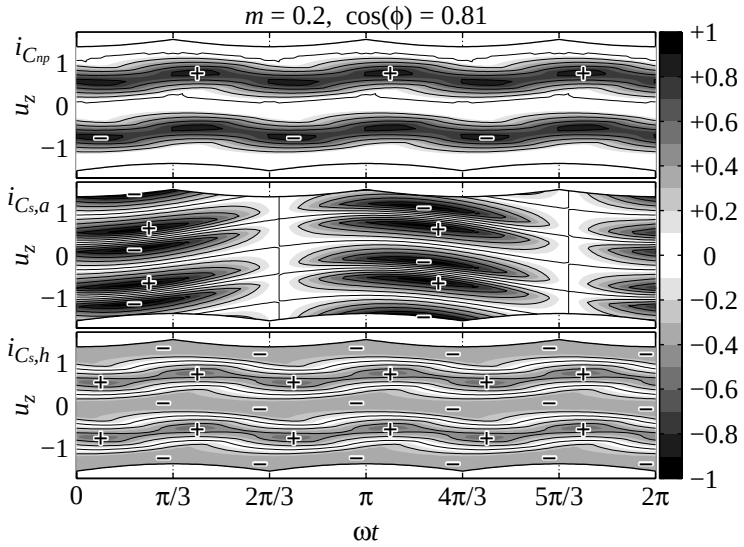



Figure 5.6: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of time and common-mode voltage, with $m = 0.2$, $\cos(\varphi) = 0.81$.

If we can keep the 'average capacitor' charged, we can keep each of them charged, because of the mentioned symmetry. And if we can *not* keep the 'average capacitor' charged, we can keep none of them charged for the same reason.

The cylinder surfaces can be flattened to a two-dimensional graph, which show the capacitor currents as a function of the output-voltage phase angle and common-mode component. Possible common-mode paths can be drawn on top of it. To find the resulting voltages, the currents must be integrated along a chosen common-mode path. The graphs are different for each output voltage and output current combination. Some examples of capacitor currents for different operating points are given in Figure 5.6, 5.7, 5.8, 5.9 and 5.10. Dark zones mean a big and light zones a small neutral-point capacitor current, whereas positive and negative zones are indicated with plus and minus signs respectively.

It is interesting to see that the capacitor currents differ a lot between the different operating points. For most operating points voltage oscillations are unavoidable. Moreover, rather large common-mode voltages might be needed to obtain zero average current (constant average voltage) in all capacitors. By integrating the capacitor currents along a chosen common-mode path, the

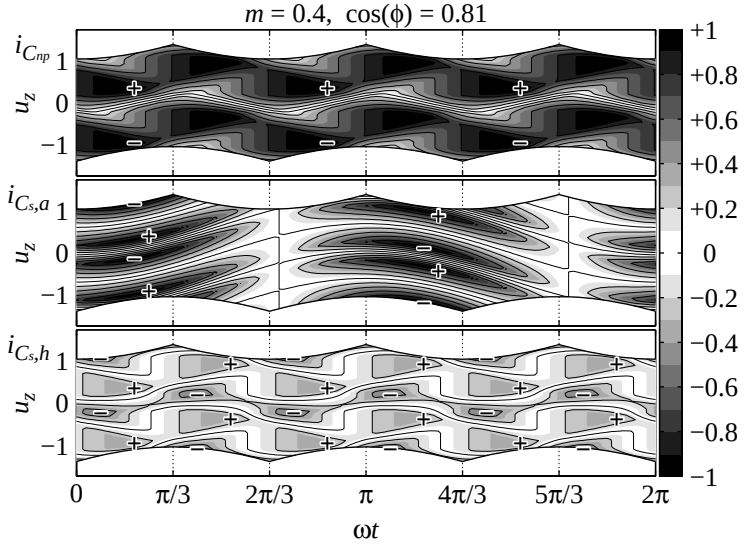



Figure 5.7: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of time and common-mode voltage, with $m = 0.4$, $\cos(\varphi) = 0.81$.

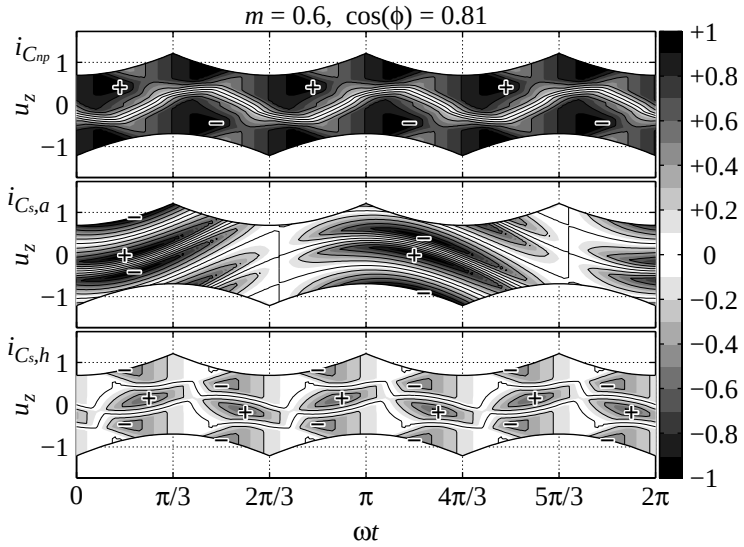



Figure 5.8: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of time and common-mode voltage, with $m = 0.6$, $\cos(\varphi) = 0.81$.

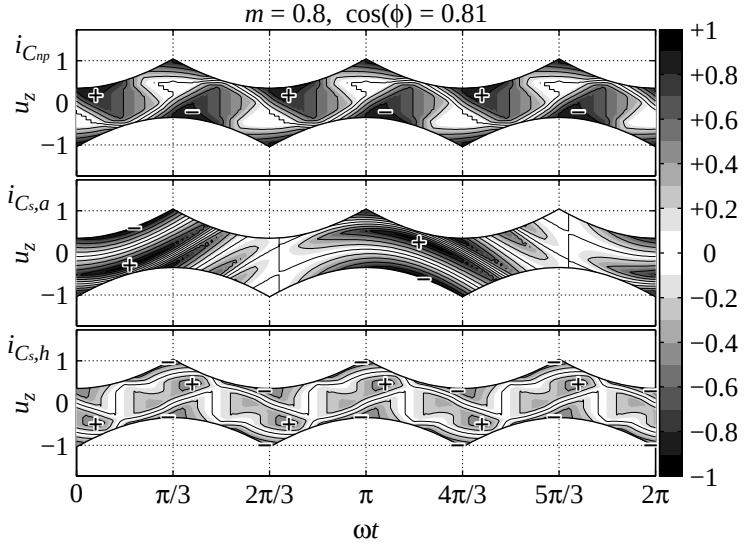



Figure 5.9: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of time and common-mode voltage, with $m = 0.8$, $\cos(\varphi) = 0.81$.

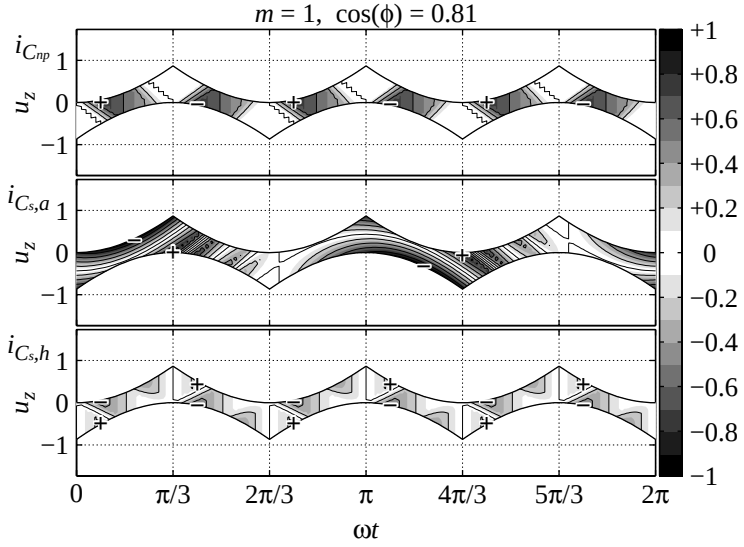



Figure 5.10: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of time and common-mode voltage, with $m = 1.0$, $\cos(\varphi) = 0.81$.

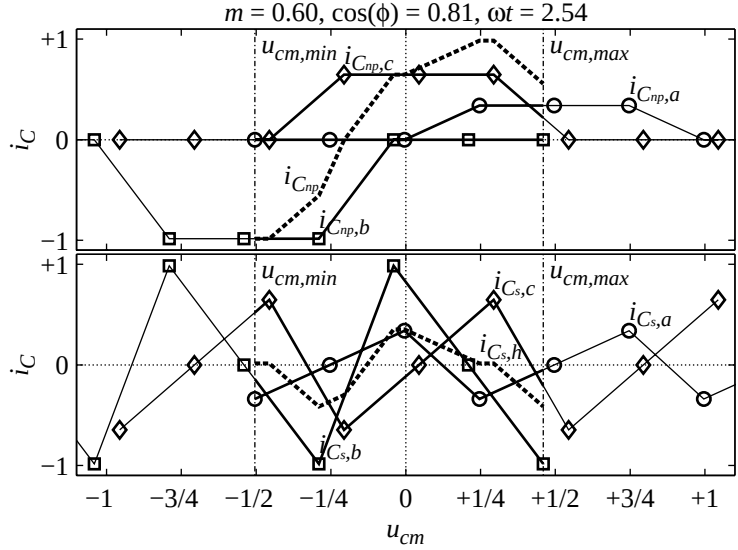



Figure 5.11: Capacitor currents of the hybrid asymmetric nine-level inverter as a function of the common-mode voltage, with $m = 0.6$, $\cos(\varphi) = 0.81$, $\omega t = 2\pi/3 + 0.45$.

amplitudes of the voltage oscillations can be calculated.

To get some better insight in the shape of the capacitor currents, we will take a look at them at a fixed instant in time. An example is given in Figure 5.11, which is a vertical cut through Figure 5.8. It shows the capacitor currents as a function of the common-mode voltage. We recognize the phase switching functions, multiplied by the phase currents and shifted by the differential-mode phase voltages, according to (5.45) and (5.46).

# Chapter 6

# Capacitor-Voltage Stabilization

In the previous chapters, we have described the power-part topology of a hybrid asymmetric multi-level inverter for industrial drives applications. We have discussed an appropriate pulse-width modulation method, and we have developed a mathematical model to describe the basic operating principle and the inverter behaviour.

Since the main-inverter neutral point and the three sub-inverter intermediate circuits are not supplied by a power source, their capacitor voltages have to be stabilized by an appropriate control algorithm. This system is unstable, and without control the non-supplied intermediate-circuit capacitor voltages will quickly run away from their nominal values. A control method is needed to stabilize those voltages, preferably without deteriorating the output voltage.

This chapter describes methods to affect the capacitor voltages without influence on the load, and analyzes their properties. Based on these insights, we propose a strategy to accomplish the desired control. We will show how this strategy can be applied to stabilize the capacitor voltages in our hybrid inverter.

## 6.1 Control Possibilities

In this section, we will look at the possibilities to influence and stabilize the intermediate-circuit capacitor voltages. These are redundant inverter states and the common-mode component of the inverter output voltage. Since these quantities do not influence the load, no interference between the inverter and

load control loops will occur.

### 6.1.1 Redundant States

As we have seen in Chapter 2, multi-level inverters often have several possibilities to generate a certain output voltage. For the load, only the voltage level is of importance, and not the way it is internally generated in the inverter. For this reason, inverter switching states that generate the same output voltage are called redundant states.

Redundant states, however, do have different influence on the inverter. Losses are mainly produced in switching and conducting semiconductor elements. Redundant states have different elements conducting current, so the losses are produced in different parts of the inverter, and by more or less efficient components. Switching to redundant states requires different, and mostly also a different number of semiconductors, to be switched. This, again, has an influence on how much and where losses are produced [5, 9, 16, 21].

Redundant states also differ in how and where the inverter output power is produced. Except for the maximal output voltage, the power mostly originates only from a part of the inverter, whereas other parts do not produce any power. Or it is even possible that one inverter part produces more power than consumed by the load, and another part absorbs the excess power [13,16]. Since the inverter power directly originates from the intermediate-circuit capacitors, and indirectly from the power supplies, the redundant states have an important influence on these elements as well. Especially non-reversible power supplies, like diode rectifiers, cannot feed back energy into the net, which must be taken into account in choosing appropriate inverter states [16]. For non-supplied intermediate-circuit capacitors, the power is directly related to the charging or discharging of the capacitors. This can thus be controlled by choosing an appropriate out of several redundant states. However, a trade-off has to be made between the possibility to control the power flow and the generated losses [16].

The choice of redundant states is of course limited to the states which have redundancies, and by the number of redundancies of those states. Capacitor-voltage control is limited by the availability of redundant states with the desired effect [16]. As a consequence, voltage stabilization can not always be done instantaneously, but only on an average in time. This method can not be used for our hybrid asymmetric nine-level inverter, because it has no redundant states.

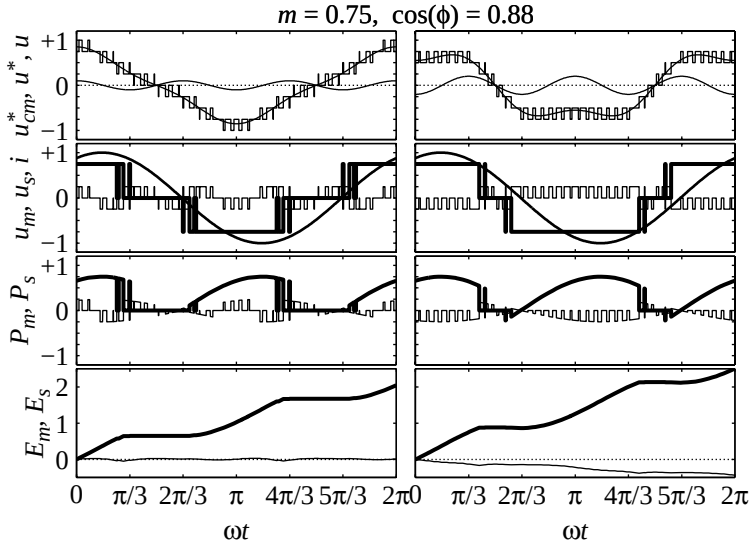



Figure 6.1: Influence of two different 3rd harmonic common-mode voltages on the load sharing within the hybrid inverter. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and main- and sub-inverter voltages $u_m$, $u_s$, powers $P_m$, $P_s$ and energies $E_m$, $E_s$.

### 6.1.2 Common-Mode Voltage

As we have seen in Chapter 4, drives have usually three-phase loads *without* the neutral connected. They are entirely controlled by the differential mode of the output voltage and the common mode has no influence on it.

The common-mode voltage, however, does have an influence on the inverter. By varying this component, it is possible to change the distribution of the fundamental output voltage between the main and sub inverter, and thus their load sharing, as is illustrated in Figure 6.1. Additionally, also the load sharing between the two capacitors in the main inverter, and thus the neutral-point voltage, will be affected. These influences on the capacitor currents and voltages correspond to the inverter model developed in Chapter 5.

Although the common-mode voltage is only one single control variable, we can use it to control several intermediate-circuit capacitor voltages together. In general, voltage stabilization can not be done instantaneously by lack of an equilibrium state, but only on an average in time. The method allows to impose zero average power in all sub inverters and the main-inverter neutral point over almost the whole amplitude, frequency and load range. The only

exception is the area of very high modulation indices ($> 0.95$) combined with high power factors. But this operating area can be avoided by proper converter design.

It is, however, not easy to guarantee power balancing by varying the common-mode voltage. In fact, we need to control four capacitor voltages, or power flows, with the aid of only one control input. Moreover, although well known, the influence of the common-mode voltage on the capacitor voltages is highly non-linear, time varying and operating-point dependent. And, last but not least, we want to impose constraints on the common-mode voltage to avoid negative side effects.

Via parasitic capacitive couplings, which are not negligible in electric motors, common-mode currents will flow via the motor frame to the ground. Those currents will partly flow through the bearings, where they can cause important damage. On the other hand, the common-mode voltage adds up to the normal (differential-mode) motor voltage and will cause additional insulation stress. For these reasons, it is important to keep the common-mode voltage and its time derivative as small as possible.

Capacitor-voltage stabilization via the common-mode inverter voltage can only be used with purely three-phase loads, *without* a neutral connection. This method can be used alone, or in conjunction with the choice of redundant states. We will use it alone to stabilize our hybrid asymmetric nine-level inverter. However, we will need an appropriate control strategy that can deal with all the properties and requirements of this method.

## 6.2 Model-Predictive Control

In the previous section, we have proposed methods to affect the capacitor voltages in an asymmetric multi-level inverter, together with their characteristics. An appropriate control strategy that can deal with all the properties and requirements is model-predictive control (MPC). In this section, we explain the principles of MPC. The following section describes how MPC can be applied to our specific control problem, the capacitor-voltage stabilization in our hybrid asymmetric nine-level inverter.

Model-predictive control is not a specific controller design, but merely a set of ideas to develop control strategies. Various techniques exist under different names. The theory of stability of model-predictive control has reached a relatively mature stage, but progress on other fronts, such as robustness to uncertainty and disturbance attenuation, is still limited. A review of model-predictive control is presented in [61], and other overviews can be found in [62, 63]. We summarize the main points in this section.

### 6.2.1 What is Model-Predictive Control?

Model-predictive control is a form of control in which the current control action is obtained by solving *on-line*, at *each* sampling instant, a finite-horizon open-loop optimal control problem, using the current state of the plant as the initial state. The optimization yields an optimal control sequence and the first control in this sequence is applied to the plant. This is its main difference from conventional control, which uses a pre-computed control law.

The strength of MPC lies in its unique ability to provide *implicit* non-linear feedback, that is to handle control problems where off-line computation of a control law (explicit feedback) is difficult or impossible. This is the case if hard constraints on controls and states are present, or if the plant is non-linear. MPC is also capable to control time-varying or multi-variable plants.

Nearly every application imposes constraints: actuators are naturally limited in force (or equivalent) they can apply, and safety limits states such as temperature, pressure or velocity. MPC has been widely applied in petro-chemical and related industries, where satisfaction of constraints is particularly important, and efficiency demands operating points on or close to the boundary of the set of admissible states and controls. Moreover, in the process industry the plants being controlled are sufficiently slow to permit its implementation.

MPC is *not* a new method of control design, but essentially solves standard optimal control problems (such as $H_2$ and $H_\infty$ linear optimal control). Where it differs from other controllers is that it solves the optimal control problem *on-line* for the current state of the plant, rather than determining *off-line* a feedback policy (that provides the optimal control for all states). The on-line solution is obtained by solving an open-loop optimal control problem in which the initial state is the current state of the system being controlled; this is a mathematical programming problem. Determining the feedback solution, on the other hand, requires solution of the Hamilton–Jacobi–Bellman differential or difference equation, a vastly more difficult task in many cases. From this point of view, MPC differs from other control methods merely in its implementation. The requirement that the open-loop optimal control problem be solvable in a reasonable amount of time (compared with plant dynamics) necessitates, however, the use of a finite horizon and this raises interesting problems.

### 6.2.2 The Open-Loop Optimal Control Problem

The system to be controlled is usually described, or approximated, by an ordinary differential equation. Since the control is normally piece-wise constant,

it is usually modeled by a difference equation

$$x[k+1] = f(x[k], u[k]). \tag{6.1}$$

We employ $\mathbf{u}$ to denote a control sequence and $\mathbf{x}^{\mathbf{u}}$ to denote a state trajectory (sequence) resulting from this control sequence

$$\mathbf{u} = \{u[k], u[k+1], \ldots, u[k+N-1]\}, \tag{6.2}$$
$$\mathbf{x}^{\mathbf{u}} = \{x[k], x^{\mathbf{u}}[k+1], \ldots, x^{\mathbf{u}}[k+N]\}. \tag{6.3}$$

Model-predictive control is obtained by solving on-line an open-loop optimal control problem of minimizing a cost function at the current state $x[k]$

$$\mathcal{P}_N(x[k]) : \min_{\mathbf{u}} V_N(x[k], \mathbf{u}). \tag{6.4}$$

The problem is subject to control and state constraints $u[i] \in \mathbb{U}$ and $x[i] \in \mathbb{X}$, $\forall i$, as well as the terminal 'stability' constraint $x[k+N] \in \mathbb{X}_f \subset \mathbb{X}$. The cost function is defined by

$$V_N(x[k], \mathbf{u}) = \sum_{i=k}^{k+N-1} V(x^{\mathbf{u}}[i], u[i]) + V_f(x^{\mathbf{u}}[k+N]). \tag{6.5}$$

It consists of the stage cost $V(x, u)$ of the states and controls up to the control horizon $N$. A suitable terminal cost $V_f(x)$ at the horizon can be added to ensure stability. The terminal time $k+N$ increases with time $k$ and is often referred to as a *receding horizon*.

Usually, the reference is chosen in the origin, which can be obtained by a suitable change of coordinates. The stage and terminal costs are often quadratic. For time-invariant systems, it is sufficient to regard the current time as zero. Now, the problem $\mathcal{P}_N(x)$ depends only on the actual state $x = x[0]$.

The solution of the problem $\mathcal{P}_N(x)$ yields the optimal control sequence

$$\mathbf{u}^0(x) = \{u^0(x)[0], u^0(x)[1], \ldots, u^0(x)[N-1]\} \tag{6.6}$$

and the value function

$$V_N^0(x) = V_N(x, \mathbf{u}^0(x)). \tag{6.7}$$

The first control $u^0(x)[0]$ in the optimal sequence $\mathbf{u}^0(x)$ is applied to the system at the actual time. This defines an implicit model-predictive control law $g(x) = u^0(x)[0]$. Contrary to explicit feedback control, MPC computes the optimal control *action* $g(x)$ for the specific state $x$, rather than pre-computing the control *law* $g$ for all states.

### 6.2.3 Stability of Model-Predictive Control

Research on stability of model-predictive control has now reached a relatively mature stage. The important factors for stability have been isolated and employed to develop a range of model-predictive controllers that are stabilizing. They differ only in their choice of the ingredients $\mathbb{X}_f$, $g_f(x)$ and $V_f(x)$ that are common to most forms of model-predictive control. The established stability conditions are merely sufficient, not necessary.

It is assumed that a stable desired equilibrium state

$$x_r = f(x_r, u_r) \tag{6.8}$$

exists under the equilibrium control $u_r$. After a suitable change of coordinates, this equilibrium is represented by the origin

$$f(0,0) = 0. \tag{6.9}$$

The stage cost is assumed at least quadratic and zero in the origin

$$V(x,u) \geq c \left\|(x,u)\right\|^2, \quad V(0,0) = 0. \tag{6.10}$$

A terminal constraint set $\mathbb{X}_f$ is defined and the purpose of the model-predictive controller is to steer the state to $\mathbb{X}_f$ in finite time. This set is a subset of the state constraint set and contains the equilibrium state

$$0 \in \mathbb{X}_f \subset \mathbb{X}. \tag{6.11}$$

Inside $\mathbb{X}_f$, a local controller $g_f(x)$ is employed, which satisfies the control constraint

$$g_f(x) \in \mathbb{U}, \quad \forall x \in \mathbb{X}_f \tag{6.12}$$

and keeps the state in $\mathbb{X}_f$

$$f(x, g_f(x)) \in \mathbb{X}_f, \quad \forall x \in \mathbb{X}_f. \tag{6.13}$$

A terminal cost $V_f(x)$ ensures closed-loop stability if

$$V_f(x) \geq V_f(f(x, g_f(x))) + V(x, g_f(x)), \quad \forall x \in \mathbb{X}_f. \tag{6.14}$$

This condition holds if $V_f$ is a control Lyapunov function in a neighborhood of the origin and $g_f$ and $\mathbb{X}_f$ are chosen appropriately. The terminal cost is ideally equal to the infinite-horizon value function $V_\infty^0$, in which case $V_N^0 = V_\infty^0$, to obtain the advantages of an infinite horizon, such as stability and robustness. In practice, however, this can generally only approximately be achieved.

Optimality does not imply stability, especially in finite-horizon problems. On the other hand, feasibility, rather than optimality, suffices for stability. Suboptimality can thus permit satisfactory control if achieving optimality is impractical. Many strategies are possible. For example, the controller may attempt to find an optimal solution (to the optimal control problem) and cease when a permitted time limit is reached. Or it may solve a simpler version (of the optimal control problem), for example one in which only the first few control actions in the sequence are optimized.

## 6.3 MPC for Capacitor Voltage Stabilization

A control method appropriate for the stabilization of the capacitor voltages in an asymmetric multi-level inverter is model-predictive control (MPC). In this section, we describe how MPC can be applied to our specific control problem, the capacitor-voltage stabilization of our hybrid asymmetric nine-level inverter.

The control algorithm will be implemented on a digital signal processor (DSP) and is thus a discrete-time system. Samples on time $kT_S$, where $T_S$ is the sampling time, are denoted with $[k]$. Vector notation is used for three-phase quantities:

$$\vec{x} = \begin{pmatrix} x_a \\ x_b \\ x_c \end{pmatrix}. \tag{6.15}$$

They contain the corresponding $a$-, $b$- and $c$-phase quantities in a column vector.

### 6.3.1 System Model

The four state variables in our control problem are the capacitor voltages of the non-supplied intermediate-circuit capacitors. They equal the integration of their currents

$$u_{C_{np}} = \frac{1}{C_{np}} \int i_{C_{np}} \mathrm{d}t, \tag{6.16}$$

$$\vec{u}_{C_s} = \frac{1}{C_s} \int \vec{i}_{C_s} \mathrm{d}t. \tag{6.17}$$

As we have seen in Chapter 5, the corresponding capacitor currents can be expressed in terms of the phase currents and the inverter switching functions

$$i_{C_{np}} = -\vec{s}_{np}(\vec{u}_{dm} + u_{cm}) \cdot \vec{i} - \frac{u_{C_{np}}}{R_{C_{np}}}, \tag{6.18}$$

$$\vec{i}_{C_s} = -\vec{s}_s(\vec{u}_{dm} + u_{cm})\vec{i} - \frac{\vec{u}_{C_s}}{R_{C_s}}. \tag{6.19}$$

In these equations, $\vec{s} \cdot \vec{i}$ is used for the dot product and $\vec{s}\vec{i}$ for the element-wise product of two vectors. Furthermore, $\vec{s}(\vec{u})$ is a vector of (scalar) function evaluations at the elements of the argument vector, and $\vec{u}_{dm} + u_{cm}$ is an element-wise addition of a constant to a vector. The switching functions depend on the phase voltages in a very non-linear way according to Figure 5.3(a). Moreover, they also depend somewhat on the capacitor voltages as can be seen in Figure 5.3(b).

A term has been added for the currents drawn by parallel discharging resistors, which are usually present in the power circuit. These resistors, assuring capacitor discharging upon converter shut-down, normally have a high impedance to prevent excessive losses. Their corresponding discharge time constants,

$$\tau_{C_m} = C_m R_{C_m} = C_{np} R_{C_{np}} = \tau_{C_{np}}, \tag{6.20}$$

$$\tau_{C_s} = C_s R_{C_s}, \tag{6.21}$$

are typically in the order of several tens to hundreds of seconds.

For our control purpose, we separated the phase voltages in a differential- and a common-mode part. Only the *common*-mode voltage is variable for our analysis, and we will use it as control variable. The *differential*-mode voltages and the phase currents are given quantities. They are imposed by the load and its control loop, and, since the main purpose of the inverter is to supply a load, can or should not be changed. They are usually symmetrical sinusoidal three-phase voltages and currents. There are of course different operating points, where those quantities take different values. Moreover, even for a stationary operating point, those quantities change with time.

As we can see, we have a highly non-linear system which varies in time. It has four states, the capacitor voltages, and one control variable, the common-mode output voltage. Since the output voltage of the inverter is limited, the common-mode voltage can only vary within a limited range. This range is defined by the difference between the maximum (minimum) possible inverter output voltage and the maximum (minimum) value of the differential-mode voltages:

$$-u_C - \min(\vec{u}_{dm}) \leq u_{cm} \leq +u_C - \max(\vec{u}_{dm}). \tag{6.22}$$

We want to keep the variations in the capacitor voltages small, but these are rather soft constraints which we will not further specify.

Since the control will be implemented on a DSP, it is a discrete-time system with a piece-wise constant control output. Therefore, we can model our system with the difference equations according to (6.16), (6.17), (6.18) and (6.19):

$$\begin{aligned} u_{C_{np}}[k+1] &= u_{C_{np}}[k] + \frac{T_S}{C_{np}} i_{C_{np}}[k] \\ &= u_{C_{np}}[k] - \frac{T_S}{C_{np}} \left( \vec{s}_{np}(\vec{u}_{dm}[k] + u_{cm}[k]) \cdot \vec{i}[k] + \frac{u_{C_{np}}[k]}{R_{C_{np}}} \right), \end{aligned} \tag{6.23}$$

$$\begin{aligned} \vec{u}_{C_s}[k+1] &= \vec{u}_{C_s}[k] + \frac{T_S}{C_s} \vec{i}_{C_s}[k] \\ &= \vec{u}_{C_s}[k] - \frac{T_S}{C_s} \left( \vec{s}_s(\vec{u}_{dm}[k] + u_{cm}[k]) \vec{i}[k] + \frac{\vec{u}_{C_s}[k]}{R_{C_s}} \right). \end{aligned} \tag{6.24}$$

In these equations, the phase voltages are the control outputs and therefore constant within a sampling interval. The phase currents, however, are continuous variables and will probably change. Although their variations will be small if the sampling time is small enough, their expected average values should be taken to obtain the best prediction.

### 6.3.2 State Prediction

The main problem of the future state prediction lies in the fact that we do not know the future state and control action of the load, more precisely its currents and voltages. Since the mechanical time constant of a typical high-power drive is much bigger than the electrical time constant of the intermediate-circuit capacitors, the output frequency can be assumed constant even during transients. As a consequence, the output voltage will hardly change in amplitude as well, but some non-negligible, although still quite small, phase jumps could occur. What remains is large uncertainty concerning the output currents during transients, since they can change considerably both in amplitude and in phase. However, since transients are usually relatively rare, we can reasonably assume stationary operation of the load according to the actual state. If practice will show that this is not sufficient in all cases, the motor control must supply additional information to improve the state prediction.

As we noticed before, even in steady-state operation the load voltages and currents change with time. But, since the frequency is known, these variation can be predicted. We will assume constant frequency and amplitude, which

means a rotation of the corresponding vector around the $z$-axis (see also Chapter 4). The rotation matrix for an angle $\vartheta$ around the $z$-axis equals

$$\mathbf{R}^{xyz}(\vartheta) = \begin{pmatrix} \cos\vartheta & -\sin\vartheta & 0 \\ \sin\vartheta & \cos\vartheta & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{6.25}$$

for vectors in $xyz$-space. In $abc$-space this becomes

$$\begin{aligned} \mathbf{R}^{abc}(\vartheta) &= \mathbf{A}^{-1}\mathbf{R}^{xyz}(\vartheta)\mathbf{A} \\ &= \begin{pmatrix} \frac{1+2\cos\vartheta}{3} & \frac{1-\cos\vartheta-\sqrt{3}\sin\vartheta}{3} & \frac{1-\cos\vartheta+\sqrt{3}\sin\vartheta}{3} \\ \ddots & \ddots & \ddots \\ \ddots & \ddots & \ddots \end{pmatrix}. \end{aligned} \tag{6.26}$$

The rotation angle for the voltage and current predictions is $\omega T_S$ every sample interval, where $\omega$ is the output frequency

$$\hat{\vec{u}}_{dm}[k+1] = \mathbf{R}(\omega T_S)\hat{\vec{u}}_{dm}[k], \tag{6.27}$$

$$\hat{\vec{i}}[k+1] = \mathbf{R}(\omega T_S)\hat{\vec{i}}[k]. \tag{6.28}$$

The motor-control output voltages and the measured currents are sampled *at* the actual time $k = 0$. However, to obtain predictions for their average values *over* the next sample interval, a rotation over half this interval must be performed

$$\hat{\vec{u}}_{dm}[0] = \mathbf{R}(\tfrac{\omega T_S}{2})\vec{u}_{dm}[0], \tag{6.29}$$

$$\hat{\vec{i}}[0] = \mathbf{R}(\tfrac{\omega T_S}{2})\vec{i}[0]. \tag{6.30}$$

All the following predictions according to 6.27 and 6.28 are now average values over the following sample interval as well, and we obtain the corresponding sequences

$$\hat{\vec{\mathbf{u}}}_{dm} = \{\hat{\vec{u}}_{dm}[0], \hat{\vec{u}}_{dm}[1], \ldots, \hat{\vec{u}}_{dm}[N-1]\}, \tag{6.31}$$

$$\hat{\vec{\mathbf{i}}} = \{\hat{\vec{i}}[0], \hat{\vec{i}}[1], \ldots, \hat{\vec{i}}[N-1]\}. \tag{6.32}$$

Putting a feasible control sequence

$$\mathbf{u}_{cm} = \{u_{cm}[0], u_{cm}[1], \ldots, u_{cm}[N-1]\} \tag{6.33}$$

and the predicted load sequences (6.31) and (6.32) into our system model (6.23) and (6.24), we obtain a predicted system state trajectory

$$\hat{\vec{\mathbf{u}}}_{C_v} = \{\vec{u}_{C_v}[0], \hat{\vec{u}}_{C_v}[1], \hat{\vec{u}}_{C_v}[2], \ldots, \hat{\vec{u}}_{C_v}[N]\}. \tag{6.34}$$

Its elements

$$\vec{u}_{C_v} = \begin{pmatrix} u_{C_{np}} \\ u_{C_s,a} \\ u_{C_s,b} \\ u_{C_s,c} \end{pmatrix} \tag{6.35}$$

contain the four variable capacitor voltages in a column vector.

### 6.3.3 Control Problem and Cost Function

The open-loop optimal control problem for the intermediate-circuit capacitor voltage stabilization, which must be solved on-line, can now be formulated as follows

$$\mathcal{P}_N(\vec{u}_{C_v}[0], \hat{\mathbf{u}}_{dm}, \hat{\vec{\mathbf{i}}}) : \min_{\mathbf{u}_{cm}} V_N(\vec{u}_{C_v}[0], \hat{\mathbf{u}}_{dm}, \hat{\vec{\mathbf{i}}}, \mathbf{u}_{cm}). \tag{6.36}$$

This problem is subject to the time-varying control constraints

$$-u_C - \min(\vec{u}_{dm}[k]) \leq u_{cm}[k] \leq +u_C - \max(\vec{u}_{dm}[k]). \tag{6.37}$$

We want to keep the variations in the capacitor voltages small, but these are rather soft constraints which we will not further specify.

The control objective is to keep the variable capacitor voltages close to their reference values, otherwise said to keep the deviation errors

$$\varepsilon\vec{u}_{C_v}[k] = \vec{u}_{C_v}[k] - \vec{u}^*_{C_v}[k] \tag{6.38}$$

small. This can be achieved by using an appropriate term in the optimal-control cost function. On the other hand, it is also important to keep the common-mode voltage $u_{cm}$ and its time derivative $\frac{\mathrm{d}u_{cm}}{\mathrm{d}t}$ as small as possible. Additionally, to obtain a 'sufficiently smooth' common-mode voltage, its second order time derivative $\frac{\mathrm{d}^2u_{cm}}{\mathrm{d}t^2}$ can be kept small as well. Since the (average) output voltage is sampled and piece-wise constant, we will use the following approximations for the mentioned time derivatives:

$$\delta u_{cm}[k] = \frac{u_{cm}[k] - u_{cm}[k-1]}{T_S}, \tag{6.39}$$

$$\delta^2 u_{cm}[k] = \frac{\delta u_{cm}[k] - \delta u_{cm}[k-1]}{T_S}. \tag{6.40}$$

We can achieve the aforementioned control requirements by using appropriate terms in the cost function.

For all the terms in the cost function, we will use the squares of the quantities to keep small. Suitable coefficients are used to weight contributions of different importance. As a result, our optimal-control cost function becomes

$$V_N(\vec{u}_{C_v}[0], \hat{\vec{\mathbf{u}}}_{dm}, \hat{\vec{\mathbf{i}}}, \mathbf{u}_{cm}) = \sum_{k=0}^{N-1} \Big[ (\varepsilon \hat{u}_{C_{np}}[k+1])^2 + \\ + (\varepsilon \hat{u}_{C_s,a}[k+1])^2 + (\varepsilon \hat{u}_{C_s,b}[k+1])^2 + (\varepsilon \hat{u}_{C_s,c}[k+1])^2 + \\ + (c_{u_{cm}} u_{cm}[k])^2 + (c_{\delta u_{cm}} \delta u_{cm}[k])^2 + (c_{\delta^2 u_{cm}} \delta^2 u_{cm}[k])^2 \Big]. \quad (6.41)$$

With this choice, positive and negative errors have the same cost contribution, and big errors are much more important than small errors.

Unfortunately, our system does not have an equilibrium state according to (6.8). For this, zero capacitor currents would be needed. The analysis of the system behaviour in Chapter 5 shows us that this can rarely be achieved for all four capacitors at the same time. As a consequence, we can not stabilize our system (in the sense of keeping it in an equilibrium state), and the stability conditions of the previous section can not be applied.

Remains the question if we can keep the system in a sufficiently small region around the reference point. Unfortunately, a proof similar to (6.11), (6.12) and (6.13) can not be found. As an example, we will look at Figure 5.9, but we have similar cases for all rather big output voltages combined with smaller power factors. There are moments in time where the neutral-point capacitor current $i_{C_{np}}$ is positive for all possible common-mode voltages. As a consequence, if the neutral-point capacitor voltage is on its 'maximum' border of a region around the origin, we can not keep the state inside this region.

Since stability can not be enforced by a suitable formulation of the optimal control problem, we will try to achieve it by tuning cost and horizon parameters. Although this is an art of 'playing games', an other method seems not to be available yet.

### 6.3.4 Problem Optimization

The solution of our open-loop optimal control problem—of minimizing the cost function described above—requires a suitable optimization algorithm. Since the problem must be solved on-line, that is at every sampling instant, the solution has to be found in a reasonable amount of time. For typical motor drives, the sampling frequency is ranging from several hundreds of hertz to a

few kilohertz. As a consequence, we have time in the order of a few hundred microseconds up to a few milliseconds to find a solution.

Function minimization in general is delicate and time consuming. It can be extremely difficult to avoid local minima. In order to obtain a good solution and to find it in few iterations, it is very useful to have a good initial guess. As shown in Section 5.3, the system has a $3^{\text{rd}}$ harmonic[1] symmetry. We will use multiples of this symmetry as initial guess for the common-mode voltage, e.g. a $3^{\text{rd}}$ and a $9^{\text{th}}$ harmonic. In steady-state and without any perturbations, this would be sufficient to stabilize the capacitor voltages [14]. Consequently, the problem optimization starts close to a feasible solution (which suffices for stability, see also Section 6.2) and is likely to find it fast. The initial guess can be further improved by taking the previous optimal solution into account.

Since the controller is usually executed at a fixed frequency, the available solution-search time has an upper limit. Therefore, the number of iterations must be limited to limit the calculation time. This will limit the precision of the found optimum, and especially may result in solutions with variable precision. However, a (once in a while) sub-optimal solution is normally sufficient for system stability (see also Section 6.2).

Our cost-function minimization is an optimization problem with $N$ (the control horizon) variables. However, while maintaining the horizon for the state prediction $N$, a reduced horizon for the control optimization $N_O$ can be used. Since the typical capacitor discharge time constants (6.20) and (6.21) are in the order of several tens to hundreds of seconds, the influence of a control action lasts long on the capacitor voltages (for a given load state). Consequently, not all controls up to the prediction horizon are needed to control the system up to there, especially if a good initial solution used. A minimum prediction horizon is required to cover the system dynamics and obtain satisfactory control performance. But it is mainly the optimization horizon—which equals the number of variables in the problem—that determines the calculation effort, and a reduced value will thus result in a faster problem solution.

Many minimization strategies somehow use the first, and maybe even the second, derivative of the cost function. If the calculation of the exact derivative can be done with reasonable effort, the optimization effort can be considerably reduced by avoiding calculation of its finite-difference approximation [64]. Although our system is highly non-linear, it is piece-wise linear and the exact derivative can be easily determined. Details of these calculations are given in Appendix A.

The minimization of our cost function is a non-linear least-squares optimization problem. We will consider two algorithms for its solution. The first

[1] Harmonics are always referred to the actual fundamental period, which depends on the output frequency.

is the non-linear least-squares optimization function '`lsqnonlin`' of the Matlab Optimization Toolbox [64]. This is a general function adapted to minimize a large variety of problems. Although it works well for the solution of our problem, its calculation effort is rather big. Moreover, its implementation is laborious, which hinders its translation to other environments. The second algorithm is a simple and computationally efficient gradient-search method (see also [64]). Writing the feasible common-mode voltage sequence (6.33) as a vector $\vec{u}_{cm}$ in the optimization space $\mathbb{R}^N$,

$$\vec{u}_{cm} = \begin{pmatrix} u_{cm}[0] \\ u_{cm}[1] \\ \vdots \\ u_{cm}[N-1] \end{pmatrix}, \tag{6.42}$$

our gradient search updates it each iteration in the direction of the steepest cost-function descent:

$$\vec{u}_{cm}^{[i+1]} = \vec{u}_{cm}^{[i]} - \alpha^{[i]} \nabla V_N^{[i]}. \tag{6.43}$$

Here, $\nabla V_N$ denotes the cost-function gradient, superscript $[i]$ the iteration number, and $\vec{u}_{cm}^{[0]}$ the initial guess. For an optimal step size, the search coefficient $\alpha$ is adapted each iteration:

$$\alpha^{[i+1]} = \alpha^{[i]} \frac{\left\| \nabla V_N^{[i]} \right\|}{\left\| \nabla V_N^{[i+1]} - \nabla V_N^{[i]} \right\|}, \quad \text{with } \alpha^{[0]} = 1. \tag{6.44}$$

The performance of this method proved to be sufficient in case of a good initial guess.

In spite of all mentioned reductions, the calculation effort remains huge. A fast processor and highly optimized program code are indispensable for a real-time implementation.

# Chapter 7

# Implementation and Results

In the previous chapters, we have described the power-part topology of a hybrid asymmetric multi-level inverter for industrial drives applications. We have discussed an appropriate pulse-width modulation method, and we have developed a strategy to stabilize its non-supplied intermediate-circuit capacitor voltages, based on a mathematical model of the inverter behaviour. For the development of these models, methods and strategies, extensive use of computer calculations and simulations has been employed. In order to validate the obtained results, a low-voltage laboratory prototype of a hybrid-inverter drive system has been built and tested. Obviously, such a system must be designed and numerical values need to be chosen for the formerly symbolic parameters.

This chapter describes the design of our hybrid inverter in a drive application. We will discuss its implementation in a simulation model, together with the obtained results. The realization of a laboratory prototype required adaptations in the controller design, which we will comment. The prototype has been subjected to extensive tests, whose results will be presented and discussed.

## 7.1 System Design

In this section, we will design our hybrid inverter together with its controllers for a drive application. Focus is on medium-voltage applications, but we will use relative quantities as much as possible to ease scaling and comparison. For reasons of size, robustness and cost, asynchronous motors are preferred in many applications. We will consider and use such a load, but a synchronous machine or a line-side converter would not significantly alter the inverter design.

### 7.1.1 Voltage Levels

The principal parameters concern the voltage levels in the converter. The nominal equivalent total intermediate-circuit voltage $u_{C,N}$ equals the sum of the main- and sub-inverter values according to (5.38):

$$u_{C,N} = u_{C_m,N} + u_{C_s,N}. \tag{7.1}$$

We choose a value equal to the nominal output voltage $U_N$:

$$\boxed{u_{C,N} = U_N.} \tag{7.2}$$

In Chapter 2, we decided to use a ratio of 3 between the capacitor voltages of the main and the sub inverter:

$$\boxed{\frac{u_{C_m,N}}{u_{C_s,N}} = 3,} \tag{7.3}$$

and with (7.1) their values become:

$$\boxed{\begin{aligned} u_{C_m,N} &= \tfrac{3}{4}u_{C,N}, \\ u_{C_s,N} &= \tfrac{1}{4}u_{C,N}. \end{aligned}} \tag{7.4}$$

In case of a 4 kV motor, these voltages are 3 kV for the main and 1 kV for the sub inverters. Using a 400 V motor, the values are 300 V and 100 V respectively.

In Chapter 3, we defined the modulation index as the ratio of the fundamental phase-voltage amplitude and the maximum inverter phase output voltage. The nominal modulation index $m_N$ is thus:

$$m_N = \frac{\sqrt{\frac{2}{3}}U_N}{u_{C,N}}. \tag{7.5}$$

Substituting the design criterion (7.2), we get:

$$\boxed{m_N = \sqrt{\tfrac{2}{3}} \approx 0.82.} \tag{7.6}$$

With this choice, we stay well within the controllable region for the sub-inverter capacitor voltages ($m < 0.95$, see Chapter 6), even allowing for 10% supply undervoltage without problems. Furthermore, the necessary common-mode voltage turns out to be very small at this modulation depth, which is ideal for operation around the nominal voltage. This is especially advantageous for a line-side converter.

### 7.1.2 Switching Frequency

The effective switching frequency $f_{sw}$ (or modulation frequency) influences several aspects of a converter. On the one hand, it permits to reduce the output harmonic content. But, on the other hand, it is limited by the device switching capabilities and generated switching losses. We choose a value of

$$\boxed{f_{sw} = 1 \text{ kHz},} \tag{7.7}$$

which is fairly reasonable for this converter in medium-voltage applications. In fact, the effective device switching rates will be lower than this value.

The main inverter modulates only in two of the eight modulation bands ($[-\frac{1}{2}, -\frac{1}{4}]$ and $[+\frac{1}{4}, +\frac{1}{2}]$ in Figure 5.3(a), see also Chapter 3). As a consequence, its IGCT devices switch at a much lower rate on average, not causing too much switching losses in spite of their higher operating voltage.

The sub-inverters switch at the specified frequency. But by taking advantage of the zero-state redundancy within the sub inverters (see Table 5.1), the effective device switching rate can be reduced by a factor 2 for most of the modulation bands. This can be accomplished for the six bands that include a zero state ($[-1, -\frac{3}{4}]$, $[-\frac{3}{4}, -\frac{1}{2}]$, $[-\frac{1}{4}, 0]$, $[0, +\frac{1}{4}]$, $[+\frac{1}{2}, +\frac{3}{4}]$ and $[+\frac{3}{4}, +1]$ in Figure 5.3(a)). In the other two bands ($[-\frac{1}{2}, -\frac{1}{4}]$ and $[+\frac{1}{4}, +\frac{1}{2}]$), we modulate directly between the two active states $+1$ and $-1$ without any redundancies. The employed IGBT devices can easily handle these switching rates due to their relatively low operating voltage.

### 7.1.3 Intermediate-Circuit Capacitors

The size of the intermediate-circuit capacitors is characterized by their energy-storage capacity $E_C$, which we shall define relative to the nominal apparent output power $S_N$. For the main inverter, the two capacitors together have a nominal energy-storage capacity $e_{m,N}$:

$$e_{m,N} = \frac{2E_{C_m,N}}{S_N} = \frac{2\frac{1}{2}C_m u^2_{C_m,N}}{S_N}, \tag{7.8}$$

and their capacity $C_m$ can be expressed as:

$$C_m = \frac{e_{m,N} S_N}{u^2_{C_m,N}}. \tag{7.9}$$

For the equivalent neutral-point capacitor $C_{np}$, which is the parallel connection of the two intermediate-circuit capacitors $C_m$ (5.20), we get:

$$C_{np} = \frac{2e_{m,N} S_N}{u^2_{C_m,N}}. \tag{7.10}$$

Similar to the main inverter, the three sub-inverter capacitors together have a nominal energy-storage capacity $e_{s,N}$:

$$e_{s,N} = \frac{3E_{C_s,N}}{S_N} = \frac{3\frac{1}{2}C_s u_{C_s,N}^2}{S_N}, \tag{7.11}$$

and their capacity $C_s$ can be expressed as:

$$C_s = \frac{2e_{s,N}S_N}{3u_{C_s,N}^2}. \tag{7.12}$$

We prefer to have oscillations of similar magnitude in the sub-inverter capacitors and the main-inverter neutral point. Since they carry similar currents (5.26) and (5.35), this can be obtained by choosing equal capacities:

$$\boxed{\frac{C_{np}}{C_s} = 1.} \tag{7.13}$$

Using (7.10) and (7.12), the ratio of these capacities can be written as:

$$\frac{C_{np}}{C_s} = 3\frac{e_{m,N}}{e_{s,N}}\left(\frac{u_{C_s,N}}{u_{C_m,N}}\right)^2. \tag{7.14}$$

Substituting the design criteria (7.13) and (7.3), the ratio of their nominal energy-storage capacities becomes:

$$\boxed{\frac{e_{m,N}}{e_{s,N}} = 3.} \tag{7.15}$$

The needed size of the intermediate-circuit capacitors is determined by their tolerable voltage oscillations. Such oscillations result from two phenomena. The first is the inverter switching linked to its modulation, and leads to oscillations at the switching frequency[1]. The second is the load sharing between inverter parts, corresponding to the inverter model developed in Chapter 5. Fundamentally, it results in oscillations with the 2nd or 3rd harmonic of the output frequency $f$, but other frequencies can be imposed in the capacitor currents (6.18) and (6.19) via the common-mode voltage. The capacitor-voltage oscillations are inversely proportional to their frequencies (at a given current). In our case, the switching frequency (7.7) is much bigger than the nominal output frequency $f_N$, which usually has values of

$$\boxed{f_N = 50 \ldots 60 \text{ Hz}.} \tag{7.16}$$

[1] A similar phenomenon occurs in the diode rectifier on the supply side, in this case at the natural commutation frequency of its 6- or 12-pulse configuration.

Consequently, the output-frequency harmonics are the dominant factor for our capacitor design.

For our design, we will use values similar to that of a modern and comparable medium-voltage drive[2]:

$$\boxed{\begin{aligned} e_{m,N} &= 15 \text{ Ws/kVA}, \\ e_{s,N} &= \ 5 \text{ Ws/kVA}. \end{aligned}} \tag{7.17}$$

With these values, the voltage oscillations in the neutral point and the sub-inverter capacitors indeed turn out to be about equal, and we will see in the following sections that their magnitudes are around 5% of the inverter step. A somewhat smaller energy-storage capacity would still be possible and give acceptable results.

Usually, parallel discharging resistors $R_{C_m}$ and $R_{C_s}$ are present in the power circuit to assure capacitor discharging upon converter shut-down. They should have a high impedance to prevent excessive losses during normal operation. We shall define these losses $P_{R_C}$ relative to the nominal apparent output power $S_N$. For the main inverter, the two resistors together dissipate the nominal power $p_{m,N}$:

$$p_{m,N} = \frac{2P_{R_{C_m},N}}{S_N} = \frac{2u^2_{C_m,N}}{R_{C_m}S_N}, \tag{7.18}$$

and their resistance $R_{C_m}$ can be expressed as:

$$R_{C_m} = \frac{2u^2_{C_m,N}}{p_{m,N}S_N}. \tag{7.19}$$

Similar to the main inverter, the three sub-inverter resistors together dissipate the nominal power $p_{s,N}$:

$$p_{s,N} = \frac{3P_{R_{C_s},N}}{S_N} = \frac{3u^2_{C_s,N}}{R_{C_s}S_N}, \tag{7.20}$$

and their resistance $R_{C_s}$ can be expressed as:

$$R_{C_s} = \frac{3u^2_{C_s,N}}{p_{s,N}S_N}. \tag{7.21}$$

[2]The energy-storage capacity in ABB's ACS 1000 medium-voltage drive [2,39]—an NPC inverter as shown in Figure 2.8—is 5 Ws/kVA [65]. It is designed for 50 or 60 Hz loads and operates at a switching frequency of 1 kHz. Due to the (approximately three times) bigger inverter step, bigger voltage oscillations are allowed, resulting in smaller capacitors.

As a result, the corresponding discharge time constants (6.20) and (6.21) become:

$$\tau_{C_m} = C_m R_{C_m} = \frac{2e_{m,N}}{p_{m,N}}, \tag{7.22}$$

$$\tau_{C_s} = C_s R_{C_s} = \frac{2e_{s,N}}{p_{s,N}}, \tag{7.23}$$

which is obtained by substituting (7.9), (7.12), (7.19) and (7.21).

The exact values are only of minor importance to our design. As an example, we propose some reasonable values:

$$\boxed{\begin{aligned} p_{m,N} &= 1.0 \text{ W/kVA}, \\ p_{s,N} &= 0.5 \text{ W/kVA}. \end{aligned}} \tag{7.24}$$

This leads to the following discharge time constants:

$$\boxed{\begin{aligned} \tau_{C_m} &= 30 \text{ s}, \\ \tau_{C_s} &= 20 \text{ s}, \end{aligned}} \tag{7.25}$$

which are in the typical order of several tens to hundreds of seconds.

### 7.1.4 Control

The controller design follows the system configuration. Compared to the principle power-part topology presented in Figure 2.11, some 'bells and whistles' are added to the circuit to use it in a drive application. This comprises the capacitor discharge resistors (7.19) and (7.21), pre-charge resistors and bypass contactors (which will be discussed in Chapter 8), and voltage and current measurements. Figure 7.1 depicts the whole electrical circuit in a drive application, including the supply net and the motor.

From the control viewpoint, the electrical circuit is part of a bigger system. On the one hand, there is the mechanical load driven by the motor, and, on the other hand, a controller is added to control our drive. The corresponding block diagram is shown in Figure 7.2. We will use the capacitor voltages and motor currents as control inputs, together with a frequency set-point. Control outputs are the switching commands for the main and the sub inverters, together with that for the pre-charge contactors. In general, the load torque is a function of the shaft speed and position. We will not look into its details in this dissertation.

The controller itself consists of two main parts: a 'charging' and a 'running' controller, as shown in Figure 7.3. The former assures proper capacitor

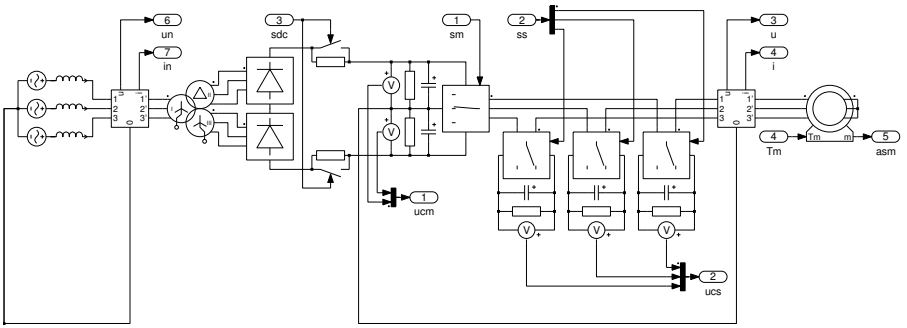



Figure 7.1: Electrical circuit of our hybrid inverter in a drive application.

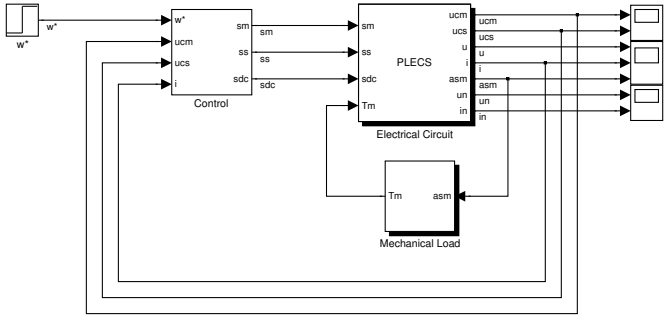



Figure 7.2: Block diagram of the whole drive system.

charging at converter start-up—which we will explain in Chapter 8—and the latter provides for motor and inverter control at normal operation. These control algorithms will be implemented on a digital signal processor (DSP) as a discrete-time system. We will sample this system synchronously to the modulation intervals (see also Chapter 3), at the times $kT_S$, where $T_S$ denotes the sampling time. Using a triangular modulation carrier of a frequency $f_{sw}$ (7.7), which comprises two modulation intervals per period, we have the following choices for the sampling time:

$$\boxed{T_S = N_S \frac{1}{2f_{sw}}, \quad \text{with } N_S \in \mathbb{N}^+.} \tag{7.26}$$

The choice of the sampling ratio $N_S$ is a trade-off between controller dynamics and available calculation time. In case of low switching frequencies—below a couple of kilohertz, as in our case—, typically values of 1 or 2 are employed.

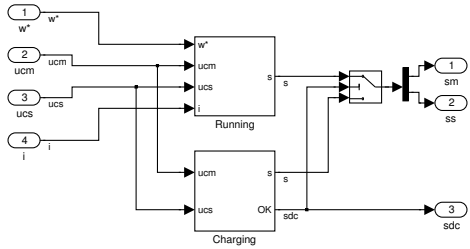



Figure 7.3: Block diagram of the drive controller.

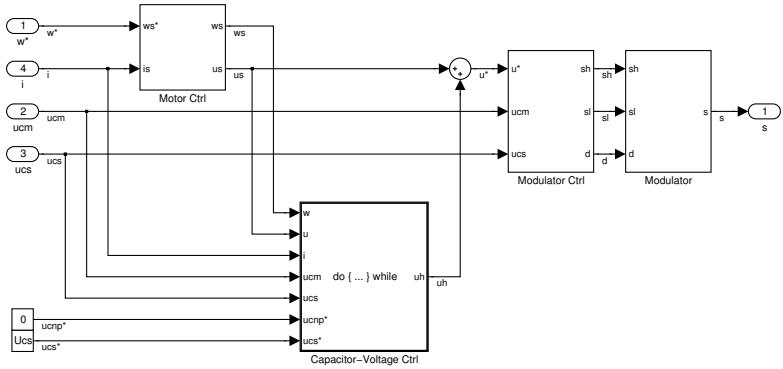



Figure 7.4: Block diagram of the normal-operation controller.

### Normal Operation

For the normal operation of our drive, we can distinguish several functional blocks (see Figure 7.4). We will discuss each of them in the following.

An indispensable part of a drive control is closely linked to the inverter and its operation mode: the modulator. We treated this subject in detail in Chapter 3. The modulator itself is implemented in (programmable) hardware corresponding to Figure 3.11, due to its continuous-time nature. Its (sampled) inputs are provided by a modulation commander, which calculates these signals according to (3.6) or (3.9). As this is executed in discrete time, we implement it on the DSP. The union of the three functional blocks—modulation commander, modulator and inverter—forms a power amplifier in our drive system, with an ideal transfer function of unity from the reference voltages to the (averaged) inverter output voltages. However, we will implement those functional blocks differently—in control software executed on a DSP, in control hardware, and in power circuitry.

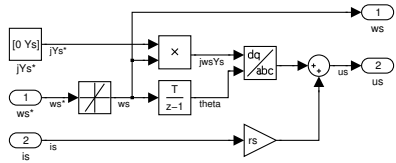



Figure 7.5: Block diagram of the motor controller.

The main functionality of a drive concerns the control of the motor and its load. We will not employ sophisticated approaches in this dissertation, but use a simple open-loop constant flux control (constant $V/f$), as shown in Figure 7.5. To improve its performance in the low-speed region, we compensate the stator-resistance voltage drop. The stator-frequency change rate is kept limited according to the motor inertia and load characteristics.

As we have seen in Chapter 2, the non-supplied intermediate-circuit capacitor voltages in our hybrid inverter have to be stabilized by an appropriate control algorithm. This functionality is performed by the capacitor-voltage controller. As proposed in Chapter 6, it acts on the common-mode component of the inverter output voltage to accomplish the desired control. This component is added to its differential-mode counterparts, which are generated by the motor controller.

### Capacitor-Voltage Stabilization

In Chapter 6, we proposed a strategy to accomplish this voltage stabilization: model-predictive control (MPC). The algorithm predicts the evolution of the capacitor voltages as a function of the common-mode voltage, utilizing a load and an inverter model. The predictions cover a fixed interval starting at the actual time. A cost function of the capacitor-voltage errors and the common-mode voltages is defined, and the optimal common-mode voltage to be applied to the system is obtained by iteratively minimizing this cost function in real time. The corresponding block diagram is shown in Figure 7.6.

In a first step, which represents the load model, the inverter output currents and voltages for the next $N$ samples (the control horizon) are predicted. Taking into account the difficulty, or even the impossibility to predict the state of the load, its prediction model simply supposes stationary operation according to the actual state (see Chapter 6). This prediction model is described by (6.27)–(6.30) and results in the prediction sequences (6.31) and (6.32). We can show that it takes considerably less floating-point operations to implement the rotations in $xyz$-space using (6.25) than in $abc$-space using (6.26), even if the transforms from and to $abc$-space using (4.3) and (4.4) are taken into account.

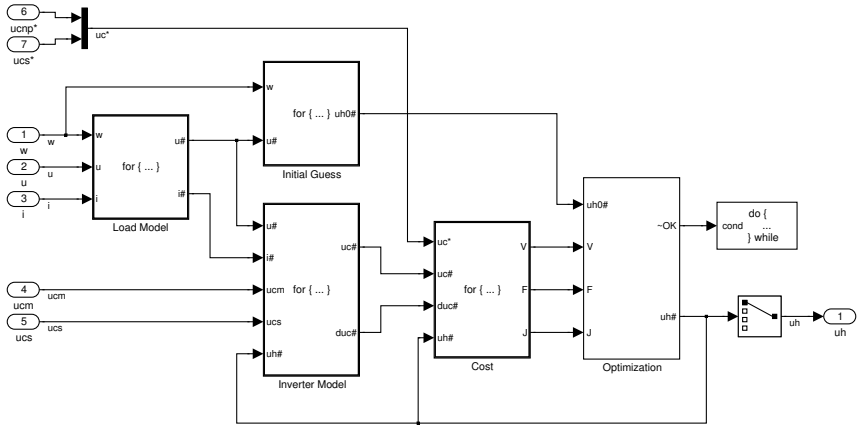



Figure 7.6: Block diagram of the capacitor-voltage controller.

Since the load is not affected by the common-mode voltage, these prediction can be kept outside the optimization iteration loop.

In a second step, which represents the inverter model, the capacitor currents and voltage evolutions are predicted using (6.23) and (6.24). The obtained prediction sequence (6.34) is based on the current and voltage predictions from the load model, (6.31) and (6.32), together with some feasible common-mode voltage sequence (6.33) from the optimizer. Although this inverter model in principle is very accurate, its output accuracy depends, of course, highly on that of its inputs taken from the load model. To benefit of a reduced optimization effort, we will calculate the exact derivative of our cost function (see Chapter 6). For this purpose, the partial derivatives of the predicted capacitor voltages with respect to the common-mode voltages will be calculated according to the developments in Appendix A as well.

The third step consists of calculating the cost function to be minimized. We decided to use the function (6.41), which is a weighted sum of squares of the capacitor-voltage errors (6.38), the common-mode voltages (6.33), and their derivatives (6.39) and (6.40). Additionally, the Jacobian matrix of the cost-elements function is calculated here also (see Appendix A).

The fourth and last step concerns the cost-function minimization to find the optimal common-mode voltage. In an iterative search, we successively adapt the common-mode voltage sequence to subsequently reduce the cost. In case of our gradient-search method, this is governed by (6.43) and (6.44). Each iteration, the inverter model and the cost function are re-evaluated to verify and improve the search. The search is terminated when the minimum is

found within a certain tolerance, or when a maximum number of iterations is attained. This last criterion is of utmost importance in a real-time application, because it ensures a maximal calculation time that has to remain smaller than the sampling time $T_S$. Once an optimal (or sub-optimal) common-mode voltage sequence is found, its first element, corresponding to the actual time, is applied to the system.

In order to obtain a good solution, avoiding local minima, and to find it in few iterations, it is very useful to have a good initial guess (see Chapter 6). We focus on imposing a 3rd and a 9th harmonic[3] as initial solution. Due to the integrations in our system (6.16) and (6.17), the capacitor-voltage oscillations will increase with decreasing frequency of its current oscillations. A minimal oscillation frequency must thus be ensured in order to limit the amplitudes (at a given output current). This can be obtained by imposing a dominant frequency in the capacitor currents (6.18) and (6.19) via the common-mode voltage. It turns out that a 3rd harmonic alone is sufficient in the higher output-frequency range ($f/f_N > 0.6 \ldots 0.8$), whereas an additional 9th is needed in the lower range. To prevent this 9th harmonic becoming too slow for very-low output frequencies down to zero, we will use a fix (asynchronous) frequency instead. A value of twice the nominal output frequency ($f_f = 2f_N$) works fine. Writing the differential-mode voltage as a complex number according to (4.1), our initial guess for the common-mode voltage $\hat{u}_{cm}$ can be expressed as:

$$\hat{u}_{cm} = \mathrm{Re}\left\{\underline{u}_{cm,3}(m)\underline{e}_{u,3} + \underline{u}_{cm,9}(m)\underline{e}_{u,9}\right\}, \tag{7.27}$$

$$\text{with } \underline{e}_u = \frac{\underline{u}_{dm}}{|\underline{u}_{dm}|}, \quad \underline{e}_{u,3} = \underline{e}_u^3, \quad \underline{e}_{u,9} = \begin{cases} \underline{e}_u^9 & 9f \geq f_f, \\ e^{j2\pi f_f t} & 9f < f_f. \end{cases}$$

Here, $\underline{u}_{cm,3}(m)$ and $\underline{u}_{cm,9}(m)$ are the coefficients containing the amplitudes and phases of its 3rd and 9th harmonic respectively. They depend on the modulation index $m$—which, in turn, is about proportional to the output frequency $f$—and have been experimentally determined (see the next sections). It could be of advantage to investigate their dependency on the load-current power factor $\cos\varphi$ as well, but this is omitted in this dissertation. In addition to this initial guess (7.27), the previous optimal solution is taken into account.

## 7.2 Simulation Model

For the development of the control methods and strategies needed to operate our hybrid inverter, extensive use of computer calculations and simulations

[3]Harmonics are always referred to the actual fundamental period, which depends on the output frequency.

has been employed. This section describes its implementation together with some obtained results.

All simulation and measurement results are presented in p.u. referred to the motor. Base values are phase-voltage amplitude, phase-current amplitude and stator angular frequency. With a nominal modulation index of 0.82, nominal main- and sub-inverter capacitor voltages are 0.92 and 0.31 respectively. Capacitor-voltage variations are expressed in percentage of the inverter step, which is the voltage between two adjacent output-voltage levels. The inverter step equals the capacitor voltage of the smallest cells [9].

### 7.2.1 Implementation

The choice of an appropriate simulation tool and the modeling details should be adapted to the problem being investigated. Our system is a combination of electrical circuits and controls, and contains discrete- and continuous-time parts. Since we focus on control development, no sophisticated semiconductor models are needed. The combination of MATLAB/Simulink [66] for control and PLECS [67] for the electric circuit is well-suited for our requirements. Moreover, the extensive set of available application-specific toolboxes facilitates the implementation and use of specialized functions.

The inverter, the motor and the proposed control method are implemented on these tools. The power supply to the intermediate circuit consists of an ideal voltage source, since we are not interested in the detailed behavior of the net, transformer and diode rectifier for the control development. Ideal switches are employed to model the inverter.

To dispose of sufficient controller dynamics, we sample it twice per switching period, corresponding to a sampling ratio

$$\boxed{N_S = 1} \tag{7.28}$$

in (7.26). Resulting from our choice for the switching frequency (7.7), the sampling time is thus

$$\boxed{T_S = 0.5 \text{ ms},} \tag{7.29}$$

corresponding to a sampling frequency $f_S = 2$ kHz.

For maximal control opportunities, the optimization horizon $N_O$ is chosen equal to the control (prediction) horizon $N$:

$$\boxed{N_O = N} \tag{7.30}$$

(see Chapter 6). Good control performance is obtained if the control horizon covers half a nominal fundamental period. For a nominal output frequency

$$\boxed{f_N = 50 \text{ Hz},} \tag{7.31}$$

this corresponds to

$$\boxed{NT_S = \frac{0.5}{f_N} = 10 \text{ ms},} \tag{7.32}$$

and leads to a control horizon of

$$\boxed{N = 20} \tag{7.33}$$

samples.

The weighting factors in the cost function (6.41) have been experimentally determined. The aim is to obtain acceptable capacitor-voltage oscillations with a rather small and smooth common-mode voltage—fairly subjective criteria. The following values were judged to give acceptable results:

$$\boxed{\begin{aligned} c_{u_{cm}} &= 0.33, \\ c_{\delta u_{cm}} &= \frac{15 \cdot 10^{-3}}{f_N}, \\ c_{\delta^2 u_{cm}} &= \frac{670 \cdot 10^{-6}}{f_N^2}. \end{aligned}} \tag{7.34}$$

These values are expressed in terms of the nominal frequency to permit scaling.

The cost-function minimization—a function of 20 variables—is performed by the non-linear least-squares optimization function of the Matlab Optimization Toolbox [64]. It works well for the solution of our problem, even in case of a poor initial guess. This is an important property to enable control development.

For the initial guess of the common-mode voltage (7.27), the coefficients have been determined by trial and error, based on insights in the system behavior gained from its modeling (see Chapter 5). This is a time-consuming procedure, especially in simulations. Due to the robustness of the employed optimization algorithm, we content ourselves with a coarse estimate, which is shown in Figure 7.7.

### 7.2.2 Results

The simulations permitted to highlight the performance of the algorithm over the whole speed and load range, as well in steady-state as during transients. The example of Figure 7.8 illustrates the good stabilization of all the capacitor voltages at two operating points. Initially the motor is running at no load, at $t = 4\pi$ its shaft is loaded with nominal torque. Due to the motor inertia and lacking its speed control, the current transient stretches over several periods.

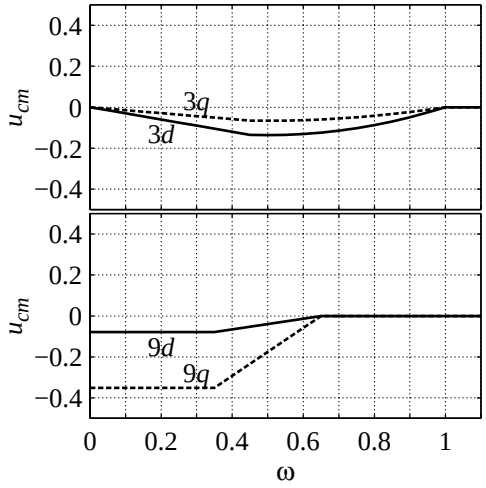



Figure 7.7: Coefficients of the 3rd and 9th harmonic for the initial guess of the common-mode voltage (7.27), as used in the simulation model. Real ($d$) and imaginary ($q$) parts of $\underline{u}_{cm,3}$ and $\underline{u}_{cm,9}$ as a function of the output frequency.

At nominal speed, the common-mode voltage is very small and essentially composed of a 3rd harmonic. At half speed, the significant common-mode components are a 3rd and 9th harmonic. Their amplitudes are acceptable for standard motors. In the no-load cases, the intermediate-circuit capacitor voltages vary only a few percent. In the full-load case, they oscillate within about 5% in steady state, and a few percent more during the transient when the current is bigger than nominal.

A fast motor start-up from standstill up to nominal speed (in less than 0.5 s) has also been successfully simulated, which demonstrates the control performance over the whole speed range in transient operation.

## 7.3 Laboratory Prototype

For the development of the control methods and strategies needed to operate our hybrid inverter, extensive use of computer calculations and simulations has been employed. In order to validate the obtained results, a low-voltage laboratory prototype of the hybrid-inverter drive system has been built and tested. Its realization required adaptations in the controller design, which we will comment in this section. The prototype has been subjected to extensive

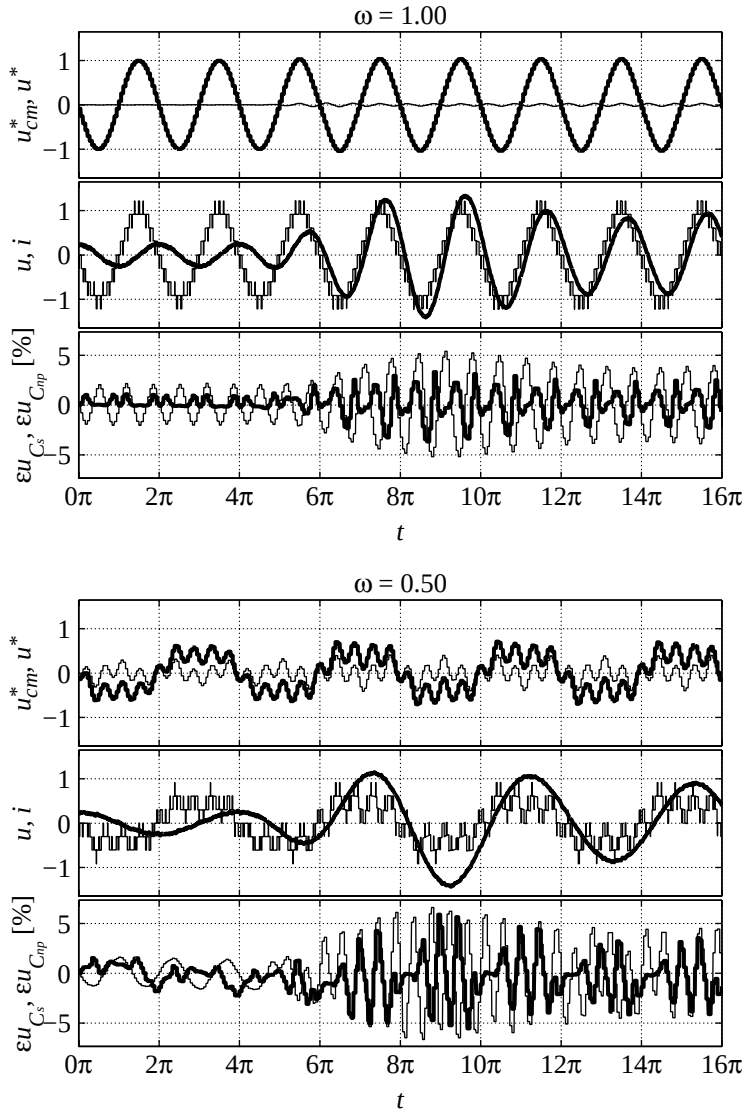



Figure 7.8: Simulation of the hybrid inverter driving an asynchronous motor: nominal-torque load step at nominal and at half speed. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

tests, whose results will be presented and discussed.

All simulation and measurement results are presented in p.u. referred to the motor. Base values are phase-voltage amplitude, phase-current amplitude and stator angular frequency. With a nominal modulation index of 0.82, nominal main- and sub-inverter capacitor voltages are 0.92 and 0.31 respectively. Capacitor-voltage variations are expressed in percentage of the inverter step, which is the voltage between two adjacent output-voltage levels. The inverter step equals the capacitor voltage of the smallest cells [9].

### 7.3.1 Implementation

The design of the laboratory prototype is adapted to an available low-voltage motor, preferably coupled to a controllable load. For our purpose, a present motor/generator set consisting of a standard asynchronous squirrel-cage motor coupled to a direct-current generator suits perfectly. The nominal data of the asynchronous motor are given in Table 7.1.

Figure 7.9 shows the laboratory prototype of the hybrid-inverter drive system as it has been realized. The whole inverter, including rectifiers, circuit breakers, pre-charge resistors, measurements and control, fits in a standard electronics rack. This rack is placed between the transformer and the motor/generator set. The transformer is fed from the 400 V/50 Hz utility grid, whereas standard laboratory power supplies are employed for the measurements and control. The direct-current generator is controlled by means of an industrial power converter (not shown).

Throughout the inverter, power modules equipped with suitable IGBT and diodes from the SEMITOP series of Semikron [68] are used. These modules are intended for mounting on printed circuit boards, and enable the realization of highly integrated inverter modules. These are well-suited for the investigation of various multi-level inverter topologies.

Table 7.1: Nominal data of the asynchronous motor.

| Parameter | Value |
|---|---|
| $U_N$ | 400 V |
| $I_N$ | 4.9 A |
| $f_N$ | 50 Hz |
| $\cos\varphi_N$ | 0.84 |
| $S_N$ | 3.4 kVA |
| $p$ | 2 |
| $n_N$ | 1425 rpm |
| $P_N$ | 2.2 kW |

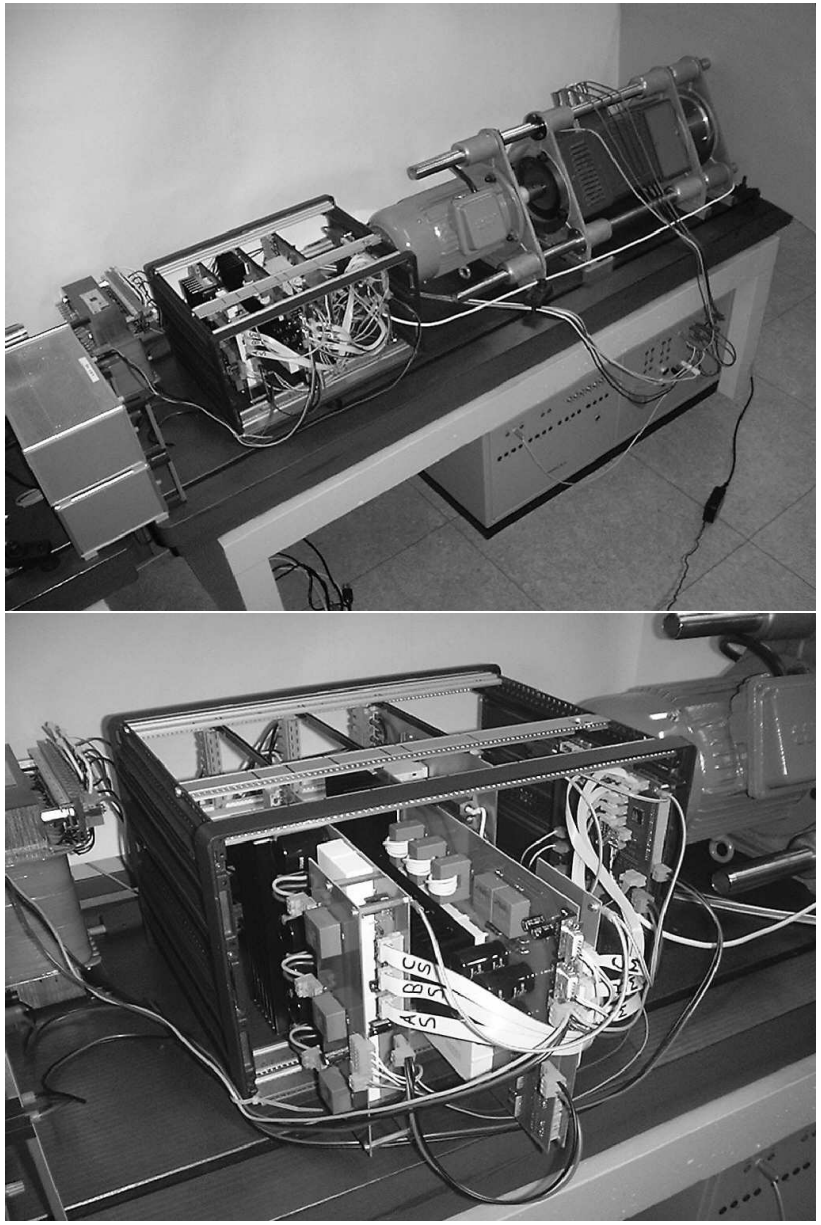


Figure 7.9: Laboratory prototype of the hybrid-inverter drive system.

The control algorithms are implemented on a SHARC DSP of Analog Devices, running at 32 MHz [69, 70]. This DSP is embedded in a hardware environment containing fast data-acquisition channels (A/D converters) and programmable logic (FPGA circuit) on a single card. A software environment is available for easy implementation of control functions, and for system management from a personal computer. An additional interface card is used to redirect the multitude of command signals to their respective gate drivers, and to collect and shape the measurement signals.

The modulator is implemented in the FPGA circuit, all other control functions run on the DSP and are programmed in C [71–73]. Because the required calculation effort is huge, highly optimized program code is indispensable. The programming style is adapted to the compiler, in order to obtain an efficient executable program. This is achieved by verifying the generated assembly-language code.

In order to have more calculation time available, the controller is sampled only once per switching period. This corresponds to a sampling ratio

$$\boxed{N_S = 2} \tag{7.35}$$

in (7.26). Resulting from our choice for the switching frequency (7.7), the sampling time is thus

$$\boxed{T_S = 1 \text{ ms},} \tag{7.36}$$

corresponding to a sampling frequency $f_S = 1$ kHz. By increasing the sampling time, we additionally benefit from a reduction of the optimization-problem size, because the same time interval is covered by a smaller number of samples in (7.32) or (7.37).

Because of remaining processor limitations, the control (prediction) and optimization horizons have been slightly reduced. They cover 0.4 and 0.25 nominal fundamental periods respectively:

$$\boxed{\begin{aligned} NT_S &= \frac{0.4}{f_N} = 8 \text{ ms}, & N &= 8, \\ N_O T_S &= \frac{0.25}{f_N} = 5 \text{ ms}, & N_O &= 5. \end{aligned}} \tag{7.37}$$

These values still lead to satisfactory performance.

Again for reasons of processor capabilities, the cost function does not yet incorporate the common-mode voltage derivatives (6.39) and (6.40). Although this can lead to a quickly varying and not very smooth common-mode voltage, it does not affect system stability. These terms incorporate aspects of output quality, and their absence can be tolerated in our laboratory prototype.

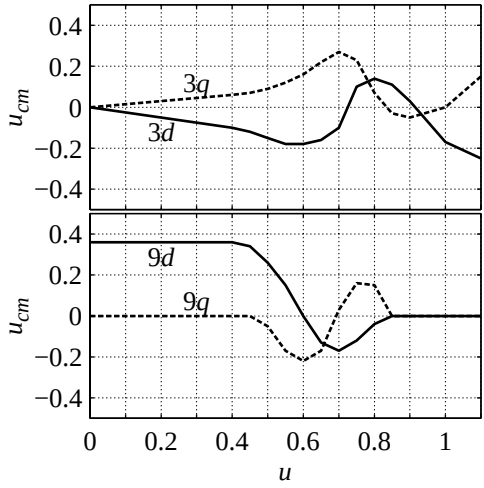



Figure 7.10: Coefficients of the 3rd and 9th harmonic for the initial guess of the common-mode voltage (7.27), as used in the laboratory prototype. Real ($d$) and imaginary ($q$) parts of $\underline{u}_{cm,3}$ and $\underline{u}_{cm,9}$ as a function of the output voltage.

The remaining weighting factor in the cost function (6.41) has been slightly reduced, which seems to give better results:

$$\boxed{c_{u_{cm}} = 0.2.} \tag{7.38}$$

The cost-function minimization—a function of 5 variables—is performed by our simple gradient-search method (6.43) and (6.44), which is sufficient in case of a good initial guess.

During the simulations, coarse estimates for the initial guess of the common-mode voltage (7.27) have been established (see Figure 7.7). Based on these experiences, the coefficients have been improved on the laboratory prototype—still by a time-consuming trial-and-error procedure. The result is shown in Figure 7.10. It must be stated however, that these are not final results. The curves have been determined as a function of the output voltage instead of the modulation index, which leads to some dependency on the supply voltage. Their dependency on the load-current power factor $\cos\varphi$ has not been determined. The curves present a compromise suitable for a broad range of load states. Other curves are possible as well, merely resulting in somewhat different capacitor- and common-mode-voltage oscillations.

### 7.3.2 Results

The prototype demonstrates the excellent performances of the stabilization algorithm over the whole speed range, as well in steady-state as during transients. In spite of the performance reductions, the system is still stable and the results show good agreement with the simulations. Motor start-up from standstill up to nominal speed, speed reversal, and sudden load changes are handled without problems.

Measurements of a load step at different speeds covering the whole operating range are presented in Figure 7.11, 7.12, 7.13, 7.14, 7.15 and 7.16. In each measurement, the motor is initially running without a load torque applied to its shaft. About in the middle of the measurement, the shaft is loaded with nominal torque by the direct-current generator. Due to the motor inertia and lacking its speed control, the current transient stretches over several periods.

The common-mode voltage is mainly as imposed by the initial guess—determined by (7.27) and Figure 7.10—, and hardly varies with the load state. At low speeds, it is mainly composed of the $9^{\text{th}}$ harmonic, respectively the fixed frequency, with a slight $3^{\text{rd}}$ harmonic. At medium speeds, we have a decreasing $9^{\text{th}}$ and an increasing $3^{\text{rd}}$ becoming the dominant component. Around nominal speed, the $3^{\text{rd}}$ harmonic is essentially the only component, but with rather small amplitudes.

At no load, the intermediate-circuit capacitor voltages vary only a few percent, with maxima up to 5% at certain speeds. At full load, they oscillate within 5 to 10%, with the maxima occurring during the transient when the current is bigger than nominal. It can be clearly seen that the oscillations decrease with increasing frequencies in the common-mode voltage. The disappearance of the $9^{\text{th}}$ harmonic around $\omega \approx 0.8$, therefore, leads to a significant increase in the capacitor-voltage oscillations—most strikingly in those of the neutral point.

The motor parameters in the simulation are typical values, which have not been adjusted to correspond to the utilized motor. In spite of this and the control modifications and performance reductions, the measurement results show good agreement with the simulations. The same operating points as in Figure 7.8 can be found in 7.13 and 7.15. The more striking common-mode voltage at nominal speed is due to the different initial guess for the optimization (see also Figure 7.7 and 7.10). Due to friction and the integrated cooling fan, the motor is not really running at no load, which explains its bigger current and the resulting bigger capacitor-voltage oscillations in these areas.

Figure 7.17 shows the current and voltage waveforms measured with an oscilloscope for a selection of speeds. The low distortion in the current waveform at a modulation frequency of only 1 kHz is due to the employment of a

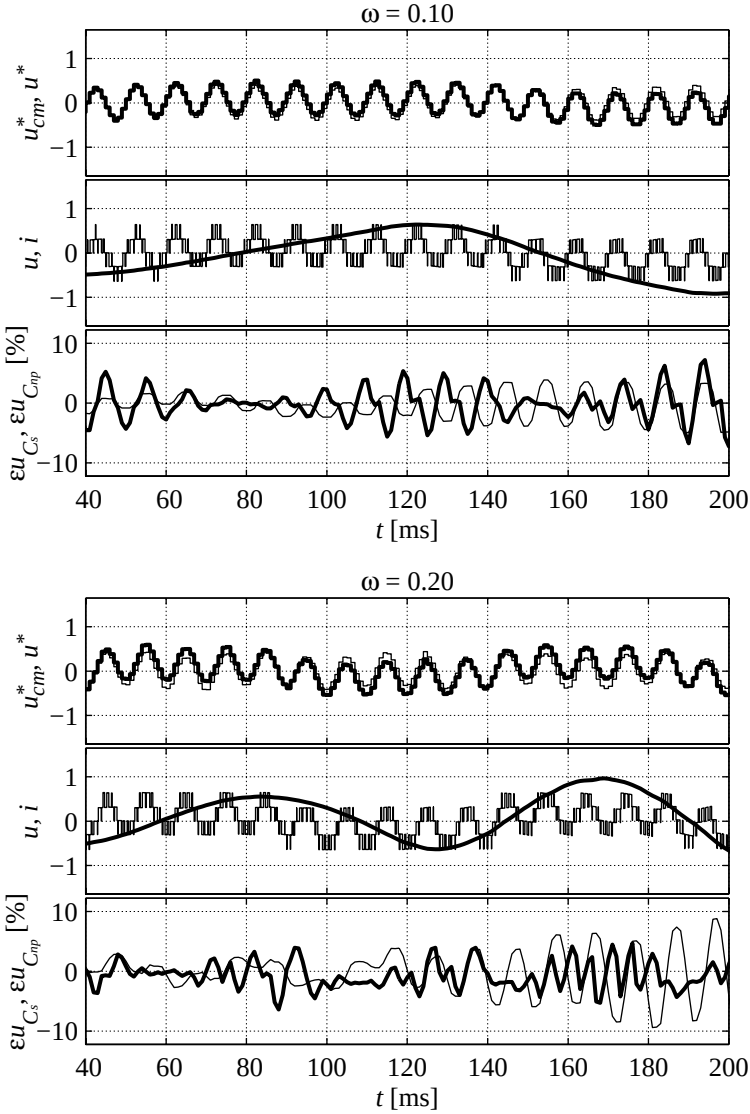



Figure 7.11: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 0.1$ and $\omega = 0.2$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

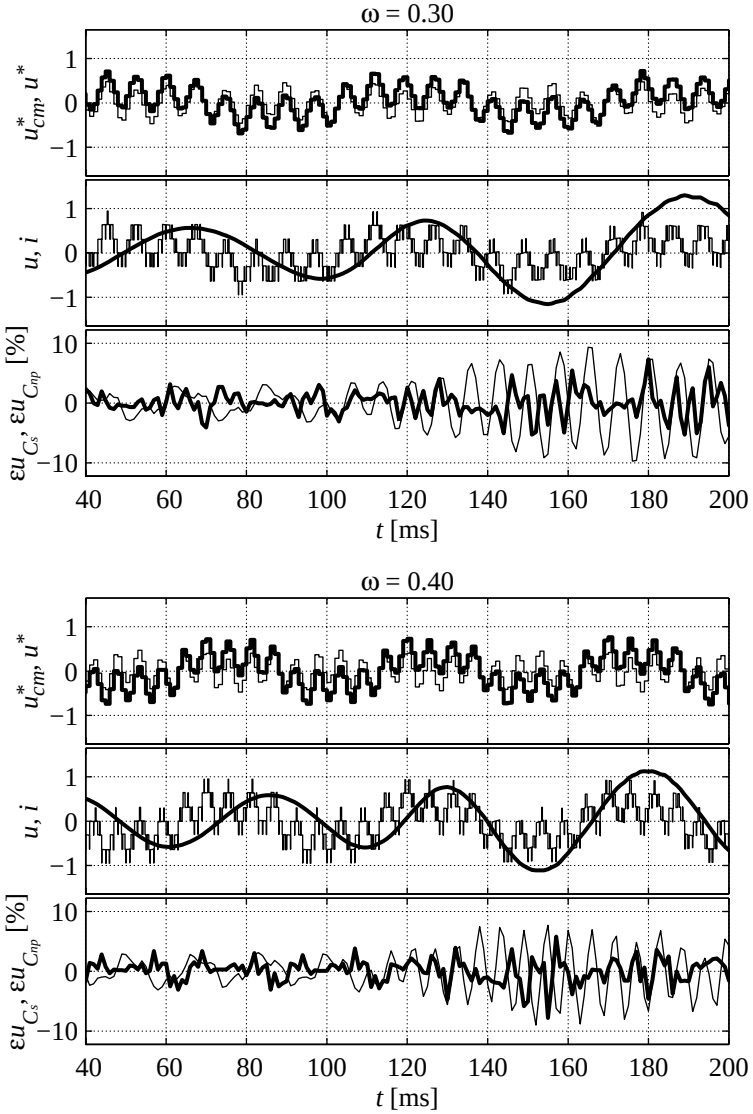



Figure 7.12: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 0.3$ and $\omega = 0.4$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

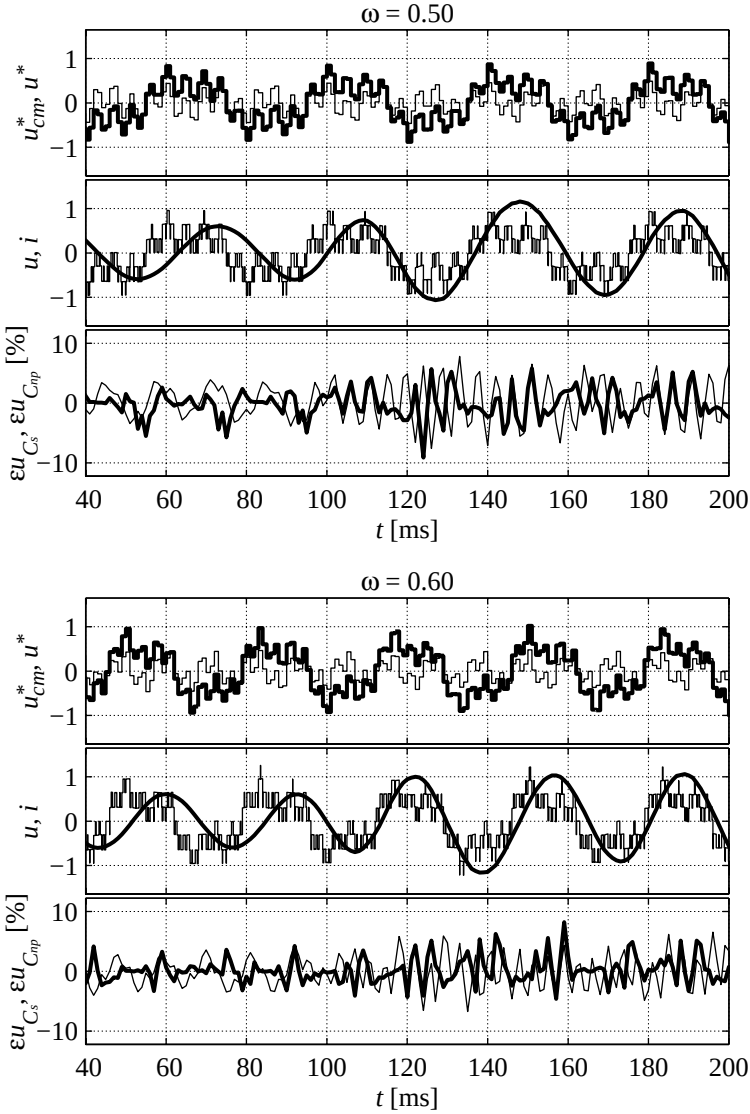



Figure 7.13: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 0.5$ and $\omega = 0.6$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

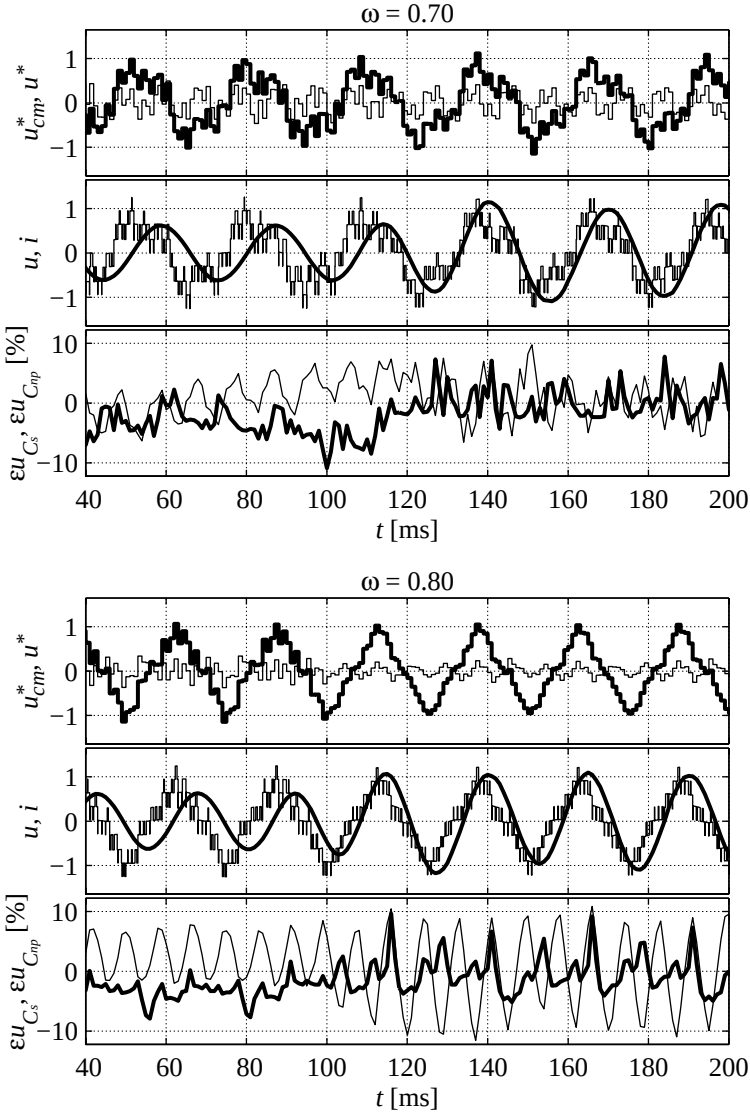



Figure 7.14: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 0.7$ and $\omega = 0.8$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

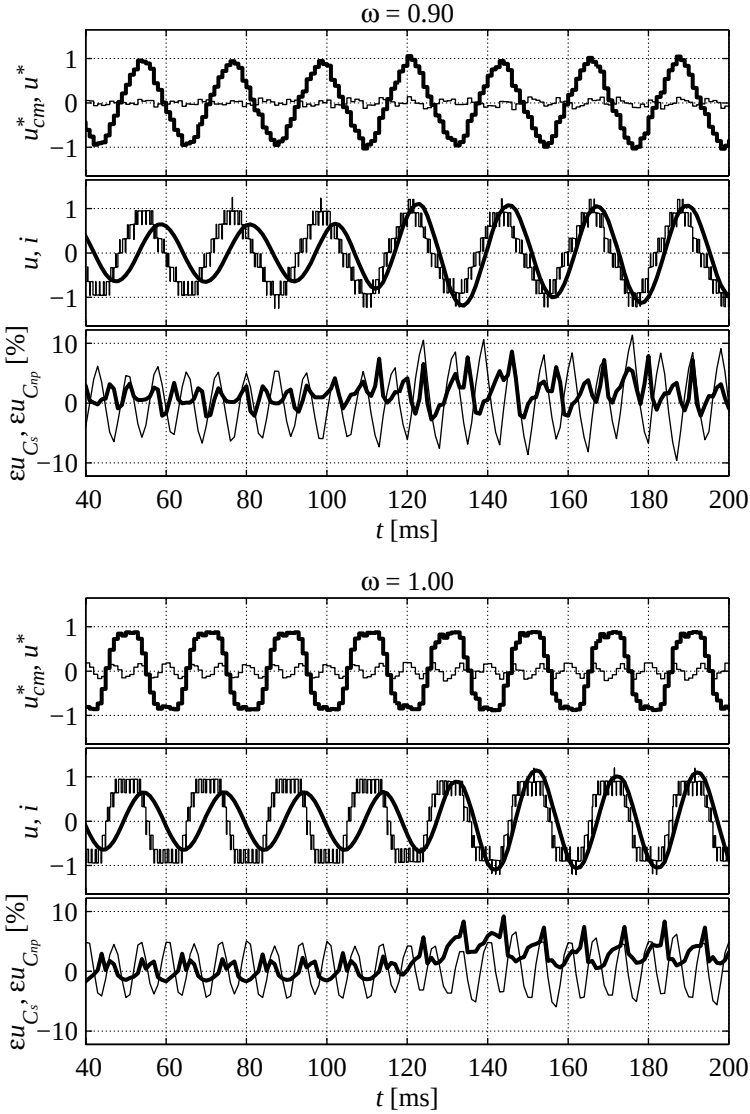



Figure 7.15: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 0.9$ and $\omega = 1.0$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

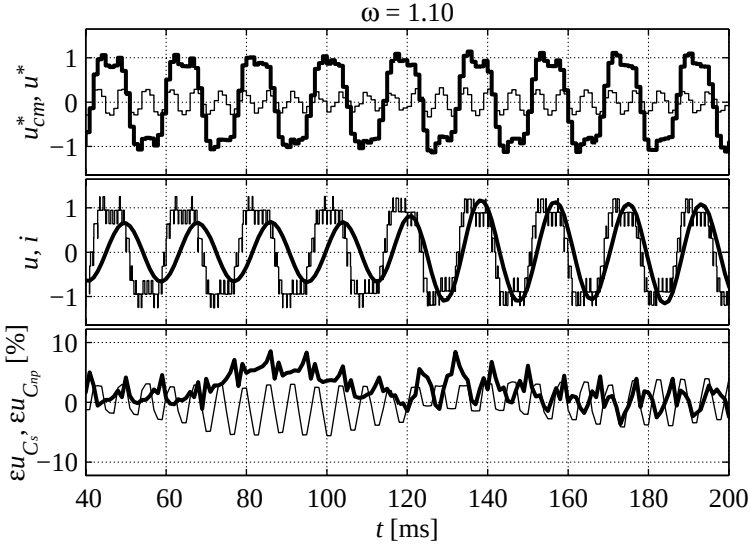



Figure 7.16: Measurement of the hybrid inverter driving an asynchronous motor: nominal-torque load step at $\omega = 1.1$. Common-mode and output-voltage reference signals $u^*_{cm}$, $u^*$, output voltage $u$ and current $i$, and sub-inverter and neutral-point capacitor voltage errors $\varepsilon u_{C_s}$, $\varepsilon u_{C_{np}}$.

nine-level inverter. We verify that the majority of the switching in the output voltage is supported by the sub inverter, whereas the main inverter clearly switches less often. Although the main inverter has to switch rapidly in repeating bursts, especially at lower speeds, its average device switching frequency never exceeds a quarter of the modulation frequency. We verify as well that the main inverter principally supplies active power, whereas the sub inverter only supplies reactive power.

Finally, we note that voltage spikes may occur in the output voltage when the main and the sub inverter switch together. This due to unequal delays in the actual commutation, resulting mainly from the dead time in the complementary-switch commands to prevent short circuit (1 $\mu$s in the laboratory prototype). This phenomenon will be enhanced by the employment of different devices with diverging switching characteristics. These spikes can be suppressed by an improved timing of the switching commands, or by the addition of a small output filter.

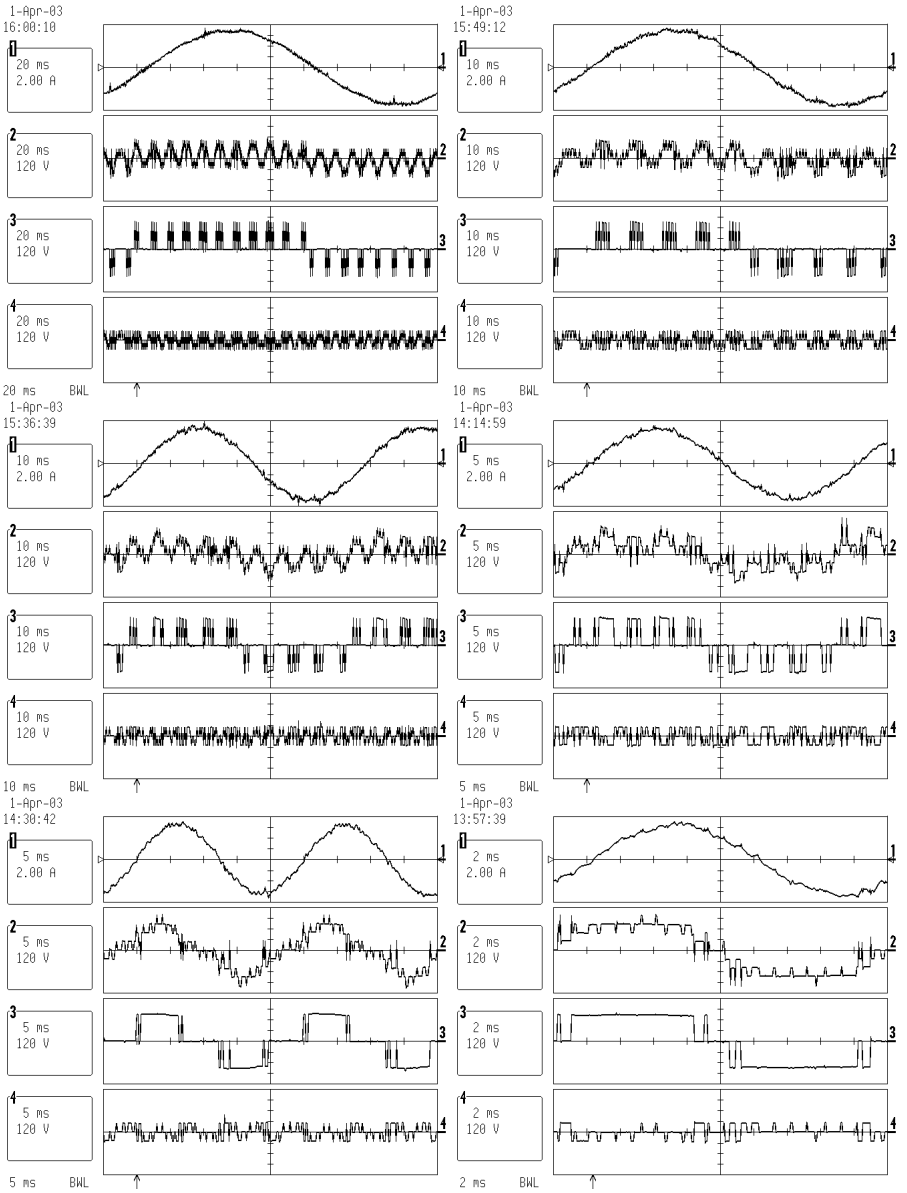



Figure 7.17: Measured current and total, main and sub phase voltages of the experimental hybrid inverter driving an asynchronous motor at nominal load, at $\omega = 0.1$, 0.2, 0.3, 0.5, 0.8 and 1.0.

# Chapter 8

# Pre-Charge Method

As we have seen in Chapter 2, pre-charging of the sub inverters upon converter start-up can not be accomplished in a classical manner. For reasons of cost and reliability, it is, however, desirable to avoid additional equipment and to dispose of an other method to perform this task.

In this chapter, we will propose a special pre-charge method for our hybrid inverter. The main inverter (NPC topology) is pre-charged in a usual way via a set of pre-charge resistors along with a bypass contactor, either on the AC or the DC side of the transformer and rectifiers. The sub-inverter intermediate-circuit capacitors are charged in parallel to and together with those of the main inverter, by exploiting certain inverter switching configurations. Measurements show its successful application in the proposed drive system.

## 8.1 Principle

Some of the switching states of our hybrid inverter lead to a power flow from the main to the sub inverters (see also Chapter 6). This occurs for states where the cell voltages in a phase are opposite [16], as is the case for output levels $-2$ and $+2$ in Figure 2.6(b). We will exploit this phenomenon, which depends only on the switching states and not on the actual voltages, for our pre-charge method. We will refer to these states as $-2$ and $+2$ in the following.

Since energy transfer can only happen in the presence of a voltage difference together with a current flow, this pre-charge method requires that current can flow in the phases. Consequently, some kind of (low impedance) load must be present. The motor to be driven can serve for this purpose very well. Pre-charging typically lasts several seconds, and the charging current is

Table 8.1: The pre-charge switching states used for our hybrid inverter.

| state number | switching vector $\vec{s}$ | switching states | | | | | |
|---|---|---|---|---|---|---|---|
| | | phase $a$ | | phase $b$ | | phase $c$ | |
| | | $s_{m,a}$ | $s_{s,a}$ | $s_{m,b}$ | $s_{s,b}$ | $s_{m,c}$ | $s_{s,c}$ |
| 0 | $(-2,-2,-2)$ | $-1$ | $+1$ | $-1$ | $+1$ | $-1$ | $+1$ |
| 1 | $(+2,-2,-2)$ | $+1$ | $-1$ | $-1$ | $+1$ | $-1$ | $+1$ |
| 2 | $(+2,+2,-2)$ | $+1$ | $-1$ | $+1$ | $-1$ | $-1$ | $+1$ |
| 3 | $(-2,+2,-2)$ | $-1$ | $+1$ | $+1$ | $-1$ | $-1$ | $+1$ |
| 4 | $(-2,+2,+2)$ | $-1$ | $+1$ | $+1$ | $-1$ | $+1$ | $-1$ |
| 5 | $(-2,-2,+2)$ | $-1$ | $+1$ | $-1$ | $+1$ | $+1$ | $-1$ |
| 6 | $(+2,-2,+2)$ | $+1$ | $-1$ | $-1$ | $+1$ | $+1$ | $-1$ |
| 7 | $(+2,+2,+2)$ | $+1$ | $-1$ | $+1$ | $-1$ | $+1$ | $-1$ |

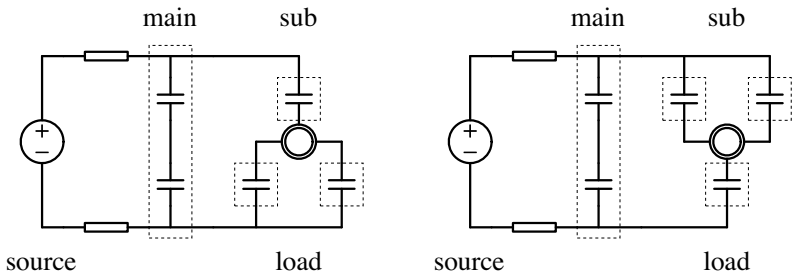



Figure 8.1: Switching configurations of the hybrid inverter pre-charge method.

correspondingly small. This current will not produce any significant torque in the motor.

As described above, two switching states exist for each phase that permit energy transfer to the sub inverter. Since they can be combined independently, there are $2^3 = 8$ converter states available, as illustrated in Table 8.1. However, if we choose the same state for all three phases (either $-2$ or $+2$, corresponding to states number 0 and 7), we have a converter common-mode state and no charging current can flow to the sub inverters. There remain six converter switching states to charge the sub inverters (states number 1 to 6). They belong to two basic configurations, which are shown in Figure 8.1. Each of them has three equivalents by exchanging phases.

For the purpose of pre-charging, other converter switching states are possible as well. E.g., those where only one or two phases are in charging configuration, and the others in some other state. We will not consider those states for our pre-charge method in the following.

With the small charging current, the motor impedance is almost negligible, and we practically have a parallel connection of the sub- and main-inverter capacitors. Consequently, they will be charged together. However, the three sub-inverter capacitors will not charge at the same rate, since two of them share the charge current whereas the third one takes the total. In order to obtain equal average charging of all sub inverters, we will alternate the six available configurations in sequence. Each configuration leads to momentary voltage differences, which, upon configuration change, will be equalized over the motor. This effect remains small by alternating the states rapidly.

## 8.2 Implementation and Results

Pre-charging of the hybrid inverter based on the described method has been implemented on the laboratory prototype (see Chapter 7). Pre-charge resistors and bypass contactor are placed on the primary side of the feeding transformer. The controller—a subsystem of the drive controller in Figure 7.3—is shown in Figure 8.2. The complete pre-charge sequence will be explained with the aid of Figure 8.3, showing[1] a measurement of an inverter and motor start-up.

Initially, all capacitor voltages equal zero. Upon closing the main circuit breaker (at $t \approx 0.5$ s), pre-charging of the main-inverter capacitors over the pre-charge resistors starts. At the same time, inverter switching as described in the previous section is executed, in order to obtain parallel charging of the sub inverters. The states are changed every 10 ms, which gives a repetition

[1] All simulation and measurement results are presented in p.u. referred to the motor. Base values are phase-voltage amplitude, phase-current amplitude and stator angular frequency. With a nominal modulation index of 0.82, nominal main- and sub-inverter capacitor voltages are 0.92 and 0.31 respectively.

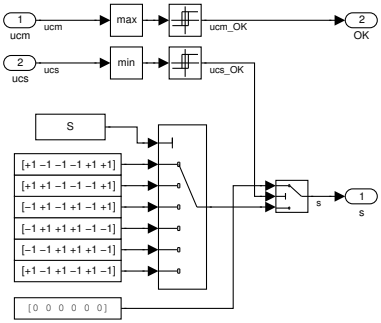



Figure 8.2: Block diagram of the pre-charge controller.

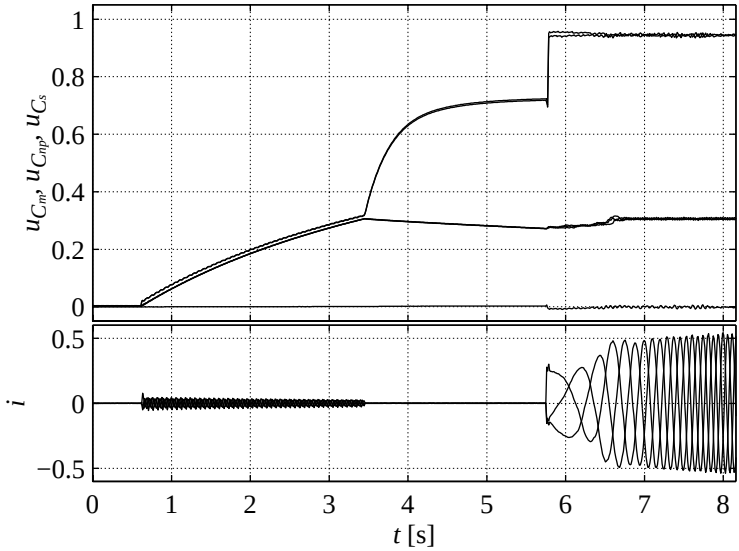



Figure 8.3: Measurement of the hybrid inverter pre-charge method. Voltages of each individual intermediate-circuit capacitor (two $u_{C_m}$, three $u_{C_s}$) and the neutral-point ($u_{C_{np}}$), together with the output currents $i$.

period of 60 ms (16.7 Hz) for all six states. As can be seen in Figure 8.3, the sub-inverter capacitors have a slightly lower voltage than those of the main inverter, due to a small voltage drop over the motor. Motor currents are about 5%. With a stator frequency of 16.7 Hz at standstill, the motor operates about in short circuit and produces negligible torque.

Once the sub-inverter capacitors reach their nominal voltage (at $t \approx 3.5$ s in Figure 8.3), which is only one third of that for the main inverter, inverter switching is stopped and the sub-inverter capacitors are kept isolated from the rest of the circuit. Charging of the main-inverter capacitors continues—much faster due to the much smaller remaining capacitance. Since the pre-charge resistors are placed on the primary side, the transformer magnetizing current causes a voltage drop which prevents the capacitor voltages reaching their nominal value. Upon closing the bypass contactor (at $t \approx 5.8$ s), the capacitors very rapidly reach their nominal voltage. At this moment, normal inverter and motor control is enabled and the motor starts running.

In the meanwhile, the sub-inverter capacitors have slowly been discharging, due to parallel discharge resistors (see also Chapter 6 and 7). These resistors, assuring capacitor discharging upon converter shut-down, normally

have a high impedance to prevent excessive losses, and a corresponding big discharge time constant (6.21) in the order of several tens to hundreds of seconds. Consequently, sub-inverter capacitor discharging remains rather small, as can be verified in Figure 8.3. As soon as the motor starts running, the voltage stabilization algorithm described Chapter 6 and 7 rapidly brings the voltages back to their nominal values. If desired, charging to a voltage somewhat higher than nominal could be performed in the first phase of the pre-charge sequence, in order to obtain voltages closer to nominal at the end of the sequence.

# Chapter 9

# Conclusion

Hybrid asymmetric multi-level inverters promise significant improvements for medium-voltage applications, both on the load and the line side. Asymmetric converters benefit from a larger number of output-voltage levels at reduced component count, which enables to increase both output quality and reliability. A hybrid converter exploits the individual advantages and strengths of different semiconductor devices for the different functions in the power conversion.

## 9.1 Topology

This dissertation investigates such a hybrid inverter. To simplify the topology furthermore, some inverter parts are deprived of their feeding from the net. They can only supply reactive power, but do provide for high output quality. The resulting topology is a very interesting solution in terms of power quality, efficiency, reliability and cost.

However, ensuring zero active power for the non-supplied cells is not an easy task. The intermediate-circuit capacitor voltages are inherently unstable and require a suitable control method for converter operation, preferably without influence on the load. In general, this can not be done instantaneously by lack of an equilibrium state, but only on an average in time. Apart from normal operation, also converter start-up is an issue to consider, for which it is desirable to limit additional equipment.

## 9.2 Obtained Results

In this dissertation, we investigate the behaviour of this new inverter, and develop methods to obtain its reliable operation for the considered applications. These methods include modulation, voltage stabilization and start-up. We establish suitable models for their foundation.

To generate the desired output voltages with our multi-level inverter, we employ a variant of the widely used and well-known pulse-width modulation (PWM) methods that is optimal in the produced harmonic content. Our modulator compensates for varying output-voltage levels, and is efficiently implemented and rapidly executed on a digital signal processor (DSP) and programmable logic (FPGA).

A coordinate transform facilitates the analysis of three-phase systems. A uniform transform from the phase quantities to their common and differential modes conserves the shape of transformed objects. This enables to visualize and better understand certain aspects of such systems, including the well-known space-vector hexagon of inverter states and the possible or even required inverter common-mode voltages. This approach is very useful to analyze the influence of the common-mode voltage on the intermediate-circuit capacitors in any multi-level voltage-source inverter.

Switches link the DC to the AC side in our hybrid inverter, and their states determine the relations between currents and voltages on both sides. Other components in our circuit—resistors, capacitors, a motor, et cetera—relate the currents to the voltages at their respective location. Mathematical models describe these relations, either exact or averaged under PWM control. Especially the influence of the common-mode voltage on the intermediate-circuit capacitors is of our interest, for the purpose of their voltage stabilization.

The non-supplied intermediate-circuit capacitor voltages in our hybrid inverter can be stabilized by an appropriate common-mode voltage. This method does not deteriorate the differential mode and remains without influence on the load. It allows the capacitor-voltage stabilization on an average in time, over almost the whole amplitude, frequency and load range. The only exception is the (avoidable) area of very high modulation indices combined with high power factors.

The properties of the proposed stabilization method are very challenging for active closed-loop control. We need to control a multitude—four in our hybrid inverter—of capacitor voltages with the aid of only one control variable. Although well known, the system is highly non-linear, time varying and operating-point dependent. Additionally, we want to impose constraints on the common-mode voltage to avoid negative side effects.

Model-predictive control (MPC) is a strategy that can deal with the men-

tioned properties and requirements. It predicts the system evolution as a function of the control inputs. A cost function of system and control quantities is iteratively minimized in real time, to find the optimal control input to apply to the system. System model accuracy, problem formulation and size, optimization strategy and efficiency, along with available calculation performance and time are critical aspects of such a controller.

The described method, which is new to power electronics, is applied to our hybrid asymmetric nine-level inverter, driving an asynchronous motor. The design of such a system leads to reasonable component and parameter values. Lacking sufficient theory, however, many parameters have empirical values.

Vast computer simulations enable the development of control methods and strategies for the operation of our hybrid inverter. Full problem formulation and generous parameters assure sufficient control dynamics and opportunities. Together with a sophisticated optimization method, the desired performance is obtained. The results demonstrate stable behaviour in steady-state and during transients over the whole operating range.

The realization of a laboratory prototype requires adaptations to the controller design. The huge calculation effort and processor limitations necessitate problem size reduction and controller execution-rate decrease, resulting in a slight quality loss. Despite the performance reductions, the system remains stable and the results show good agreement with the simulations. Motor start-up from standstill up to nominal speed, speed reversal, and sudden load changes are handled without problems. Instantaneous response of a real-time system enables improved parameter determination.

Upon converter start-up, the non-supplied intermediate-circuit capacitors can be charged in parallel with the supplied ones, avoiding additional equipment. This is achieved by exploiting certain switching configurations. The necessary current can flow via the drive's motor, without producing any significant torque in it. Measurements show its successful application in the investigated drive system.

## 9.3 Recommendations

Although the developed methods show stable and reliable operation of our hybrid asymmetric multi-level inverter, several issues request further investigation. On the one hand, the design of the methods proposed in this work is to a broad extend empirically based. A more sound theoretical foundation could lead to better performance or to reduced processor requirements. On the other hand, additional items need to be addressed for a successful implementation as a commercial product. Finally, the proposed methods are not limited to

the investigated topology, but can be more widely applied.

System stability is only experimentally verified. Operating-range limitations should be theoretically analyzed to dispose of clear limits. Thorough investigation of the system response to transients should enable the detection of possibly critical domains.

The actual load model bases on rather rudimentary assumptions for its state prediction. The requirements on the prediction accuracy should be investigated and the need for better models analyzed.

A large variety of common-mode-voltage waveforms can stabilize the intermediate-circuit capacitor voltages. The applied one depends largely on the form of the cost function and the imposed constraints, which define performance optimality. They are subjective and empirical in their present form. All possible stable solutions should be investigated, and the optimal one selected based on objective criteria. This (operating point dependent) target solution will enable the choice of proper terms and their weighting factors in the cost function and of possible hard constraints.

The initial guess for the problem optimization must be close to the final solution to minimize the required iterations. A value equal to a pre-defined target solution, probably depending on the modulation index and the power factor, is expected to satisfy the needs. This guess can be improved by taking the previous optimal solution into account.

Efficient problem optimization can be achieved by employment of a strategy that is adapted to the problem. Possible gain for our application should be examined.

The required prediction and optimization horizons depend on system dynamics and required control performance. Thorough understanding of these relations is needed to enable the choice of optimal values.

The capacitor-voltage stabilization is by far the most resource-consuming task in the proposed drive control system, and limits the performance of the other control functions. Its required dynamics should be examined, for the purpose of possible implementation at a lower sampling rate than the other control tasks.

A detailed investigation of the required converter and component switching frequencies is needed for device selection, in relation with their operating voltages. Switching and conduction losses are strongly related to these aspects. Component losses and overall converter efficiency should be analyzed in view of practical medium-voltage applications.

In case of device failures, damage to the rest of the inverter, to the load, to the network or to the environment could occur. Analysis of the power-circuit behaviour in fault cases and development of a protection concept is required to prevent such damage.

The aim of the investigated topology and proposed control methods is improvement of existing converter solutions. Achievement of this goal should be verified by detailed comparison of performance criteria.

The proposed capacitor-voltage stabilization controller works in conjunction with a motor controller that generates rather predictable voltages. Motor-control strategies like direct torque control (DTC)—often employed in industrial drives—generates less predictable voltages. Consequences on the voltage stabilization should be investigated in view of a possible co-operation.

The proposed methods are not limited to the investigated topology, but can be applied to other topologies or control problems as well. In a similar converter, but one that includes redundant states, the selection of such states and the related device commutations could be incorporated in the cost function to achieve optimal operation.

# Appendix A

# Jacobian-Matrix Calculation

As we have discussed in Chapter 6, the calculation effort can be reduced by determining the exact derivative of our optimization problem. Since we have a piece-wise linear system, this is a relatively easy and straight-forward task. This appendix describes in detail how the derivative is calculated.

As we have seen in Chapter 6, we can model our system with the difference equations (6.23) and (6.24), which we repeat here for convenience:

$$\begin{aligned} u_{C_{np}}[k+1] &= u_{C_{np}}[k] + \frac{T_S}{C_{np}} i_{C_{np}}[k] \\ &= u_{C_{np}}[k] - \frac{T_S}{C_{np}} \left( \vec{s}_{np}(\vec{u}_{dm}[k] + u_{cm}[k]) \cdot \vec{i}[k] + \frac{u_{C_{np}}[k]}{R_{C_{np}}} \right), \quad \text{(A.1)} \\ \vec{u}_{C_s}[k+1] &= \vec{u}_{C_s}[k] + \frac{T_S}{C_s} \vec{i}_{C_s}[k] \\ &= \vec{u}_{C_s}[k] - \frac{T_S}{C_s} \left( \vec{s}_s(\vec{u}_{dm}[k] + u_{cm}[k]) \vec{i}[k] + \frac{\vec{u}_{C_s}[k]}{R_{C_s}} \right). \quad \text{(A.2)} \end{aligned}$$

The control objective is to keep the capacitor-voltage errors (6.38),

$$\varepsilon \vec{u}_{C_v}[k] = \vec{u}_{C_v}[k] - \vec{u}^*_{C_v}[k], \quad \text{(A.3)}$$

and the common-mode voltage variations (6.39) and (6.40),

$$\delta u_{cm}[k] = \frac{u_{cm}[k] - u_{cm}[k-1]}{T_S}, \quad \text{(A.4)}$$

$$\delta^2 u_{cm}[k] = \frac{\delta u_{cm}[k] - \delta u_{cm}[k-1]}{T_S}, \quad \text{(A.5)}$$

small. In order to obtain this goal, we decided to solve an open-loop optimal control problem, for which we have chosen the cost function (6.41):

$$V_N(\vec{u}_{C_v}[0], \hat{\vec{\mathbf{u}}}_{dm}, \hat{\vec{\mathbf{i}}}, \mathbf{u}_{cm}) = \sum_{k=0}^{N-1} \Big[ (\varepsilon \hat{u}_{C_{np}}[k+1])^2 + \\ + (\varepsilon \hat{u}_{C_s,a}[k+1])^2 + (\varepsilon \hat{u}_{C_s,b}[k+1])^2 + (\varepsilon \hat{u}_{C_s,c}[k+1])^2 + \\ + (c_{u_{cm}} u_{cm}[k])^2 + (c_{\delta u_{cm}} \delta u_{cm}[k])^2 + (c_{\delta^2 u_{cm}} \delta^2 u_{cm}[k])^2 \Big]. \quad \text{(A.6)}$$

This cost function is a sum of squares, and its minimization a least-squares optimization problem.

In a general form, the least-squares cost function (A.6) can be expressed as:

$$V_N(\vec{u}_{C_v}[0], \hat{\vec{\mathbf{u}}}_{dm}, \hat{\vec{\mathbf{i}}}, \mathbf{u}_{cm}) = \sum_i f_i^2 = \vec{F}^T \vec{F}, \quad \text{(A.7)}$$

with $\vec{F}$ a column vector of all the cost-element functions $f_i$. The cost-function gradient $\nabla V_N$ in the optimization space $\mathbb{R}^N$ consists of its partial derivatives with respect to the common-mode voltages

$$\nabla V_N = \frac{\partial V_N(\vec{u}_{C_v}[0], \hat{\vec{\mathbf{u}}}_{dm}, \hat{\vec{\mathbf{i}}}, \mathbf{u}_{cm})}{\partial \mathbf{u}_{cm}} = 2\mathbf{J}^T \vec{F}, \quad \text{(A.8)}$$

where

$$\mathbf{J} = \frac{\partial \vec{F}}{\partial \mathbf{u}_{cm}} \quad \text{(A.9)}$$

is the Jacobian matrix of the cost-elements vector function. The elements of this Jacobian matrix are of different types. We will derive expressions for each of them in the following.

As can be easily verified using (A.4) and (A.5), the elements of the Jacobian matrix for the common-mode voltage and its variations are:

$$\mathbf{J}_{k,l}^{u_{cm}} = \frac{\partial (c_{u_{cm}} u_{cm}[k])}{\partial u_{cm}[l]} = \begin{cases} c_{u_{cm}} & k = l, \\ 0 & k \neq l; \end{cases} \quad \text{(A.10)}$$

$$\mathbf{J}_{k,l}^{\delta u_{cm}} = \frac{\partial (c_{\delta u_{cm}} \delta u_{cm}[k])}{\partial u_{cm}[l]} = \begin{cases} +c_{\delta u_{cm}}/T_S & k = l, \\ -c_{\delta u_{cm}}/T_S & k = l+1, \\ 0 & k \neq l, l+1; \end{cases} \quad \text{(A.11)}$$

$$\mathbf{J}_{k,l}^{\delta^2 u_{cm}} = \frac{\partial (c_{\delta^2 u_{cm}} \delta^2 u_{cm}[k])}{\partial u_{cm}[l]} = \begin{cases} +c_{\delta^2 u_{cm}}/T_S^2 & k = l, l+2, \\ -2c_{\delta^2 u_{cm}}/T_S^2 & k = l+1, \\ 0 & k \neq l, l+1, l+2. \end{cases} \quad \text{(A.12)}$$

The indices $k, l$ refer to the prediction and control sample respectively, and can take values from the actual time up to their horizons $k = 0 \dots N-1$ and $l = 0 \dots N_o - 1$.

The elements of the Jacobian matrix for the capacitor-voltage errors consist of several terms, but their calculation is a straight-forward task. Assuming constant reference values for the capacitor voltages—or at least values that do not depend on the common-mode voltage—, the partial derivatives of the capacitor-voltage errors (A.3) equal those of their actual voltages.

The Jacobian-matrix elements for the neutral-point capacitor voltage (A.1) are:

$$\mathbf{J}_{k,l}^{\varepsilon\hat{u}_{C_{np}}} = \frac{\partial \varepsilon\hat{u}_{C_{np}}[k+1]}{\partial u_{cm}[l]} = \frac{\partial \hat{u}_{C_{np}}[k+1]}{\partial u_{cm}[l]} - \underbrace{\frac{\partial \hat{u}^*_{C_{np}}[k+1]}{\partial u_{cm}[l]}}_{=0} =$$

$$= \frac{\partial \hat{u}_{C_{np}}[k]}{\partial u_{cm}[l]} + \frac{T_S}{C_{np}} \frac{\partial \hat{\vec{i}}_{C_{np}}[k]}{\partial u_{cm}[l]} = \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \frac{T_S}{C_{np}} \frac{\partial \hat{\vec{i}}_{C_{np}}[k]}{\partial u_{cm}[l]}. \quad \text{(A.13)}$$

Using (A.1) and noting that the switching functions depend also on the actual capacitor voltages (see Chapter 5), the partial derivatives of its current can be expressed as:

$$\frac{\partial \hat{\vec{i}}_{C_{np}}[k]}{\partial u_{cm}[l]} = -\vec{i}[k] \cdot \left( \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial u_{cm}[l]} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_{np}}[k]} \frac{\partial \hat{u}_{C_{np}}[k]}{\partial u_{cm}[l]} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,a}[k]} \frac{\partial \hat{u}_{C_s,a}[k]}{\partial u_{cm}[l]} + \right.$$

$$\left. + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,b}[k]} \frac{\partial \hat{u}_{C_s,b}[k]}{\partial u_{cm}[l]} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,c}[k]} \frac{\partial \hat{u}_{C_s,c}[k]}{\partial u_{cm}[l]} \right) - \frac{1}{R_{C_{np}}} \frac{\partial \hat{u}_{C_{np}}[k]}{\partial u_{cm}[l]} =$$

$$= -\vec{i}[k] \cdot \left( \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial u_{cm}[l]} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_{np}}[k]} \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,a}[k]} \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,a}} + \right.$$

$$\left. + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,b}[k]} \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,b}} + \frac{\partial \hat{\vec{s}}_{np}[k]}{\partial \hat{u}_{C_s,c}[k]} \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,c}} \right) - \frac{1}{R_{C_{np}}} \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}}. \quad \text{(A.14)}$$

Substitution of (A.14) in (A.13) leads to:

$$\mathbf{J}_{k,l}^{\varepsilon\hat{u}_{C_{np}}} = -\frac{T_S}{C_{np}}\vec{i}[k]\cdot\frac{\partial\hat{\vec{s}}_{np}[k]}{\partial u_{cm}[l]} + \left(1-\frac{T_S}{\tau_{C_{np}}}\right)\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \\ - \frac{T_S}{C_{np}}\vec{i}[k]\cdot\left(\frac{\partial\hat{\vec{s}}_{np}[k]}{\partial\hat{u}_{C_{np}}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \frac{\partial\hat{\vec{s}}_{np}[k]}{\partial\hat{u}_{C_s,a}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,a}} + \right. \\ \left. + \frac{\partial\hat{\vec{s}}_{np}[k]}{\partial\hat{u}_{C_s,b}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,b}} + \frac{\partial\hat{\vec{s}}_{np}[k]}{\partial\hat{u}_{C_s,c}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,c}}\right). \quad \text{(A.15)}$$

The Jacobian-matrix elements for the sub-inverter capacitor voltages (A.2) are (with $ph = a, b, c$):

$$\mathbf{J}_{k,l}^{\varepsilon\hat{u}_{C_s,ph}} = \frac{\partial\varepsilon\hat{u}_{C_s,ph}[k+1]}{\partial u_{cm}[l]} = \frac{\partial\hat{u}_{C_s,ph}[k+1]}{\partial u_{cm}[l]} - \underbrace{\frac{\partial\hat{u}^*_{C_s,ph}[k+1]}{\partial u_{cm}[l]}}_{=0} = \\ = \frac{\partial\hat{u}_{C_s,ph}[k]}{\partial u_{cm}[l]} + \frac{T_S}{C_s}\frac{\partial\hat{i}_{C_s,ph}[k]}{\partial u_{cm}[l]} = \mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,ph}} + \frac{T_S}{C_s}\frac{\partial\hat{i}_{C_s,ph}[k]}{\partial u_{cm}[l]}. \quad \text{(A.16)}$$

Using (A.2) and noting that the switching functions depend also on the actual capacitor voltages (see Chapter 5), the partial derivatives of its currents can be expressed as:

$$\frac{\partial\hat{i}_{C_s,ph}[k]}{\partial u_{cm}[l]} = -i_{ph}[k]\left(\frac{\partial\hat{s}_{s,ph}[k]}{\partial u_{cm}[l]} + \frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_{np}}[k]}\frac{\partial\hat{u}_{C_{np}}[k]}{\partial u_{cm}[l]} + \right. \\ \left. + \frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_s,ph}[k]}\frac{\partial\hat{u}_{C_s,ph}[k]}{\partial u_{cm}[l]}\right) - \frac{1}{R_{C_s}}\frac{\partial\hat{u}_{C_s,ph}[k]}{\partial u_{cm}[l]} = \\ = -i_{ph}[k]\left(\frac{\partial\hat{s}_{s,ph}[k]}{\partial u_{cm}[l]} + \frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_{np}}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_s,ph}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,ph}}\right) + \\ - \frac{1}{R_{C_s}}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,ph}}. \quad \text{(A.17)}$$

Substitution of (A.17) in (A.16) leads to:

$$\mathbf{J}_{k,l}^{\varepsilon\hat{u}_{C_s,ph}} = -\frac{T_S}{C_s}i_{ph}[k]\frac{\partial\hat{s}_{s,ph}[k]}{\partial u_{cm}[l]} + \left(1-\frac{T_S}{\tau_{C_s}}\right)\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,ph}} + \\ - \frac{T_S}{C_s}i_{ph}[k]\left(\frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_{np}}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_{np}}} + \frac{\partial\hat{s}_{s,ph}[k]}{\partial\hat{u}_{C_s,ph}[k]}\mathbf{J}_{k-1,l}^{\varepsilon\hat{u}_{C_s,ph}}\right). \quad \text{(A.18)}$$

Due to the causality of our system (A.1) and (A.2), the common-mode voltage has only influence on future capacitor voltages, and not on the actual or previous ones. Consequently, only the corresponding partial derivatives can take non-zero values:

$$\frac{\partial \hat{u}_{C_v}[k]}{\partial u_{cm}[l]} = \begin{cases} \cdot & k > l, \\ 0 & k \leq l. \end{cases} \tag{A.19}$$

The Jacobian matrices for the capacitor-voltage errors (A.15) and (A.18) are thus lower-triangular matrices, containing zeros everywhere above the main diagonal:

$$\mathbf{J}_{k,l}^{\varepsilon \hat{u}_{C_v}} = \begin{cases} \cdot & k \geq l, \\ 0 & k < l. \end{cases} \tag{A.20}$$

The switching functions depend only on the actual reference and capacitor voltages (see Chapter 5), and their partial derivatives with respect to the common-mode and capacitor voltages—as they occur in (A.15) and (A.18)—can thus be expressed in a general manner as:

$$\frac{\partial \hat{s}_{np,ph}[k]}{\partial u_{cm}[l]}, \frac{\partial \hat{s}_{s,ph}[k]}{\partial u_{cm}[l]} = \begin{cases} \partial s/\partial u & k = l, \\ 0 & k \neq l; \end{cases} \tag{A.21}$$

$$\frac{\partial \hat{s}_{np,ph}[k]}{\partial \hat{u}_{C_{np}}[l]}, \frac{\partial \hat{s}_{np,ph}[k]}{\partial \hat{u}_{C_s,ph}[l]}, \frac{\partial \hat{s}_{s,ph}[k]}{\partial \hat{u}_{C_{np}}[l]}, \frac{\partial \hat{s}_{s,ph}[k]}{\partial \hat{u}_{C_s,ph}[l]} = \begin{cases} \partial s/\partial u_C & k = l, \\ 0 & k \neq l. \end{cases} \tag{A.22}$$

According to the developments in Chapter 3 and 5, the general switching function $s$ obeys:

$$\text{if } u_1 \leq u \leq u_2 \quad \begin{cases} d_1 = \dfrac{u - u_2}{u_1 - u_2}, \\ d_2 = \dfrac{u - u_1}{u_2 - u_1}, \\ s = d_1 s_1 + d_2 s_2; \end{cases} \tag{A.23}$$

for an output voltage $u$ in the modulation band $[u_1, u_2]$ with switching states $\{s_1, s_2\}$. It can be easily verified that its partial derivatives equal:

$$\frac{\partial s}{\partial u} = \frac{s_2 - s_1}{u_2 - u_1}, \tag{A.24}$$

$$\frac{\partial s}{\partial u_1} = \frac{s - s_2}{u_2 - u_1}, \tag{A.25}$$

$$\frac{\partial s}{\partial u_2} = \frac{s_1 - s}{u_2 - u_1}. \tag{A.26}$$

Taking the correct values for $\{u_1, u_2\}$ and $\{s_1, s_2\}$, we can use (A.24) directly for (A.21). In order to find values for (A.22), we will develop it further:

$$\frac{\partial s}{\partial u_C} = \frac{\partial s}{\partial u_1}\frac{\partial u_1}{\partial u_C} + \frac{\partial s}{\partial u_2}\frac{\partial u_2}{\partial u_C}. \tag{A.27}$$

Here, we can use (A.25) and (A.26). The remaining factors $\partial u_1/\partial u_C$ and $\partial u_2/\partial u_C$ depend on the realization of the voltage levels by the inverter. In our case, these levels are determined by (5.37):

$$\begin{gathered} u_k = s_{m,k} u_{C_m} + s_{np,k} u_{C_{np}} + s_{s,k} u_{C_s}, \\ \text{with } s_{m,k}, s_{s,k} \in \{-1, 0, +1\}, \quad s_{np,k} = 1 - |s_{m,k}|\,; \end{gathered} \tag{A.28}$$

which is illustrated in Table 5.2 and Figure 5.3. Consequently, the mentioned factors can take the values

$$\frac{\partial u_k}{\partial u_{C_{np}}} = s_{np,k}, \tag{A.29}$$

$$\frac{\partial u_k}{\partial u_{C_s}} = s_{s,k}. \tag{A.30}$$

Although the developed equations may seem complicated, its implementation is rather straight-forward by using appropriate sub-functions and look-up tables. It takes less calculation effort than determining finite-difference approximations, which need multiple re-evaluations of the state predictions and cost function.

# Bibliography

[1] P. Hammond, "A new approach to enhance power quality for medium voltage AC-drives," *IEEE Transactions on Industry Applications*, vol. 33, no. 1, pp. 202–208, Jan. 1997.

[2] M. Buschmann and J. Steinke, "Robust and reliable medium voltage PWM inverter with motor friendly output," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, vol. 3, 1997, pp. 502–507.

[3] J. Lai and F. Peng, "Multilevel converters—a new breed of power converters," *IEEE Transactions on Industry Applications*, vol. 32, no. 3, pp. 509–517, May 1996.

[4] R. Menzies, P. Steimer, and J. Steinke, "Five-level GTO inverters for large induction motor drives," *IEEE Transactions on Industry Applications*, vol. 30, no. 4, pp. 938–944, July 1994.

[5] N. Schibli, T. Nguyen, and A. Rufer, "A three-phase multilevel converter for high-power induction motors," *IEEE Transactions on Power Electronics*, vol. 13, no. 5, pp. 978–986, Sept. 1998.

[6] F. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611–618, Mar. 2001.

[7] A. Rufer, M. Veenstra, and K. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 1999.

[8] J. Song-Manguelle, S. Mariéthoz, M. Veenstra, and A. Rufer, "A generalized design principle of a uniform step asymmetrical multi-

level converter for high power conversion," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 2001.

[9] S. Mariéthoz and A. Rufer, "Design and control of asymmetrical multi-level inverters," in *Proceedings of the IEEE Industrial Electronics Society Conference (IECON)*, 2002.

[10] H. Grüning, "Leistungselektronische Schaltungsanordnung," German Patent DE 196 15 855, Apr. 20, 1996.

[11] P. Steimer, "Verfahren zum Betrieb einer leistungselektronischen Schaltungsanordnung," German Patent DE 197 20 787, May 17, 1997.

[12] M. Manjrekar and T. Lipo, "A hybrid multilevel inverter topology for drive applications," in *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, vol. 2, 1998, pp. 523–529.

[13] M. Manjrekar, P. Steimer, and T. Lipo, "Hybrid multilevel power conversion system: A competitive solution for high-power applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 3, pp. 834–841, May 2000.

[14] P. Steimer and M. Manjrekar, "Practical medium voltage converter topologies for high power applications," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 3, 2001, pp. 1723–1730.

[15] P. Steimer and M. Veenstra, "Leistungselektronische Schaltungsanordnung und Verfahren zur Uebertragung von Wirkleistung," European Patent EP 1 253 706, Oct. 30, 2002.

[16] S. Mariéthoz and M. Veenstra, "Alimentation d'onduleurs multiniveaux asymétriques: Analyse des possibilités de réalisation et méthodes de répartition de la puissance," in *Actes de la Conférence des Jeunes Chercheurs en Génie Electrique (JCGE)*, 2003.

[17] P. Steimer, H. Grüning, J. Werninger, E. Carroll, S. Klaka, and S. Linder, "IGCT—a new emerging technology for high power, low cost inverters," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 2, 1997, pp. 1592–1599.

[18] S. Bernet, R. Teichmann, A. Zuckerberger, and P. Steimer, "Comparison of high-power IGBT's and hard-driven GTO's for high-power inverters," *IEEE Transactions on Industry Applications*, vol. 35, no. 2, pp. 487–495, Mar. 1999.

[19] M. Gutierrez, G. Venkataramanan, and A. Sundaram, "Performance characterization of integrated gate commutated thyristors," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 1, 1999, pp. 359–363.

[20] P. Hammond, "Medium voltage PWM drive and method," U.S. Patent 5,625,545, Apr. 29, 1997.

[21] N. Schibli, "Symmetrical multilevel converters with two quadrant DC-DC feeding," Ph.D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne (CH), 2000.

[22] P. Steimer, H. Grüning, J. Werninger, P. Dähler, G. Linhofer, and R. Boeck, "Series connection of GTO thyristors for high-power static frequency converters," *ABB Review*, no. 5, pp. 14–20, 1996.

[23] R. Boeck, O. Gaupp, P. Dähler, E. Bärlocher, J. Werninger, and P. Zanini, "Bremen's 100-MW static frequency link," *ABB Review*, no. 9/10, pp. 4–17, 1996.

[24] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Transactions on Industry Applications*, vol. 17, no. 5, pp. 518–523, Sept. 1981.

[25] G. Venkataramanan and A. Bendre, "Reciprocity-transposition-based sinusoidal pulsewidth modulation for diode-clamped multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 1035–1047, Oct. 2002.

[26] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE Journal*, vol. 2, no. 1, pp. 45–50, Mar. 1992.

[27] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, 1992, pp. 397–403.

[28] G. Gateau, T. Meynard, and H. Foch, "Stacked multicell converter (SMC): Topology and control," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 2001.

[29] T. Meynard, H. Foch, F. Forest, C. Turpin, F. Richardeau, L. Delmas, G. Gateau, and E. Lefeuvre, "Multicell converters: Derived topologies," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 978–987, Oct. 2002.

[30] O. Mueller and J. Park, "Quasi-linear IGBT inverter topologies," in *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, vol. 1, 1994, pp. 253–259.

[31] O. Mueller and R. Gran, "Reducing switching losses in series connected bridge inverters and amplifiers," U.S. Patent 5,734,565, Mar. 31, 1998.

[32] S. Hosseini and R. Mathur, "A binary multi-level voltage-source inverter for static VAr generation," in *Proceedings of the IEEE Canadian Conference on Electrical and Computer Engineering (CCECE)*, vol. 2, 1997, pp. 427–430.

[33] A. Damiano, M. Fracchia, M. Marchesoni, and I. Marongiu, "A new approach in multilevel power conversion," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, vol. 4, 1997, pp. 216–221.

[34] T. Lipo and M. Manjrekar, "Hybrid topology for multilevel power conversion," U.S. Patent 6,005,788, Dec. 21, 1999.

[35] K. Corzine and Y. Familiant, "A new cascaded multilevel H-bridge drive," *IEEE Transactions on Power Electronics*, vol. 17, no. 1, pp. 125–131, Jan. 2002.

[36] A. Damiano, M. Marchesoni, I. Marongiu, and A. Taffone, "Optimization of harmonic performances in multilevel converter structures," in *Proceedings of the IEEE International Symposium on Industrial Electronics (ISIE)*, vol. 2, 1997, pp. 341–346.

[37] X. Kou, K. Corzine, and Y. Familiant, "Full binary combination schema for floating voltage source multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 891–897, Nov. 2002.

[38] M. Gerber, E. Drabek, and R. Müller, "Die Lokomotiven 2000—Serie 460—der Schweizerischen Bundesbahnen," *Schweizer Eisenbahn-Revue*, no. 10, pp. 321–377, 1991.

[39] S. Malik and D. Kluge, "ACS 1000—world's first standard AC drive for medium-voltage applications," *ABB Review*, no. 2, pp. 4–11, 1998.

[40] F. Schettler, "Vorrichtung zur Erhöhung der Grundschwingungs-Leistungsausbeute eines selbstgeführten Wechselrichters," German Patent DE 195 35 552, Apr. 11, 1996.

[41] A. Schönung and H. Stemmler, "Geregelter Drehstrom-Umkehrantrieb mit gesteuertem Umrichter nach dem Unterschwingungsverfahren," *Brown Boveri Mitteilungen*, vol. 51, no. 8/9, pp. 555–577, Aug. 1964.

[42] H. van der Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulsewidth modulator based on voltage space vectors," *IEEE Transactions on Industry Applications*, vol. 24, no. 1, pp. 142–150, Jan. 1988.

[43] H. van der Broeck, "Analysis of the harmonics in voltage fed inverter drives caused by PWM schemes with discontinuous switching operation," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, vol. 3, 1991, pp. 261–266.

[44] V. Blasko, "Analysis of a hybrid PWM based on modified space-vector and triangle-comparison methods," *IEEE Transactions on Industry Applications*, vol. 33, no. 3, pp. 756–764, May 1997.

[45] A. Hava, R. Kerkman, and T. Lipo, "A high-performance generalized discontinuous PWM algorithm," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, Sept. 1998.

[46] A. Hava, R. Kerkman, and T. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, Jan. 1999.

[47] J. Steinke, "Switching frequency optimal PWM control of a three-level inverter," *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp. 487–496, July 1992.

[48] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A new multilevel PWM method: A theoretical analysis," *IEEE Transactions on Power Electronics*, vol. 7, no. 3, pp. 497–505, July 1992.

[49] S. Fukuda and K. Suzuki, "Using harmonic distortion determinig factor for harmonic evaluation of carrier-based PWM methods," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 2, 1997, pp. 1534–1541.

[50] L. Tolbert and T. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1098–1107, Sept. 1999.

[51] M. Veenstra and A. Rufer, "PWM-control of multi-level voltage-source inverters," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 3, 2000, pp. 1387–1393.

[52] S. Mariéthoz, "Mesure et amélioration des performances des modulateurs multiniveaux," in *Actes de la Conférence des Jeunes Chercheurs en Génie Electrique (JCGE)*, 2003.

[53] V. Blasko, V. Kaura, and W. Niewiadomski, "Sampling of discontinuous voltage and current signals in electrical drives: A system approach," *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1123–1130, Sept. 1998.

[54] S. Mariéthoz, École Polytechnique Fédérale de Lausanne/Laboratoire d'Électronique Industrielle, Lausanne (CH), 1999–2003, private communications.

[55] H. Bühler, "Volume 1: Théorie," in *Réglage de Systèmes d'Électronique de Puissance*, 1st ed., ser. Collection Électricité. Lausanne (CH): Presses Polytechniques et Universitaires Romandes, 1997.

[56] E. Watanabe, R. Stephan, and M. Aredes, "New concepts of instantaneous active and reactive powers in electrical systems with generic loads," *IEEE Transactions on Power Delivery*, vol. 8, no. 2, pp. 697–703, Apr. 1993.

[57] M. Aredes, J. Häfner, and K. Heumann, "Three-phase four-wire shunt active filter control strategies," *IEEE Transactions on Power Electronics*, vol. 12, no. 2, pp. 311–318, Mar. 1997.

[58] H. Akagi, S. Ogasawara, and H. Kim, "The theory of instantaneous power in three-phase four-wire systems: A comprehensive approach," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 1, 1999, pp. 431–439.

[59] C. Newton and M. Summer, "Neutral point control for multi-level inverters: Theory, design and operational limitations," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 2, 1997, pp. 1336–1343.

[60] S. Fukuda and Y. Matsumoto, "Optimal regulator based control of NPC boost rectifiers for unity power factor and reduced neutral point potential variations," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, vol. 2, 1997, pp. 1455–1462.

[61] D. Mayne, J. Rawlings, C. Rao, and P. Scokaert, "Constrained model predictive control: Stability and optimality," *Automatica*, vol. 36, no. 6, pp. 789–841, June 2000.

[62] D. Mayne, "Model predictive control: The challenge of uncertainty," in *Digest of the IEE Colloquium on Model Predictive Control*, 1999.

[63] P. Roberts, "A brief overview of model predictive control," in *Digest of the IEE Seminar on Practical Experiences with Predictive Control*, 2000.

[64] T. Coleman, M. Branch, and A. Grace, *Optimization Toolbox User's Guide*, software manual, The MathWorks, Inc., Natick, MA (USA), 1999. [Online]. Available: http://www.mathworks.com/access/helpdesk/help/pdf_doc/optim/optim_tb.pdf

[65] M. Veenstra, ABB Industrie AG, Turgi (CH), 1996–1998, experiences from the ACS 1000 development team.

[66] *Using MATLAB*, software manual, The MathWorks, Inc., Natick, MA (USA), 1999. [Online]. Available: http://www.mathworks.com/access/helpdesk/help/pdf_doc/matlab/using_ml.pdf

[67] *PLECS User Manual—Preliminary Edition*, software manual, Plexim GmbH, Zürich (CH), 2002. [Online]. Available: http://www.plexim.com/downloads/plecs/manual.pdf

[68] *SEMITOP Cool Components*, product information sheet, SEMIKRON International Dr. Fritz Martin GmbH & Co. KG, Nürnberg (D), 1998. [Online]. Available: http://www.semikron.com/databook/vorspann/semitope.pdf

[69] M. Montemari and M. Nicollerat, *Présentation de la Carte SHARC*, internet slide show, École Polytechnique Fédérale de Lausanne/Laboratoire d'Électronique Industrielle, Lausanne (CH), 1998. [Online]. Available: http://leiwww.epfl.ch/sharc

[70] *ADSP-2106x SHARC User's Manual*, 2nd ed., Analog Devices, Inc., Norwood, MA (USA), 1997.

[71] *ADSP-21000 Family C Tools Manual*, 3rd ed., Analog Devices, Inc., Norwood, MA (USA), 1995.

[72] *ADSP-21000 Family C Runtime Library Manual*, 3rd ed., Analog Devices, Inc., Norwood, MA (USA), 1995.

[73] C. Delannoy, *La Référence du C Norme ANSI/ISO*. Paris (F): Éditions Eyrolles, 1998.

# List of Figures

# List of Tables

# Curriculum Vitae

Martin Veenstra  Born on 20 November 1970 in Groningen, The Netherlands

## Employment

1998–2003 Assistant-Doctorant at *École Polytechnique Fédérale de Lausanne, Laboratoire d'Électronique Industrielle (EPFL-LEI)*, Lausanne, Switzerland.

- Research work towards Ph.D. degree on hybrid asymmetric multi-level inverters for industrial drives (sponsored by *ABB Industry*).
- Miscellaneous projects on power electronics for power generation (for *EdF*, *Alstom Power*).
- Education assistance for semester works and diploma students.

1995–1998 Research Engineer at *ABB Corporate Research*, Baden-Dättwil, Switzerland.

- Components for high-power IGBT traction drives (for *ABB Transportation Systems/ADtranz*).
- Control of large IGCT industrial drives (job rotation at *ABB Industry*, Turgi, Switzerland).

## Education

1989–1995 *Delft University of Technology*, Delft, The Netherlands.

- M.Sc. in Electrical Engineering, cum laude.

1983–1989 *Sint-Maartenscollege*, Haren/Groningen, The Netherlands.

- VWO Diploma (university preparatory education).

# Publications

M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multi-level inverter for competitive medium-voltage industrial drives," in *Proceedings of the IEEE Industry Applications Society Annual Meeting (IAS)*, 2003.

M. Veenstra and A. Rufer, "Non-equilibrium state capacitor voltage stabilization in a hybrid asymmetric nine-level inverter: Non-linear model-predictive control," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 2003.

S. Mariéthoz and M. Veenstra, "Alimentation d'onduleurs multiniveaux asymétriques: Analyse des possibilités de réalisation et méthodes de répartition de la puissance," in *Actes de la Conférence des Jeunes Chercheurs en Génie Electrique (JCGE)*, 2003.

J.-M. Strubin, M. Veenstra, and A. Rufer, "Linear induction motor demo-track: a tool for renewed motivation in electrical engineering," in *Proceedings of the International Symposium on Linear Drives for Industry Applications (LDIA)*, 2001.

J. Song-Manguelle, S. Mariéthoz, M. Veenstra, and A. Rufer, "A generalized design principle of a uniform step asymmetrical multilevel converter for high power conversion," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 2001.

J. Song-Manguelle, M. Veenstra, S. Mariéthoz, and A. Rufer, "Convertisseurs multiniveaux asymétriques pour des applications de moyenne et forte puissance," in *Actes du Colloque Electronique de Puissance de Futur (EPF)*, 2000.

M. Veenstra and A. Rufer, "PWM-control of multi-level voltage-source inverters," in *Proceedings of the IEEE Power Electronics Specialists Conference (PESC)*, vol. 3, 2000, pp. 1387–1393.

A. Rufer, M. Veenstra, and K. Gopakumar, "Asymmetric multilevel converter for high resolution voltage phasor generation," in *Proceedings of the European Power Electronics and Applications Conference (EPE)*, 1999.

M. Veenstra, "Ontwerp en realisatie van een aandrijving met een asynchrone machine met fluxgeoriënteerde sturing, gevoed door een spanningsinvertor met stroomregeling," Master's thesis, Technische Universiteit Delft, Delft (NL), Sept. 1994.

# Patents

P. Steimer and M. Veenstra, "Leistungselektronische Schaltungsanordnung und Verfahren zur Uebertragung von Wirkleistung," European Patent EP 1 253 706, Oct. 30, 2002.

R. Fried, J. Skindhoj, M. Veenstra, and P. Etter, "Verfahren zur Herstellung einer Kaltleiteranordnung sowie Verwendung der Kaltleiteranordnung als Strombegrenzer," German Patent DE 198 08 025, Sept. 2, 1999.

A. Stuck and M. Veenstra, "Vorrichtung zur Strombegrenzung," German Patent DE 196 48 381, June 4, 1998.