High Frequency Equivalent Circuit of GaAs Depletion and Enhancement FETs for Large Signal Modelling

M. Berroth and R. Bosch
Fraunhofer Institute for Applied Solid State Physics
Eckerstr. 4, D-7800 Freiburg, FRG

Abstract

For the design of digital circuits as well as for power amplifiers, the nonlinear modelling of GaAs FETs is a necessity. We use an extended equivalent circuit, which takes into account the gate current of positive biased transistors as well as the symmetrical nature of the devices at low drain voltages. A fast method to determine the elements of the equivalent circuit from measured S-parameters is presented which delivers for the first time good agreement for all operating points. A valid large signal description of the device can be obtained by implementing the bias dependences of the intrinsic elements into a circuit simulator like SPICE.

I. Introduction

For MMIC designs, small-signal equivalent circuits of GaAs FETs are used up to millimeter wave frequencies [1,2]. Recently developed MODFETs with very high transit frequencies have threshold voltages of about 0 volt [3]. The operating point for maximum transconductance and highest transit frequency is at positive biased gate. However at these bias points, the gate current can not further be neglected. Another problem occurs in switching applications, when the drain to source voltage of the FET comes close to 0 volt. In this case the symmetrical nature of the physical device has to be reflected in the equivalent circuit. We therefore propose an extended equivalent circuit together with a fast method to determine its elements from S-parameter measurements for all operating points and without frequency limitations. Only such an equivalent circuit, which describes the transistor at all bias points precisely,

can be used to evaluate the bias dependences of the intrinsic circuit elements. This is essential for large signal applications.

II. The Small-Signal Equivalent Circuit

The complete small-signal equivalent circuit is shown in Fig. 1. The circuit is divided into the external part with eight parasitic elements and the intrinsic device, containing nine elements defined by 10 variables ($\underline{g}_m = |g_m|e^{-j\omega\tau}$). All external elements are considered to be constant for all operating points. All intrinsic elements depend on the applied gate and drain voltages. For operating points with forward biased gate, the differential resistances of the gate to source and gate to drain diodes are modelled by the resistances R_{fs} and R_{fd}. At low drain voltages, the resistor R_{dg} has to be included due to the more symmetric behaviour of the transistor.

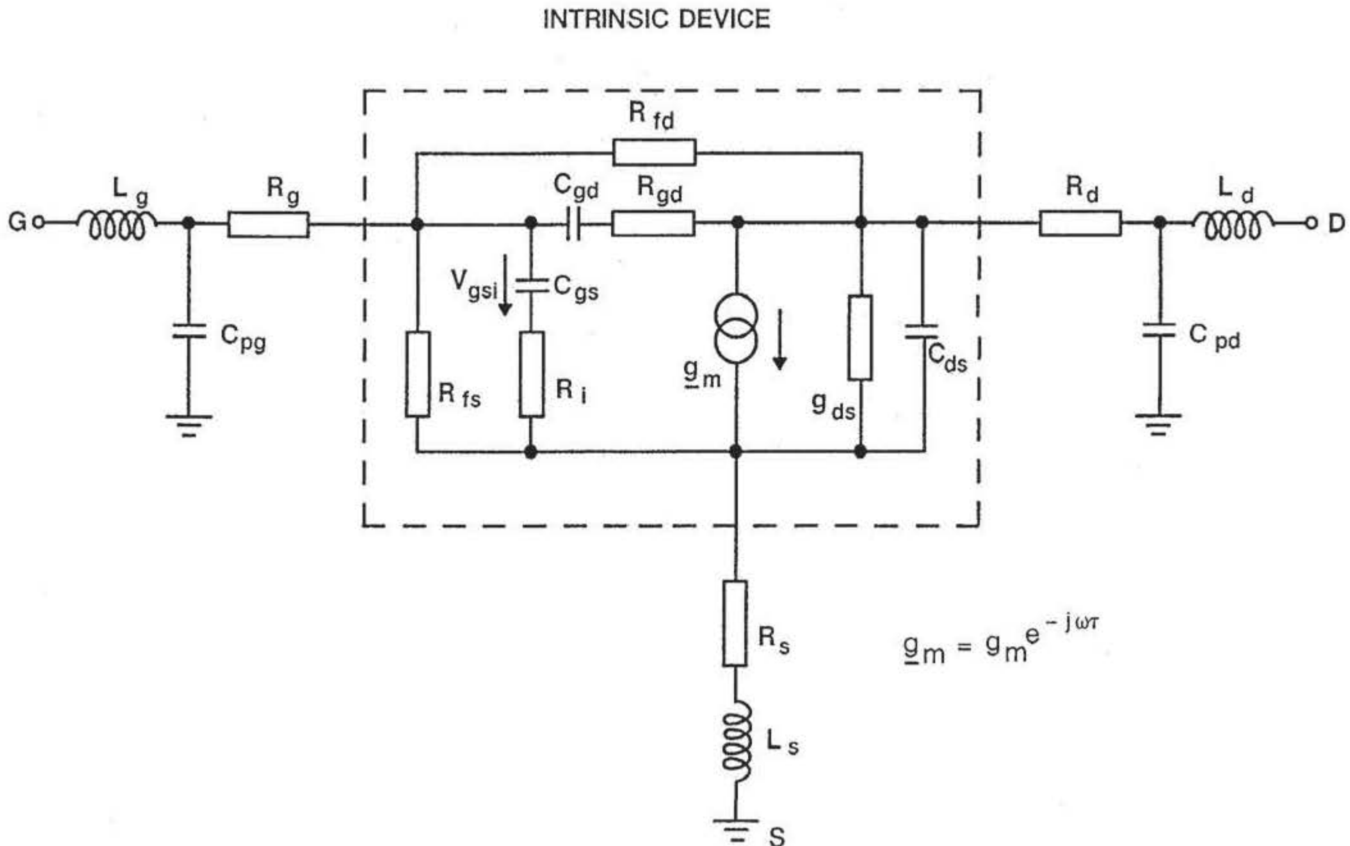

Fig. 1: Extended small-signal equivalent circuit of a field effect transistor including gate current and resistive feedback.

III. Parameter Extraction

Our method to extract the element values from S-parameter measurements is similar to [1,5,7], however applied to the extended circuit. Furthermore the frequency limitations of [1,5] have been overcome by a fully analytic solution of the intrinsic Y-parameter equations. First, the external parasitic elements have to be determined by so-called "cold modelling" at a drain to source voltage of 0 volt as described in [1,2,4]. Then "hot" measured S-parameters ($V_{ds} > 0V$) are deembedded from the external parasitic elements to obtain the equivalent Y-parameters of the intrinsic device for any bias and frequency. As additional relations for the differential resistances R_{fs} and R_{fd} either DC measurements or the S-parameters obtained at very low frequencies can be used. At each bias point the remaining eight parameters can be calculated for each measured frequency independently:

$$C_{gd} = -\frac{Im(Y_{12i})}{\omega}(1+\left(\frac{Re(Y_{12i})+g_{fd}}{Im(Y_{12i})}\right)^2) \quad (1)$$

$$R_{gd} = \frac{Re(Y_{12i})+g_{fd}}{\omega C_{gd} Im(Y_{12i})} \quad (2)$$

$$C_{gs} = \frac{Im(Y_{11i})+Im(Y_{12i})}{\omega}\left(1+\frac{(Re(Y_{11i})+Re(Y_{12i})-g_{fs})^2}{(Im(Y_{11i})+Im(Y_{12i}))^2}\right) \quad (3)$$

$$R_i = \frac{Re(Y_{11i})+Re(Y_{12i})-g_{fs}}{\omega C_{gs}(Im(Y_{11i})+Im(Y_{12i}))} \quad (4)$$

$$g_m = \sqrt{((Re(Y_{21i})-Re(Y_{12i}))^2+(Im(Y_{21i})-Im(Y_{12i}))^2)\,D1} \quad (5)$$

$$\tau = \frac{1}{\omega}arcsin\left(\frac{Im(Y_{12i})-Im(Y_{21i})-\omega C_{gs}R_i(Re(Y_{21i})-Re(Y_{12i}))}{g_m}\right) \quad (6)$$

$$C_{ds} = \frac{Im(Y_{22i})+Im(Y_{12i})}{\omega} \quad (7)$$

$$g_{ds} = Re(Y_{22i})+Re(Y_{12i}) \quad (8)$$

where

$$D1 = 1+(\omega R_i C_{gs})^2.$$

Equations (1) through (8) are valid
i) for drain voltages greater than zero volt,
ii) for positive and negative gate voltages and
iii) for all frequencies for which the equivalent circuit is valid.
As there are no time consuming iteration loops in the hot modelling evaluation procedure, this method can effectively be used for on-wafer S-parameter measurements with real-time parameter extraction.

V. Measurements and Results

Several different types of HFETs as well as MESFETs fabricated at our Institute have been investigated to verify our model and parameter extraction method and to compare it with the results of other procedures. The "hot modelling" method described in [1] is limited to frequencies below 5 GHz, which is a severe limitation for present and future applications of GaAs FET devices. Furthermore, as the influence of the differential resistances is not considered in [1], the method can not be used for operating points with a significant gate current. Fig. 2 shows an enhancement type heterostructure FET with a gate voltage of 0.75 volts and a drain voltage of 1.5 volts. The crosses indicate the measured S-parameters of a heterostructure FET with pulse doped layers on both sides of the undoped channel with a gate length of 0.5 μm. The circles show the results of our method. Obviously, our model yields a good agreement with the measured data up to the measurement limit of 40 GHz, showing that our model extrapolations to higher frequencies are reliable. The low error averages E_{ij} of our improved model should be noted.
As the accuracy of our parameter extraction is great and the computation time is negligeable, we can calculate the small-signal equivalent circuit elements at many operating points. Thus the bias dependence of all internal elements is quickly established. Due to the validity of the equivalent circuit for all operating points, these voltage dependences of the equivalent circuit elements can be utilized for large-signal model development.

V. Conclusion

An extended small-signal equivalent circuit for GaAs field effect transistors is proposed. It includes the effects of the differential resistances of the gate to source and gate to drain diodes as well as the serial resistance of the feedback capacitance. A fast and accurate method to determine all elements of this equivalent circuit at all bias points and without frequency limitations is presented. Direct computation from analytical expressions, without iteration, allows this parameter extraction procedure to be used for real-time on-wafer parameter extraction. Large-signal calculations are possible by inserting the voltage dependences evaluated for the elements into suitable simulation programs like SPICE.

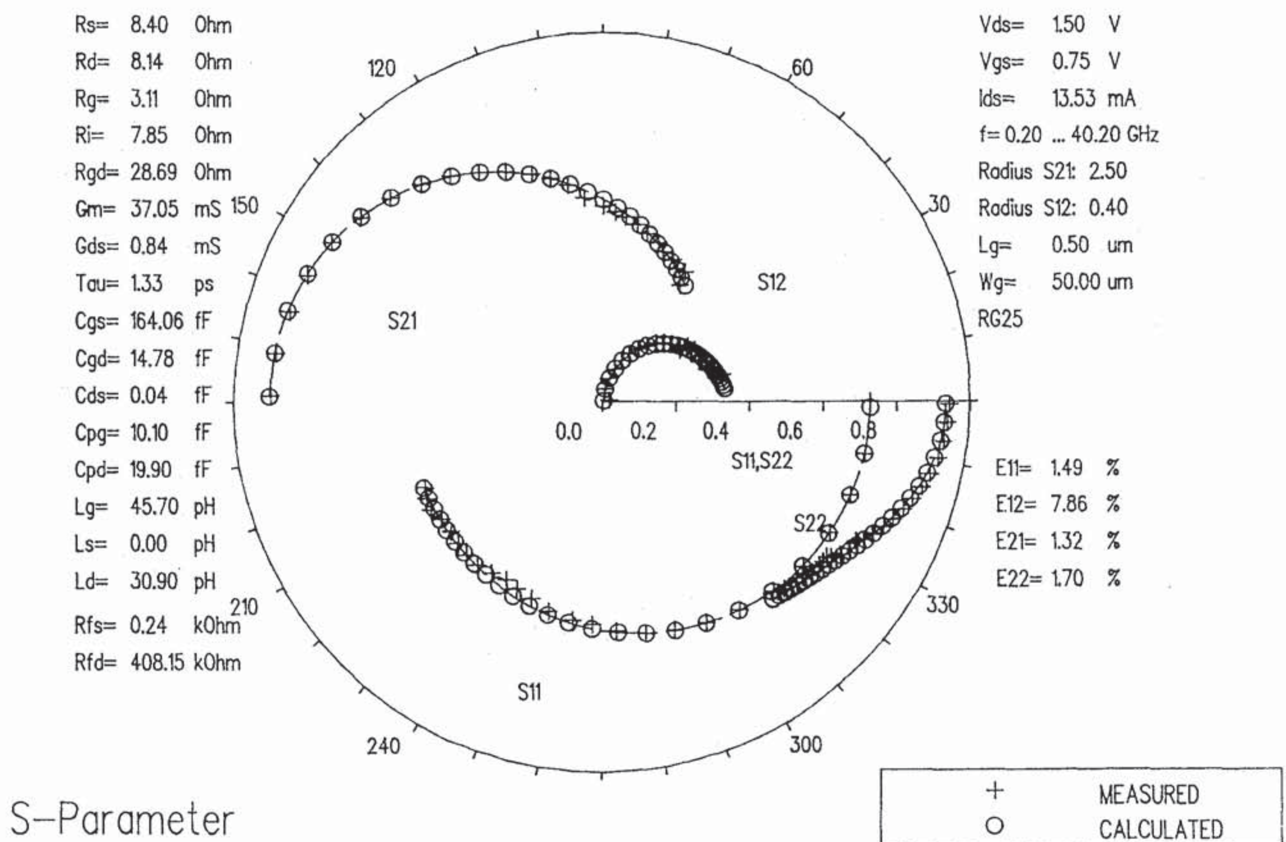

Fig. 2: Comparison of measured data of a 0.5 μm enhancement heterostructure field effect transistor (crosses) with simulation results of our procedure presented by circles.

References

[1] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A New Method for Determining the FET Small-Signal Equivalent Circuit," IEEE Trans. Microwave Theory Tech., vol. MTT-36, pp. 1151-1159, July 1988.
[2] W. R. Curtice and R. L. Camisa, "Self-consistent GaAs FET models for amplifier design and device diagnostics," IEEE Trans. Microwave Theory Tech., vol. MTT-32, pp. 1573-1578, Dec. 1984.
[3] Loi D. Nguyen et. al., "Influence of Quantum-Well Width on Device Performance of $Al_{0.30}Ga_{0.70}As/In_{0.25}Ga_{0.75}As$ (on GaAs) MODFET's," IEEE Trans. Electron Devices, vol. ED-36, no. 5, pp. 833-838,May 1989.
[4] T.-H. Chen and M. Kumar, "Novel GaAs FET Modelling Technique for MMICs," Technical Digest, 1988 GaAs IC Symposium, Nashville, pp. 49-52, Nov. 1988.
[5] R. A. Minasian, "Simplified GaAs MESFET Model to 10 GHz," Electron. Lett., vol. 13, no. 8, pp. 549-551, 1977.
[6] P. L. Hower and N. G. Bechtel, "Current Saturation and Small-Signal Characteristics of GaAs Field Effect Transistors," IEEE Trans. Electron Devices, vol. ED-20, no. 3, pp. 213-220, Mar. 1973.
[7] M. Berroth and R. Bosch, "Broad Band Determination of the FET Small-Signal Equivalent Circuit," to be published IEEE Trans. Microwave Theory Tech., July 1990