Digital Dynamic Frequency Dividers for Broad Band Application up to 60 GHz

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Abstract

A broad band dynamic frequency divider based on pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.25}Ga_{0.75}As$ MODFETs and passive loads will be presented. Stable operation from 28 GHz up to 51 GHz with a power consumption of 440 mW could be shown.
SPICE network simulation predicts operation in the 35 GHz - 60 GHz range for a divider circuit using an advanced E/D AlGaAs/ InGaAs MODFET process.

Introduction

Very high speed frequency dividers are key components in many applications, such as in measurement and communication systems. Using 0.2 µm GaAs MESFETs [1] and 0.25 µm inverted AlGaAs HEMTs [2], operating frequencies of 26.5 GHz have been reported for dynamic dividers. Static dividers based on Si bipolar transistors [3], AlGaAs/GaAs HBTs [4] and AlInAs/ GaInAs HBTs [5] have achieved frequency limits of 25 GHz, 34.8 GHz, and 39.5 GHz, respectively.
A dynamic frequency divider operating in the 18-34 GHz range based on our E/D AlGaAs/GaAs/AlGaAs quantum well transistor process was presented in [6].
A measured operation performance enhancement to 28 GHz - 51 GHz by the use of pseudomorphic $Al_{0.2}Ga_{0.8}As/In_{0.25}Ga_{0.75}As$ MODFETs and passive loads will be presented here.

Process Technology

We have developed a mix-and-match technology combining e-beam with optical lithography whereby the e-beam is used for writing the gates only. Mushroom shaped gates were used to reduce the resistance of 0.15 µm gates [7].

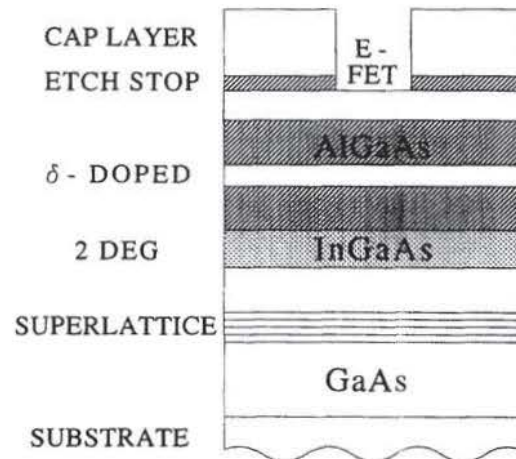Fig. 1. MODFET layer structure

The layer structure as shown in fig.1 including n^+-cap, δ-doped GaAs supply layer, AlGaAs spacer and pseudomorphic InGaAs channel was grown by MBE.

The typical growth conditions are published in [8]. Precise control of the threshold voltage was guaranteed by an AlGaAs etch stop using a dry etch process.

In our process sequence we have E-type MODFETs, NiCr thin film resistors, MIM capacitors, and two layers for interconnections. The top layer can be formed as air-bridges thus reducing parasitic capacitances.

Circuit Design

The maximum input frequency to static dividers is restricted to about $1/2t_{pd}$, where t_{pd} is the delay time of the used logic gate. Dynamic frequency dividers generally can reach two times higher input frequencies. The simplest dynamic frequency divider can be built up using an inverter and a buffer connected in series [1]. The output of the buffer is fed back to the inverter input by a transfergate. The inverter will be switched with half the frequency of the transfergate. The time in which the transfergate is switched on will be shorter than the delay of the inverter buffer chain, and that delay in turn will be no longer than one input pulse period. These conditions give the lower and upper limits for stable operation of the divider.

During that time when the tranfergate is switched off, the logic state is stored only in the capacitance of the high ohmic inverter input node. For short rise and fall times, however, the gate capacitance of the transfergate can cause logic errors.

The use of a memory-type flip-flop for data storage as proposed in [2] is more reliable. To switch the memory-type flip-flop symmetrically, two ring oscillator chains are used. Differential outputs then become available.
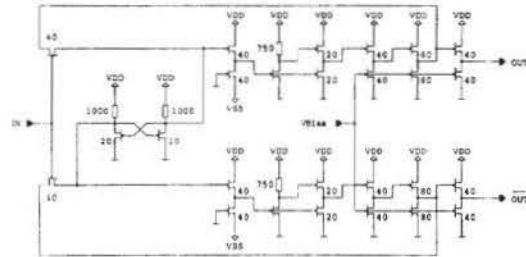

Fig. 2. Divider based on E-type MODFETs

Fig.2 shows a circuit schematic of an appropriate realization based on E-type MODFETs and NiCr ohmic resistors.

The circuit was optimized by SPICE network simulation based on an in-house developed heterojunction field effect transistor model [9].

The inverters of the ring oscillator chains are designed in SBFL for high logic swing and low output impedance. Three source follower buffers are used for appropriate signal delay and level shifting.

The memory-type flip-flop is built up by two E/R-DCFL inverters using 1 kΩ resistors for high logic swing. They normally would not achieve 30 GHz operation, but in this case the outputs are directly driven.

The gate width of the transfergates is a trade-off between a high on-conductance and a low capacitive load for the driving source follower.

SPICE simulation predicted 26 GHz - 50 GHz operation for this circuit design.

Results

Fig. 3 is a micrograph of the divider circuit. The chip size is 1 mm x 1 mm, the internal divider measures about 200 μm x 220 μm. The input is applied to the bond pads using a 50 Ω coplanar line on chip terminated to match 50 Ω.

Fig. 3. Micrograph of the Divider Circuit

Stable operation was measured in the frequency range from 28 GHz up to 51 GHz with a power consumption of 440 mW.

Fig.4 shows the pulse diagram of the 51 GHz input and 25.5 GHz output.

To the best of our knowledge, this is the highest input frequency ever reported for frequency divider circuits in any technology.

The circuit runs at a power supply of V_{DD}= +3.5 V and V_{SS}= -0.5 V. The required input voltage swing is less than 800 mV at 28 GHz and decreases as the frequency increases.
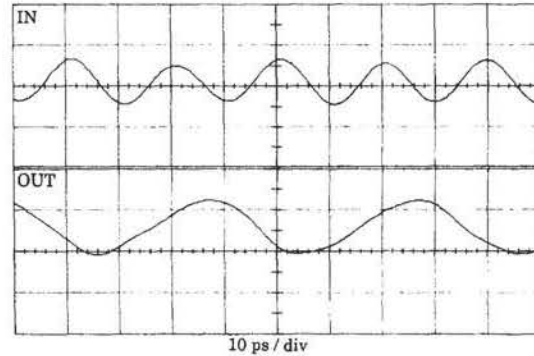

10 ps / div

Fig. 4. Measured Pulse Diagram

Circuit Enhancement by an E/D Process

Fig.5 shows the circuit schematic for a similar divider circuit based on an E/D AlGaAs/InGaAs MODFET process.

D-type FET active loads led to a further increase of speed, and a less sophisticated circuit design. Only two source follower buffers are still necessary.

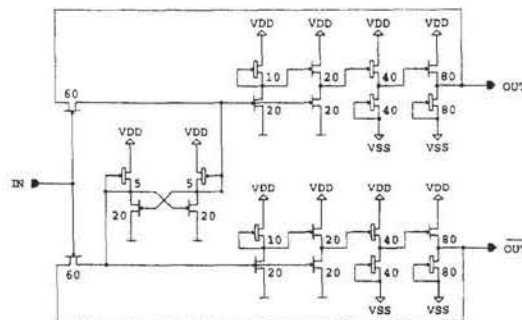SPICE network simulation predict operation in the 35 GHz - 60 GHz range for that divider circuit.

Fig. 5 Divider based on E/D MODFETs

Summary

The design and performance of a broad band dynamic frequency divider based on E-type AlGaAs/InGaAs MODFETs was presented. Stable operation could be shown in a frequency range from 28 GHz - 51 GHz with a power consumption of 440 mW. 35 GHz - 60 GHz operation can be predicted for a divider circuit based on an E/D MODFET process available in the next future.

References

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