7.5 Gb/s Monolithically Integrated Clock Recovery Using PLL and 0.3 μm Gate Length Quantum Well HEMTs

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Abstract: A monolithically integrated clock recovery (CR) circuit making use of the phase-locked loop (PLL) circuit technique and enhancement/depletion AlGaAs/GaAs quantum well high electron mobility transistors (QW-HEMTs) with gate lengths of 0.3 μm has been realized. A novel preprocessing circuit was used. In the PLL a fully-balanced varactorless VCO has been introduced. The VCO has a centre oscillating frequency of about 7.5 GHz and a tuning range greater than 500 MHz. A satisfactory clock signal has been obtained at the bit rate of about 7.5 Gb/s. The power consumption is less than 200 mW at the supply voltage of -5 V.

1. Introduction

At our institute a set of ICs has been developed for h.s. (high-speed) optical transmission systems at bit rates above 10 Gb/s [1]. The only lack is an IC for CR in the same rate range. In fact, the IC realisation of CR is becoming the bottleneck of the h.s. system integration worldwide [2]. Though several fundamental subcircuits at the rates greater than 6 Gb/s have emerged [2-4], the rates of the realized ICs for a full CR function are limited to 4 Gb/s, both for the CR category with a surface-acustic-wave (SAW) filter [5,6] and with a PLL [7]. This paper describes a M(onolithic)IC for the CR with a PLL at the rate of 7.5 Gb/s.

2. Circuit Principle

The block diagram of the CR with a PLL is shown in Fig. 1. Except $C_{12,22}$ and $R_{12,22}$ — taking account of the possibility to adjust the performance of the LF (loop filter), all components required for a CR were integrated on chip.

In the preprocessor block the input data signal, assumed having an NRZ (non-return-to-zero) format, is processed that the signal v_i' that has a strong spectral line

among its continuous spectrum is generated. The phase of v_i' is then compared in the phase detector (PD) with that of the oscillating signal v_o' from the VCO. By this way the phase differency signal v_p is obtained. After filtering, the voltage controlling signal v_{co} of the VCO is formed. Using this signal, the phase of v_o will follow that of v_i in step.

As preprocessor there are two typical structures, i.e., (a) a differentiating circuit followed by a rectifier and (b) an EX(clusive)-OR logic circuit plus a $T_b/2$ delay element. The first structure is simply integrated. The disadvantage is that its output is single-ended, what is not favourable for the interconnection with a double-balanced PD mostly used. In the second structure the EXOR alone is easily integrated into the system, whereas the $T_b/2$ delay element is not. In our design, therefore, a modified circuit was used.

The circuit diagram of our preprocessor is shown in Fig. 2. It can be considered as a mixed version of two typical structures, or as a modified EXOR circuit. Instead of a normal difference current amplifier for the lower level of the EXOR, a capacitively-coupled current amplifier (C^3A) [5] was used as a differentiating circuit. Using this circuit, a peaked, unipolar voltage pulse will be generated at every level transition of the input data signal. If HEMTS EF_5 and EF_7 are activated at the transitions from "0" to "1", HEMTS EF_6 and EF_9 will be activated at the transitions from "1" to "0". Thus, the clock signal carried by the transitions is detected. Since the modified circuit has a fully-balanced structure and the delay element which is difficult to integrate but necessary for the preprocessor with a typical EXOR can be removed, the modified preprocessing circuit is very favourable for the monolithic integration of the system.

The circuit of the PD in PLL has an analogue structure as that of the preprocessor except the loads. The operation amplifier (OPAM) consists of three stages of differential amplifiers. In these amplifier depletion HEMTs were used as active loads to increase the gain. According to simulations a total gain greater than 60 dB can be obtained from the OPAM.

As the key part of the PLL, a fully-balanced varactorless VCO has been found on the basis of the circuit in [8]. Two capacitively-coupled Darlington pairs are used for the active unit. The gate-drain junctions of the input HEMTs of the Darlington pairs are used as varactors. Instead of an external 1/4 open-circuited transmission line in [8], two on-chip inductors are used for the frequency and phase stabilizing elements.

3. Fabrication

The same process as for all ICs in [1] was used for the fabrication of our CR chip. The detail description of the process can be found, for example, in [9]. The gate length of the HEMTs is 0.3 µm. The transit frequency f_T of the typical E-HEMT is 50 GHz. For capacitors the MIM-structure was chosen. The airbridge capability was used for the realization of inductors. The chip area is 1.5x1 mm^2.

4. Experimental Results

The chip was measured on wafer using 50 Ω coplanar test probes. The power consumption of the chip is less than 200 mW at the supply voltage of -5V. The VCO has a centre frequency of about 7.5 GHz. The total control range is more than 500 MHz. Fig. 3a shows a free-running spectrum of the VCO at the centre frequency of about 7.8 GHz. The spectral linewidth is less than 500 KHz. This value is one half of that given in [10], what can be attributed to the balanced structure of our VCO. The ratio of the centre frequency to the spectral linewidth is about 16 000, approxmately one sixth of that given in [8], and the phase noise estmated from the spetrum is about -88 dBc/Hz at an offset of 1 MHz, 22 dB higher than the value given in [11]. If we take into account the fact that the $1/f$ noise of the GaAs FETs is 20-30 dB greater than that of the bipolar transistors [12], the obtained values from the free-running VCO can be considered as in good order. Fig. 3b shows the spectrum of the output signal measured from the in-locked VCO. In this case the -3 dB spectral linewidth was immediately reduced to the level of the input signal, i.e., about 15 kHz.

Fig. 4 shows the measured waveforms of the input PRBS (pseudorandom bit sequence) with a length of 2^{10}-1 at the bit rate of about 7.5 Gb/s and the output clock signal of the CR chip. The time jitter is about 2 ps.

5. Conclusion

We have designed, fabricated and tested a clock recovery IC using the PLL technique and AlGaAs/GaAs QW-HEMTs. The operating bit rate as high as 7.5 Gb/s was demonstrated. The power consumption is less than 200 mW.

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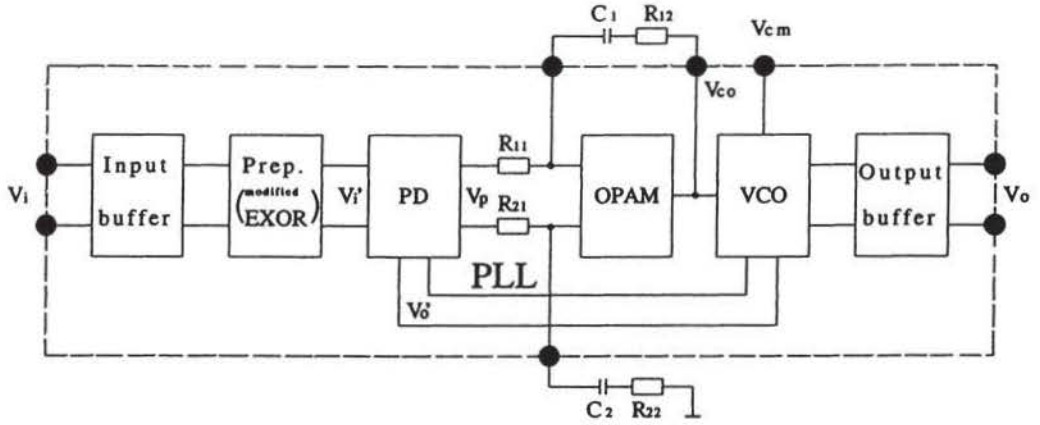
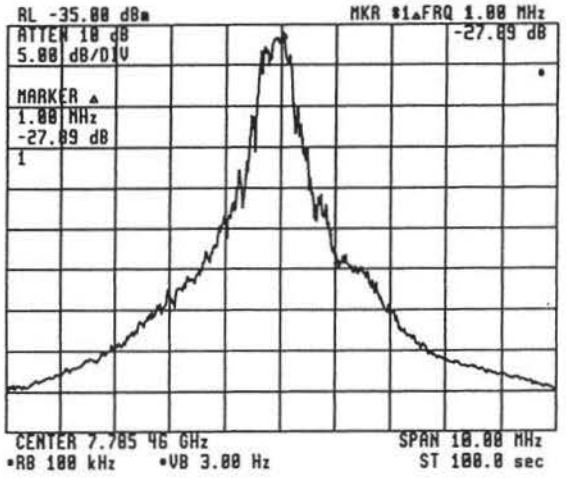


Fig. 1 The block diagram of the monolithically integrated 7.5 Gb/s CR.



(a)

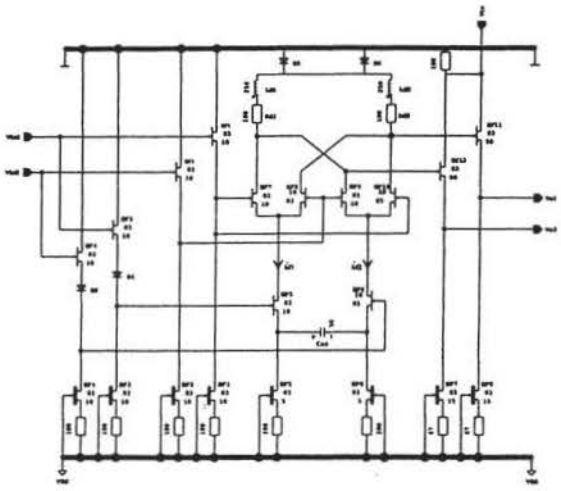
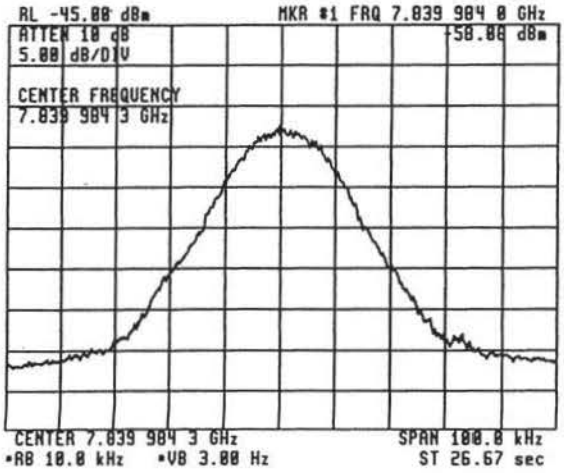


Fig. 2 Circuit diagram of the preprocessor.



(b)

Fig. 3 Near-carrier Spectra of the free-running (a) and the in-locked (b) VCO.

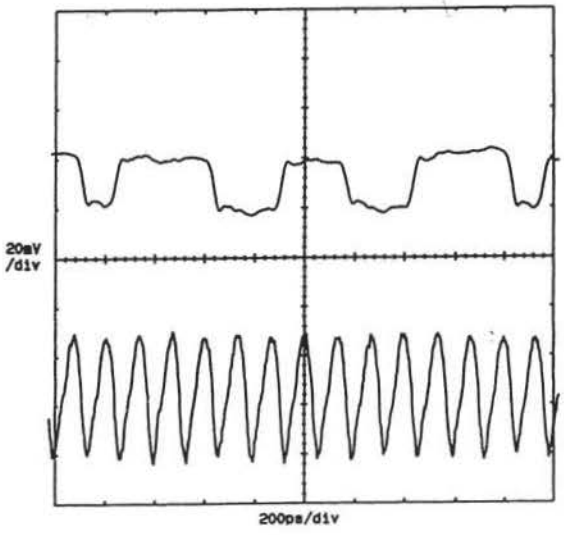


Fig. 4 Input (top) and output (bottom) signal waveforms of the 7.5 Gb/s CR.