Microelectronic Engineering 15 (1991) 327–330
Elsevier

A 2.5 ns 8x8-b Parallel Multiplier Using 0.5 μm GaAs/GaAlAs Heterostructure Field Effect Transistors

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Abstract

To increase performance of GaAs LSI digital circuits, a 0.5 μm recessed gate process has been developed and utilized for an 8x8-b parallel multiplier. The chip contains about 3000 heterostructure field effect transistors and has a power consumption of 1.5 W. The best results of the maximum multiplication time measured were below 2.5 nsec.

1. INTRODUCTION

There is a continual need for increasing the speed of integrated circuits. For VLSI densities, extreme low power consumption of the logic cells is crucial. Although silicon ECL delivers GHz clock rates, power consumption is a limiting factor for integration. A promising candidate for extreme high-speed, low power digital circuits is the GaAs/AlGaAs heterostructure field effect transistor. Using an advanced E/D recessed gate process [1] with 0.5 μm gate length, unloaded gate delays of 25 psec are obtained with direct-coupled FET logic (DCFL) inverters. To demonstrate integration complexity and the excellent speed-power product of this technology, an 8x8-b multiplier was designed and fabricated using half micron gates.

2. CIRCUIT DESIGN AND SIMULATION

The basic cells of the circuit such as inverters, NOR gates and push-pull output drivers have been optimized with using an adapted SPICE model. The simulation results have been verified by measuring ring oscillators with various fan-ins and fan-outs. Due to the strong dependency of the gate delay of DCFL gates upon the load which has to be driven, the use of super buffered FET logic (SBFL) is advantageous at fan-outs higher than four. The width ratio of the enhancement to depletion type transistor is 2:1. The data used for simulation are summarized in Table 1.

25	psec	fan-in=fan-out=1
3,5	psec	per fan-in
19	psec	per fan-out
34	psec	per mm 1. Metal 3 μm width
27	psec	per mm 2. Metal 5 μm width

Table 1. Gate delays used for logic simulation.

The complete logic is built up using inverters and NOR gates with four or less inputs. To simplify layout, the full and half adder cells are designed as button cells, which wires the core of the multiplier automatically. The block diagram of the 8x8-b parallel multiplier is shown in Figure 1.

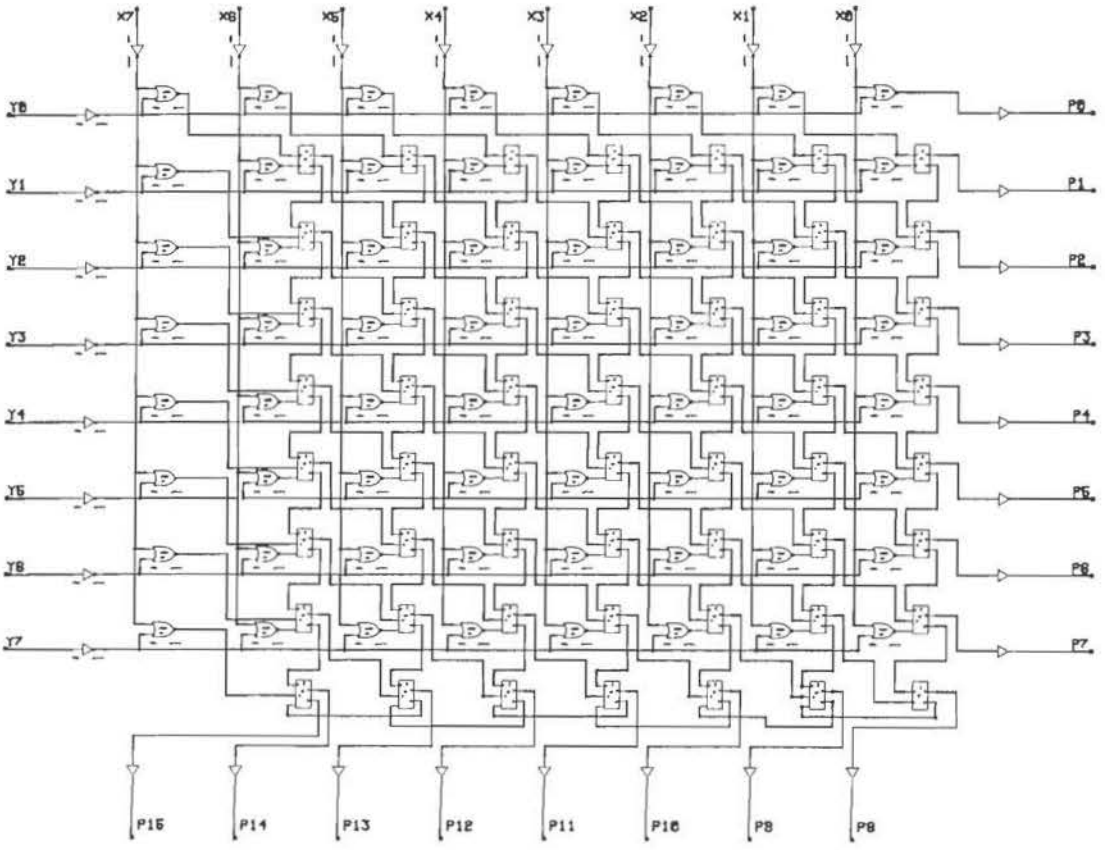

Figure 1. Logic schematic of the 8x8-b parallel multiplier.

The straightforward carry save architecture was chosen for its modular structure and repetetive layout. The multiplier consists of 48 full adders and 8 half adders. An on-chip self-test was implemented by an additional feedback inverter from P15 to Y0. By ap-

plying logical high to the highest Y and all X input pins, the multiplier oscillates at the highest output pin. The oscillation frequency is determined by the longest path through the multiplier. Thus the worst case multiplication time can easily be measured by this oscillation mode.

3. RESULTS

The chip size is 2.0x2.0 mm^2 and contains about 3000 transistors. At a supply voltage of 1.5 volts, the power dissipation is below 1.5 W. The functional tests are performed in the MHz range using standard digital test equipment. A yield of 10 % of fully functional chips was achieved on 2 inch wafers. The high speed testing was done using the oscillating mode. Best results show a maximum multiplication time of less than 2.5 nsec as shown in Figure 2.

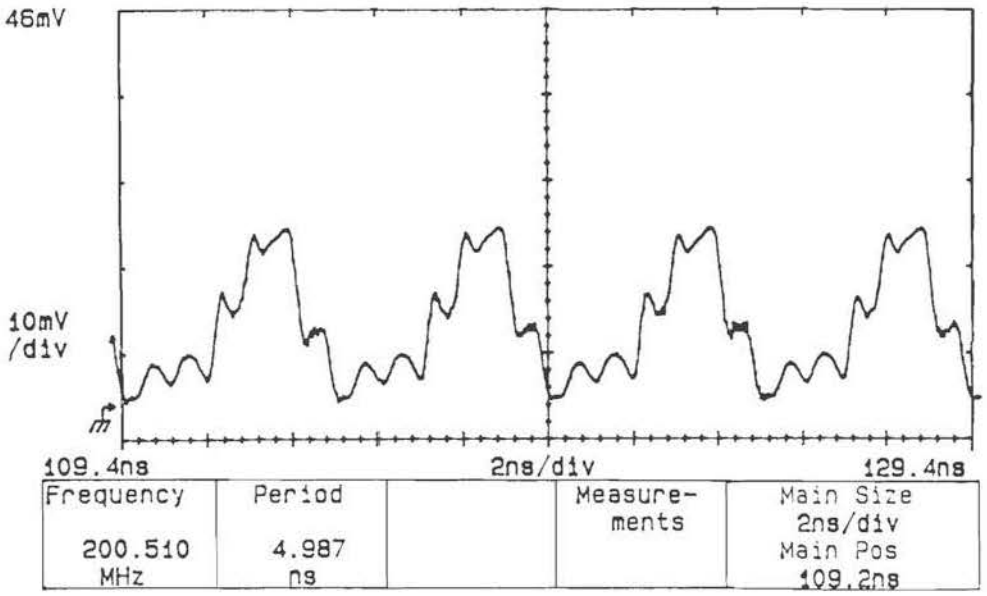

Figure 2. MSB output signal of the 8x8-b multiplier in the self-test oscillation modus.

Further improvements can be achieved by reduction of the gate length of the heterostructure field effect transistors. Figure 3 presents the gate delay of unloaded ring oscillators with 53 stages and varying gate length. For half micron inverters, a delay per stage of 25 psec was measured. Ring oscillators with a gate length of 0.3 μm show a typical gate delay of 16 psec per stage. First results on 0.2 μm ring oscillators deliver a typical delay of 11 psec with best values even below 10 psec at room temperature. These results

indicate that flash multipliers with less than 1 nsec multiplication time can be fabricated in the near future.

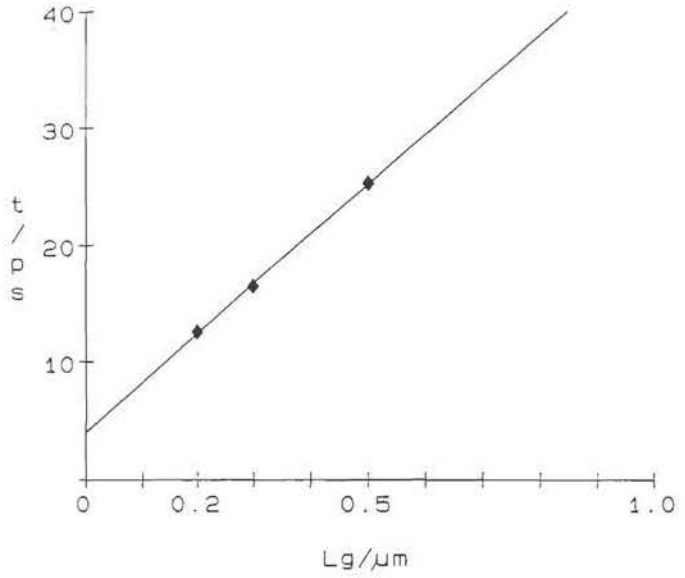

Figure 3. Gate length dependency of unloaded inverter gate delay.

4. CONCLUSION

Using an advanced E/D recessed gate process with 0.5 μm gate length heterostructure field effect transistors, an 8x8-b parallel multiplier has been designed and fabricated. A 10 % yield of fully functional chips has been achieved on 2 inch wafers. The maximum multiplication time was measured below 2.5 nsec for the best devices with a power consumption of 1.5 W. These results demonstrate the high-speed, low power performance of GaAs LSI circuits.

ACKNOWLEDGEMENT

The financial support of the Bundesministerium für Forschung und Technologie through the GAE-project NT2778 is gratefully acknowledged.

REFERENCES

[1] A. Hülsmann, G. Kaufel, K. Köhler, B. Raynor, J. Schneider, and T. Jakobus, Jpn. J. Appl. Phys., 29, 2317 (1990).