18 Gbit/s MONOLITHICALLY INTEGRATED 2:1 MULTIPLEXER AND LASER DRIVING USING 0·3 μm GATE LENGTH QUANTUM WELL HEMTs

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A monolithically integrated 2:1 multiplexer and laser diode driver was developed, using AlGaAs quantum well HEMTs of 0·3 μm gate length. The DC and modulation current is 25 and 45 mA, respectively. Open eye diagrams were measured at bit rates up to 18 Gbit/s with pseudorandom data streams.

Introduction: Monolithically integrated high speed optical transmitters are encouraging for future optical communication systems. Last year we successfully developed a 20 Gbit/s 2:1 multiplexer (MUX) IC [1] and a 15 Gbit/s laser diode driver (LDD) IC [2]. Based on the results obtained with those two ICs, we have recently designed and realised a monolithically integrated 2:1 MUX and LDD (MUXLDD). With this MUXLDD and the high-speed laser diode developed also at our institute [3], we are close to realising the aim of a monolithically integrated optical transmitter.

Circuit design: The circuit diagram of the MUXLDD is shown in Fig. 1. The 2:1 MUX consists of a logic part with

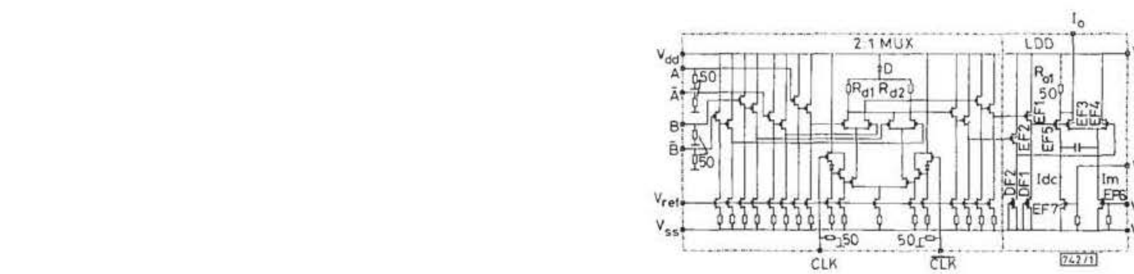

Fig. 1 *Circuit diagram of MUXLDD*

two high speed, alternatively closed switches. To speed up the switch process and to reduce the crosstalk, the differential input form was used for both input data signals and the clock signal of the MUX. For each input signal, two stage source followers were used as buffers. The three stage source followers between the MUX and LDD have two functions: they act as a buffer and, together with the diode D over R_{d1} and R_{d2}, offer a high enough voltage drop, so that EF_3 and EF_5 do not suffer from saturation.

In the LDD part a capacitively coupled current amplifier (C^3A) was introduced to speed up the switchoff process of the laser diode (LD), as in Reference 2. The circuit itself, nevertheless, was improved by merging half of the C^3A into the conventional current amplifier. The current I_{dc} serves both as the bias current of EF_5, and as a DC supply to the driven LD. Owing to this concept, a more ideal waveform of the output signal was obtained, as shown in Fig. 2. The undesired amplitude increase of the output signal of the LDD in Reference 2 was removed.

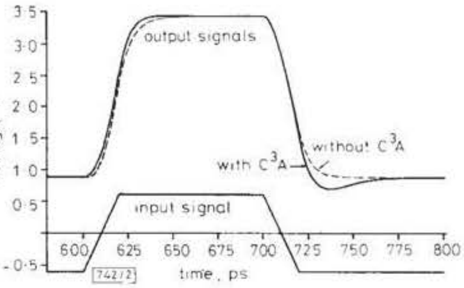

Fig. 2 *Simulated waveforms of LDD with C^3A and same circuit without C^3A, at 10 Gbit/s*

The high speed test of the MUXLDD had to be carried out with a 50 Ω measurement setup. To simulate the load condition with low-ohmic LDs, an additional 50 Ω load resistor was laid out on-chip from the supply voltage V_{DD} through an air bridge to the output of the LDD. If an LD is to be connected, the resistor can be disconnected by breaking the air bridge off. To reduce the Miller effect, the unused side of the output stage, i.e. the drain of EF_4, was directly connected to the supply voltage V_{DD} on chip.

Fabrication: The photomicrograph of the 1 × 1 mm² chip is shown in Fig. 3. The quantum well HEMTs were fabricated

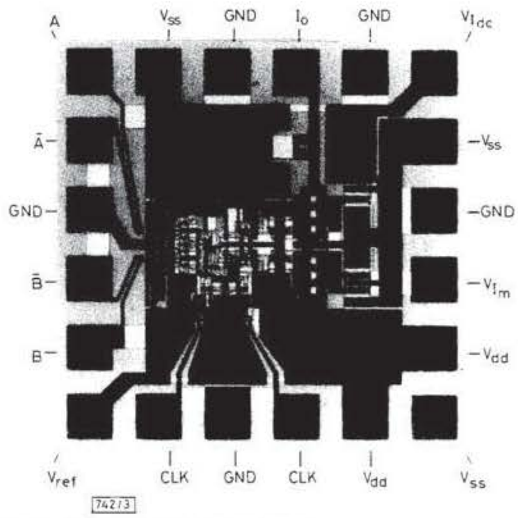

Fig. 3 *Photomicrograph of MUXLDD chip*

using epitaxial GaAs/AlGaAs layers grown by MBE. Both enhancement and depletion mode HEMTs were processed on the same wafer using reactive ion etching for the gate recess. 0·3 μm long gates were obtained by electron beam direct writing. The enhancement HEMTs typically exhibit a maximum transconductance of 500 mS/mm, a maximum drain current of more than 180 mA/mm and a transit frequency of ~45 GHz. NiCr resistors and MIM capacitors were used for passive devices [4, 5].

Measurement results: The chips were measured on-wafer using 50 Ω coplanar test probes. The maximum DC and modulation output current was equal to 25 and 45 mA, respectively. The total DC current and power consumption at maximum output current were ~120 mA and 600 mW, respectively. For dynamic measuring, an Anritsu 10 Gbit/s data generator with *data* and *data* outputs and a Tektronix 11801A oscilloscope were used. Open eye diagrams were obtained at bit rates up to 18 Gbit/s with a pseudorandom data stream of length $2^{23} - 1$, as shown in Fig. 4. With a data stream of a 31 bit-long fixed pattern, the maximum bit rate was able to increase up to 20 Gbit/s as shown in Fig. 5. The large-signal bandwidth of the same LDD on a separate chip was ~10 GHz.

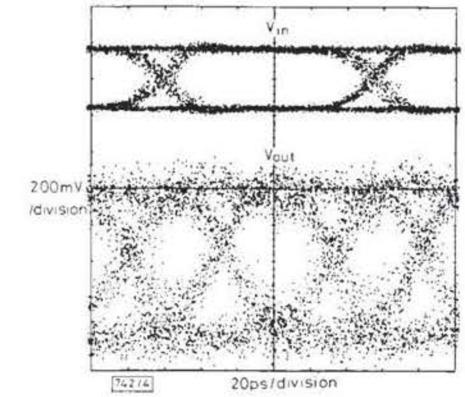

Fig. 4 *Eye diagrams of input and output signals at 18 Gbit/s with pseudorandom data stream of length $2^{23} - 1$*

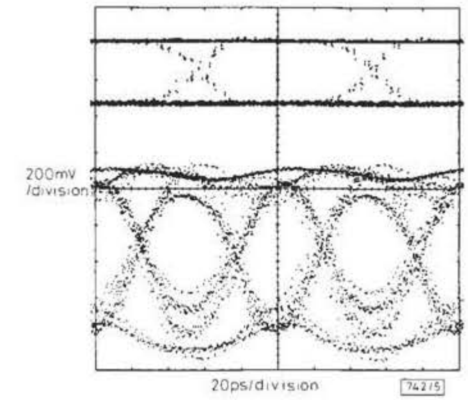

Fig. 5 *Eye diagrams of input and output signals at 20 Gbit/s with data stream of 31 bit-long fixed pattern*

Conclusion: We have designed, fabricated and tested a monolithically integrated 2 : 1 multiplexer and laser driver IC using AlGaAs/GaAs quantum well HEMTs. The maximum output DC and modulation current was 25 and 45 mA, respectively. Open eye diagrams were measured at bit rates up to 18 Gbit/s with a pseudorandom data stream and up to 20 Gbit/s with a data stream of a 31 bit-long fixed pattern.

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