Technology and Physics

Of

Gate Recessed GaN/AlGaN FETs

Masters Thesis
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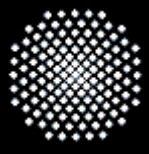

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My Affections,

To my loving parents who always provided me a shelter under strong sun shines;
My brothers who are my arms of strength, courage and directors;
A precious gift of God, My sisters

Adil Mahmood MALIK

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Chapter 1

Introduction

Gallium Nitride (GaN), a wide band gap semiconductor, gained importance as Heterostructure Field Effect Transistors (HFET) in the early 90s. The fabrication of first HFET [1.1] opened a door for tremendous research over GaN FETs. Currently GaAs/AlGaAs Modulation Doped FETs (MODFET) are utilized with limitations in high power applications. The reason for such limitation is poor physical and electrical properties concerning to GaAs. But now a day GaN with astonishing features compared to GaAs for high power, electrical and optoelectrical devices is a hot topic of research. The reason is based on its interesting physical properties like thermal stability, high breakdown voltage, chemical inertness and electrical properties as well as a property of wide band gap which plays an important role in blue Lasers and devices with low noise. GaN High Electron Mobility Transistors (HEMTs) and MODFETs are important electrical devices for high speed electronics.

With the technological advent to control layer thickness in crystal growth by Metal Organic Vapor Phase Epitaxy (MOVPE) and Molecular Beam Epitaxy (MBE), HFET emerged with new horizons. Structures with different layers are grown and characterized. Group III-Nitride devices are highly promising for numerous applications. For the optical/display applications, LASERs and light emitting diodes (in the visible and UV emission range) are used [1.4, 1.5]. On the other hand

the electrical properties of gallium nitride are being utilized in order to fabricate the electrical devices that provide high performance e.g., field effect transistors working at high temperature, high frequencies or high power. Talking about field effect transistors grown over different substrates, *gate recess technology* is indeed important to have *better control over the channel*, *higher modulation speed*, etc. but, off course, it is a very difficult process step which needs high precision. Gate recessed HFETs are useful to reduce *pinch off voltage* and the gate leakage current of the device.

In this thesis "Technology and Physics of gate recessed GaN/AlGaN HFETs" some geometrical aspects of recess and gates are investigated. Additionally some problems of the recess technology e.g. etching defects, the control of recess etching depths, misalignments of recess will be discussed.

This thesis is divided into the following chapters,

Chapter 2 is mainly concerned with some of the most important physical properties of III-nitrides. An overview of different types of FET based on GaN is given in Chapter 3. The theoretical models which are used in this thesis are also illustrated.

Chapter 4 introduces the technology which is used to fabricate recessed gate GaN/AlGaN HFETs. A *recessed gate* is formed by etching the surface down and then deposition of gate metals in this region. Theoretically it is a way to improve control over the channel [1.3]. Etching is done with Electron Cyclotron Resonance-Reactive Ion Etching (ECR-RIE). Optical and e-beam Lithography is also discussed here.

Chapter 5 presents the results and discussion of realized recessed gate HFETs. Here basically characterization is done as a function of recess spacing (L_g), recess depth (t_{recess}), and source drain spacing. Transconductance, drain currents and source resistance are important parameters in transistor characteristics. HFETs with recessed gate fabricated, show good channel control as the transconductance is as high as 220 mS/mm with 250 nm T-gate and a shift in the pinch off voltage could be seen.

A detailed epitaxial layer structure and transistor layout is given in appendixes with process technology and instruments used.

Chapter 2

Group-III Nitrides

Gallium Nitride is a promising semiconductor for optical, electrical and opto-electrical applications because of its advantageous properties such as large energy bandgap, good thermal and chemical stability, and physical hardness.

2.1 -MATERIAL PROPERTIES

2.1-1 Crystal Structure

Group III Nitrides are usually found in Wurtzite (WZ), zinc blende and rock salt configurations. At ambient conditions, the thermodynamically stable structure is Wurtzite for bulk AlN, GaN, and InN and zinc blende for BN. The wurtzite structure has a hexagonal unit cell and thus two lattice constants, c and a shown in Fig. 2.1. The hexagonal unit cell contains 6 atoms of each type. The wurtzite structure consists of two interpenetrating hexagonal closed packed (HCP) sub lattices, each of one type of atom, offset along the c-axis by 5/8 of the cell height c.

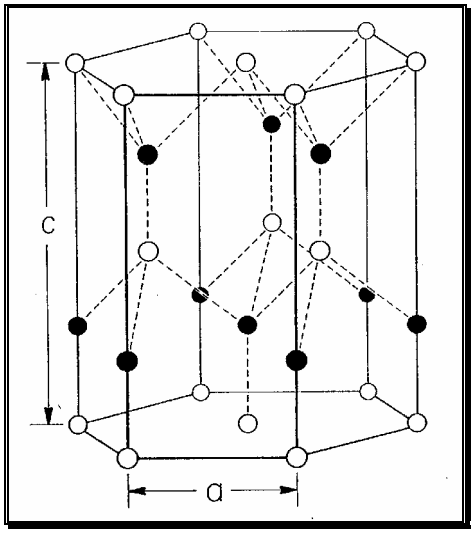


Fig. 2.1 *Crystal structure of Wurtzite GaN. Note that, for WZ-GaN lattice parameters (a and c) are 3.1892±0.0009 Å and 5.1850±0.0005Å respectively. [2.1]*

The zinc blende structure has a unit cell, containing four group III elements and four nitrogen elements Fig. 2.2a. The position of atoms within the unit cell is identical to the diamond crystal structure. Both structures consist of two interpenetrating face centered cubic (FCC) sub lattices, offset by one quarter of distance along a body diagonal. Each atom in the structure may be viewed as positioned at the center of a tetrahedron with its four neighbors defining the four corners of a tetrahedron (see Fig. 2.2b)

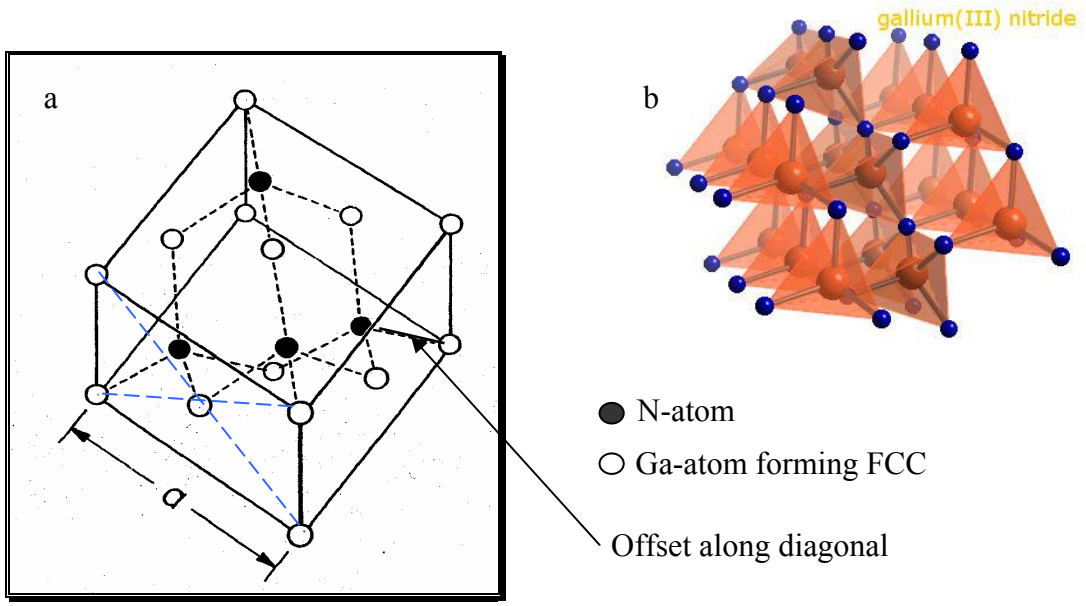


Fig. 2.2 *Crystal structure of a Zincblende configuration of GaN. (a) FCC unit cell. (b) View of tetrahedron structures of GaN in which each fourth atom (Ga) is shared with the second tetrahedron.*

The WZ and zincblende structures are similar. In both cases, each group III atom (Al, Ga, In) is coordinated by four nitrogen atoms; conversely, each nitrogen atom is coordinated by four group III atoms. The main difference between these two structures is in the stacking sequence of closest packed diatomic planes. For WZ, the stacking sequence of (0001) planes is in <0001> direction and for zinc blende the stacking sequence of (111) planes is in <111> direction. The difference in both structures can be seen by viewing along a chemical bond in the <111> or <0001> (c-axis) direction: the second nearest neighbors are staggered in zinc blende crystal but are eclipsed in the WZ (Fig 2.3). All group III-Nitrogen bond lengths are equivalent in the zinc blende structures but there are slightly differing III-Nitrogen bond lengths in the wurtzite structures. [2.2]

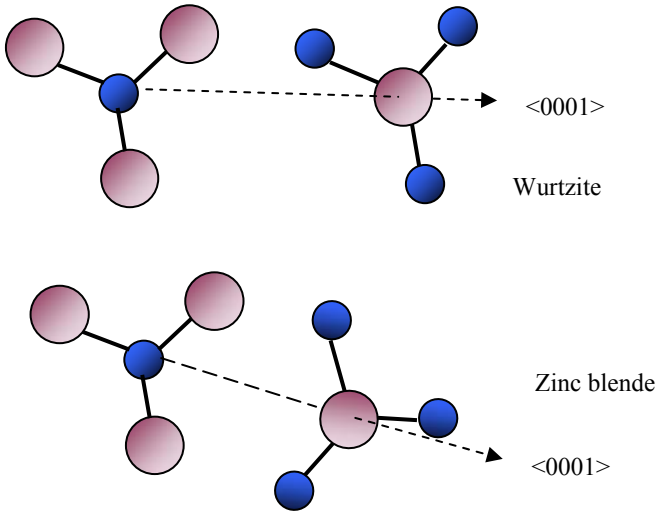


Fig. 2.3 *A comparison of bonds between closed packed planes for the crystal structures. In the WZ there is an eclipsed bond configuration while in the zinc blende the bond configuration is staggered.[2.2]*

2.2 ELECTRICAL PROPERTIES

2.2-1 Polarization

It is now widely recognized that built in electric fields due to polarization-induced charges play an important role in the electrical and optical properties of Nitride heterostructures grown in [0001] orientation. These fields also provide a source of a 2-dimensional electron gas in AlGaN/GaN heterostructures. In HFETs, the understanding and controlling of the source of electrons is important for the optimization of their performance.

2.2-1.1 Spontaneous Polarization

Due to strong electronegativity of Nitrogen (3) compared to Al (1.5), Ga (1.6) and In (1.7) the binding electron is attracted towards N in III- Nitrides. This results in deformation of regular tetrahedral structure as the c/a becomes smaller than that of an ideal tetrahedral one (c/a = 1.633). So we experience a spontaneous polarization without applying external electric field. The coefficient of spontaneous polarization can be determined theoretically from [2.3].

For AlGaN the spontaneous polarization is [2.4],

$$P_{SP} = (-0.052x - 0.0029)\left[\frac{C}{m^2}\right] \qquad (2.1)$$

Where x is the aluminium concentration. These field polarizations are compensated by the inner free electrons but for a bi-layer (two materials) system, there will be a local surface charge [2.5].

$$\Delta P = P_{SP}^{2} - P_{SP}^{1} = \sigma \qquad (2.2)$$

σ is surface charge density at the interface of the two systems with polarization P_{sp}^{1} and P_{sp}^{2} respectively.

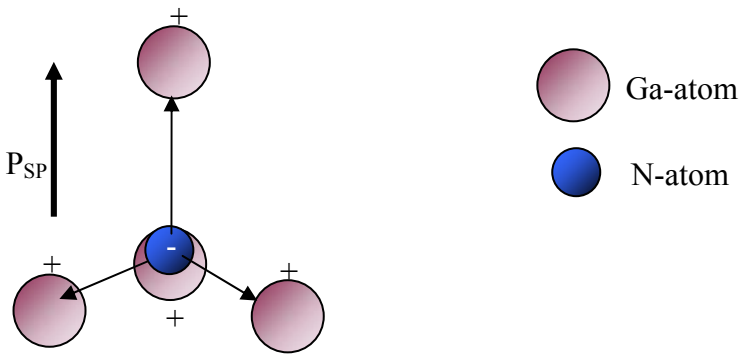


Fig. 2.4 *Spontaneous polarization in GaN*

2.2-1.2 Piezoelectric Polarization

This is due to mechanical stress in a crystal. In AlGaN the lattice constant a_0, is smaller than that of GaN, therefore GaN experiences a tensile stress (if a heterostructure is made from GaN and AlGaN), changing the bond angles and lattice constants from the non-stressed or stress free values. The piezoelectric polarization in the direction of c-plane is given by [2.4]

$$P_{PE} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{c_{13}}{c_{33}}) \qquad (2.3)$$

Strain experienced in the bi-layer system with substrate lattice constant a_0 and cover lattice constant a.

Where a is the lattice constant in the strained case and a_0 is the relaxed lattice constants. The piezoelectric coefficients e_{ij} and elastic constants c_{ij} can be determined from the table of constants. With the polarization effects, surface states and the density of 2DEG at interface can be increased or decreased [2.7], [2.8].

2.3 GROWTH OF GaN LAYERS

The high melting temperatures and dissociation pressures are the main obstacles in obtaining large single crystals of III-N compounds, which can serve as substrates for the homoepitaxial growth (when a material is grown epitaxial on a substrate of the same material). Therefore, III-V films have been grown heteroepitaxially (if the layer and the substrate are different materials, like GaN on SiC, GaN on Sapphire, GaN on Si) on a number of substrates [2.9], [2.20-23] which match more or less close to the lattice constants and thermal expansion coefficient of III-V nitrides. [2.10].

Recent technology named Metal Organic Vapor Phase Epitaxy (MOVPE) is used to grow GaN layers (GaN, AlGaN or doped AlGaN) over substrate of Sapphire (Al_2O_3). Fig. 2.5 shows a schematic representation for the process of crystal growth.

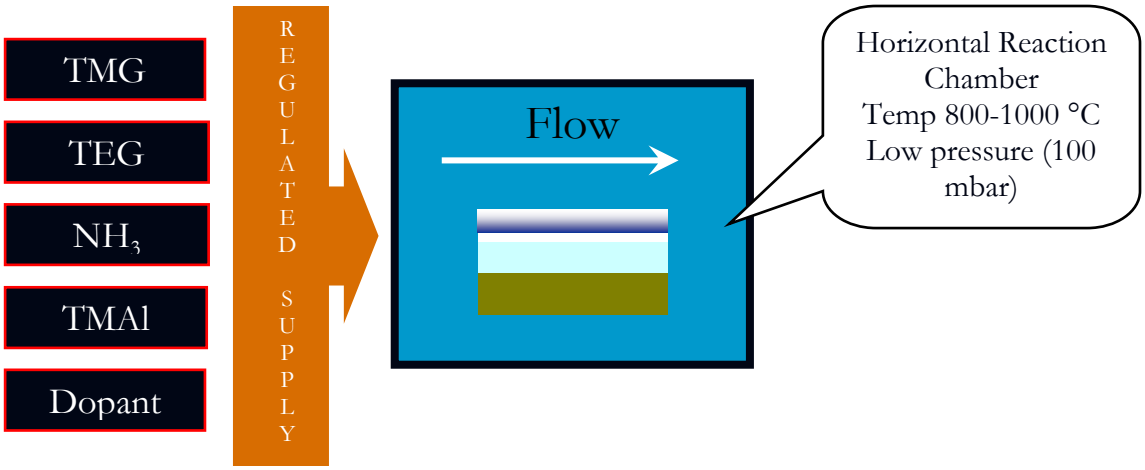


Fig. 2.5 *A schematic diagram of MOVPE for GaN layer growth.*

In Fig. 2.5 the components (elements) of III-N semiconductor are in the form of gases transported to the substrate in the reaction chamber. Ammonia (NH_3) with carrier gasses like H_2 or N_2 is injected into the Reactor. Group III elements are fed into the reactor in the form of metal organic compounds like Tri Methyl Gallium TMG [$(CH_3)_3Ga$] or Tri Ethyl Gallium TEG [$(C_2H_5)_3Ga$]. At a high temperature (800-1000 °C) [2.11], [2.12] in the reaction chamber, metal organic compound reacts with the N_2 to form a layer of GaN over sapphire substrate.

With MOVPE a very thin (tens of nanometers) GaN or AlN low-temperature *buffer layer* is grown between the substrate and epitaxial layer in order to

- Reduce the lattice and thermal mismatch.
- To promote nucleation sites for the layers grown over the substrate.
- The buffer layer decreases interfacial free energy, permitting two-dimensional growth of the III-N layer.
- The most important development is the discovery that AlN and GaN buffers lead to significant improvements in surface morphology and the electrical properties of the films [2.13].

2.3-1 Sapphire (Al_2O_3)

Sapphire was a first standard substrate on which GaN was epitaxially grown and remains the most frequently used substrate for GaN epitaxial growth so far [2.9],[2.23], mostly due to its low price, the availability of large-area crystal of good quality and its transparent nature.

For device application the structural quality of the epitaxial films is very important, since dislocations, stacking faults and other extended defects may significantly reduce carrier life times and consequently device efficiency. Defects originate due to large thermal mismatch between the nitrides and their substrate materials, most epitaxial nitride films are subject to some degree of strain, which is introduced during the post cooling. Stacking faults are a common form of a strain relaxation in face-centered cubic crystals. The most seen defect represents dislocations, which are formed in the epitaxial layer to reduce the lattice mismatch and the strain of postgrowth cooling. These dislocations are also a result of thermal expansion mismatch that is propagated through all layers [2.10].

2.3-2 Doping with Si

Controlled n-type conductivity in GaN is generally achieved by Si doping. Si substitutes Ga atoms in the lattice, providing a loosely bounded electron. The ionization energy of the Si level (temperature dependent) in GaN was reported approx. 27 meV [2.14], [2.15] and 12-17 meV as measured by Hall Effect [2.16]. The solubility of Si in GaN is high, of the order of 10^{20} cm $^{-3}$. Therefore, Si is suitable for III-Nitrides doping and most frequently used [2.10].

The thicknesses of Si doped AlGaN spacer layers of samples we used to fabricate HFET/MODFET are given in Tab. [2.1] and the layer structure is shown in appendix A.

Sample	Doping	Thickness of Doped AlGaN layer (≈ nm)	Thickness of AlGaN layer (≈ nm)
HB3869 b, c, d	-	-	-
HB3874	Si	15	15
HB3876	Si	15	35
HB3877	Si	5	45

Table 2.1 *Samples and doped layer thickness.*

2.4 GaN AND OTHER III-Nitrides

Table (2.2, 2.3, and 2.4) shows some useful information regarding to GaN and other III-Nitrides. GaN is a mostly favored semiconductor as its promising properties are suitable for both electrical (FETs, BJTs) and optoelectrical device (LD, LEDs). The use of GaN is due to its wide band gap, high electron velocity and high break down voltages.

Properties of GaN		
Wurtzitic polytype		
Band gap	3.39 eV at 300K	3.50 eV at 1.6K
Lattice constants	a = 3.189Å	c =5.185 Å
Thermal expansion	5.59×10^{-6}/K	3.17×10^{-6}/K
Thermal conductivity	1.3 W/cmK	
Index of refraction	n (1eV) = 2.33	n (3.38) = 2.67
Dielectric constants	$\varepsilon_0 = 10$	$\varepsilon_\infty = 5.5$
Zinc blende polytype		
Band gap energy	3.2-3.3 eV at 300K	
Lattice constant	a = 4.52	
Index of refraction	n (3eV) = 2.9	

Tab. 2.2 *Properties of GaN, source: [2.10]*

The breakdown voltage for GaN is > 70 V, compared to that of GaAs 30V [2.19]. The saturation velocity of carriers is nearly 2×10^7 cm/sec which is higher than that of GaAs [2.17]. Another interesting feature of GaN/AlGaN over GaAs/AlGaAs system is the large band gap discontinuity (discussed in chapter 3).

Properties of AlN		
Wurtzitic polytype		
Band gap	6.2 eV at 300K	6.28 eV at 5K
Lattice constants	a = 3.112Å, c =4.982 Å	
Thermal expansion	4.2×10^{-6} /K	5.3×10^{-6} /K
Thermal conductivity	2 W/cmK	
Dielectric constants	$\varepsilon_0 = 8.5$	$\varepsilon_\infty = 4.68$- 4.84
Zincblendee polytype		
Band gap energy	5.11 eV at 300K *theory*	
Lattice constant	a = 4.38 Å	

Tab.2.3 *Properties of AlN; source [2.10]*

Properties of InN		
Wurtzitic polytype		
Band gap	1.89 eV at 300K	
Lattice constants	a = 3.548Å	c =760 Å
Thermal expansion	4.2×10^{-6} /K	5.3×10^{-6} /K
Thermal conductivity	2 W/cmK	
Dielectric constants	$\varepsilon_0 = 15.3$	$\varepsilon_\infty = 8.4$
Zincblendee polytype		
Band gap energy	2.2 eV at 300K *theory*	
Lattice constant	a = 4.98 Å	

Tab. 2.4 *Properties of InN; source [2.10]*

Impressive progress in the development of GaN/AlGaN materials and devices for high power, high temperature application was obtained during the past few years. Record microwave power of 6.8 W/mm, as well as high temperature and low noise performance of GaN/AlGaN HFET have been demonstrated [2.18].

Chapter 3

GaN FETs

A *Field Effect Transistor* is an important device in electrical application. It is worthy to mention that a FET as a uni-polar device and there is only one type of carrier in the conducting channel. Off course, this enhances the mobility of the carriers and efficiency of the structure compared to a bipolar transistor. The reason is manifold, like recombination of holes and electrons, inter scattering and diffusion of carriers, etc...

3.1- FAMILY OF GaN FETs

Because it is easy to grow vertical structure for FET using GaN, we see following types of FETs using gallium nitride.

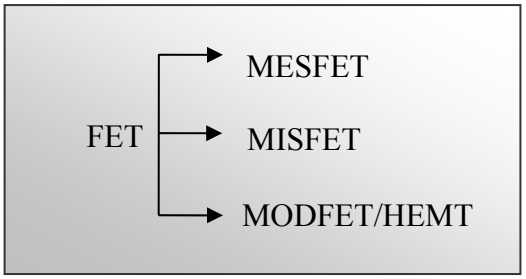


Fig. 3.1: *Family of FET which could be fabricated using Gallium Nitride.*

3.1-1 MESFET

Fig. 3.2 shows a typical n-channel MESFET-Structure. The name, **Me**tal **S**emiconductor **FET** is given because *a metallic gate is directly deposited on the surface of semiconductor*. The n-channel is from 200- 600 nm thick, Si-doped and it is modulated by the gate contact (by the barrier potential Φ_b that creates depletion region of Schottky diode) which is typically Pt/Au or Ni/Au. The carrier concentration in the channel is of the order of 10^{17} cm^{-3}. The first field effect transistor from GaN was a MESFET from M. A. Khan. [1.1]

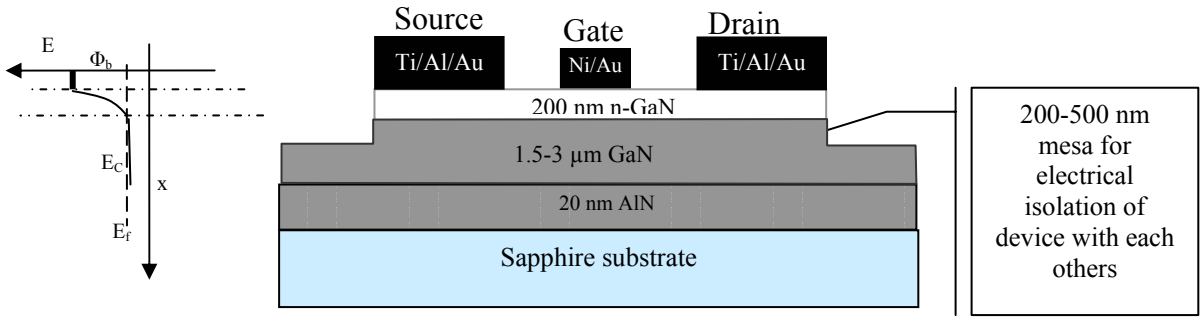


Fig. 3.2: *A Schematic diagram for GaN MESFET. Note that mesa is necessary for all structure fabrication. Ohmic contacts and gate is directly metallized over the surface of semiconductor. At the left side a conduction band diagram for MESFET is shown.*

3.1-2 MISFET

M**etal **I**nsulator **S**emiconductor **FET, shown in Fig.3.3 an insulator layer (usually silicon nitride or silicon oxide) is used to make the gate contact. It is necessary to reduce the injection of carrier through the gate barrier. Metal Oxide Semiconductor FET (MOSFET) is a good example of MISFET as metal oxides beneath the gate play an important role of insulation.

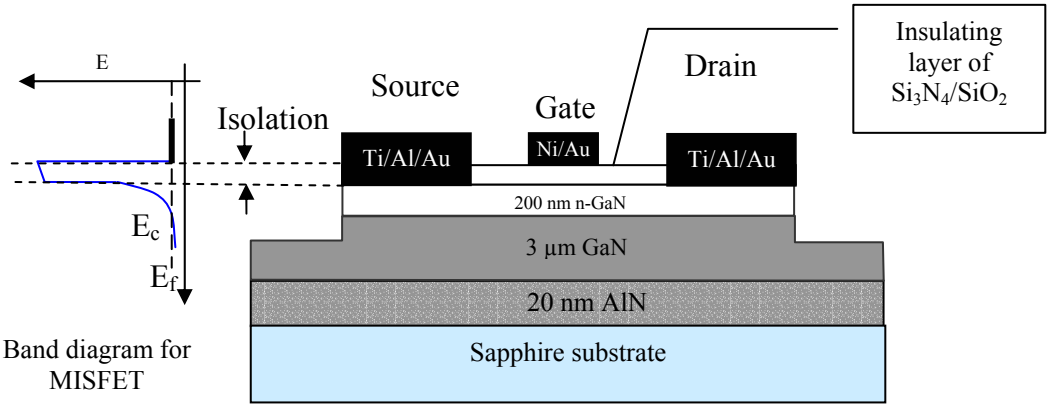


Fig. 3.3: *Schematic diagram of MISFET. Note that only ohmic contacts are metallized over the surface of semiconductor where as gate contact is isolated by oxide layers.*

In Fig. 3.3 a band diagram for MISFET is shown. The conduction band moves towards E_f or crosses it in enhancement mode, with the applied gate voltage and determines the flow of current (carriers) through the active channel of the transistor.

3.1-3 HEMTs and MODFETs

A class of Heterostructure FETs (HFETs) named **H**igh **E**lectron **M**obility **T**ransistor (HEMT) is obtained when the channel layer is doped to spatially separates ionized donors form the electrons in the 2DEG, leading to enhanced channel mobility [3.2] Fig. 3.4. The coulomb interaction between electrons and donors in n+ AlGaN layer is reduced resulting higher mobility of the physically separated electrons. At present the maximum mobility recorded is nearly 1700 cm^2/Vsec with carrier density $1\times10^{13}/cm^2$ [3.3] for the samples grown by MOVPE.

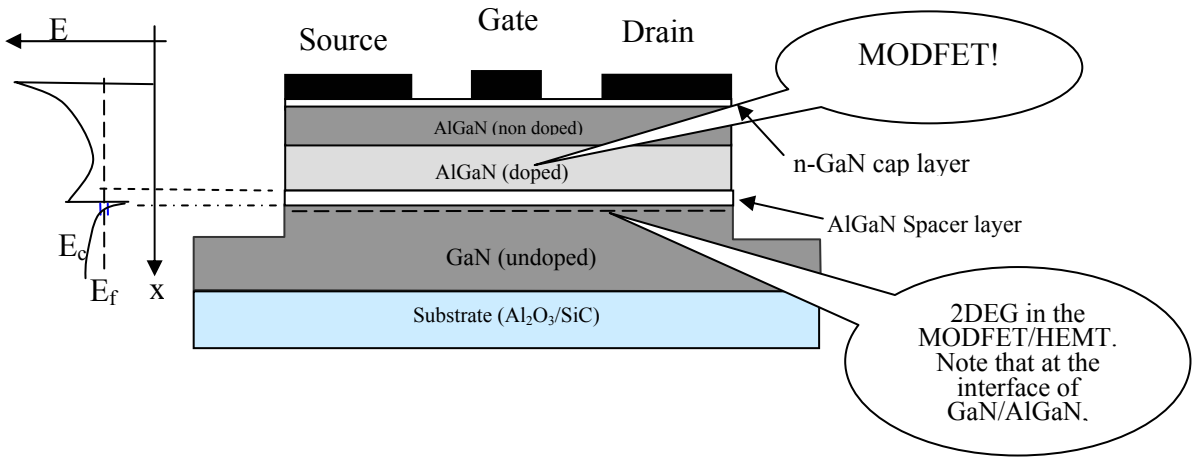


Fig. 3.4 *Layer structure for GaN MODFET/HEMT. In a sense HEMT is also called PI-HEMT as there is polarization induction.*

Modulation-doped **T**ransistor (MODFET) is another kind of field effect transistor that can be grown on GaN. As described above, the semiconductor layer needs to be doped with n-type impurities to generate more electrons in the layer. However, this procedure causes the electrons to slow down because they end up colliding with the impurities residing in the same region that were used to generate them in the first place. MODFET is a smart device to resolve this contradiction because in the MODFET the electrons are additionally separated in a confinement layer e.g. InGaN layer with high mobility.

A MODFET accomplishes this by use of high mobility electrons generated using the *hetero-junction* of a thin doped AlGaN layer or a thin InGaN layer and a GaN layer. The electrons generated in AlGaN drop completely into the next GaN layer to form a depleted AlGaN layer, because the hetero-junction created by different band-gap material forms a steep canyon in the

GaN side where *the electrons can move quickly without colliding with any impurities*. (For the details of 2DEG see section 3.2.)

The advantage of the GaN/AlGaN system is in the availability of more band gap discontinuity. This leads to higher mobility and also provides a dense 2DEG (> 10^{13} cm^{-2}) because of the availability of more density of states [1.3], compared to band gap discontinuity of GaAs/AlGaAs system that gives only 10^{12} cm^{-2} carriers. Real spatially transferring of hot electrons from channel to barrier is negligible for GaN systems. Injection from the gate contact is also reduced by the larger Schottky barrier height. Formation of 2DEG in GaN/AlGaN interface is due to electron affinity and bandgap discontinuity. AlGaN is wider in bandgap (lower electron affinity) compared to the bandgap of GaN (high electron affinity). See more details in next section.

3.2 HETERO STRUCTURE $GaN/Al_xGa_{1-x}N$ FET

A Hetero Structure is a structure grown with semiconductors of different energy band gaps. Using nice compromising features of GaN and AlGaN for 2DEG (two dimensional Electron Gas at the interface of GaN/AlGaN interface as already discussed in chapter 2), High electron mobility transistor can be fabricated.

3.2-1 Theoretical background

GaN and AlGaN are two different semiconductors as differing in their band gaps. $GaN/Al_xGa_{1-x}N$ Heterostructure is grown as Wurtzite AlGaN layer over Wurtzite GaN substrate. The type I band alignment (in which the discontinuities conduction band and valance band are at same **k**) between AlGaN and GaN has been shown to form a potential well and a Two Dimensional Electron Gas (2DEG) at the heterointerface [1.3], [3.4]. When these materials are brought into contact, thermal equilibrium requires alignment of their respective Fermi levels (E_f). This induces conduction (E_c) and valence (E_v) band bending in both the AlGaN and GaN layers and can cause the GaN conduction band at the interface to drop below E_f. Since (for n- type material) the Fermi level can be viewed as an electrochemical potential for electrons, majority electrons will accumulate in the narrow gap material just below the heterointerface to fill the *quasi triangular potential well* between E_c and E_f.

The electrons are confined by a distance shorter than their deBroglie wavelength, causing quantization of allowed energy levels in the potential well. Depending on the structures, there may be more than one allowed energy levels below E_f, although only the lowest allowed level

will be substantially populated at room temperature. With the heterointerface on one side and a potential barrier on the other, electrons in the 2DEG are only free to move along the plane of the interface. A thin 'Sheet' of negatively charged (electrons) is formed responsible for the electrical transport. Fig. 3.5 a, b shows a schematic layer structure and band diagram with triangular quantum well formation.

3.2-2 The Two-Dimensional Electron Gas (2DEG) in GaN/AlGaN

In order to obtain the 2DEG concentration in the triangular QW at the interface of GaN/AlGaN, Poisson's Eq (3.1) and Schrödinger's Eq (3.2) are solved self consistently [1.3].

$$\frac{d^2E_c}{dz^2} = -8\pi n(z) \tag{3.1}$$

$$-\frac{\hbar^2}{2m^*}\frac{d^2\psi_i}{dz^2} + E_c(z)\psi_i = E_i\psi_i \tag{3.2}$$

Where *z* is the coordinate in a direction perpendicular to the *i-AlGaN/i-GaN* heterostructure with origin at the *i-AlGaN/i-GaN* heterointerface, positive values in the *i-GaN* active layer, and negative values are in *i-AlGaN* layer. As shown in Fig 3.5b the $E_c(z)$ is the conduction band position, Ψ_i is the wave function of the electron, m* is the effective mass of the electron in GaN, n(z) is the electronic concentration at point *z* , *h* is the Planck's constant.

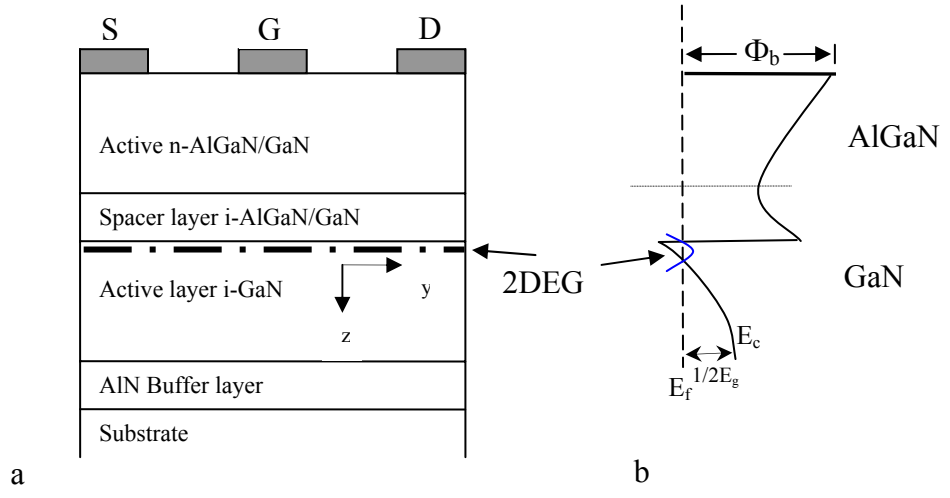


Fig. 3.5: *(a) The layer sequence in GaN/AlGaN HFETs. (b) Quantum Well formation at the band edge discontinuity, and creation of 2DEG.*

A simultaneous solution of Eq. (3.1) and Eq. (3.2) thus gives the concentration of electrons *n(z)* at various locations along the width of the triangular Quantum well. When unintentionally doped, GaN shows a donor implanted behavior. However, these donors don't affect the 2DEG concentration, because most of them are not ionized at the interface, owing to the Fermi level lying above the conduction band. If, for the sake of convenience, the origin of the energy is chosen at the edge of conduction band level of GaN at the GaN/$Al_xGa_{1-x}N$ interface, and if the unintentional donor concentration in the bulk of GaN is accounted for, then the first boundary condition may be written as

$$E_c\left(z \to +\infty\right) = E_F + \tfrac{1}{2} E_g \tag{3.3a}$$

which is plotted in Fig. 3.5b

or

$$E_c\left(z \to +\infty\right) = E_F + k_B T \ln\left(\frac{N_c}{N_d}\right) \tag{3.3b}$$

Where N_c is the effective electron density of states, N_d is the donor impurity density in the bulk GaN, E_f is the Fermi level, and E_g is the energy band gap, all for GaN. Note that for practical situation, this boundary condition affects the 2DEG concentration. The two other conditions are

$$\left(\frac{dE_c}{dz}\right)_{z=0} = 8\pi n_{2D} \tag{3.4a}$$

$$\psi_i\left(z \to \pm\infty\right) = 0 \tag{3.4b}$$

Where n_{2D} is the 2DEG. The value of the electron concentration at the point *z*, *n(z)* is given as,

$$n(z) = \sum_{i=1}^{\infty} N_i \left|\psi_i(z)\right|^2 \tag{3.5}$$

Where,

$$N_i = \frac{k_B T}{2\pi} \ln\left[1 + \exp\left(\frac{E_F - E_i}{k_B T}\right)\right] \tag{3.6}$$

Equations (3.1) and (3.2) are solved using trial wave function of the form

$$\phi_n(z) = \left(z + z_0\right) e^{-b_n z} \text{ For } z \geq 0 \tag{3.7a}$$

$$\phi_n(z) = z_0 e^{\left(\frac{1}{z_0} - b_n\right)z} \quad \text{For } z < 0 \tag{3.7b}$$

The wave function is obtained by employing Eq.(3.8) with C^i_v as a variation parameter

$$\psi_i = \sum_{v=1}^{\infty} C_v^i \phi_v \tag{3.8}$$

Although theoretically the summation series of Eq.(3.5) and (3.8) can extend up to infinity, a value of $v = 10$ appears to be sufficient for self-consistency. This calculation, for a given 2DEG concentration, yields the conduction band, the Fermi level (also the quasi Fermi level of the electrons), the energy levels of the electrons in the triangular well, and the electronic concentration as a function of z. The drain current and the transconductance can also be calculated [1.3]. One can extract from this mathematical model the information about the 2DEG as a function of gate voltage, the transconductance with different thickness of $Al_xGa_{1-x}N$ layer, where x is the concentration of Aluminum. For example, the concentration of 2DEG is simulated as a function the thickness of AlGaN layer. These supporting calculations could also be a base to explain the characteristics of a gate recessed HFETs, where the thickness of AlGaN is varied only under the gate electrode.

3.3 GATE RECESSED GaN/AlGaN HFET MODELLING

Field effect transistor (FETs) involve transport of one type of carriers only, which are electrons in most cases, as the electron mobility is higher than that of holes. In a HFET (as discussed in chapter 2) the 2DEG plays a key role for electrical charge transport where the charge flows in a channel parallel to the device surface between two ohmic source and drain contacts. A third electrode (gate) is metallized in between of the source and drain contacts. It modulates the 2DEG density by field effect. The source is grounded and the drain-source voltage is called V_{ds}, while the gate-source voltage is called V_{gs}. I_{ds} are the current between source and drain and I_{gs} is the current entering into the gate. *The ability of the gate to modulate the current flow between source and drain is expressed by the transconductance ($g_m = \partial I_{ds}/\partial V_{gs}$ at constant V_{ds}).* Fig. 3.7 shows an equivalent circuit with the most important electrical components to describe a FET.

3.3-1 DC Characteristics

An idealized FET is characterized as follows, in order to give a large current in the On-state , the density, mobility , and saturation velocity of the electrons in the channel are large, and the parasitic resistances i.e. R_s are small. To reduce the currents in the OFF-state, the gate has to sustain electric fields without leaking. In the following discussion *capital alphabets in subscripts are used to show parameters when transistor is characterized using DC values and small subscripts for AC/HF characterization.*

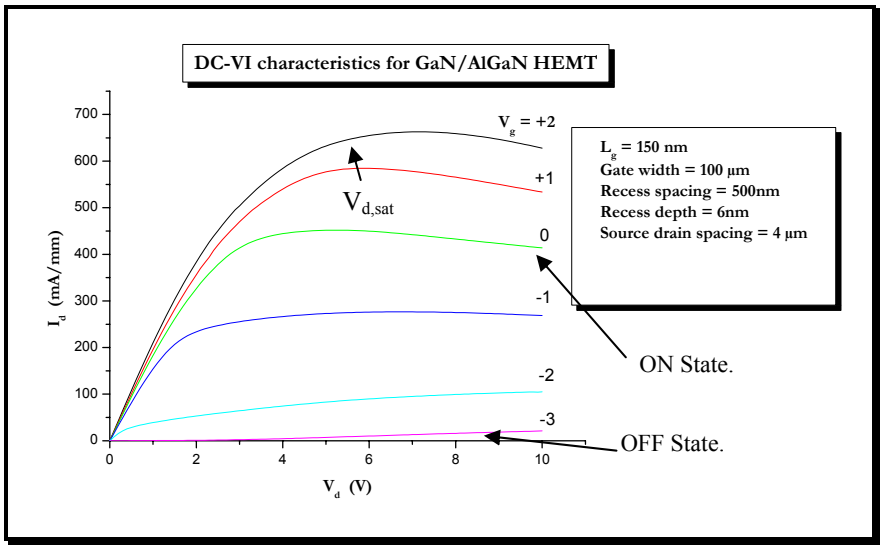


Fig. 3.6: *I(V) characteristics of a gate recessed FET working in enhancement and depletion modes.*

Fig. 3.6 is a plot of drain current as a function of source drain voltage. The picture shows the DC characteristics of FET in depletion and enhancement mode. A drain current, (I_D) flows in the channel when drain source voltage (V_{DS}) is applied and under a gate voltage (V_G). For small drain source voltages (given for linear region of drift velocity $v_D = \mu E$) the drain current is calculated [5.1] as given in Eq. 3.9

$$I_D = \left(\frac{W}{L_G}\right)\mu C_G\left[(V_G - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] \text{ for } V_{DS} \le V_{DS,sat} \tag{3.9}$$

And for saturation region, e.g. $v_D = v_{sat}$

$$I_D = \frac{1}{2}\left(\frac{W}{L_G}\right)\mu C_G(V_G - V_{th})^2 \text{ for } V_{DS} > V_{DS,sat} \tag{3.10}$$

Where W is the gate width, C_G is Gate capacitance, and V_{th} is threshold voltage as shown in Fig. 3.6. With different gate voltages we can drive the transistor either in enhancement mode or in depletion mode.

The measurement of I_d is done at a given gate voltage. The transconductance of an FET is defined as follows.

$$g = \left.\frac{\partial I_D}{\partial V_G}\right|_{V_{DS}=Const} \tag{3.11}$$

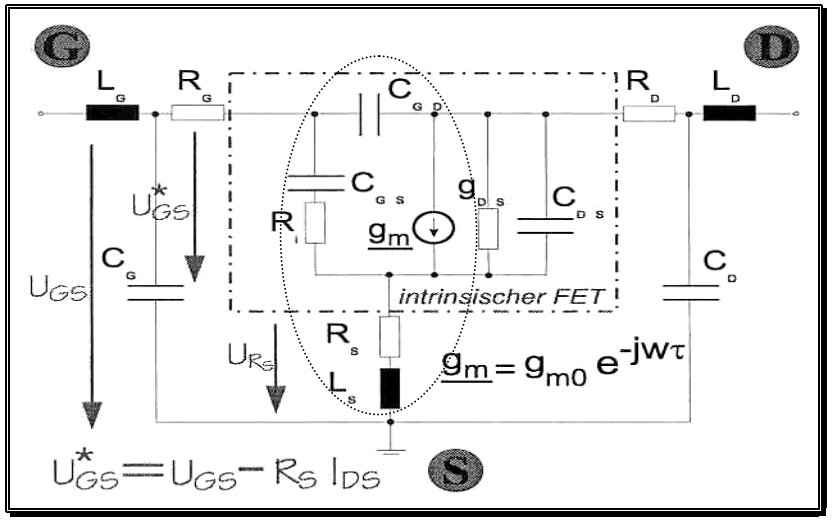


Fig. 3.7: *FET equivalent circuit. Note intrinsic transconductance is different compared to the extrinsic transconductance. FET is a two port network.*

It is interesting to note that parasitic resistance affects the characteristics of HFET. Therefore, a very important motivation for a gate recess is the reduction of the effective gate-source voltage by the voltage drop on R_s (feedback) induced by I_d. The source resistance is the most important (see chapter 5). The intrinsic transconductance of FET can be derived from Fig.3.7 (more simplified circuit is shown in Fig. 3.8) and a simple circuit calculation as,

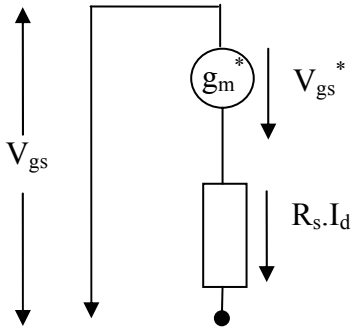


Fig. 3.8: *An equivalent circuit for the FET with intrinsic voltage source V_{gs}* and connected source resistance.*

$$V_{gs} = V_{gs}^{*} + I_{ds} \cdot R_s \equiv \frac{I_{ds}}{g_m^{*}} + I_{ds} \cdot R_s \equiv I_{ds}\left(\frac{1}{g_m^{*}} + R_s\right) \tag{3.12}$$

For $g_m = \frac{I_{ds}}{V_{gs}}$ we have $g_m^{-1} = \frac{1}{g_m^{*}} + R_s$

or $g_m = \frac{g_m^{*}}{1 + R_s \cdot g_m^{*}}$ (3.13)

Where g^*_m is intrinsic transconductance and R_s is source resistance as shown in the Fig.3.7 and Fig. 3.8. From Eq. 3.13, we see that the intrinsic transconductance is of FET is always larger than its extrinsic transconductance.

3.3-2 HF Characteristics

As discussed in [3.5], a HFET is like a two port network. The input signal is applied to the gate and source, and output is measured between the drain and source. The scattering parameters (S-parameters) are used for HF characterization of a FET. Fig. 3.9 shows a schematic representation of two port network of a FET.

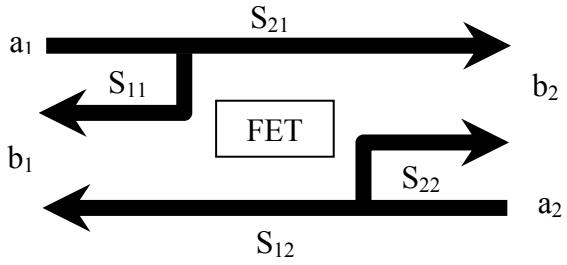


Fig. 3.9: *S-parameters with incident waves (a_1, a_2) and reflected waves (b_1, b_2) for a device to be tested.*

The linear equations describing the two-port network are given as [3.6].

$b_1 = S_{11}.a_1 + S_{12}.a_2$ i.e, reflected + transmitted

$b_2 = S_{21}.a_1 + S_{22}.a_2$ i.e, transmitted + reflected (3.14)

Where a_1 and a_2 are amplitudes of the incident waves (flow into) and are independent variables. b_1 and b_2 amplitudes of the reflected and transmitted waves (flow out of the network S_{ij}) and are dependent variables. We can write,

$$S_{ij} = \left.\frac{b_i}{a_j}\right|_{a_m=0} \tag{3.15}$$

The coefficients of S_{ij} are called scattering parameters and are defined as follows (Eq. 3.16)

$$\left.\begin{aligned} S_{11} &= \left.\frac{b_1}{a_1}\right|_{a_{2=0}} && \text{Forward reflection coefficient} \\ S_{12} &= \left.\frac{b_1}{a_2}\right|_{a_{1=0}} && \text{Backward transmission coefficient} \\ S_{21} &= \left.\frac{b_2}{a_1}\right|_{a_{2=0}} && \text{Forward transmission coefficient} \\ S_{22} &= \left.\frac{b_2}{a_2}\right|_{a_{1=0}} && \text{Backward reflection coefficient} \end{aligned}\right\} \tag{3.16}$$

As an FET is not only a passive two port network, but shows also amplification of transmitted signals and it is characterized by the maximum available gain (MAG) which is the power gain of a two port network when both the input and the output are conjugate impedance matched and it is the highest gain that can be achieved by lossless tuning on the input and output ports. (That means b_2 = max, and b_1 = min, so that all power is in one direction)

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|\left(k \pm \sqrt{k^2 - 1}\right) \tag{3.17}$$

MUG, maximum unilateral gain, another parameter, which is the gain that would exist if the output-to-input feed back in the transistor is cancelled by another feedback network, with both ports conjugate matched. [5.10]

$$MUG = \frac{1}{2}\frac{\left|\frac{S_{21}}{S_{12}} - 1\right|^2}{k\left|\frac{S_{21}}{S_{12}}\right| - R_e\frac{S_{21}}{S_{12}}} \tag{3.18}$$

Where *k,* the stability factor , is defined below

$$k = \frac{1 + |\det S|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}S_{21}|} > 1 \qquad \text{and } detS = S_{11}S_{22}\text{-}S_{12}S_{21} \tag{3.19}$$

In the HF measurements another factor $h_{21,}$ which is the forward current gain with the output shorted circuit. It is related to the *S* matrix as,

$$h_{21} = \frac{-2S_{21}}{1 - S_{11} + S_{22} - \det S} \tag{3.20}$$

It is related to transit frequency such that the gain h_{21} approaches to one for $f = f_t$. The unity short-circuit current-gain frequency, f_t is defined as [3.5] in Eq. 3.21

$$h_{21}\big|_{f=f_t} = 1 \qquad \Leftrightarrow \qquad 20\log(h_{21})\big|_{f=f_t} = 0 \tag{3.21}$$

f_t can additionally be described by Eq.3.22. f_t shows the transport time of a carrier at v_{sat} from source to drain assuming that only the distance L_g must be taken into account.

$$f_t = \frac{g}{2\pi C_{gs}} = \frac{v_{sat}}{2\pi L_g} \tag{3.22}$$

Where L_g is the gate length; to improve f_t it is necessary to reduce the gate length, v_{sat} is normally fixed. And the maximum frequency f_{max} ,

$$MUG\big|_{f=f_{max}} = 1 \qquad \Leftrightarrow \qquad 20\log(MUG)\big|_{f=f_{max}} = 0 \tag{3.23}$$

f_{max} of a device may be either above or below f_t the exact relationship of these figures of merit depends on the specific values of the terms that govern them. High frequency measurement is usually done above 100MHz. [3.6]

3.4 LINEAR TLM

One of the most common methods for quantitatively assessing the performance of ohmic contacts on a semiconductor is to measure the specific contact resistance (ρ_c) [3.9]. The Transfer Length model (TLM) offers a convenient method to determine specific contact resistivity for a planar ohmic contact.

Fig. 3.10 is a schematic diagram of a semiconductor material with ohmic contact pads prepared for TLM analysis. It can be seen that the sample is first mesa etched usually to a semi-insulating substrate or to a depth where there is a natural depletion layer such as between n+ and p+ material. This is done in order to isolate columns of the conductive epitaxial layer there by restricting current flow within the mesa height. Metal pads, of finite width, w, and length, d, are then deposited on the mesa at a linearly increasing pad spacing, L, such that $L_1 < L_2 < L_3$.

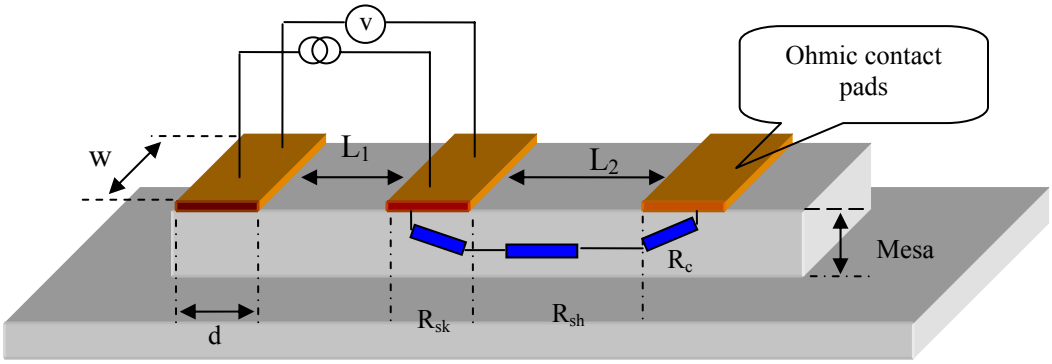


Fig. 3.10: *A schematic diagram of a semiconductor material with ohmic contact pads for TLM analysis.*

The TLM technique relies on the assumption that the semiconductor material under the contact has not been doped differently compared to the bulk material, and the accuracy of the method depends on the ability of control the separation between the contacts [3.7].

According to *Shockley, the total resistance R_t between any two contacts (of length d and width w) separated by distance l could be measured as a function of l.* The resulting equation, Eq. 3.24, between R_t and *l* provides an estimate of R_c through the so called "transfer length" L_t.

$$R_t = 2R_c + \frac{R_{sh}.l}{W} \tag{3.24}$$

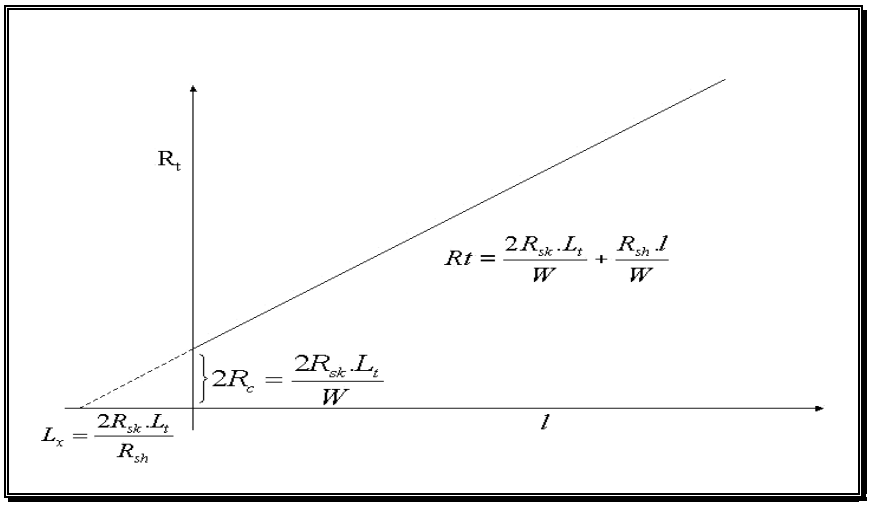


Fig. 3.11 *Plot of total contact-to-contact resistance as a function of l to obtain transfer length and contact resistance values.*

The transfer length is measured form the interaction of the *l* curve for $R_t = 0$ as shown in Fig. 3.11. Here $-l = 2L_t$, for $R_{sk} = R_{sh}$. R_{sh} is the sheet resistance of the semiconductor outside the contact and R_{sk} is the sheet resistance of the layer directly beneath the contact shown in Fig. 3.10. To describe R_t (l) with the assumption of an electrically long contact $d >> L_t$ Eq. 3.24 is valid [3.7].

However, the data show that the experimental results could not be satisfied unless a modification is made to the sheet resistance beneath the ohmic contact. To determine the Ohmic contact parameters with the TLM, resistance measurements $R_1$and R_2 are made between adjacent contacts as shown in Fig.3.10.

The contact resistance R_c, can be shown to be equal to, [3.8]

$$R_c = \frac{R_{sk}.L_t}{W}\coth\left(d/L_t\right) \tag{3.25}$$

With $$L_t = \sqrt{\rho_c/R_{sk}} \tag{3.26}$$

Hence for $d \geq 2L_t$,

$$R_t = \frac{2R_{sk}.L_t}{W} + \frac{R_{sh}.l}{W} \tag{3.27}$$

The relationship (Eq. 3.27) shows that, if the sheet resistance under the contact is significantly modified, then $L_x \neq L_t$. In that case, the correct value of ρ_c is found by performing additional experiments.

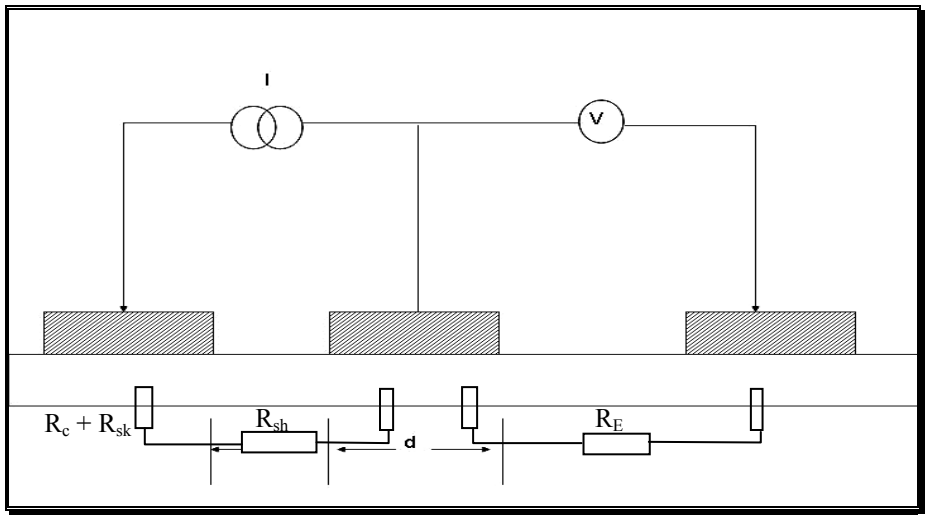


Fig. 3.12: *Experimental setup for obtaining total resistance and contact end resistance values*

The end contact resistance (R_E) measurement is the standard technique to make a current flow between two contacts (Fig.3.12) and to measure the potential between one of these contacts and an opposite outside contact pad. The value of R_E is then V/I.

In terms of the TLM contact parameters, this can be shown to be

$$R_E = \sqrt{\frac{R_{sk}.\rho_c}{W}}.\frac{1}{\sinh\left(d/L_t\right)} \tag{3.28}$$

$$= \frac{\rho_c}{L_t.W}.\frac{1}{\sinh\left(d/L_t\right)} \tag{3.29}$$

on eliminating R_{sk} and using Eq. 3.24, 3.25 and 3.27, we get

$$\frac{R_c}{R_E} = \cosh\left(d/L_t\right) \tag{3.30}$$

Then L_t may be found and thus ρ_c determined from Eq. 3.26

Table 3.1 shows the sample measured for the contact resistances and sheet resistance. Here the method used is End Resistance TLM but in some cases only simple linear TLM model was used.

sample	Spacer Layer AlGaN	Contact resistance. R_c (ohm)	Sheet resistance R_{sh} (ohm)	Resistance under contacts. R_{sk} (ohm)	Specific contact resistivity ρ_c (ohm-cm^2)	End resistance R_E (ohms)	Transfer length. L_t (μm)
HB3869b	None doped	6.108	619.4*	619.4*	1.349xe-5	-	1.479
HB3869c	´´	5.728	530.37*	530.37*	1.39xe-5	-	1.62
HB3869(*e*)+	´´	1.85	587	2.2	1.5xe-4	0.6	83
HB3869(*g*)+	´´	12.45	346	28	1.18xe-3	2.5	65
HB3874	Si Doped	10.645	417	24	1.053xe-5	4.5	66.4
HB3874(*I*)+	´´	8.3	408	4.98	3.11xe-3	7†	250‡
HB3874(*k*)+	´´	8.55	351	15	1xe-3	2.7	82

Tab. 3.1: *TLM results for all samples used to fabricate gate recessed HFETs.*

The table shows that doping the spacer layers of AlGaN could help in reducing the sheet resistance. The sheet resistance ranges from 351 Ohm to 619 Ohms in doped and undoped samples respectively. Contact resistivity ranges from 10^{-3} to 10^{-5} Ohm-cm^2. Linear TLM measurements were taken for the sample HB3874 at different fields (named as *e, g, I, k,*) and these fields are additionally marked with + sign in Tab. 3.1

* measured by simple linear TLM values and the others are with TLM End contact resistance setup. † and ‡ do not hold the Eq. 3.31

$$\frac{R_c}{R_E} \geq 2 \tag{3.31}$$

Which describes a limit for the range in which we can trust the model; otherwise the error gets higher [5.4]. Contact resistances R_c are in the range ≈10 ohms which could be considerably high for HF circuit demands.

Chapter 4

Device Technology

This chapter gives an overview of device technology we used to fabricate heterostructure FETs. It deals with both lithographic processes, that is by optical and e-beam lithography. Samples with GaN/AlGaN layers grown over Sapphire substrates by MOVPE crystal growth technology (discussed in Chapter 2) were used to fabricate Gate Recessed GaN/AlGaN Heterostructure FETs and Modulation Doped FETs. Sample layer structures and device dimensions are given in Appendix A and B respectively. The chapter also highlights the ohmic and Schottky contacts and in the end recess technology with its advantages and disadvantages will be considered.

4.1 PROCESS TECHNOLOGY

4.1-1 Micron and sub-micron lithography

Lithography, the basic and important fabrication step in realization of the microstructures and nanostructures, is a process of transferring geometric patterns defined by a mask on the surface of a substrate. A photosensitive polymer film is spun on the substrate, dried, and then exposed to the proper geometrical pattern through a photo *mask* to ultraviolet (UV) light or other radiation (electrons, then we have electron resists). After exposure, the substrate is soaked in a solution that *develops* the exposed regions of the photosensitive material. Fig. 4.1 is showing basic idea of lithography. A typical mask *aligner* for micron lithography (KarlSuss MJB3) is shown in Appendix D.

Depending on the type of polymer used, either exposed or unexposed areas of the film are removed in the developing process .The substrate is then placed in an ambient that etches surface area that is not protected by the polymer patterns. Because the polymeric material resists the etching process, they are called *resists* and if light is used to expose the structure pattern, they are called *photo resists*. There are two kinds of photo resists, negative photo resists and positive

photo resists. Negative resists become less soluble in developer when they are exposed to radiation, and positive resists become more soluble after exposure see Fig. 4.1 (top right).

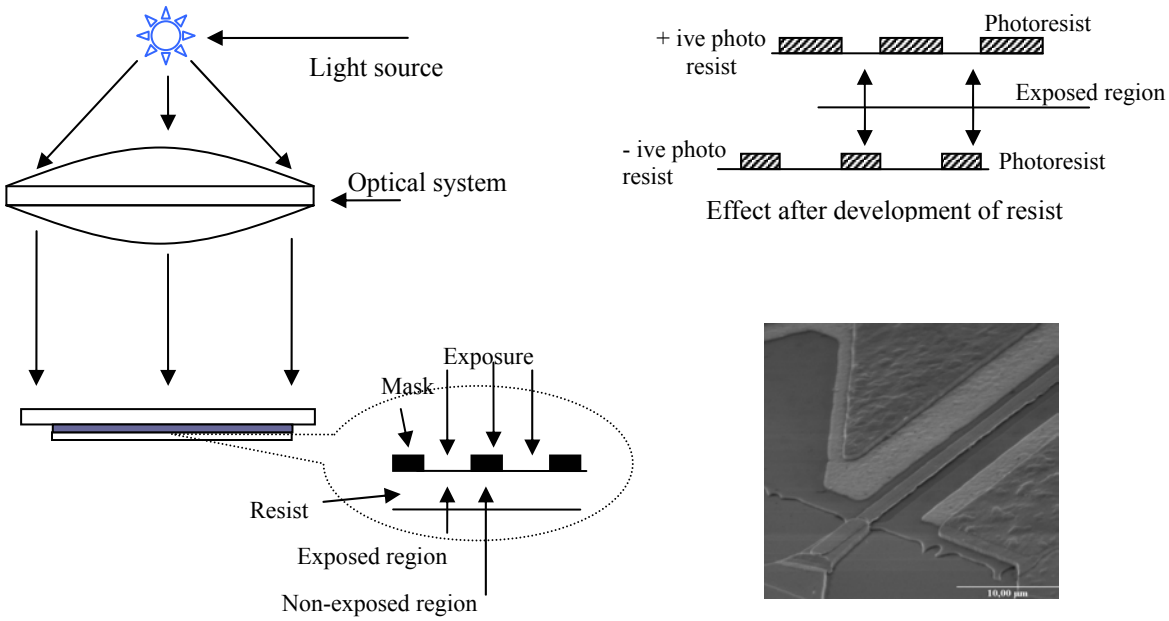


Fig. 4.1: (Left) A *Schematic presentation of contact lithography. Note that mask and substrate are physically in contact with each other. (Top right) different photo resist development process. (Bottom right) A SEM photograph of one of our fabricated FET with optical lithography*

The photolithography was used to fabricate FETs with dimensions ≥ 1.5 µm. But we have also fabricated devices with dimensions smaller than this limit. A gate length of ~ 250 nm was achieved by using Electron Beam Lithography. Fig. 4.2 shows a schematic representation of setup used for Electron beam lithography. An electron beam is sharpened and focused on the substrate with an e-beam resist. This shaping and focusing of e-beam is done by different electrostatic lenses shown in the Fig. 4.2. With the help of projection lens we get a sharp and well focused beam of electrons required to define a pattern on the substrate. Electron beam lithography offers several advantages for lithographic pattern transfer. The resist geometries ≤ 1-µm can be generated (e.g. T-Gates fabrication with ≤ 250 nm). Samples can be patterned directly without a mask.

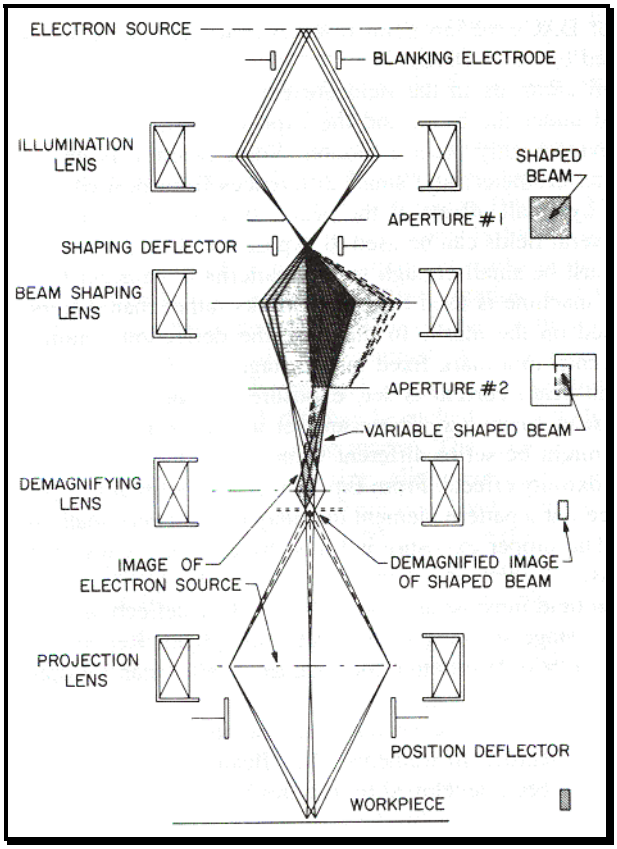


Fig.4.2 *A schematic diagram of electron optical system. Figure from VLSI Technology, (1988). Model JEOL JBX6A3*

A method of trilayer resist was used in order to realize the gate with T-shapes shown in Fig. 4.3. The principle is the sensitivity of the multilevel resists which is different when exposed to electron beam dose. For this reason thickness and composition of the resist layers determines the quality of the structures to be defined by e-beam.

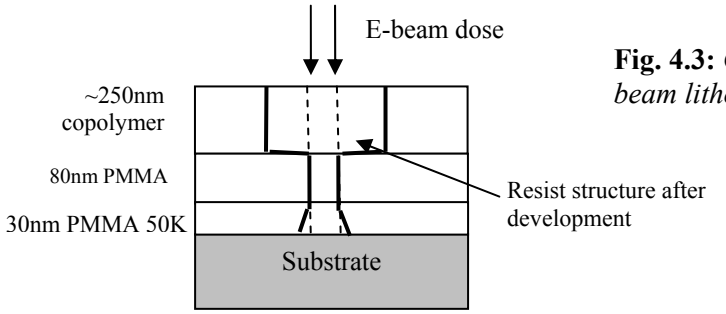


Fig. 4.3: *General multilevel resist for T-Gates e-beam lithograph.*

Talking about the structure size in fabrication *resolution* of the lithography system plays an important role. The resolution is defined in terms of the minimum feature that can be repeatedly

exposed and developed in at least 1 μm of resist. The resolution of a feature is calculated as following

$$R = \frac{K_1 \cdot \lambda}{NA} \tag{4.1}$$

Where λ is the wavelength of light used, NA is the numerical aperture of the stepper lens and K_1 is usually referred as "k-factor" for the processing and it is characteristic to specific lithographic process.

The resists which are spun over the substrate is proportional to the resulting percent solid in the resist and inversely proportional to the square root of the spins speed [4.1], [4.2].

4.2 FABRICATION PROCESSES

The fabrication of HFETs involves photolithography, e-beam lithography, metallization for the contacts and etching of an isolated area (mesa) or a recess for the gate. Comparing to the previous semiconductor materials like GaAs, GaN is more stable because of its promising material qualities like chemical inertness. But this stable chemical nature of GaN can cause some problems in fabrication processes, for an example, in the case of reactive ion etching for recess (see details in ECR-RIE etching section)

In Fig. 4.4 a flow chart of the processes is shown that we have done in order to fabricate FETs based on GaN/AlGaN heterostructures in our microstructure laboratory.

1: Cleavage and cleaning

We cleaved our samples in a first step to obtain suitable wafer sizes for further processing. The sizes of a sample are approx. 7x7 mm^2, 15x7 mm^2 and 15x15 mm^2. Cleaning of samples is necessary after each lithography step. It is done by soaking the samples into warm Acetone then in warm Propanol. This removes all organic layers from the surface. Oxides from the surface of some samples are removed by Hydro Choloro Acid (HCl). It's necessary to have a very clean surface for

- The lithography of ohmic contacts.
- After etching of the mesa, as to remove all remaining from the sample, dirt, or other chemicals which might be deposited on the sample surface.

- After lift-off processes as to have a clean sample, free of any undesired metal pieces left.
- After making recess lithography, a careful cleaning is necessary. It is required because the recess spacings in case of e-beam are in sub-micron regime. A little dirt may disturb the metallization of gate deposition.

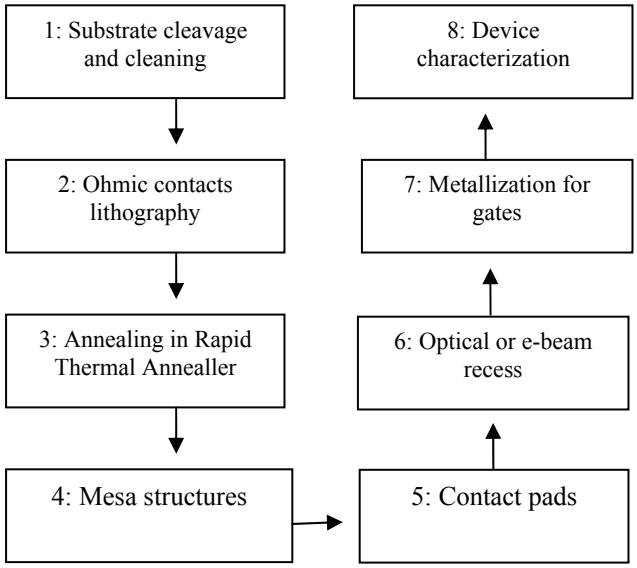


Fig. 4.4: *Sequence of steps involved in the fabrication of gate recessed GaN/AlGaN HFET.*

2: Ohmic Contacts:

Then Ohmic contacts are realized by optical lithography and a metallization. Metallization is done by evaporating a metal directly to a very clean surface of the substrate (will be discussed in section 4.4). The lithography for ohmic contacts is a negative process and is based on following steps

- HMDS spun on the sample with 2000 revolution per second (rps) for 5 sec (spin 1) and then 6000 rps for 40 sec. with *Spinner Convac ST146*.
- Photo resist AZ 5214E spun like HMDS.
- After this the sample was soft baked at 90 °C for 90 sec on a hot plate.
- For ohmic contact lithography the sample was exposed by *KarlSuss Mask Aligner MJB3* for 1.5- 5 sec. Post bake of sample at 120 °C for 60 seconds leads now to a change in the behavior of the resist. It turns a positive to a negative resist behavior. For this reason, this baking is also called the image reversal step.
- Flood exposure for 15 second, for an improvement in the solubility of the resist.

- Development of the exposed sample with a solution of Az developer: water (1:1) for 30 second.

All these process parameters give well defined structures for the ohmic contact metallization. The sample is now ready for Ti/Al/Au metallization. The thickness is chosen to 20/120/200 nm [4.4]. After evaporating these metals (discussed later shortly), lift-off of undesired metal part is done by putting the sample into warm Acetone for some time. Then cleaning is done in the same way as described in part 1.

3 Annealing

After metallization of ohmic metals (Ti/Al/Au), they are annealed at 870 °C for 45 seconds in Nitrogen atmosphere. It is done by Rapid thermal annealler (Model *shs 100 ast electronic GmbH*). A detailed process of annealing is discussed in section 4.4- metallization.

4 Mesa Formation (Positive process)

Like the ohmic contact lithography, mesa is fabricated in a same procedure. The difference is post baking and flood exposure. Because the mesa lithography is a positive process so we do not need these steps. After developing an additional hard bake is done to give the photo resist a higher etch selectivity in the ECR-RIE step. For details refer to Appendix C. The sample after lithography is ready for the ECR-RIE etching. This process is carried out by pure optical lithography as the dimensions of a mesa are ~100 μm. After mesa etching, samples are cleaned by warm Acetone and Propanol as in the part 1.

5 Contact Pads (Negative process)

There is a need to have electrical connection with the ohmic contacts because it is very difficult to make direct contact to the small device structures. These contact pads of Cr/Au (20/500 nm) are usually done in the same way by using metallization (evaporation of metal in metallization chamber).

6 Recess formation (Positive process)

According to [4.3] the gate recess process is one of the most critical steps in the fabrication of recessed HFETs. Samples are processed with optical and e-beam lithography depending on the desired recess spacing. A *JBX-5DII (U) electron lithography system* was used for short gates. We used ECR-RIE in order to etch our samples.

7 Gate Metallization (Positive process)

This is in principle the same metallization procedure as done for ohmic contacts or contact pads. Gate metals are Ni/Au with 100/150 nm. For small gate lengths e-gun is preferred (for details see

metallization). This is because the base pressure of ~ 10^{-8} mbar is much lower than that of in thermal evaporation chamber and secondly, it is very problematic to evaporate Ni in thermal evaporation chamber because the Tungsten boats (used to hold the metal for evaporation) soon get damaged.

4.3 DRY ETCHING TECHNIQUE

(Mesa and recess for gate)

In order to analyze HFET performance, we must have an electrically isolated area where the transistor can be fabricated. For this reason we etch a mesa which is an important part of a transistor on which the ohmic contact lithography is done. We used an ECR-RIE TePla (*Technics Plasma GmbH*) setup for mesa etching.

In Fig. 4.5 we show the principle experimental set up of an ECR-RIE dry etching setup. We apply RF and μ-wave frequency to generate a DC bias in the plasma as well as to generate the plasma by ECR effect [4.16]. This allows the grounded electrode to have a significantly larger area because it is in fact the chamber itself. This larger grounded area combined with the lower operating pressures (5.0-100.0 mTorr) leads to significantly higher plasma-sheath potentials (20-500 V) at the substrate surface, which results in higher ion energy. The ECR-effect (a resonant absorption of he μ-wave in a plasma resulting the higher ion densities) results for a given ion energy, the higher ion densities in the plasma,

$$J_{current} = (Velocity).\ (Density)$$

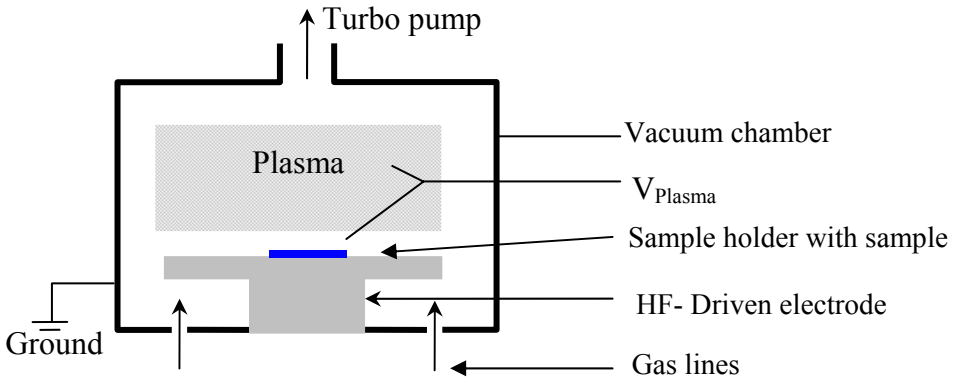


Fig. 4.5: *A schematic representation of an ECR-RIE setup with vacuum vessel for different plasmas and HF-electrode for high freq. operation in dry etching of a sample.*

For ECR-RIE following parameters were used in etching the samples shown in Tab. 4.1.

Sample	**Mesa height Measured (nm)**	**Gate recess depth Intended (nm)**	**Etching rate/ gases. Ar(1.8sccm)/Fr(0.3sccm)**
HB3869b	220 nm	6, 12, 18	*The etching rate is not the same for all samples. It fluctuated, but we controlled it with reference samples.*
HB3869c	220 nm	6, 12, 18	
HB3869d	220 nm	6, 12, 18	
HB3874	560 nm	6, 12, 17	
HB3876	560 nm	16, 22, 28	
HB3877	560 nm	16, 22, 28	

Tab. 4.1: *Samples, mesa height and gate recess depths. Note that the etching is done by ECR-RIE.*

DC biasing = 100V, Gas mixture = Argon (1.89 sccm) and Freon (0.30 sccm), HF power = 70 W
From the reference samples we measured the height of the mesa structures with profile-meters (*Dektak*) and calculated etching rates between 12 – 17 nm/min. For etching the mesa structures of 200 nm or 500 nm, the calculated etching time is applicable. But there are two experimental problems to control the gate recess etching process:

1: to etch a recess of intended depth of 6 nm, this calculated rate leads to a very short etching time of 30 sec.

2: we do not know when the reaction started after switching HF-power on.

Because of the chemical inertness and high bond strengths of the III-V nitrides dry etching is necessary and the ion induced damage in the nitrides appears to be less apparent than that in other III-Vs. [4.19]. But still further refinement in etching rates with suitable parameters (DC biasing, Gases, etc.) is necessary in order to know precisely the etching profiles in nitrides.

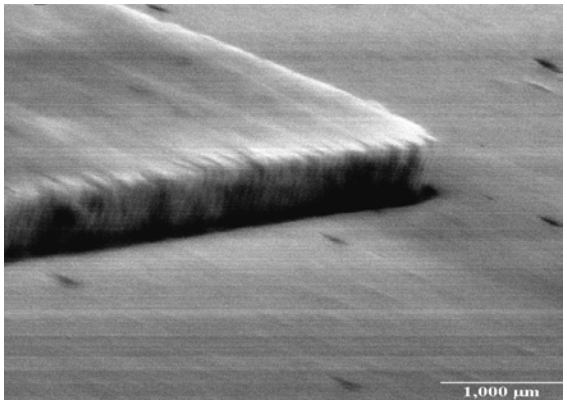


Fig. 4.6: *SEM photograph of an etched mesa, with a mesa height of 500 nm using ECR-RIE technology.*

4.4 METALLIZATION

Metallization is a step in which a metal is evaporated and deposited on the clean surface of a semiconductor. We are using two different methods for evaporating the metals. First, with a simple metallization chamber in which a metal is evaporated using a Tungsten boat. A tungsten boat is like a resistor, which gets heated when current is passing though it. The whole metal (load in the boat) melts and evaporates. Thus it is deposited on a well cleaned surface of the semiconductor. The second one is an electron-gun metallization. In e-gun, a carbon crucible is used to hold metals which are surrounded by cooling environment. A beam of electrons (with accelerated voltage ~10 kV) is focused to hit the metal, makes a very small region of metal to melt and evaporate. This is due to the high energy of electrons. By using the e-gun method, we can evaporate metals of very high melting point as platinum.

Two types of metal contacts in HFET were fabricated i.e. Ohmic and Schottky contacts. To strengthen the ohmic contacts and to have a large area to contact the probe-electrodes, we have extended contacts pads by photolithography and metallization of Cr/Au (20/500 nm in thickness) on present Ti/Al/Au (20/120/200 nm) ohmic contacts. Those are ohmic in nature. Chromium metal is used for adhesion to the semiconductor surface. For the gate contacts of Ni/Au (100/150 nm) with gate lengths in the sub-micron regime compared to that of ohmic contacts, we need a very clean surface and process atmosphere. For gate length 1.5 μm (optical gate) simple evaporation of metal under good vacuum is enough. But for the gate length of 250 nm, e-gun metallization chamber is necessary. The reason is the better defined evaporating environment. In e-gun the base pressure is ~ 10^{-8} mbar that confirms that there is no other impurity in the deposited metal layer. The gate contacts are Schottky contacts. The choice of metal system determines the ohmic or Schottky behavior.

In Tab. 4.2 some attributes of contacts are summarized.

1	*Low contact resistance*
2	*Should be stable in oxidizing ambient.*
3	*Mechanical stability. Good adherence, low stress.*
4	*Surface smoothness*
5	*Stability throughout processing*
6	*Good device characteristics and lifetime.*
7	*Should not contaminate device, wafer or working apparatus.*
8	*Easy to etch for pattern generation.*

Tab. 4.2: *Desired properties of a metallization material.*

4.4-1 Ohmic contacts

Since the frequency characteristics, noise characteristics and power capability of a transistor is dependent substantially on the quality of ohmic contacts. A uniform reproducible low resistance ohmic contact is an important requirement in a fabrication process. According to literature we have a wide variety of combinations for metals deposited over GaN to have ohmic behavior [4.4-4.9], [4.20]. In the case of GaN we have selected Ti/Al/Au metal layers for ohmic contacts due to the possibility to have low specific contact resistivity, good surface adhesion and with long life time [4.15]. Specific contact resistances ρ_c could be as low as about $9x10^{-6}$ Ohm-cm^2.

Sample	Sample characteristics	Ohmic metallization sequence.	Method	Obtained thickness (nm)	Deposition Rate (nm/min)	Contact resistivity ρ_c (ohm.cm$^{2)}$
HB3869 b, c, d	**Non doped**	**Ti/Al/Au**	**Metallization chamber**	**20/120/200**	**0.2/0.2/0.2**	**$1.34e^{-5}$**
HB3874	**Si doped**	´´	´´	**22/125/210**	´´	**$1.05e^{-5}$**
HB3876	**Si doped**	´´	´´	´´	´´	**$9.92e^{-4}$**
HB3877	**Si doped**	´´	´´	´´	´´	**$6.5e^{-4}$**

Tab. 4.3: *Ohmic contact metallization, a combination of Ti, Al and Au results in ohmic contacts after annealing in RTA at 870 °C for 45 sec in N_2 environment.*

Table 4.3 shows the multilayer ohmic contact metallization we used to fabricate our transistors. We have different samples with/without Si doping in the spacer layer of AlGaN. Here we have used metallization chamber for evaporating Ti/Al/Au (the sequence for metallization is Ti, Al and then Au). The layer thickness was selected to be 20/120/200 nm for all samples. The rate of evaporation for all the metallic layers was controlled to be 0.2 nm/min. The specific contact resistivity was measured by linear TLM (discussed in chapter 3). It ranges from ~10^{-4} to 10^{-5} ohm-cm^2.

4.4-1.1 Annealing and ohmic behavior

A number of studies have been made to investigate the Ohmic contact formation mechanism on n-type GaN. Ti-based contact are reported to show ohmic behavior (<10^{-4} ohm-cm^2) after annealing at an elevated temperature (> 600 C°). This could be attributed to the creation of

nitrogen vacancies, which act as donors for electrons, below the contact as a result of the formation of TiN through the reaction of Ti with GaN.[4.21]

In this process we bake (sinter) the metallized sample (samples with bilayer or trilayer metals) to get them alloyed. The annealing process was motivated by much recent work in Rapid Thermal Annealing (RTA), where the annealing temperature is in the order of seconds [4.10]. Our samples were annealed in a N_2 environment after the deposition of Ti/Al/Au layers using annealing RTA programmed to a temperature of 870 °C in 45 sec. An interesting aspect of annealing is not simply to repair damage caused by etching but also to have better resistivity after damage repair.

a b

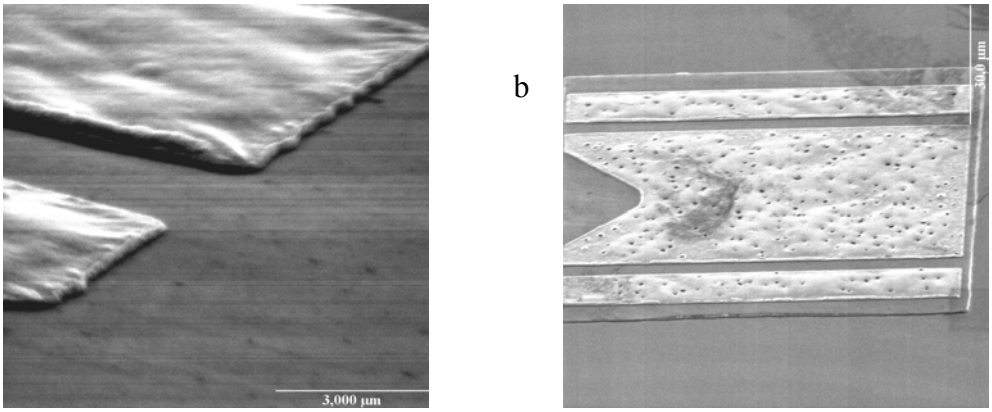


Fig. 4.7: *Different views for ohmic contacts with Ti/Al/Au Metallization for (a) before and (b) after annealing with RTA at 870 °C for 45 sec in N_2 environment.*

4.4-2 Schottky Contacts and Schottky Barrier (gate contact)

4.4-2.1 Physics of Schottky Barriers

A metal-semiconductor contact is known as a Schottky barrier after W. Schottky, who first proposed a model for barrier formation. First significant step towards understanding the rectifying action of metal-semiconductor contact was presented by Schottky [4.11] based on potential barrier at the interface between the metal and the semiconductor.

According to Schottky, a barrier results from the difference in the work function of the two materials. The energy band diagrams in Fig. 4.8 illustrate the process of barrier formation. Fig.4.8a represents the electron energy band diagram of a metal of work function Φ_m and an *n*-type semiconductor with work function Φ_s which is smaller than Φ_m.

Figure.4.8b shows the energy band diagram after the contact is made and thermodynamical equilibrium is reached. The difference of metal work function and semiconductor work function

is given by $qV_i = (\phi_m - \phi_s)$ where V_i is expressed in volts and is known as contact potential barrier which an electron moving from the semiconductor into the metal has to surmount.

$$\phi_B = (\phi_m - \chi_s) \tag{4.2}$$

Eq. 4.2 represents Schottky idea of barrier height. ϕ_B represents the barrier potential for the Schottky contact with a semiconductor of work function ϕ_m.

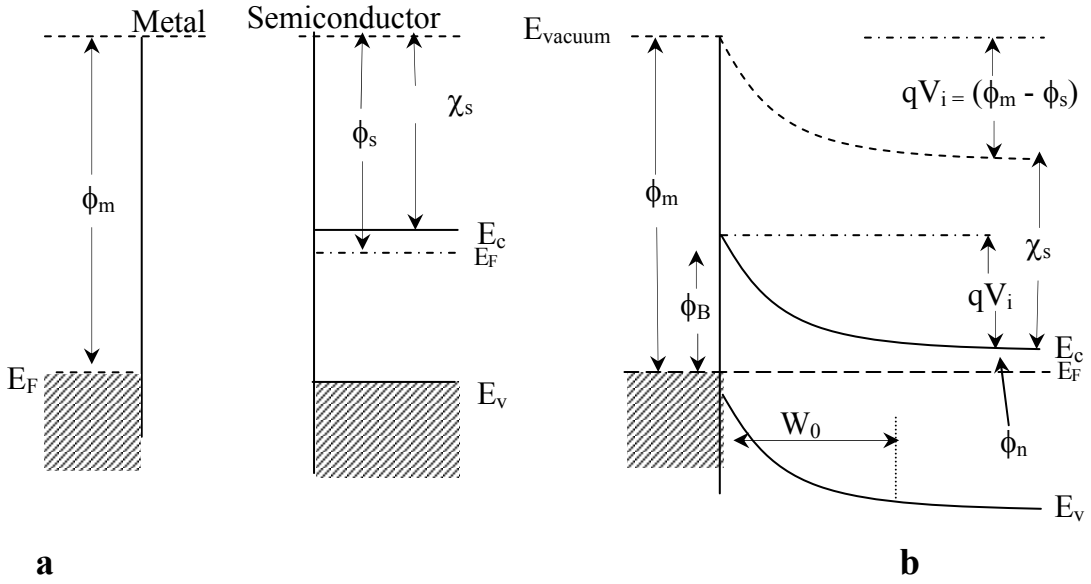


Fig. 4.8: *Electron energy band diagram of metal contact to n-type semiconductor. (a) Neutral materials from each other. (b) Thermal equilibrium situation after contact has been made.*

The current transport through the metal–semiconductor barrier is mainly due to majority carriers in contrast to a *p-n junction* where minority carrier are responsible. The current transport/density can be calculated according to the thermionic Emission/Diffusion-theory [4.13].

$$J = A^* T^2 \left[\exp\left(\frac{-q\phi_b}{kT} \right) \right] \left[\exp\left(\frac{qV}{kT} \right) - 1 \right] \tag{4.3}$$

where J is current density, A* is the effective Richardson constant for thermionic emission into a vacuum, T is absolute temperature, Φ_b is Schottky barrier and V is the applied voltage.

Sample	Gate metallization	Method	Thickness
HB3869 b, c, d	Ni/Au	Metallization chamber	100/200
HB3874	Ni/Au	E-gun	100/150
HB3876	Ni/Au	E-gun	´´
HB3877	Ni/Au	E-gun	´´

Tab. 4.4: *Schottky contact metallization by Ni/Au*

Group III-Nitrides are more ionically bonded than their phosphide and arsenide counterparts as a result of larger electronegativity difference between the component elements. The nitrides experience less Fermi level stabilization or ´pinning` at the surface than in covalent compounds. Thus the barrier height of contacts (Ni/Au in our case) to the nitrides analog to the contact materials such as Si, GaAs, InP, SiC. Therefore we can say barrier heights on GaN vary with the choice of contact metal. However, investigations using material of lower defect density and lower background carrier concentration are required.

4.5 Recessed Gate Technology

From the literature and experimental view points a gate recess plays a significant role in device performance of GaAs [5.14] and GaN based HFETs [4.17-18]. It provides an improvement in the transconductance of the structures compared to none recessed ones [1.3]. A gate recess is also important to reduce source resistance R_s [4.12] which is useful for high frequency circuits.

4.5-1 T-gates

T-gate technology is used to improve the device characteristics by reducing the gate resistance at very small gate length. Fig.4.9 (right) shows a schematic representation for a recessed T-gate HFET and on the left is a SEM photograph of a fabricated T-gate depicted. The basic idea of a T-gate is a reduction of R_g by increasing the "T" and keeping on the same time the gate length L_g small. But at the same time the gate capacitance C_g increases. Therefore the width of the T-gate head must be chosen as a trade-off value between resistance and capacitance [4.14]. We fabricated gate lengths of 250 nm (base of T-gates) by e-beam lithography.

Table 4.5 is a representation of samples and process technology used to fabricate gates. We have realized gate lengths, as discussed earlier, in the optical and e-beam regime. Optical gates of 1.5 µm were fabricated by optical lithography and T-gates of 250 nm length were processed by e-beam lithography.

Sample	Gate category	Length
HB3869 b, c, d	Optical lithography.	1.5 µm
HB3874	e-beam lithography	250 nm
HB3876	´´	250 nm
HB3877	´´	250 nm

Tab. 4.5: *samples, gate length and Lithography used to fabricate FETs.*

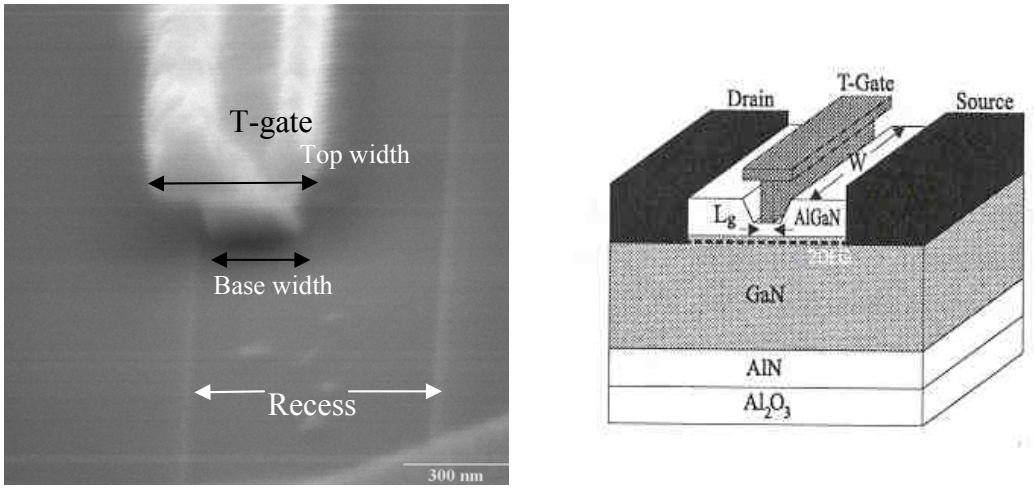


Fig. 4.9: *Left: SEM picture of T-Gate with top width nearly 250 nm and with base width 100 nm; metallized by e-gun process. Right: a principle structure of gate recessed GaN/AlGaN HFET is shown.*

Problems and disadvantages

- Recess spacing in optical lithography, we chose ranges from 1.5 µm to 7.5 µm, can be very accurately controlled and a gate length of 1.5 µm can be deposited exactly in the center of it. The recess spacing in e-beam lithography ranges from 130 nm to 2.5 µm and the L_g is ~ 250 nm. The problem here is to align a T-gate position exactly in the center of recess area that is due to our mixed device processing with optical and e-beam lithography. The optical lithographic mask has an alignment precision of ± 0.5 µm. For all the optical processes a

variation of structure size/alignment in this range is expected. But for e-beam lithography the alignment of structure should be smaller than 100 nm. Therefore the adjustment of crosses which could be used for controlling e-beam writing was a demanding step. Well precise e-beam lithography is needed to control L_{dep}. L_{dep} is the region in recess which starts from the gate to the recess ending see Fig. 4.11. In our case it could be as small as ~160 nm which is comparable to the base width of the T-gate (~ 250 nm). Hence to align a gate exactly in the center of the recess area depends critically on the precision of the e-beam marks.

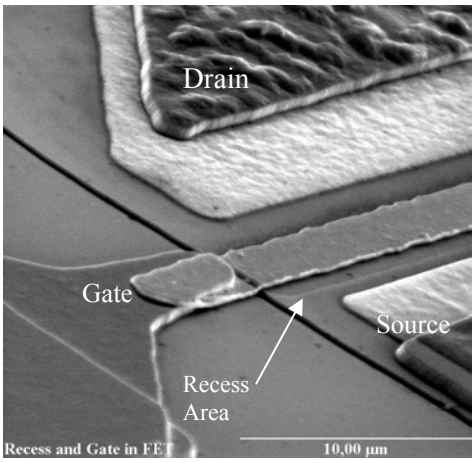


Fig. 4.10: *SEM picture of fabricated gate recessed GaN/AlGaN HFET; note the gate is not in the center of recess area.*

- The annealing process is also an important factor. The ohmic contact boundaries should be, in principle, very smooth and equidistant to the gate. Fig. 4.11 shows the effect of temperature treatment and depicts the ohmic contact layer could not be kept equidistant to the gate. It might cause some changes in breakdown voltage, DC and HF characteristics.

- Control of the ECR-RIE step is another important fact for getting well recessed gates. Etching rates, orientation and etching defects of the surface of recess can affect badly resistances as well as gate barrier and could cause variations in DC and HF characteristics.

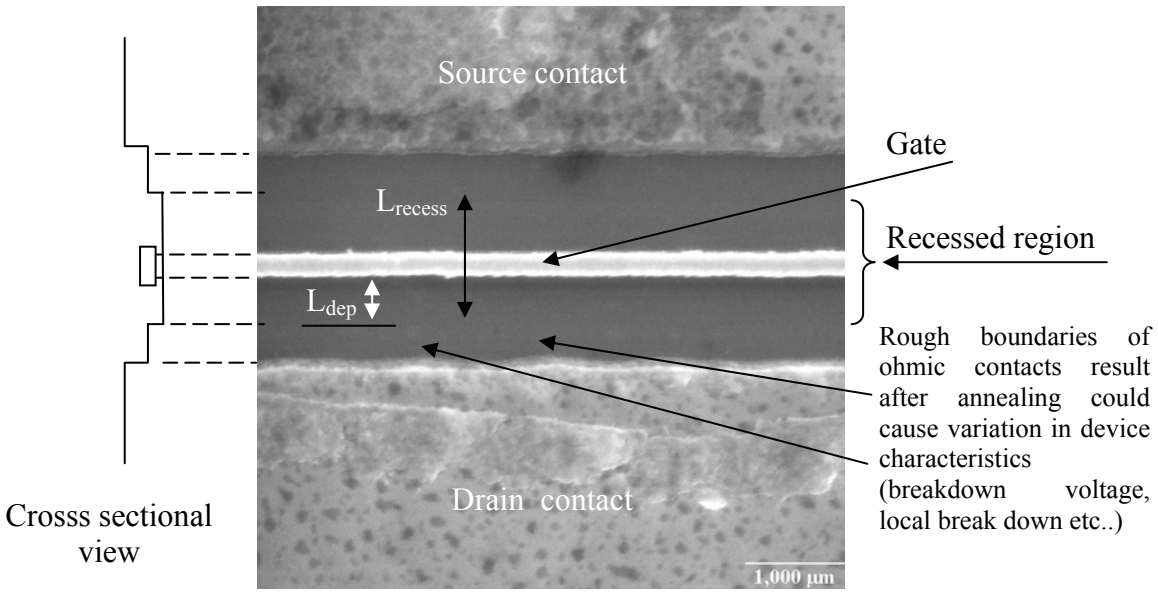


Fig. 4.11: *(right) SEM picture of FET showing ohmic contact layer, notifying the shape of boundaries after annealing. (Left) A schematic cross sectional view of HFET with a T-gate*

A gate recess processing is an important step in FET fabrication. The device processing comprises both kinds of lithography, i.e. optical and e-beam. The procedure for the direct writing e-beam lithography is attractive because an e-beam system is capable of sub micrometer resolution and has the best level-to-level registration capability of the major lithographic techniques. An e-beam system has the advantage of flexibility. Lithographic steps can be optimized. For these reasons ohmic, recess and gate processing should be done by precise e-beam and the rest of the steps (mesa, contacts, etc...) with optical lithography. Secondly, the refinement for ECR-RIE parameters control (like etching time, HF power, gases etc.) is necessary in order to have high quality devices.

Chapter 5

Device Characterization Of Gate Recessed HFET

In this chapter, characterization of gate recessed HFET is reported and discussed. Usually the HFET is characterized by its maximum drain current, pinch off voltage and its transconductance. Parasitic resistance like source resistance, diode characteristics of FET are also important to study with respect to high speed modulation.

We have processed HFETs with different geometrical layouts in order to

- Find out some optimized parameters (geometrical)
- To make the process as easy as possible.
- To see which one of these parameters (geometrical) is the most important/critical (a small fluctuation may cause big variations) for the devices performance.

To analyze the geometry dependence, we have fabricated the HFETs with the geometrical variation shown in Fig. 5.1.

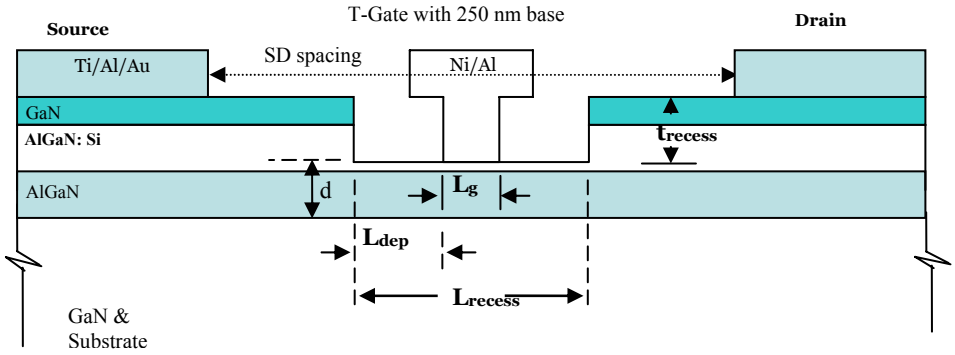


Fig. 5.1*: A schematic diagram explaining all geometrical variations we made to observe their effects on the performance of a HFET.*

In Fig. 5.1 a general layer structure for the samples processed with different geometrical variations of the HFETs is shown. These geometrical parameters (shown in Fig 5.1) are recess spacing (L_{recess}), source drain spacing (SD-spacing) and recess depth (t_{recess}). *d* means the thickness of the channel. These geometrical parameters were varied in order to see what happens physically to the device performance. Gate recess technology was implemented on GaN/AlGaN samples to fabricate HFET and a schematic picture of such structures is shown in Fig. 5.1. Samples are with optical gates (1.5 µm) HB3869 (b, c, d) and with e-beam gates (250 nm) HB3874, HB3876 and HB3877. A layer structure for each sample is shown in appendix A. Expected and reported results are discussed according to these parameters as source drain spacing, recess spacing and recess depth.

A general discussion of the results expected and obtained will be discussed as a Further Analysis, Temperature Effect and HF characterization of HFETs.

5.1 V-I Characteristics of Gate recessed GaN/AlGaN HFETs

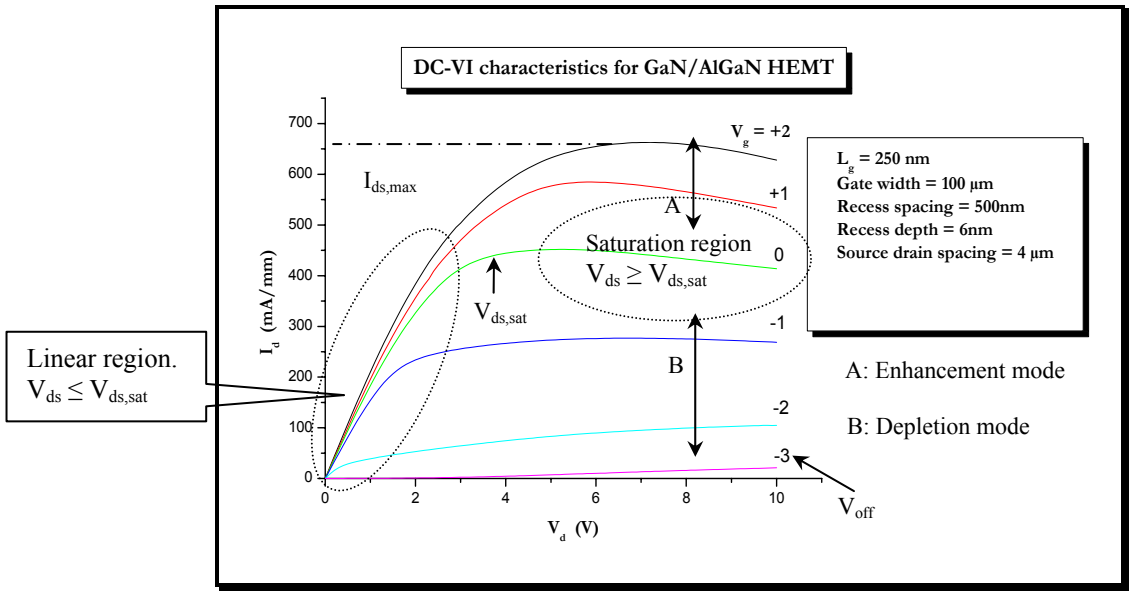


Fig. 5.2: *DC VI characteristics of gate recessed GaN/AlGaN HFET*

Fig. 5.2 depicts a typical DC V (I) characteristics of a HFET based on GaN/AlGaN of certain structures. Here the recess spacing is 500 nm and V_{ds} ranges from 0 to 10 V. The gate biasing is from +2 to -3 V. The gate biasing determines either the transistor is working in enhancement mode (as "A" shown in Fig. 5.2) or in depletion mode (as "B" shown in Fig 5.2). In general, a positive voltage is applied to the gate for an n-channel transistor operating in enhancement mode. For n-channel depletion mode transistor, negative potential on the gate is applied that can

even make the transistor channel closed. This situation is called "pinch off" or better to say "switch off" and the voltage required on the gate for pinch off is denoted as $V_{off.}$ The pinch off depends on the gate-source and drain source biasing. Talking about the HFETs gate-source biasing tends to keep channel electrons stuck to the AlGaN/GaN surface and drain source biasing tends to drag them away to the drain.

The V-I curve can be divided in a linear region where the drain current varies linearly with the applied drain source voltage. This region is also known as ohmic region (with $V_{ds} << V_{ds,\ sat}$). At a point, $V_{ds} \geq V_{ds,\ sat}$, shown as $V_{ds,\ sat}$ in Fig.5.2, the second region starts which is called as saturation region. We see, even with no gate potential ($V_g = 0$) there is a flow of carriers (drain current I_{ds}). This is due to the presence of physically separated electrons in the form of 2DEG as already discussed in chapter 3. The current that becomes maximum ($I_{ds,max}$) at zero gate voltage is due to the drain source biasing. Afterwards we see in Fig.5.2 a constant current or saturated current that flows in the transistor channel because of the electrons that have acquired maximum saturated velocity. In some cases, when the transistor is in saturation region and $V_{ds} >> Vd_{s,sat}$, we see a decrease in $I_{d,max}$. This decrease in current $I_{d,max}$ is due to an increase in resistance offered by inter-collision of the carriers at v_{sat} when the transistor gets heated. This problem can be seen more clearly in Fig. 5.2, when the transistor is working in enhancement mode.

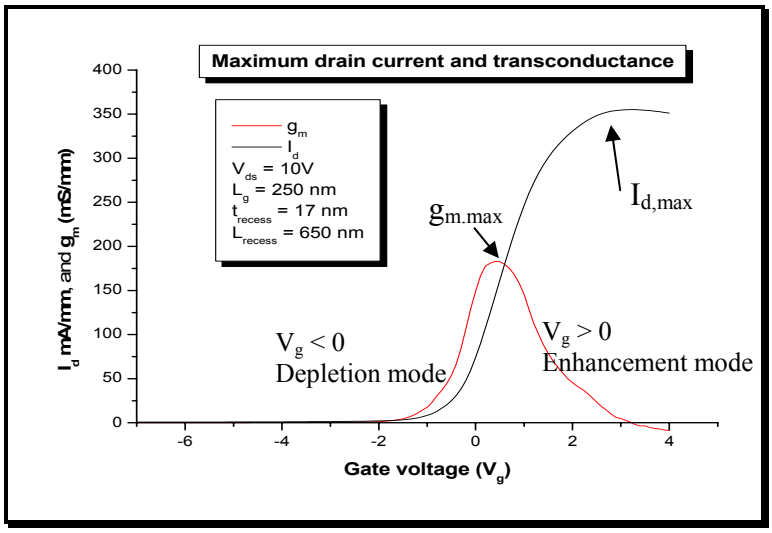


Fig.5.3: *The measurement of maximum drain current and maximum transconductance.*

Because of the shift in the threshold voltage with recess depth (will be discussed shortly), we get the maximum current in recessed transistors only in enhancement mode of a FET. Fig. 5.3 shows the drain current variation with gate voltage. It also depicts the transconductance of a

HFET as a function of gate voltage. The transconductance is at maximum i.e., $g_{m,max}$ when Vg ≡ $V_{g,\,max}$ and corresponds to the point where the carriers in 2DEG attain their maximum value. As g_m is proportional to [n_{2D} (V_{gs}) - n_{2d} (V_{ds})], V_{ds} needed to be large enough in order to provide a large value of n_{2D} (V_g). [1.3]. After this maximum value of g_m, the large drain voltage decreases g_m. The transconductance is measured at V_{ds} = 10V.

5.2 SOURCE DRAIN SPACING

In a first experimental series the effect of SD-spacing were investigated. It is clear that the device processing is easier for the wider source and drain ohmic contacts, but we do not know how critical it is in order to get high performance HFETs. The source and drain ohmic contact metallization was kept constant (Ti/Al/Au) and the spacing between these contacts was varied. The device specifications regarding to HFET layout is given in Appendix B.

5.2-1 Drain Source currents

It is important to state that the HFET structures were fabricated to keep constant the recess spacing and the gate length in both kinds of FET devices (optical gates and e-beam gates). We want to observe the effect of SD spacing. With increase in SD spacing, we decrease I_d and transconductance slightly because we increase the resistance which is created from the sheet of semiconductor. Fig.5.4 shows the effect of increasing SD spacing in sample HB3874 with a gate length of 250 nm.

We expect weak effect on I_d with respect to SD-spacing. The reference transistors (black lines) show a decrease in drain source current due to increase of SD spacing as expected. Fig 5.4 also depicts an increase in I_d form 750mA/mm to 1000 mA/mm for the sample HB3874 with a gate length of 250 nm, for non recessed or reference transistors. The case of recessed transistors can be also seen in Fig. 5.4. The difference in drain current for the transistors with 6 nm recess depth (shown as blue lines) is due to the fact that this family of transistor was taken from different position of the same sample. The same is true (i.e. transistor from different positions of the same sample) for the transistors with 17 nm recess depth (green lines). Therefore it is important to note the landscape the wafer/substrate in order to analyze variation of the device geometry.

If we now consider the different recess depths (in Fig. 5.4), we see a strong dependence between the recess depth and lowering of $I_{d,\,max}$. This will be discussed in detail in the section of recess depth.

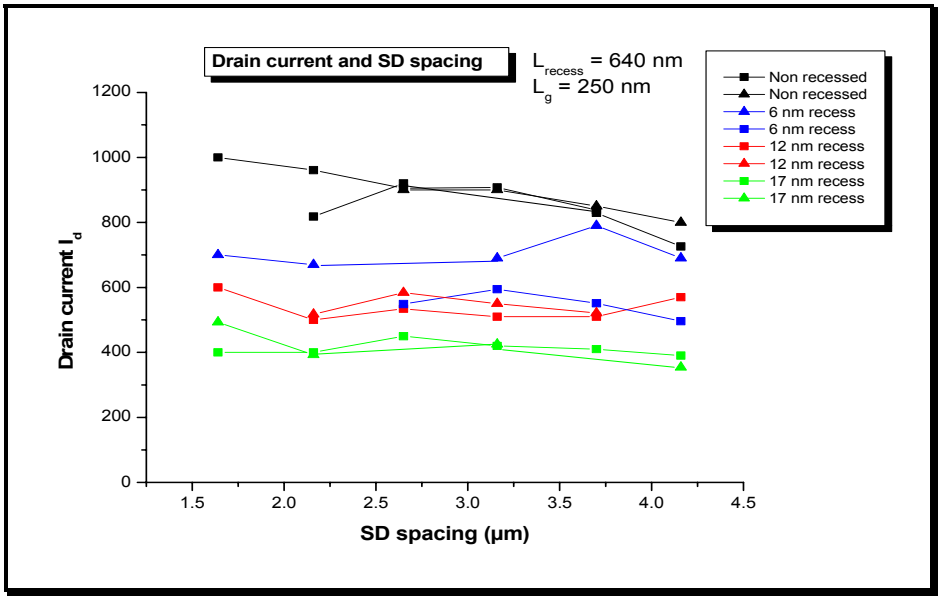


Fig.5.4 *Graph between drain current and SD spacing for the gate length 250 nm. And recess spacing is 650nm.*

We can summarize that the SD spacing is not a very critical parameter for the transistor operation behavior. It would be better to make a transistor small if one wants to have higher currents. But on the other hands, if the size of the Transistor (SD spacing) is a little large, the breakdown voltage will be higher due to increased gate-drain distance. Off course, it is also easier to process the transistor with larger geometry because one can use optical lithography.

5.2-2 Transconductance

In the last section we have seen that the drain current is only a weak function of the SD spacing. Now we want to investigate how strongly the transconductance depends on it. We know that g_m depends on the source resistance R_s (Eq. 5.1) and increasing R_s leads to decrease g_m. For this reason the transconductance would also be lowered by increasing the SD spacing (because it includes an increase in R_s). This can be seen in Fig. 5.5 for optical gates. But due to process technology we could not get enough data points in optical gate sample for an exact experimental explanation.

In Fig. 5.5 we see the transconductance, is a weak function of the SD-spacing. The transistors with 18 nm recess depth show that the active channel (2DEG) is damaged by this too deep recess etching.

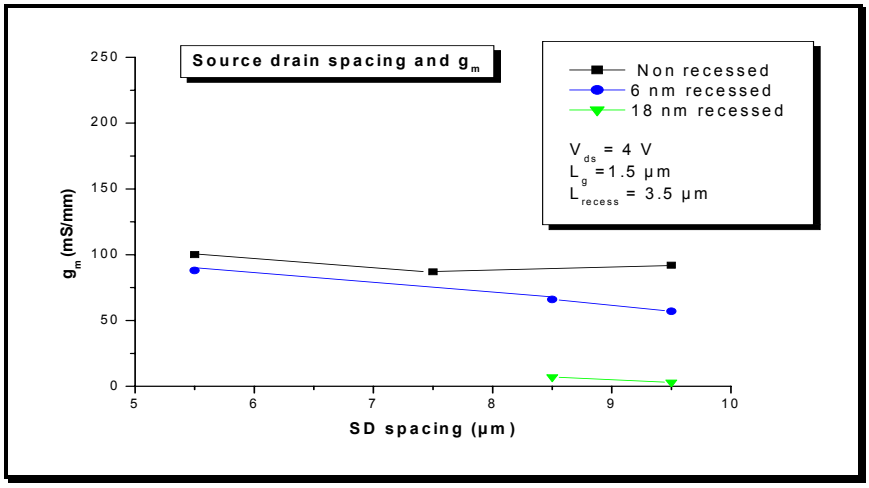


Fig. 5.5: *SD spacing and transconductance for Transistors with 1.5 µm gate length and the gate are finger shaped.*

Fig. 5.6 shows the transistors with gates in sub-micron regime (L_g = 250 nm). Here g_m is measured at a drain source voltage of 10 V. It is also showing a slight decrease in g_m with increasing SD spacing. From the reference transistors (black line) we can imagine the sample homogeneity with respect to resistances. Again we attribute this decrease in transconductance of the recessed transistors (12 and 17 nm recess depths) in comparison with the reference transistors simply to the distance between source and drain and also inclusion of recess that leads to an increase of R_s.

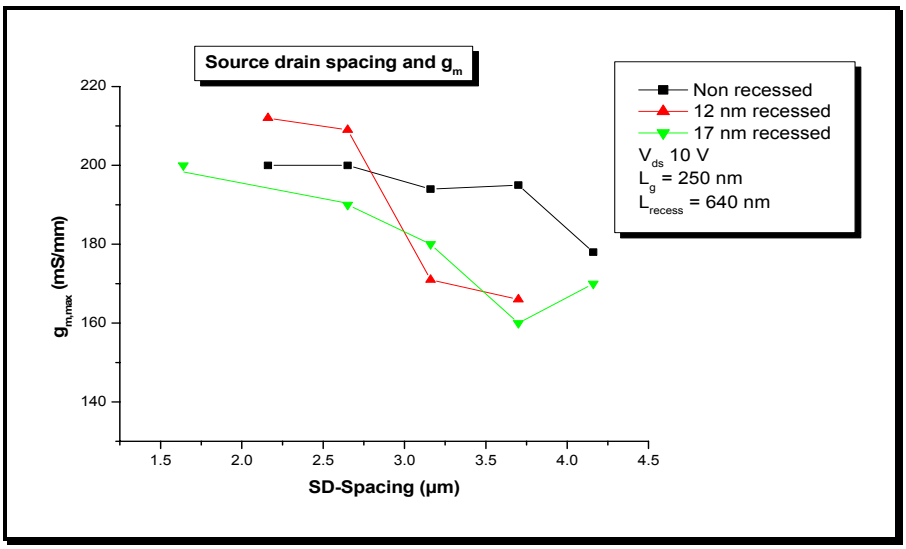


Fig. 5.6: *SD spacing and transconductance for Transistors with gate lengths in sub-micron (250 nm) and the gates are T-shaped.*

5.3 RECESS SPACING

5.3-1 Drain source current

In this section we will see what happens to drain source currents of a recessed in comparison to a non recessed device with the variation in recess spacing (L_{recess}).

In the first step the layout of devices is designed to analyze the drain current as a function of recess spacing (L_{recess}) variation. In the example of Fig. 5.7 we kept the gate length constant at 250 nm and SD spacing at 2.6 µm (HB3874). This figure shows the maximum drain current in the HFET as a function of recess spacing. We get a clear variation of I_d with variation of recess spacing. We observe an increase in $I_{d,\,max}$ for decreasing recess spacing.

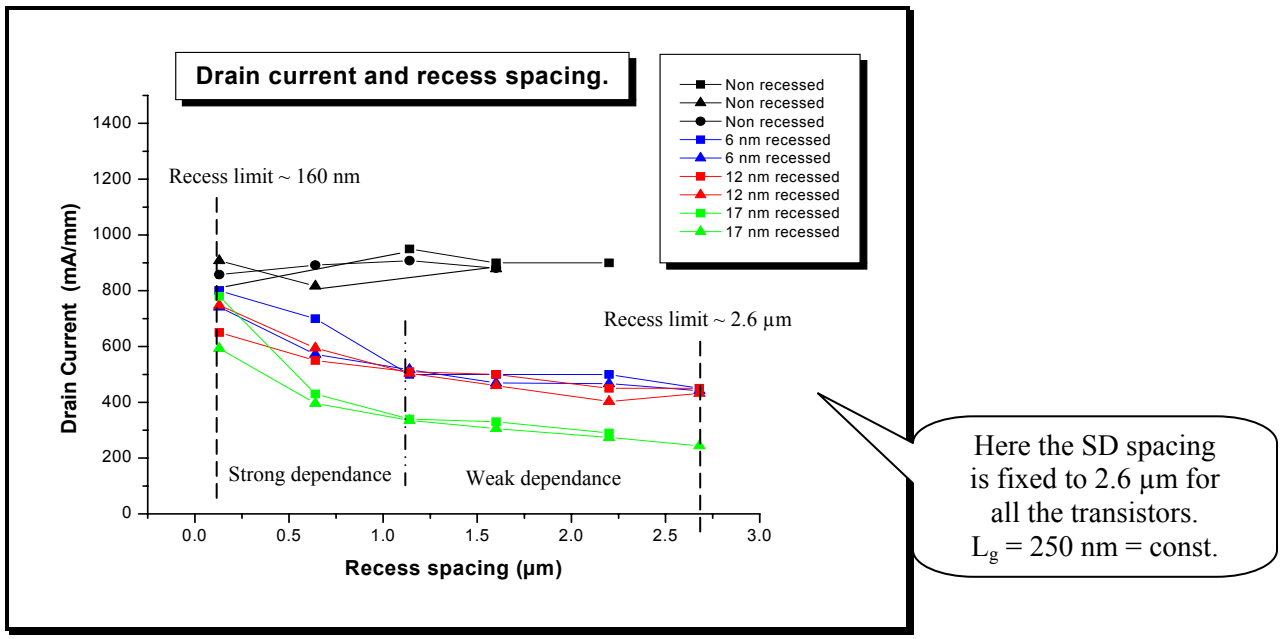


Fig. 5.7: *Graph showing the collective result of different recess spacing on maximum drain currents with different recess depths.*

The black lines (points) in the figure represent as a reference transistor without recess. The little variation in black lines is due to technological errors like a little misalignment, none homogeneity of the sample, etc…but their variation is small enough to see the geometrical variation. The blue lines (points) are representing, transistors with 6 nm recess depth, red lines (points) are for 12 nm recess depth and green lines (points) are for 17 nm recess depth. We also observe in the figure that the drain current is not much strongly depending on recess spacing above approximately 1 µm recess spacing but below this value it is strongly depending and increases sharply for a given recess depth.

We see additionally that if the recess is deep, the source drain current is lowered. It will be explained in the section 5.4 where the effect of variation in recess depth on drain source current and transconductance will be discussed.

5.3-2 Transconductance

Now let us consider the dependence of transconductance on recess spacing. From the above description of drain current and L_{recess}, it seems that recess spacing is more critical compared to SD spacing. From the Fig. 5.8, with a gate length of 250 nm and recess depth of 17 nm, we observe that a decrease in the recess spacing leads to an increase in transconductance of HFET (green line). Furthermore, the transconductance improves for L_{recess} values below 500 nm because it crosses the values of non recessed transistors (shown in black lines). The geometrical lower limits of recess spacing are 160 nm (e-beam gates sample) and 1.5 µm (optical gate samples).

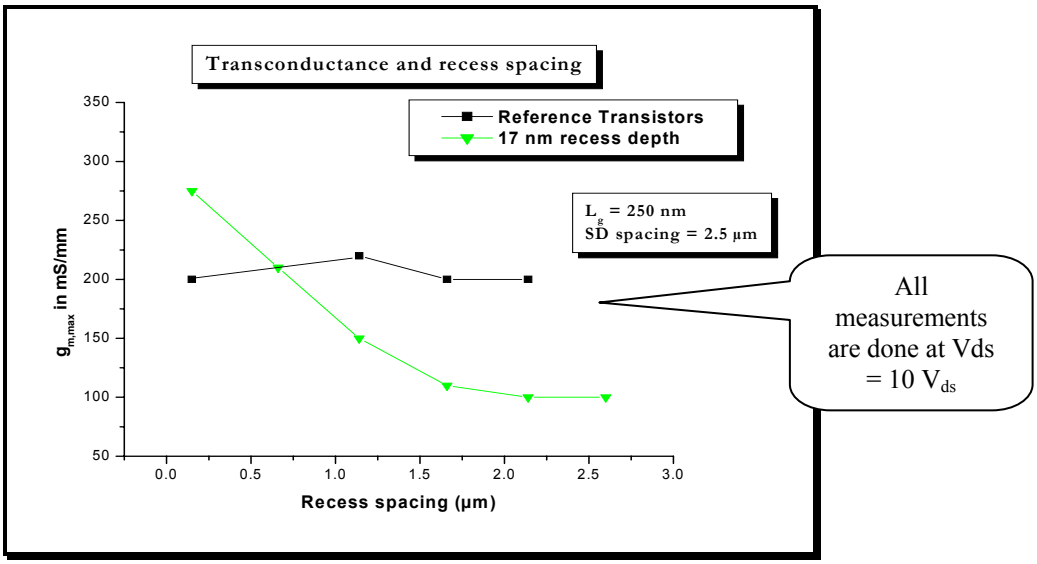


Fig. 5.8: *Minimization of recess spacing leads to an increase of transconductance (g_m). This graph is for e-beam gates with gate length 250 nm, T-shaped.*

Figure 5.8 shows the transconductance with respect to recess spacing for the sample HB 3874 with e-beam gates. We observe maximum g_m = 280 mS/mm for 17 nm recessed HFET at V_{ds} = 10 V. Normally one expects in GaAs-HFET always an increase of g_m due to decrease in R_s. However, even in the case of GaAs, surface (depletion regions) can work like a virtual gate (for details see further analysis section). The reason for increasing the transconductance in GaN-HFET could also be due to decrease in the parasitic source resistance R_s (see further analysis), and surface effects originating after recess etching processes shown in Fig. 5.8.

Fig. 5.9 represents some of transistor geometries and surface defects. These surface defects originated in recess etched area could gate 2DEG. Therefore, we can also say, for longer recess spacing (L_{recess}) or deeper recess (t_r) gate is masked by virtual "defect gate".

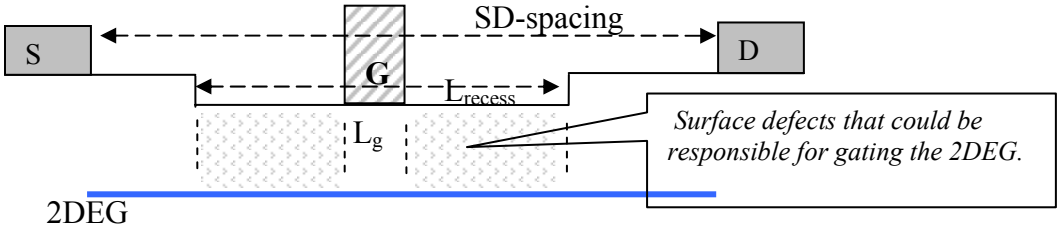


Fig. 5.9: *A schematic diagram for the geometry of parameters varied and surface defects that could originate to affect the 2DEG in GaN/AlGaN HFETs.*

Now talking about the sample with optical gates (L_g = 1.5 µm) Fig. 5.10 shows the transconductance as a function of recess spacing for the sample HB3869c. For samples with gate length of 1.5 µm, recess spacing is from 1.5 µm to 7.5 µm. The transconductance, with decreasing recess spacing, increases from 60 mS/mm to 100 mS/mm for recess depth of 12 nm at V_{ds} = 6 V. In general we see for optical gates we get a similar behavior with respect to recess spacing as we have observed for e-beam gates. In the Fig. 5.10 we also see different limits (geometrical boundries) in the transistor fabrication. At the left side, there is the gate length limit and at the right hand side of the graph is the SD-spacing limit.

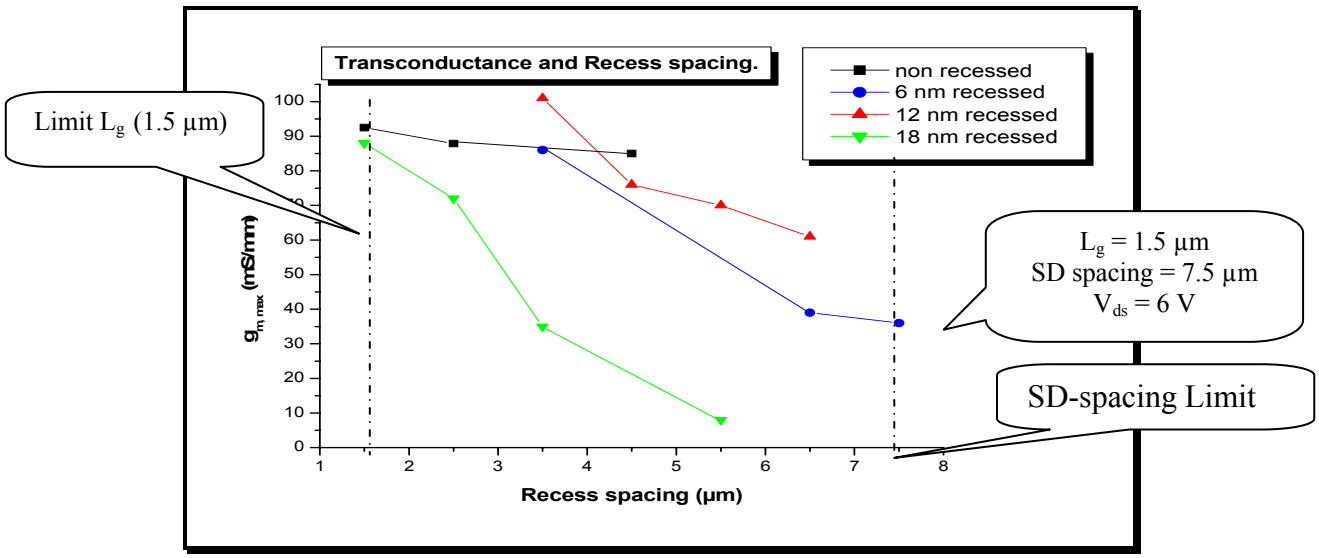


Fig. 5.10: *Transconductance and recess spacing for sample HB3869c. The gates are in optical regime (1.5 µm.)*

We have also a "point" (here it is a wider region) where the transconductance of the recessed transistor crosses the reference value for non recessed transistors. If we look at the ratio of L_{recess}/L_g this "point" seems to be at $L_{recess}/L_g \leq 3$. Therefore the improvement in transconductance due to recess spacing could be achieved if one makes the recess as smaller as $3L_g$. Due to restricted time for my thesis, further optimization in geometry could not be tested in this work.

5.4 RECESS DEPTH

5.4-1 Drain source current

A third geometrical variable in our HFETs we have varied was the recess depth (t_{recess}), see Fig. 5.1. Transistors with different recess depth were fabricated. The recess depths for the samples are approximately 6, 12 and 18 nm. It is important to select the depth of recess according to remaining channel thickness *d*, because too deep etching could lead to touch the active channel and damage the 2DEG. An optimum recess depth etching could lead to a better control over the channel current and threshold voltage [1.3]. Appendix A shows the layer thicknesses of all the samples used for the study of gate recess technology.

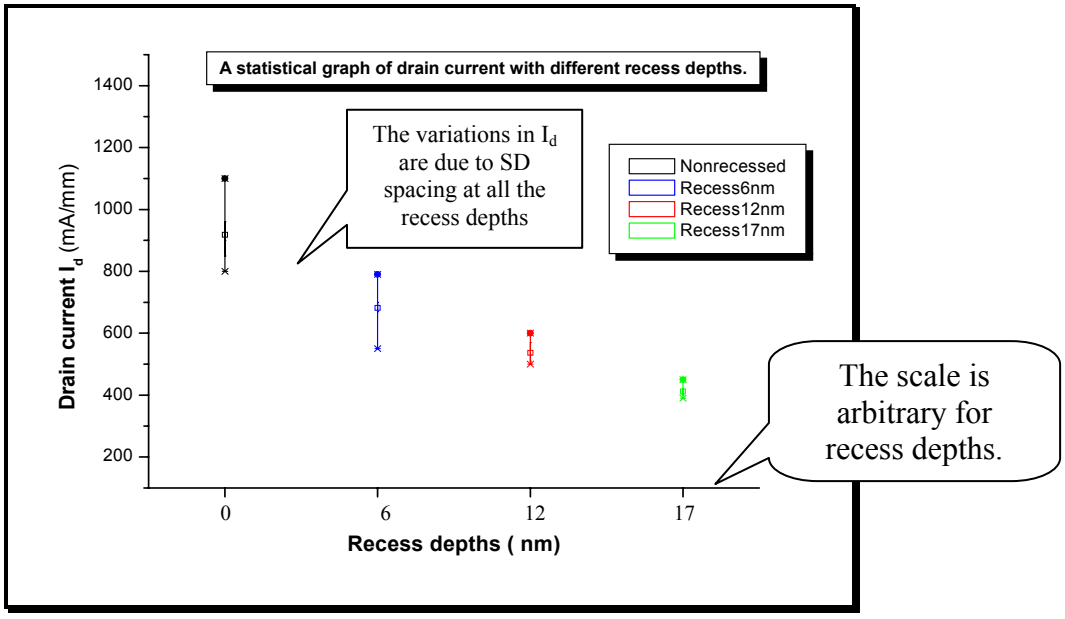


Fig. 5.11: A *picture of drain currents as a function of recess depths. Note that the variation in I_d at a specific recess depth is due to the SD spacing because it is not same for all the transistors. (Sample HB3874 with gate length of 250 nm and recess spacing of 650 nm for all transistors)*

In Fig.5.11 we depict the source drain currents plotted as a function of the recess depths for our fabricated HFETs. The error bars at a certain recess depth account for current variations for the different SD-spacings. As we see in Fig. 5.11 I_d decreases for increasing recess depths. We explain the decreasing drain current for increasing recess depth as follows:

- Firstly, etching out the channel decreases the carrier concentration from the AlGaN layer (undoped or doped) that provides n-carriers to 2DEG at the heterointerface of GaN/AlGaN. If this spacer layers of AlGaN is reduced in thickness (recessed for gate deposition) which could mean we have less donor concentration that leads to lower current density in the active channel of HFET.
- Secondly, it could be due to increasing parasitic resistances like source resistance R_s. (the increase in resistance can be seen in next section of further analysis).
- On the other hand the gate capacitance C_g, ($C_g \sim 1/d$) is increased which can possibly increase the carrier density beneath the gate. As drain current depends on mobility and carrier density, so the mobility of the carriers could be lowered.

5.4-2 Transconductance

In principle, the deeper the recess, the higher will be the transconductance. It is experimentally observed in GaN HFETs [5.1] like seen in GaAs [5.14]. Fig. 5.12 represents the measured transconductance of fabricated HFETs. In this series of experiments we have varied the recess depth.

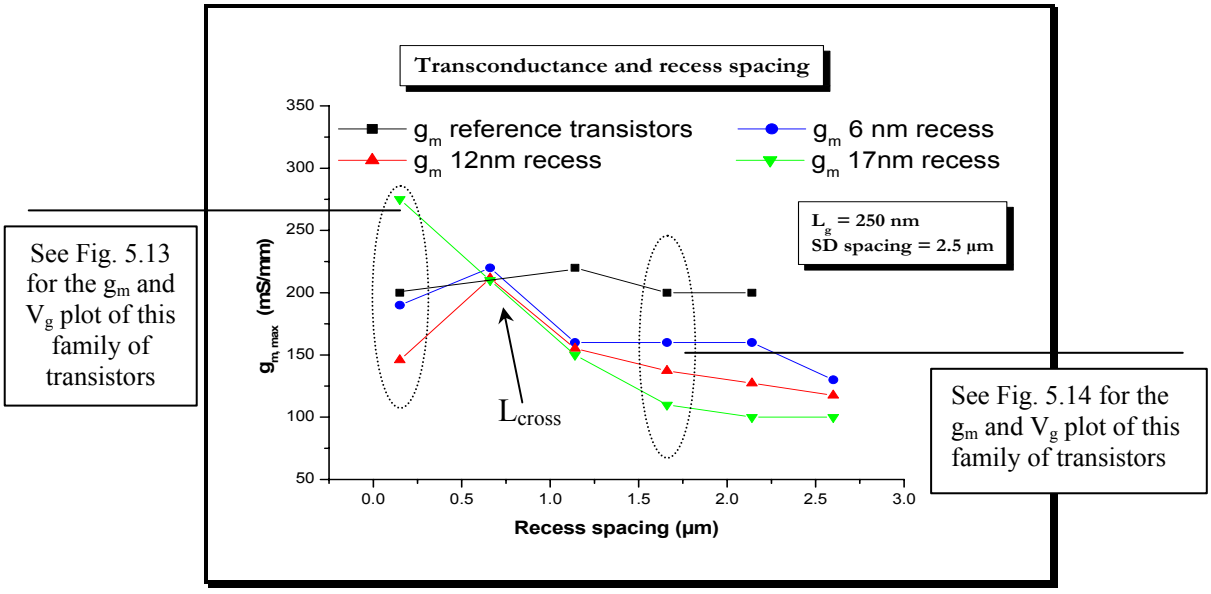


Fig. 5.12: *Recess depth and transconductance of HFETs measured as a function of recess spacing for the transistors with e-beam gates.*

In the above figure the black line is representing the transistors with not recess depth and is denoted as reference. The other three lines, blue, red and green represents 6, 12, and 17 nm gate recess depths in HFETs. This figure shows a gradual increase in transconductance with decrease in recess spacing (above ~1 μm) at a certain recess depth. The values of g_m are lower than that of reference transistors for such a region. But then g_m sharply increases below this value of L_{recess} (< 1 μm) and crosses the reference line at a point shown as "L_{cross}" in the Fig. 5.12. It means we can improve the g_m of a HFET with gate recess. This result is shown in a Fig. 5.13 which is the improvement of g_m at 17 nm recess depth.

It is interesting to note that the spacing between the gate and the recess (shown geometrically as L_{dep} in Fig. 5.1) is very small at this point L_{cross}, i.e. approx 150 nm and difficult to control this region as it needs very precise e-beam lithography. This point "L_{cross}" is also seen in Fig. 5.20 which shows the variations in resistances (total resistances) with respect to recess depths and recess spacing. From these Figures (5.12 and 5.20) we can conclude a main point that in GaN/AlGaN recess geometries (L_{recess}) seems to be very tighter than in GaAs/AlGaAs HFETs. A reason could be found in surface states (charges induced by spontaneous and piezo fields) which are more critical in GaN. [5.11],[5,15]

5.4-3 Recess Depth and Threshold voltage (V_{th})

Threshold voltage for a transistor is defined as the voltage required to make a current flow in the channel between the source and drain contacts. In other words it is also called *turn on* voltage. The threshold voltage of the HFET is an important parameter that determines the depletion and enhancement modes of a transistor. In our studies, the experimental result for threshold voltage (a decrease in V_{th} with recess depth) satisfies the theoretical results [1.3]. Our HFETs (gate recessed) show if the recess is deep the threshold voltage is shifted from higher values to lower.

Fig.5.13 and 5.14 depicts the behavior of the transconductance as a function of gate voltage on the left and right side of the crossing point in Fig. 5.12. The transconductance is measured at the V_{ds} = 10 V. For a certain recess depth we observe in figure that g_m increases with negative gate biasing then reaches to $g_{m,max}$ and afterwards falls again to zero. This is because of the 2DEG (carriers) that varies according to gate voltage (negative), becomes saturated at $V_g = V_{g,\,max}$ and attains $g_{m,max}$ then due to maximum saturation of these carriers (that become constant) $g_{m,max}$ falls to zero. [1.3]

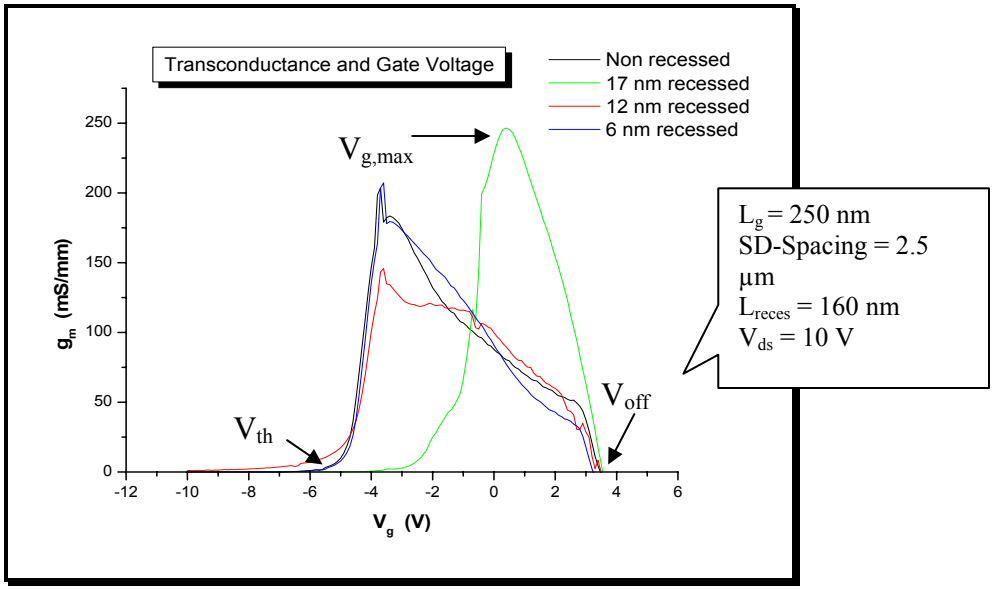


Fig. 5.13: *g_m as a function of gate voltage. Note that the g_m variation with respect to recess depths. This picture represents g_m of the family of transistor at the left side of the crossing point in Fig. 5.11*

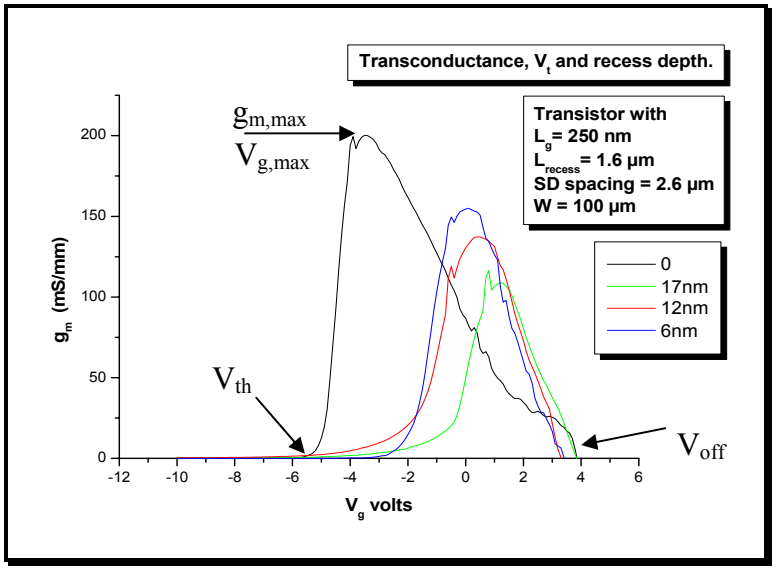


Fig. 5.14a: *transconductance as function of gate voltage Vg for various recess depths. L_g, L_{recess} and SD-spacing are kept constant (Values see in set). This picture represents gm of the family of transistors at the right side of the crossing point in Fig. 5.11*

In Fig 5.14a we also see the on-set (threshold voltage) moves towards higher gate voltages for increased recess depth (t_{recess}). This result is in accordance with the literature [1.3]. It can also be seen in these two figures that the V_{off} remains nearly the same for different recess depths. This is due to the density of states that become infinite for the carriers at certain V_{ds}. The decrease in

$g_{m,\ max}$ with recess depth could be explained on the basis of increased resistances (see the following section). In Fig 5.14a, V_{th} shifts from -5 V to nearly -2 V from none recessed to 17 nm recessed HFETs and with the recess depths of 12 and 6 nm it is approximately -4 and -3 respectively.

We can announce another important result that is also observed in our gate recessed HFETs. This result is a shift in threshold voltage V_t with recess spacing L_{recess} at a particular recess depth t_{recess}. The transconductance of the transistors with 17 nm recess depth is plotted in Fig. 5.14b. In this Fig. the varying parameter is only the recess spacing and it ranges from 2.66 µm down to 0.15 µm. As a result of decreasing the recess spacing, we observe a shift in V_t towards higher negative values (from -1 V to -3V)

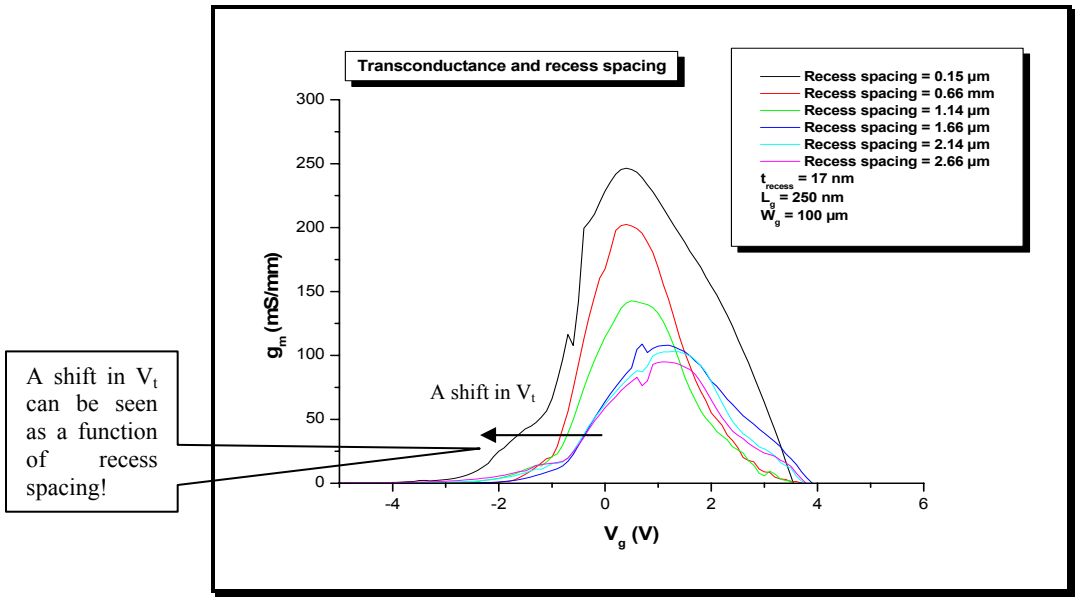


Fig. 5.14b: Threshold voltage and recess spacing at a particular recess depth (17 nm). The figure shows a shift in V_t with recess spacing.

It is already discussed in recess spacing section that with a decrease in recess spacing, there is an increase in g_m at a particular recess depth. This observation can also be seen in Fig. 5.14b for a 17 nm recess depth.

From the variation/shift in threshold voltage with recess depth in Fig. 5.13, and 5.14a (and also seen in other samples), we can infer whether the structures are recessed or not. This fact (shift of V_{th}) points out that the transistors in Fig. 5.13 with supposed recess depth of 6 and 12 nm are not really etched down to these recess depths.

The missing point is, that recess etching can also improve g_m as long as a L_{recess} is adjusted suitably. This is the new and also searched result depicted in Fig. 5.12.

5.5 FURTHER ANALYSIS

5.5-1 Concept of virtual gates

A reason for the drain current and transconductance collapse in a HFET could be due to a charging up of a second virtual gate.

This virtual gate is physically located in the gate-drain region. This is because of the large bias voltages present on the device during its performance. The surface states in the vicinity of the gate trap electrons and this region where these electrons are attracted acts like a negatively charged virtual gate. If there a negative charge exists on the surface, the potential becomes negative, depleting the channel of electrons and leading to extension of the depletion region. Hence, the effect of surface negative charge is acting like a negatively biased metal gate as shown in Fig.5.15a. Hence two gates exist on the surface between the source and drain. These act like as connected in series as shown in Fig.5.15b. This figure shows a simple idea of added gate voltages.

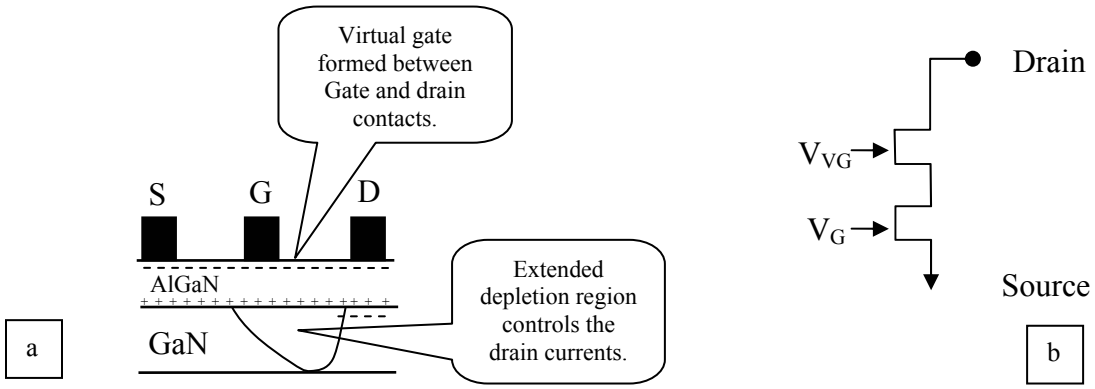


Fig. 5.15: *(a) Model of a device showing the location of the virtual gate, (b) schematic representation of the device including the potential of virtual gate that is added in series with actual gate potential. [5.6]*

The potential on the metal gate is controlled by the applied gate bias while the potential on the second gate, called virtual gate is controlled by the total amount of trapped charges in the gate drain access region. The output drain current is now controlled by the mechanism that supplies the charges to the surface, and removes charge from the virtual gate, in addition to the applied gate bias, [5.6]

5.5-2 Resistances

Parasitic resistances in HFET can be understood according the equivalent circuit shown in Fig. 3.7. These resistances like source resistance directly affect device performance parameters such

as transconductance, gain and noise figure. *The source resistance R_s is the sum of all resistances from the source contact to the gate contact.* Between the extrinsic transconductance and the intrinsic transconductance of an HFET we have a decrease of the first compared to the second due to the voltage drop on the source resistance. A simple model for this decrease could be derived from Fig.3.8. (Already discussed in chapter 3, section 3.3-1) [5.4]

$$g_m = \frac{g_m^*}{1 + R_s \cdot g_m^*} \tag{5.1}$$

Where g_m is the measured transconductance and g_m* is the intrinsic transconductance of a HFET. Eq. 5.1 is very important to analyze the performance of our transistors because it tells us something about the source resistance R_s. If the source resistance increases, then a decrease in the drain currents and transconductance can be seen. [5.12]

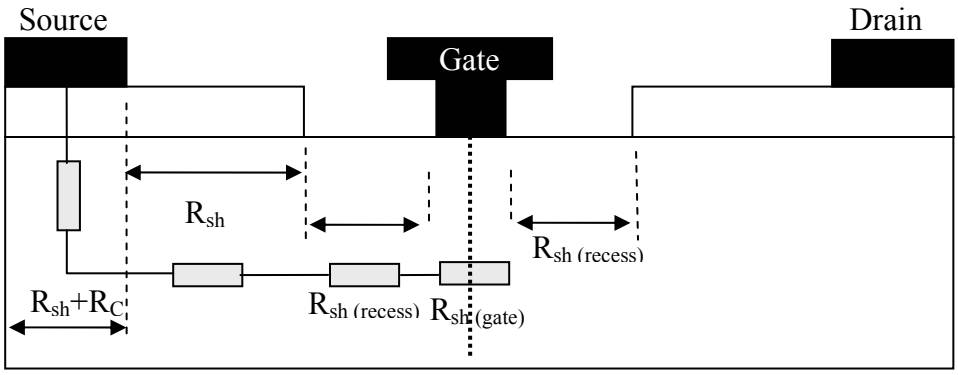


Fig. 5.16: *A schematic diagram for the calculation of source resistance in recessed gate MESFET. The middle line under gate depicts the fact that there is the same resistance circuit on both sides of a symmetric gate between source and drain contacts.*

It's important to compute R_s in optimum way as possible, because the design and/or the processing conditions may change the values of R_s, [5.5],[5.11]. One way for the calculations for resistance is shown in Fig. 5.16. In this figure all possible resistances are schematically depicted. The recess spacing, position of the gate in the recess and itself position of recess between the SD spacing; can cause a variation in R_s. The source resistance is analyzed by using physically based (Fig. 5.16) equivalent circuit for R_s. A single component of this circuit is measured using TLM and R_s is calculated by Eq.5.2 based on this equivalent model using measured parameters R_{sh} from TLM.

$$R_s = R_{sh} + R_C + R_{sh\ (non\ recess)} + R_{sh\ (recess)} + R_{sh\ (gate)} \tag{5.2}$$

Where R_s is the source resistance. The sheet resistance $R_{sh\ (recess)}$ in the recessed region is difficult to determine accurately. For that reason it is difficult to determine exactly R_s even R_c, R_{sh} are

known. Anyway, for deeply recessed structures, the source resistance can be significant. From a source resistance point of view, $R_{sh\ (recess)}$ should be minimized. See also the effect on g_m is shown in Fig. 5.12.

A more detailed explanation for the increase in the parasitic resistance is given in the following Fig.5.17.

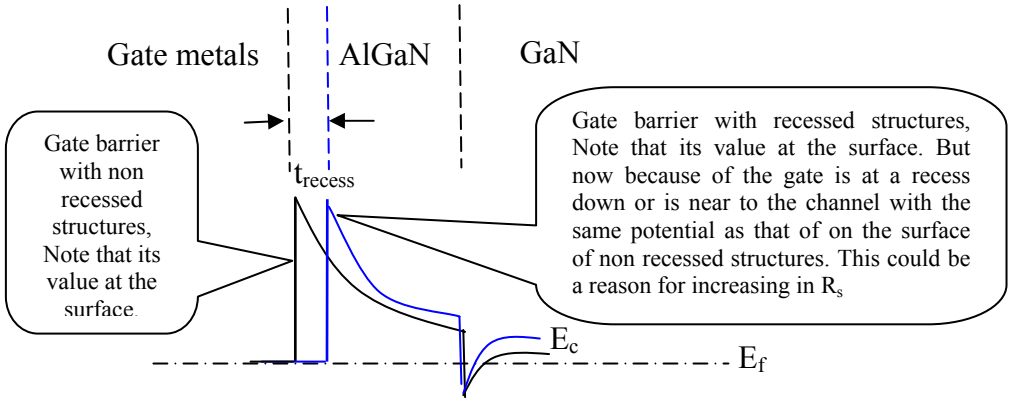


Fig. 5.17: *A theoretical picture for the explanation of an increase in parasitic source resistance in recessed structures.*

When the gate is recessed down to t_{recess}, the recess surface experiences the same surface potential as that of non recessed surface potential. Now this potential, shown in Fig 5.17, is more effective to the channel and the resulting carrier density is less compared to that of non recessed structures.

There is one another important point to consider while measuring the source resistance, the sheet resistance and the contact resistances. Because of our mask layout, we have two transistors (see Appendix B) on the mesa. One can denote them as an upper one and a lower one as shown in Fig. 5.18.

Source ohmic contact on mesa; note that they are not of the same size.

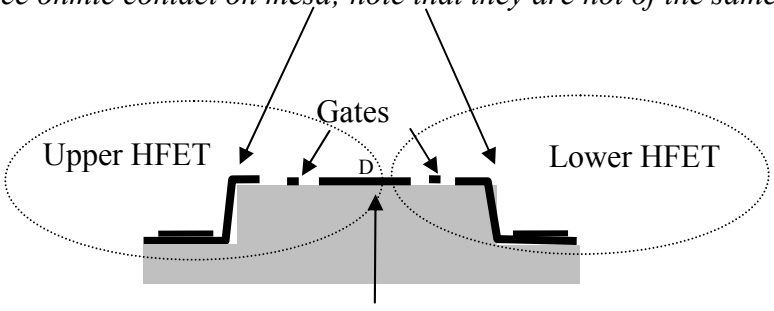


Fig. 5.18: *A side view of single transistor on mesa to illustrate the contacts that could be responsible for the variations in contact resistances for upper and lower FETs .Note that the ohmic contact area for the upper transistors is less compared to that on the lower ones.*

The difference in both transistors is due to the position of the ohmic metal contact on mesa. This can be seen by an optical microscope. Mostly the gates are now asymmetrically positioned; they are nearer to the lower source compared to the upper source ohmic contact.

Until now we have discussed the theoretical explanation for the resistances (i.e. source resistance), now we want to show the actual behavior of our recessed HFETs. The Fig. 5.19 shows how the resistance varies with SD-spacing. In figure the green dots represent the measured contact resistance of the upper transistors, the green blocks represents the resistance of the lower transistors. Similarly the red color dots and blocks represent the measured contact resistance of upper and lower FET respectively. The measurement is a simple determination of V(I) characteristics between the ohmic contacts, and from these measurements we calculate the resistance. The green ones are recessed to 6 nm where as the red ones are none recessed. Line 1 (Black line with the blocks) and line 2 (blue line with the blocks) in the figure gives the contact resistance of TLM pads. It is calculated by the Eq. 5.3 using sheet resistances measured from TLM and SD spacing from the actual distance taken from SEM. Equation 5.3 is applied to calculate R_{SD}.

The resistance under the contacts and the sheet resistance, both vary with the sample landscape.

$$R_{SD} = \frac{2R_{sk}L_t}{W} + R_{sh}\frac{SD(spacing)}{100\mu m} \qquad (5.3)$$

The little offset between the two lines is due to different contact resistances and the steepness of the lines is dependent on the sheet resistance of the sample. (See table 3.1 in chapter 3 for R_{sh} and R_c and L_t used to calculate the resistance between the source and drain). The figure depicts the resistance between source and drain in FETs, increases with increase in SD-spacing. The resistances for 6 nm recessed FETs (shown in green color) are comparatively higher than none recessed ones (red color).

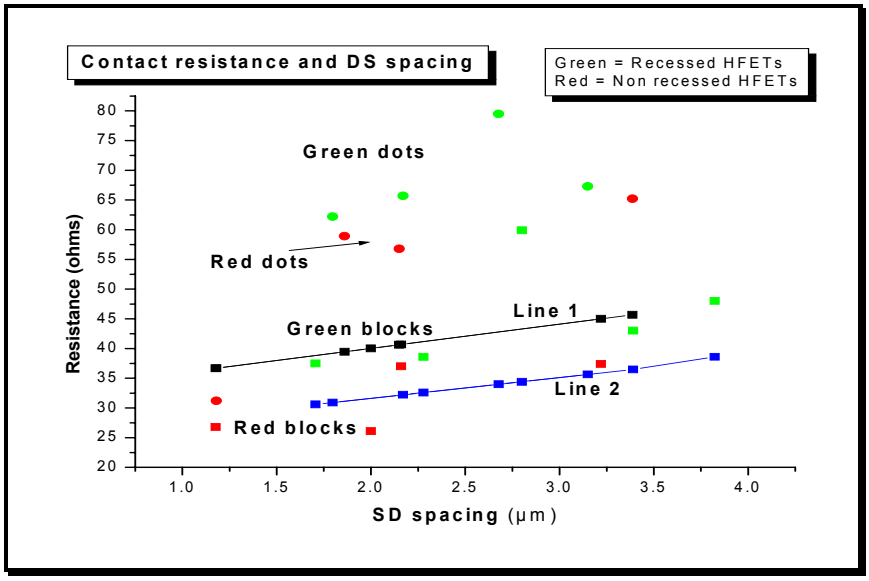


Fig. 5.19: *The variation of contact resistance with SD-spacing and recess depths in sample HB387. Further explanations see the text.*

A result that we can conclude from the Fig. 5.19 is the difference in the resistances of the upper and lower transistors. We have seen that the transistors located at the upper end of mesa are showing more resistance in comparison to those located at the lower end.

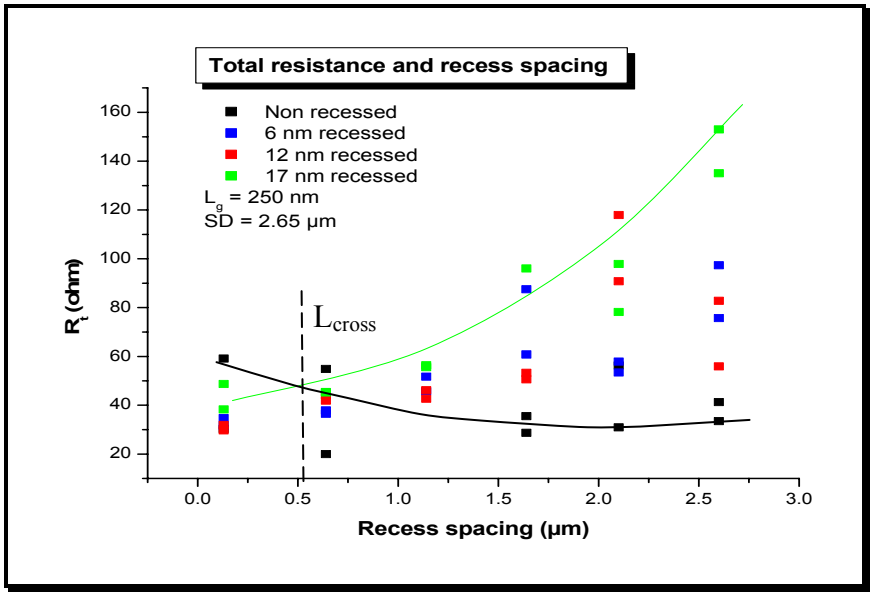


Fig. 5.20: *The variation of contact resistance with recess spacing and with recess depth in sample HB3874*

Now we talk about the resistances (total resistance R_t between the source and drain) measured as a function of recess spacing. From Fig. 5.20 we can conclude various important results.

- In Fig. 5.20, the transistors with recess are offering more resistance compared to that with non recess. But a careful observation of this figure shows that the resistance R_t decreases for L_{recess} < nearly1 μm. A hand drawn green line is shown in the figure to show the decrease in resistance as a function of recess spacing for the transistors with 17 nm recess depth.
- The changes in resistances while recess spacing is varied are also shown in Fig 5.20. Here we see a large variation in resistance if the recess depth is increased. Another point to note is, that the values spread more by increase in recess spacing. With a detailed study of the variation of total resistance as a function of recess spacing we observe that there seems to be also a "crossing area" as shown in the figure as "L_{cross}". R_s can be improved with respect to L_{recess}. It can also be compared to Fig. 5.12 where the transconductance improvement can be achieved if $L_{recess} < L_{cross}$.

Because of these big variations in resistances (Fig. 5.19 and 5.20.) we renounced to calculate exact values of the parasitic resistance especially R_s. But an interesting feature of the results is the crossing point/area that can be observed in resistance and transconductance (Fig. 5.12 and Fig. 5.20). This result hints an engineer to optimize fabrication process so this can be achieved for the recess spacing $L_g/L_{dep} > 5/7$.

5.5-3 V-I Curve Modeling for Gate Recessed GaN/AlGaN HFET

In this section we give the modeling for IV-curves for gate recessed field effect transistors based on Gallium Nitride Heterostructures. This refined model includes the channel thickness and saturation of velocity. In the basic Eq. 3.9 for the drain current, there is only the concept of constant mobility, but in reality and also discussed in literature [5.10] it is necessary to take a model which includes saturation of velocity. One of the models used here is [5.10]

$$v = \mu_{eff} \cdot E(x) = \mu \cdot \frac{1}{1 + \frac{E(x)}{E_{sat}}} \cdot E(x) \qquad (5.4)$$

With $E_{sat} = v_{sat}/\mu$, under the assumption that the total potential between the gate and the drain (V_{ds}) is under the whole gate with length L_g. So we can write equation $E(x) = V_{ds}/L_g$. Using Eq. 5.4 and 3.9 we can write, [5.10]

$$I_d' = \frac{I_d}{1 + \frac{V_{ds}}{L_g \cdot E_{sat}}} \qquad \text{for } V_{ds} \leq V_{ds,sat} \qquad (5.5)$$

Where $I_d = \left(\frac{W}{L_g}\right)\mu C_g\left[\left(V_g - V_{th}\right)V_{ds} - \frac{V_{ds}^2}{2}\right]$ and I_d' is the drain current with the concept of varying mobility. Because we only replace the constant mobility "μ" in Eq. 3.9 to a new Eq. 5.5 based on the concept of varying mobility "μ_{eff}". The region for which $V_{ds} \geq V_{ds,sat}$ is considered to be at constant or saturated electron velocity.

With the mobility, the saturation point is also changed, because

$$\left.\frac{\partial I_d}{\partial V_{ds}}\right|_{V_g \approx const} \overset{!}{=} 0 \qquad \text{for } V_{ds} = V_{ds,sat} \tag{5.6}$$

The Eq. 3.9 holds $V_{ds} = V_g - V_{th}$ but now $V_{ds,\,sat}$ can be calculated as (with parameters E_{sat} or v_{sat})

$$V_{ds,sat} = L_g \cdot E_{sat} \cdot \left\{\sqrt{1 + \frac{2\left(V_g - V_{th}\right)}{L_g \cdot E_{sat}}} - 1\right\} \tag{5.6}$$

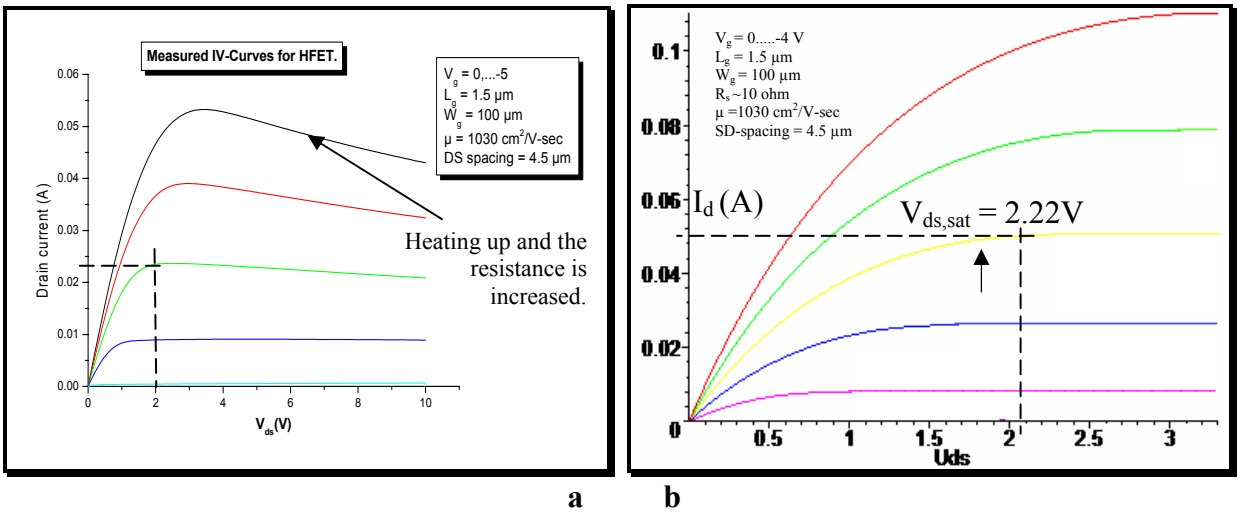


Fig. 5.21: *(a) experimentally measured and (b) simulated IV-Curves for FET with gate length of 1.5 µm.*

For simulation of V-I curves, we used μ = 1030 cm^2/V-sec (Hall-measurements), v_{sat} = 2x10^7 cm/sec and E_{sat} = 2x10^4 V/cm. Fig. 5.21b shows that in simulation of the curves we get $V_{ds,sat}$ = 2.22 V with $I_{d,sat}$ 0.05 A at V_g = -2 V. But for the experimentally measured curves (Fig. 5.21a) shows at V_g = - 2 V, we get $V_{ds,sat}$ = 2 V with $I_{d,sat}$ = 0.023 A. From the above figures we observe that experimentally measured currents are lower compared to simulated ones (Fig 5.21b). The reason for drain current decrease is given on the basis of resistances that are present in a transistor but not in simulated curves [5.10] (see Fig. 5.22a and b)

For higher currents we have even a heating problem.

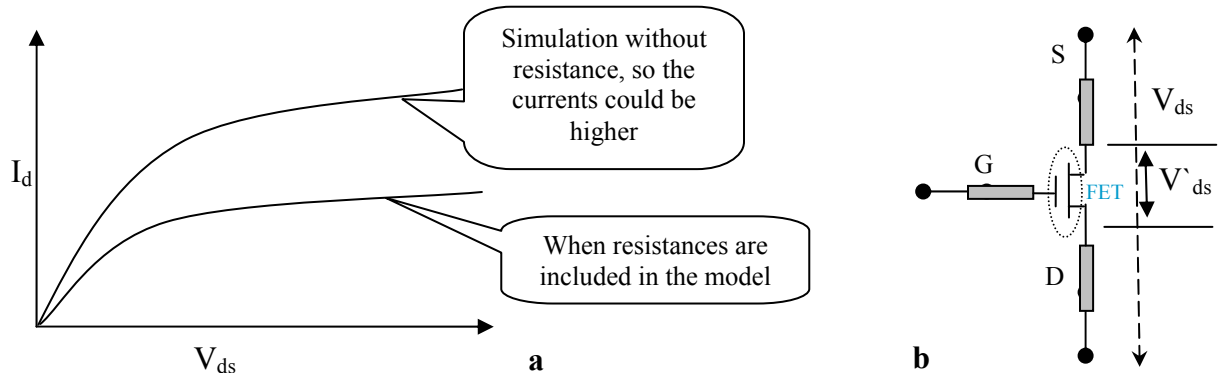


Fig. 5.22: *A schematic diagram explaining why we get lower currents (**a** IV-curves) in experimental situation when FET connected in a network (**b**).*

If the resistances (i.e., source resistance, R_s, and R_{ds}) are included, using the Eq. 5.7 (based on Fig.5.22b), in the simulation of the experimentally measured curves shown in the figure 5.21a, then we get a situation depicted in Fig. 5.23.

$$V'_{DS} = V_{DS} - I_D(R_s + R_d) \qquad (5.7)$$

$$V'_{GS} = V_{GS} - I_D R_s \qquad (5.8)$$

This indicates at V_g = -2, $V_{ds,sat}$ = 1.94 V with $I_{d,sat}$ = 0.020 A, which is approximately equal to that of the measured one.

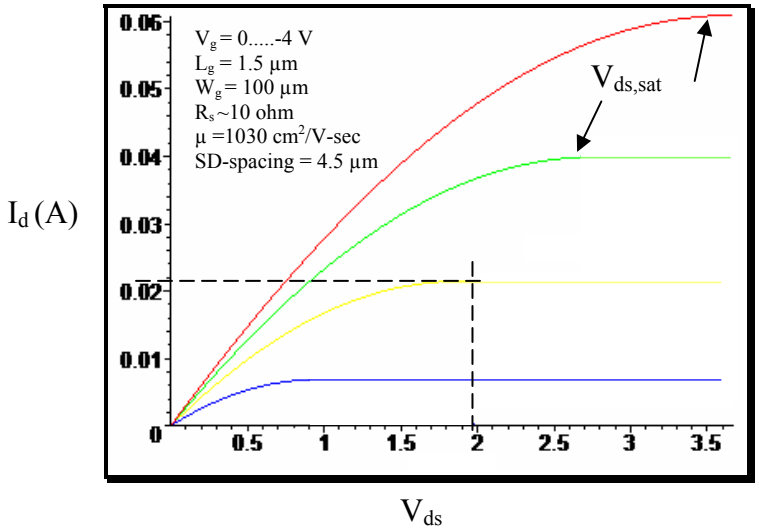


Fig. 5.23: *Simulated V (I) curves for GaN/AlGaN HFET with the resistance included in the characteristics.*

5.5-4 Break down voltage and recess depth

We have also measured the breakdown voltages for our HFETs with gate length of 1.5 µm. Important to note here is the effect of recess depth (sample HB3869c). We have gate recess depths of 6, 12, 18 nm and the inset of device fabrication in Fig.5.24 gives a geometrical parameters of the HFET. We selected the transistors whose parameters are given in Tab. 5.2 with the same recess spacing but with different recess depths. The recess spacing is 6.5 µm. the selection of this family of transistors was based on the gate symmetry where it is in the middle of the source and drain contacts.

The gate length is approx 1.5 µm in all transistors. The breakdown measurements were done at a gate biasing equal to pinch off/threshold voltage for each gate recessed transistor (see Tab. 5.2).

Recess Depth (nm)	Recess Spacing (µm)	Gate Length (~µm)	Pinch off Voltage (-V)	Breakdown Voltage (V)
No recess	6.5	1.5	6	88
6	6.5	1.5	5	75.6
12	6.5	1.5	3.1	88.79
18	6.5	1.5	2.4	69.4

Tab. 5.2: *the experimental setup at which we have measured the breakdown voltages for gate recessed HFETs.*

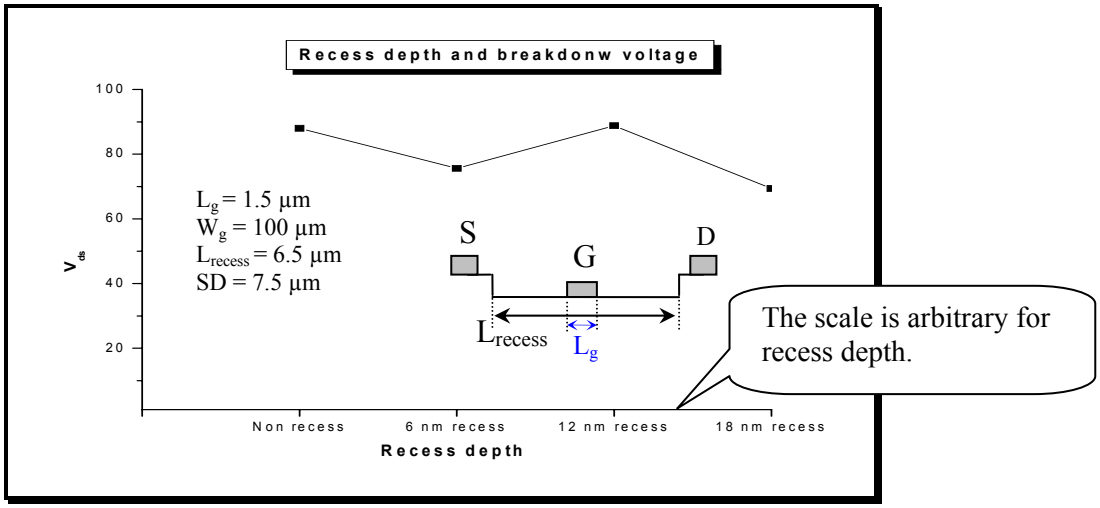


Fig. 5.24: *Graph between gate recess depth and breakdown voltage of HFET with same recess spacing and gate length.*

Fig. 5.24 shows that the breakdown voltage decreases slightly (~ 70 V) with recess depth. The transistors with recessed gates show slightly lower breakdown voltages when compared to non recessed ones. But there is no clear result. This could be due to a wide recess spacing, which seems to be the more important parameter rather than recess depth in gate recessed HFET performance.

Another point observed in the experiment was, that the breakdown for the transistors having smaller recess spacing (2.5 µm) compared to the above mentioned ones (6.5 µm) was higher. These transistors can withstand a drain source voltage up to 100 V. But precisely speaking the voltage drop along the gate would be reduced by the potential drop across the source resistance (calculated in section 5.4-3). Fig. 5.25 shows another transistor with smaller recess spacing (2.5 µm) that withstands higher drain source voltage.

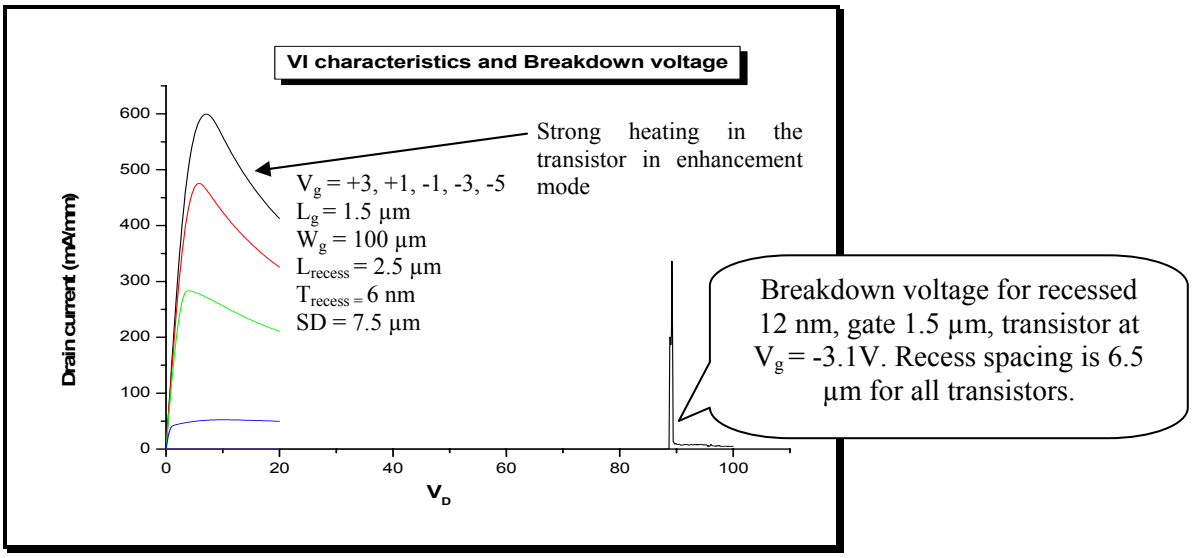
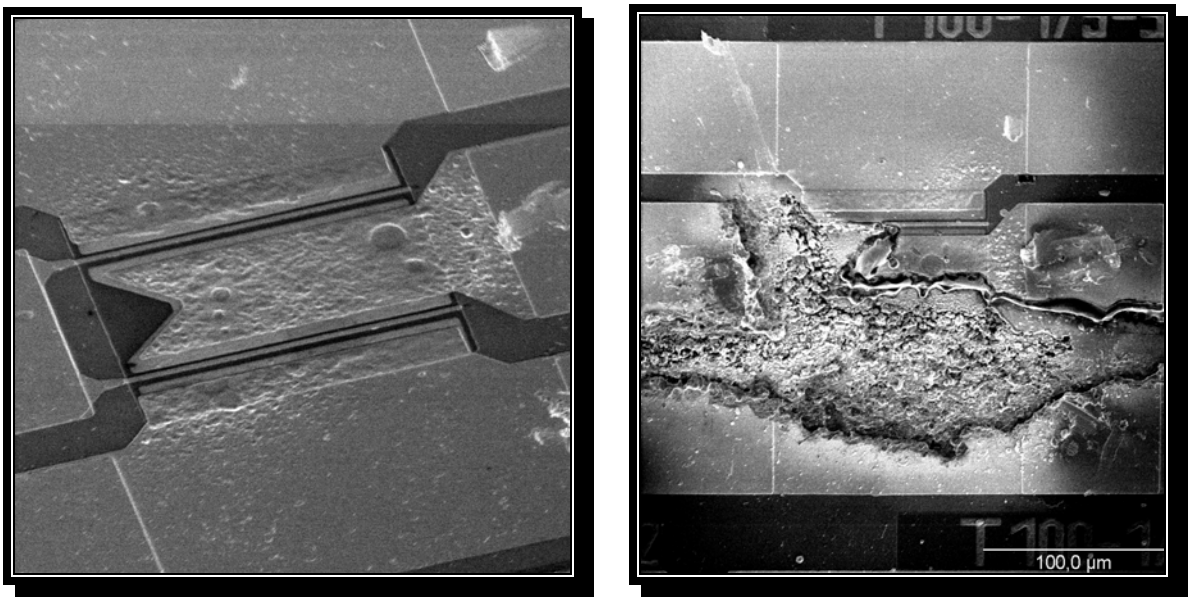


Fig. 5.25: *Breakdown voltage for one of the selected family of gate recessed transistors. VI curves with $V_{ds} \leq 20$ V are also shown.*

The calculated breakdown field is in a wide range with variations that could be depending on recess depths and gate drain distance. For non recessed devices the calculated breakdown field is comparable to literature (~ 66MV/m) [5.4]. This leads to increase in resistance and consequently reduces the drain current.

In Fig. 5.26 we show a SEM pictures for the transistors before and after the breakdown measurement. It is interesting to observe the destroying strength of fields created between the gate and the source due to the ohmic heat. The electric field is high enough, depending on the

gate drain spacing, that it can melt the gate, drain and source metals and even damage the substrate area under these metal contacts.



a b

Fig. 5.26: *SEM photos for transistors (a) before, (b) after breakdown measurement*.

5.6 TEMPERATURE TREATMENT

In this work the effect of temperature treatment (annealing) on the transistor performance was also investigated. Transistors in a virgin state (after complete fabrication and ready to be electrically characterized) were characterized to I_d and g_m, etc… Then to test the devices, they were temperature treated at 550 °C for one minute in N_2 environment. The results show an increment in transconductance from the virgin state measurements as seen in Fig.5.27. Here the reference transistors, which are none recessed, show little variation but remain same in transconductance before and after temperature treatment. As also observed in [5.7], [5.8]. One reason could be given as the temperature treatment may change the surface states or may remove the defects caused by a gate recess in the recessed transistors. Temperature treatment probably affects ohmic behavior [5.8], but observing the slightly affected non recessed transistors, we can say the main effect to improve gate recessed transistor performance could be only due to removal of surface effects [4.8]. There could be changes in surface charges, forming a space charge domain, that are aligned after temperature treatment and causing a reduction in scattering

of free electrons (2DEG) or enhance the mobility of electrons leading to an increase in channel current.

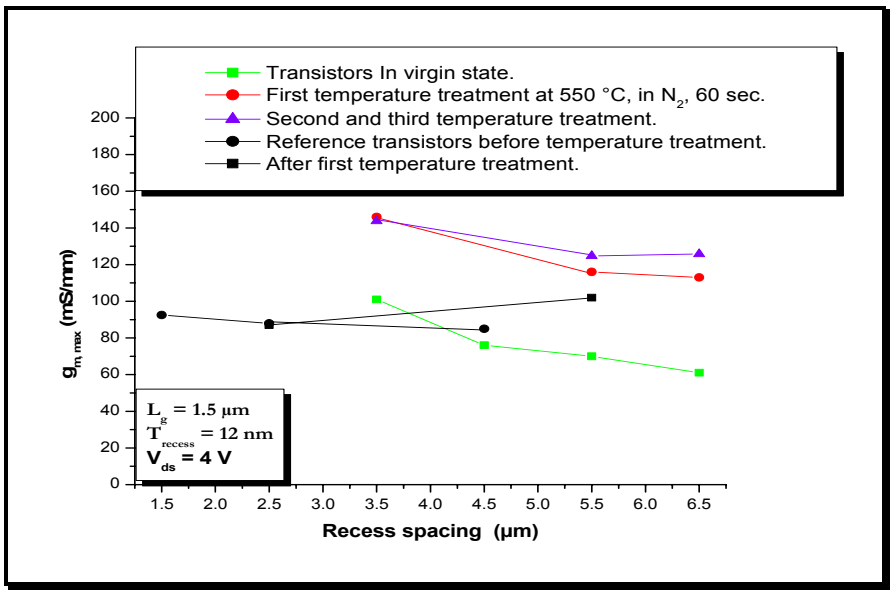


Fig. 5.27: *Improvement in g_m as a result of temperature treatment in N_2 environment at 550 °C for one minute per step*

The Fig. 5.27 shows quite nicely that before the temperature treatment the transconductance of FET with recess 12 nm and a gate length of 1.5 µm, was nearly 100 mS/mm but after the first time treating the sample with temperature at 550 °C in N_2 environment in Rapid Thermal Annealler the transconductance increased to approx 150 mS/mm. This effect we have also observed for the other transistors of the same sample HB3869c.

5.7 HF- Characterization

GaN is highly promising for high power transistors operating at microwave frequencies [5.9],[5.13]. The characterization of high-frequency transistors is an important and sometimes difficult task. The difficulty primarily stems from the fact that the performance of a device in a circuit can depend upon the circuit in which it is placed. High-frequency transistors are characterized by a gain function measured from a carefully calibrated HF-measuring setup, (see chapter 3 section HF-characteristics modeling).

There are some intrinsic quantities like the drain to source conductance G_o and drain-gate capacitance C_{dg}, but two other important resistive parasitic elements are inevitable. These are

gate resistance R_g, which represents the resistance of the gate electrode(s), and the source resistance R_s, which represents the series resistance of the source ohmic contact and the semiconductor material between the gate and source electrodes. Using these physical quantities we can relate the maximum frequency $f_{max,}$ [3.5] and transit frequency f_t as shown in Eq. 5.7. The transit frequency f_t for a transistor is the frequency at which the forward current gain h_{21} extrapolates to one. (Already discussed in the section 3.3-2 of chapter 3)

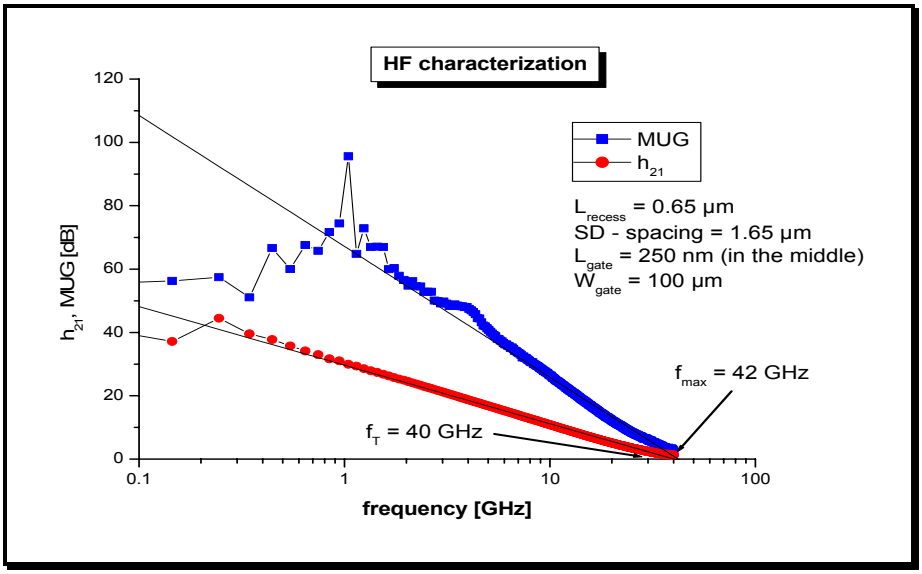


Fig. 5.28: *HF characteristics for a gate recessed GaN/AlGaN HFET fabricated on Sapphire substrate.*

$$f_{\max} = \frac{f_T}{2\left[G_o\left(R_g + R_s\right) + 2\pi f_T C_{dg} R_g\right]^{1/2}} \tag{5.9}$$

In Eq. 5.9, the drain-gate capacitance C_{dg} also represents the gate recess depth in HFET. With a gate recess we change the capacitance which is one of the controlling parameters in the Eq. 5.7. In Fig. 5.28 we have a HF characterization of a gate recessed GaN/AlGaN HFET. The transit frequency f_t is 40 GHz, which is our best result in this series. Transit frequency f_t can be related with the saturation velocity v_{sat} and gate length L_g as in Eq.5.10 (already discussed in chapter 3).

$$f_t = \frac{g}{2\pi C_{gs}} = \frac{v_{sat}}{2\pi L_g} \tag{5.10}$$

From the interpretation of the above equation, we can calculate the real gate length. In the HF-characteristics, we observe the transit frequency is 40 GHz. Taking this measured value of transit

frequency and v_{sat} = 2x10^7 cm/sec [1.3], the resultant gate length differs from the actual or real length. The reason could be the effect of additional gates which might become effective after etching a gate recess due to the significant changes in the surface states in the recessed region L_{recess} and where the gate metallization is done.

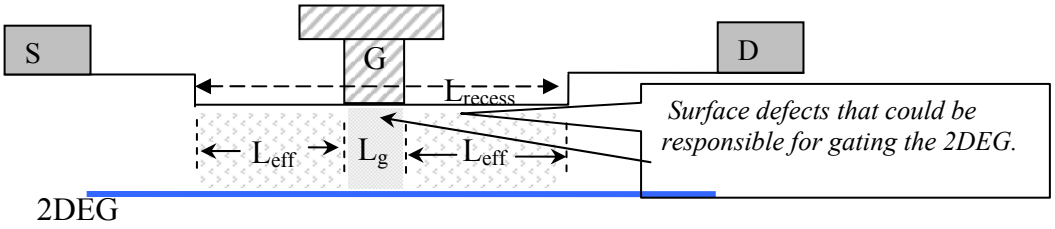


Fig. 5.29: *A schematic diagram for the surface states in recess region and under a gate that could affect the HF-characteristics of GaN/AlGaN HFETs.*

Therefore, due to these additional effective gates (see Fig.5.29) which also limits the saturation velocity of electrons in 2DEG (Eq. 5.10), we observe the transit frequency is reduced. We see also in Eq. 5.9, due to high series resistance of gate R_g, and source R_s, the maximum frequency is reduced and becomes nearly equal to the transit frequency f_t of the Field Effect Transistor for higher frequencies (as it is in our case).

Chapter 6

Summary

My work was focused on the fabrication of *gate recessed Field Effect Transistors* based on Gallium Nitride Heterostructures. According to the past investigations on recessed gate FETs in the GaAs/AlGaAs material system some improvements (drain current, transconductance, HF-performance) could be expected also for the GaN/AlGaN material system. But these are not clearly confirmed up to now. The devices grown on sapphire (0001) possessing doped and undoped AlGaN spacer layers were fabricated and characterized. The device layers were grown by MOVPE (Metal Organic Vapor Phase Epitaxy). Vertical transistors with different geometrical parameters were fabricated to analyze *the effect of recessed gates* on the device performance. Mainly drain current and transconductance were analyzed with and without recess and variation in recess spacing. Some of the results obtained from the characterization of HFETs are in agreement with theories. One example is the variation of recess spacing: (for smaller *recess spacing* with a constant gate length), I_d and transconductance of a FET increases. Similarly if the source drain spacing is decreased, we see also the expected result of an increase in I_d, and g_m. From a series of different recess spacings we found a value of $L_{recess} \leq 3L_g$ at which the devices are working better in the recessed case.(see chapter 5).

Recess depth is a key in GaAs/AlGaAs HFETs to enhance transconductance and in the other way to reduce the device threshold voltage. Transistor with different recess depths (6, 12 and 17 nm) were also a part of this analysis. The transconductance should increase with recess geometries. With recessed gate HFETs (undoped) and gate length in optical regime (L_g = 1.5 µm) we obtain the highest $g_m \mid_{Vds\,=\,10v}$ = 140 mS/mm at a recess spacing of 3.5 µm and recess depth of 12 nm. Where as for the recessed gate (doped with Si) and *T-shaped gates* with length in e-beam lithography regime (L_g = 250 nm) the highest $g_m \mid_{Vds=10v}$ = 280 ms/mm at recess spacing of ~160 nm and recess depth of 12 nm. The devices also show high I_d upto 1000 mA/mm with positive gate biasing of 3V. Fig. 5.6 is a good representation for drain current.

In the case of transconductance of devices versus recess depth we face a little problem with source resistances. In principle, as there in literature, g_m should increase after etching a gate

recess. It is a critical step in fabrication of HFETs as it controls the channel conductance. Our structures have more parasitic resistances which play a significant role in determining the device characteristics specially g_m. These are going to increase and probably are the reason for reduction of transconductance with recess etching. (Eq. 5.1)

A recessed gate also determines the *gate leakage current* in a device. The devices, characterized as a function of *threshold voltage* and recess depth, show good results as that ones seen in literature.[1.3] (Fig. 5.13)

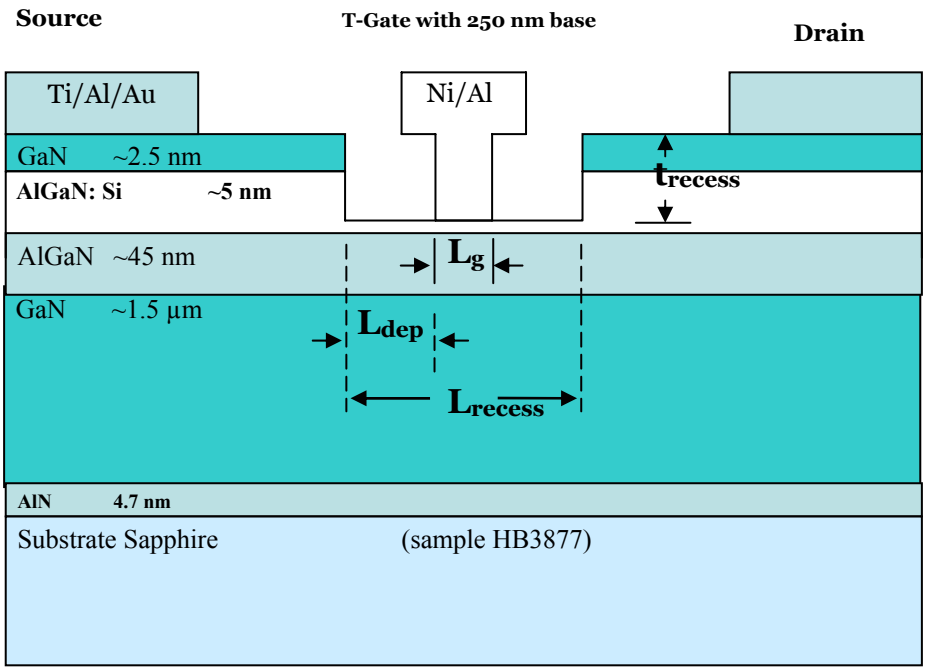
An important conclusion for the GaN/AlGaN HFETs is seen from Fig. 5.12. This figure depicts an idea for the device processing with respect to recess spacing and shows what can be done with gate recess in GaN/AlGaN for the improvement of the gate-recessed device performance. There is not always improvement, even if the gate is placed correctly. One can have advantage and disadvantage depending on the L_g/L_{recess} ratio and recess depth. The same conclusion, the improvement in transconductance of FET, can be seen in Fig. 5.20, where the total resistance is plotted with respect to recess spacing. From these figures, we can say that these parameters (recess depth, and recess spacing) are much tighter in GaN than in GaAs, possibly due to the surface states in GaN which are not present in GaAs. Furthermore, we can say these results, with respect to recess spacing L_{recess}, are new and were observed experimentally.

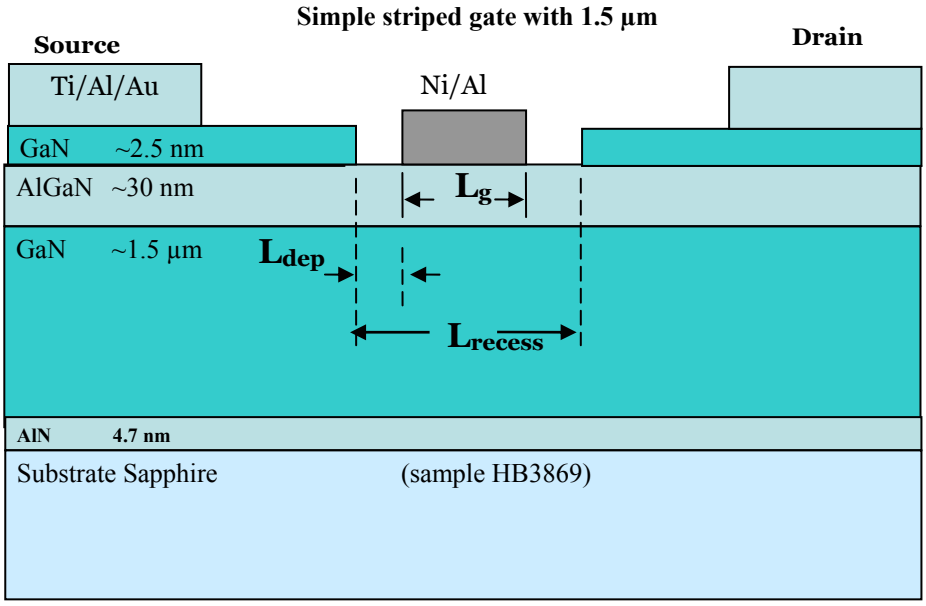
GaN is highly promising for high power transistors operating at microwave frequencies. We have seen that GaN HFETs possess a large potential for high power application and high frequency performance as well (Chapter 5 section 5.7).

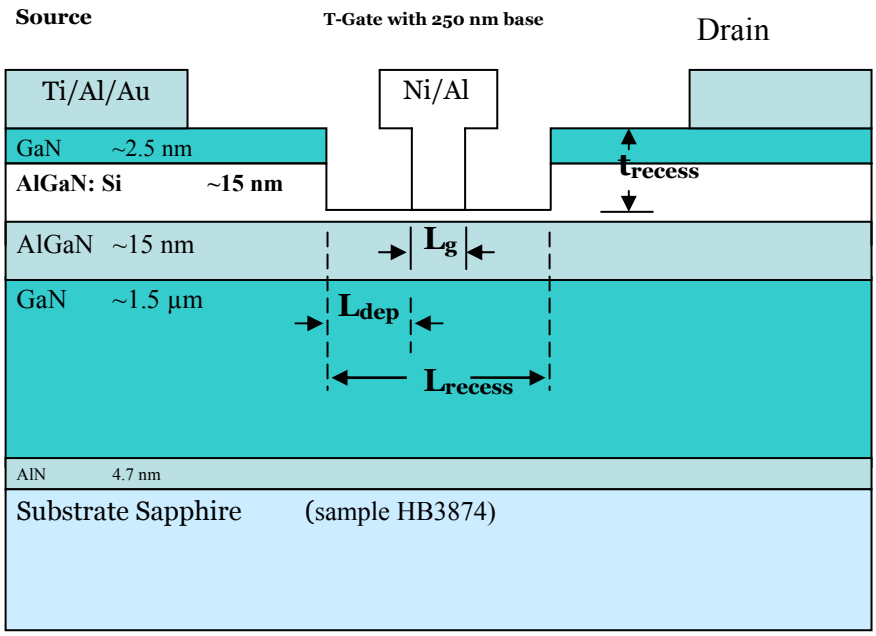
Future prospects of recessed gate technology in GaN/AlGaN HFETs depend on many factors. Some are very important like doping the spacer layer with donor impurities, reducing the source resistance R_s by additional contact layer on AlGaN, suitable annealing strategies after the metallization in the fabrication process and well precise e- beam lithography is playing a key role. A little miss-alignment in positioning a cross could lead to miss-aligned recess that in turn is responsible for a deviation from good characterization of that device. Surface defects, etching profiles with ECR-RIE, inherited defects in GaN, and well-positioned gates in the recess are some important aspects which have to be considered.

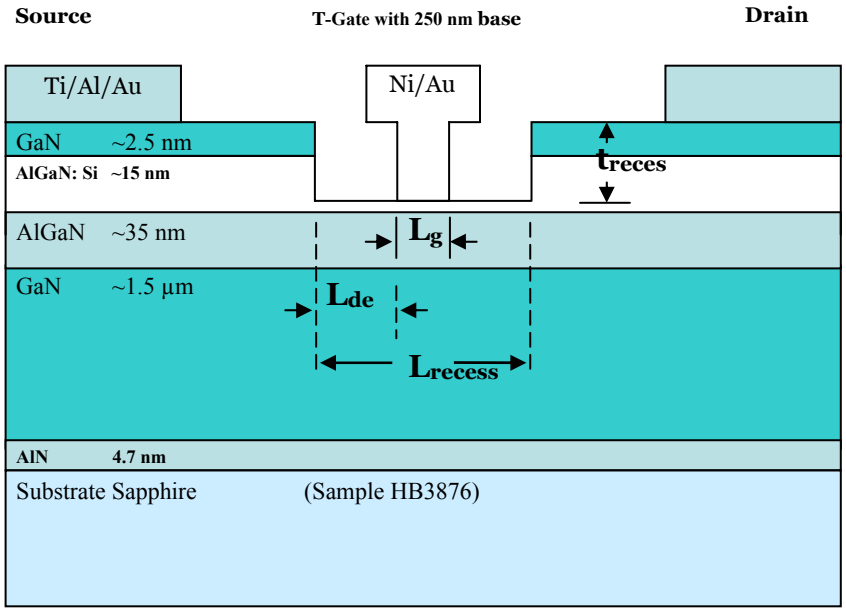
Appendix A

Layer Structure of GaN/AlGaN HFETs






Source
T-Gate with 250 nm base
Drain
Ti/Al/Au
Ni/Al
GaN ~2.5 nm
AlGaN: Si ~15 nm
AlGaN ~15 nm
GaN ~1.5 µm
AlN 4.7 nm
Substrate Sapphire
(sample HB3874)
t_{recess}
L_g
L_{dep}
L_{recess}


Source
T-Gate with 250 nm base
Drain
Ti/Al/Au
Ni/Au
GaN ~2.5 nm
AlGaN: Si ~15 nm
AlGaN ~35 nm
GaN ~1.5 µm
AlN 4.7 nm
Substrate Sapphire
(Sample HB3876)
t_{reces}
L_g
L_{de}
L_{recess}

Appendix B

Layout of HFET

Fig.B.1 shows a layout of typical Pi-gate FET grown on GaN. The name Pi-gate is due to the shape of gates. For optical and e-beam structures the difference is in the recess lengths, gate lengths and source drain spacing. The geometry of the structures is nearly same. Optical lithography structures are

Range of gate length	= Fixed to 1.5 µm
Range of recess length	= 1.5 µm to 7.5 µm (at SD = 7.5µm)
Range of source drain spacing	= 3.5 µm to 9.5 µm (at L_{recess} = 3.5 µm)
Width of a transistor	≈ 100 µm, (and for also e-beam transistors)

Where as the specifications for e-beam HFET, with same geometry, but

Range of gate length	= fixed to 250 nm
Range of recess length	= 160 nm to 2.60 µm (at SD = 2.6 µm)
Range of source drain spacing	= 1.15µm to 4.15 µm (at L_{recess} = 650 nm)

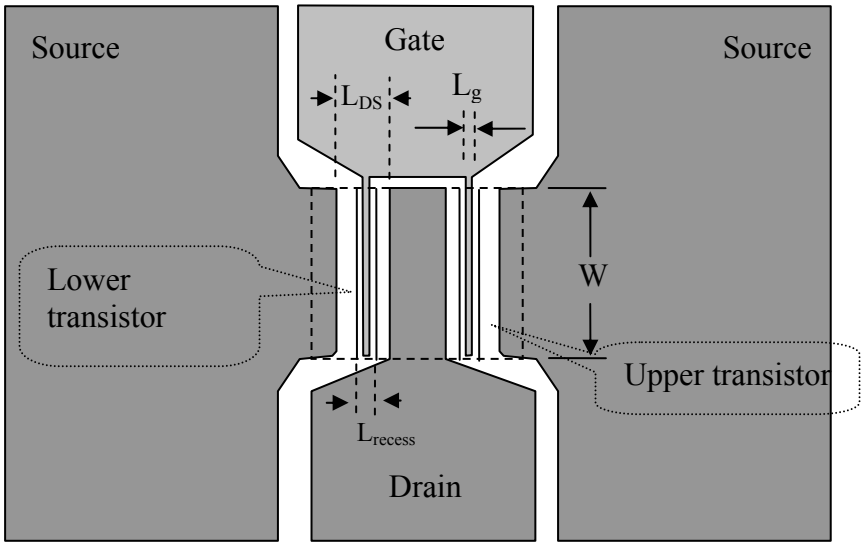


Fig.B.1. *Layout of GaN/AlGaN HFET grown over Sapphire. This kind of mask is often called Pi-mask and the transistors are Pi-gate HFET.*

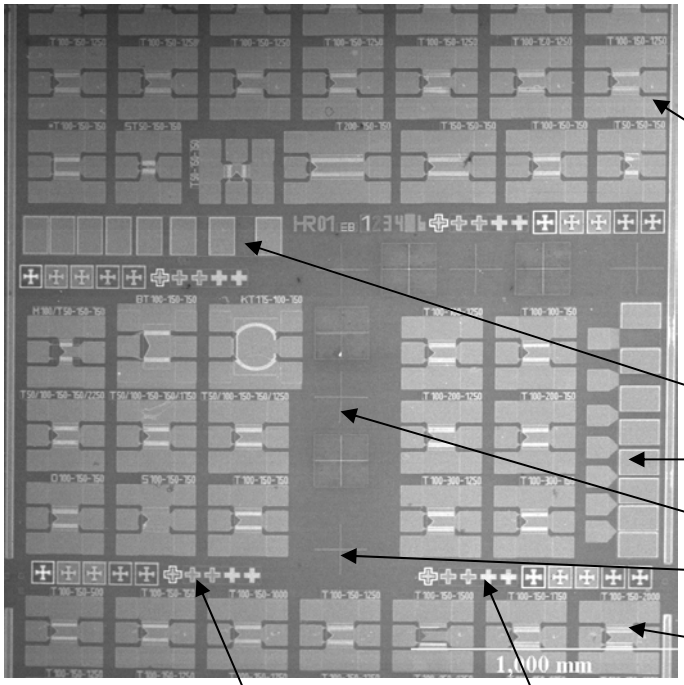


Fig.B.2 *SEM photograph of sample 3874, TLM structures are also fabricated to measure the contact resistance. The contact pad size is 100x150 µm*^{2}.

Appendix C

Lithographic process details

Masking for structure	Processes required.	Parameters	Remarks!
1-Optical Ohm. Negative process.	Photoresist	Both	HMDS, Az5214E
	Spin	200*10 for 5sec 600*10 for 40sec	
	Soft bake	90 °C for 90 sec	
	Boarders expose	5 sec	Varied if necessary
	Development	2:1 (Az: water) for 45 sec.	
	Structure Expose	1.5 sec*	
	Bake	120 °C and 60 sec	
	Flood expose	15sec	
	Development	1:1 (Az: water) for 30 sec	

After this optical ohm step, the sample is ready for the deposition of metallization of Ti/Al/Au the parameters for the metallization can be seen by the reference booklet.
After METALLIZATION

Liftoff	Put is Acetone		
	Clean with propanol.		
	Dry with Nitrogen.		

Alloying	Gases system	Use OB870.1	
	Recipes	Open N_2	
	Time	Turn on the pump.	
	Cleaning + Dry N_2		

2-Mesa Positive process.	Photoresist.	Both	
	Spin.	Same as in first	
	Soft bake.	90degrees for 90 sec	
	Borders expose.	8 sec*	
	Development.	2:1 (Az: water), 45-60sec.	
	Mask for mesa.	3.5-4 seconds	
	Development.	1:1 for 40 sec.	
	Hard bake.	100 °C for 60 sec 155 °C for 120 sec	
	ECR-RIE		
	Removal of Photoresist.		
	Depth by Daktalk.		
	Clean		

3-Contact Negative process.	Photoresist	Same	
	Spin	2000, 5sec; 6000, 40 sec	
	Soft bake	90 degrees for 90 sec	
	Border expose	5 sec	
	Development	2:1 Az and water 45sec	
	Mask for structures.	1.5 sec.	
	Bake	120 °C for 60 sec	
	Flood expose.	15 sec*	
	Development	1:1 Az and water.30sec	
Metallization.	Cr/Au	20/500nm. Take ref. book	
Lift-off		Warm Acetone, Propanol.	
Oven bake.			

Negative Process. **4-Pads**	Photoresist	Same	
	Spin	Same as first	
	Bake	90 degrees for 90 sec	
	Boarders expose	1.5 sec*	
	Develop	2:1 Az and water	
	Mask for pads.	1.5 sec	
	Bake	120 degree for 60 sec	
	Flood expose	15 sec.*	
	Development for structure.	1:1 Az and water. For 30sec	
Metallization.	Cr/Au.	20/500 nm using parameter for usual.	
Lift-off		Acetone and Propanol.	

5- Optical, e-beam Recess. Positive Process. .	Photoresist	Same	
	Spin	2000 and 6000	
	Bake	90 degree for 90 sec	**I can process thrice for different depths**
	Borders expose	8 sec*	
	Development	2:1 (Az: Water) 45-60 sec.	
	Masking for recess	3.5- 4 sec	
	Development	1:1 for 40 sec	
	Bake hard.	100C for 60 sec, 155C for 120 sec.	
Ion beam etching.	Ion beam etching		
Removing ,cleaning	Acetone + propanol		

6-Optical, e beam gates Positive Process.	Photoresist	Same	
	spin	2000 and 6000; 5, 40 sec	
	Bake	90 C for 90 sec	
	Border expose	8 sec	
	Development	2:1 (Az:water) 45-60 sec	
	Making expose	3.5 –4sec *	
	Development	1:1 for 40 sec	
Metallization By E-Gun.	Ni/Au	100/150 nm	
Liftoff	Liftoff.	Acetone -Propanol	

Now in the end Clean and Dry the sample with the usual way.

Again clean and dry

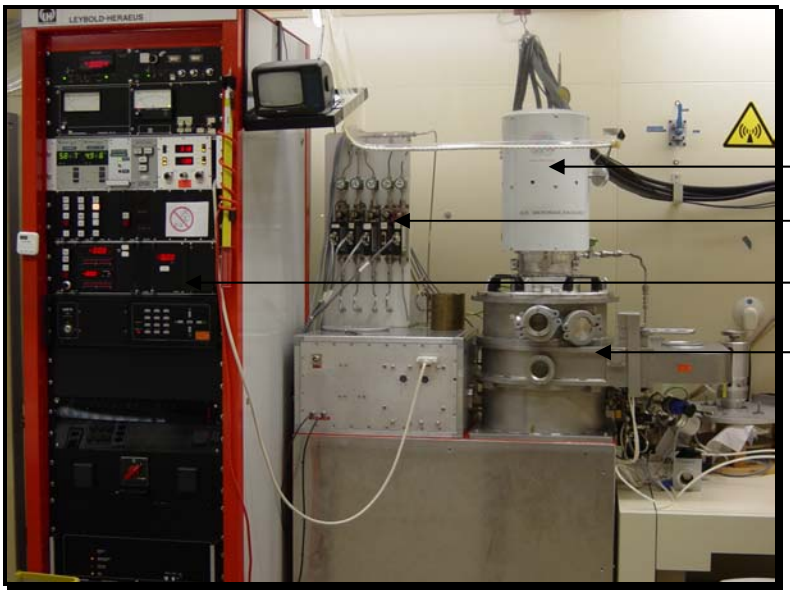
Put into oven

And for pads or contact make the steps again like in pads step. Photoresist, spin, bake and all like pads formations.

* are the parameters that can be varied according to the lithographic results.

Appendix D

Instruments



ECR-RIE
TePla
Plasma Technics GmbH

Ion source

Gas controls

Computerized controls

Sample holder

Metallization chamber
3119- Microelectronics

Vacuum chamber and sample is hanged on ceiling.

Computer controls for thickness of layers

Window to view the sample

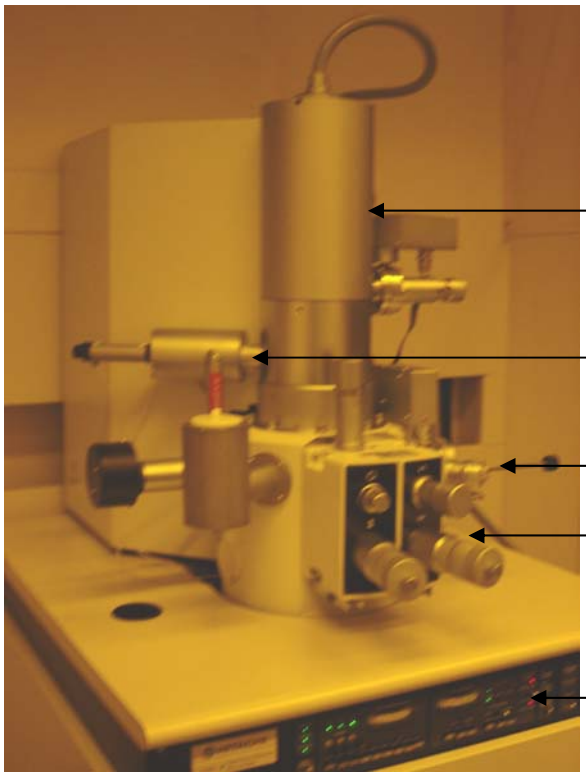
Manual controls for metallization

E-Gun metallization chamber.
Pfeiffer Vacuum PLS 500

Deposition controls

Window to view the sample

Power supply



Electron Microscope
Hitachi S800

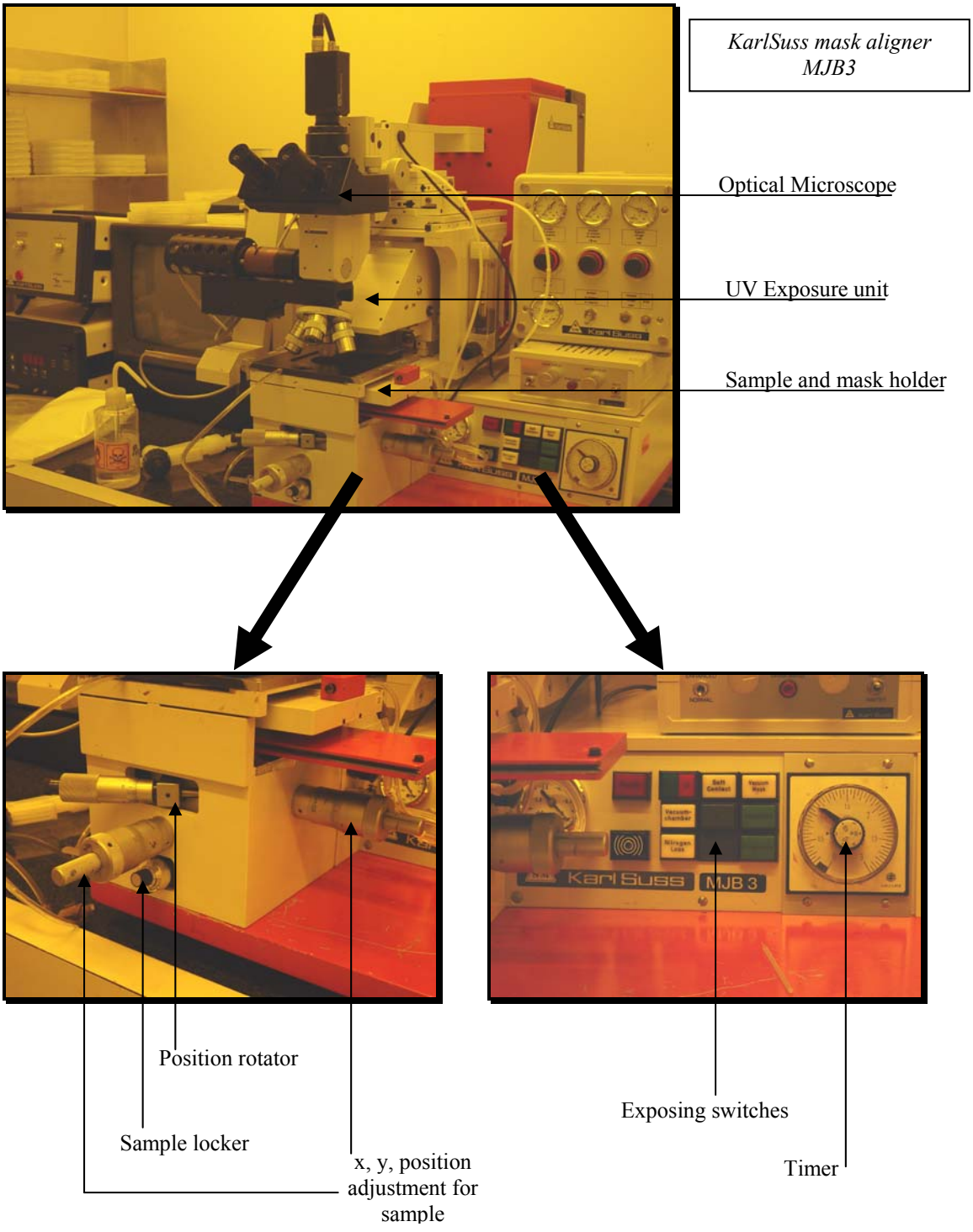
Electron source

Electrostatic optics

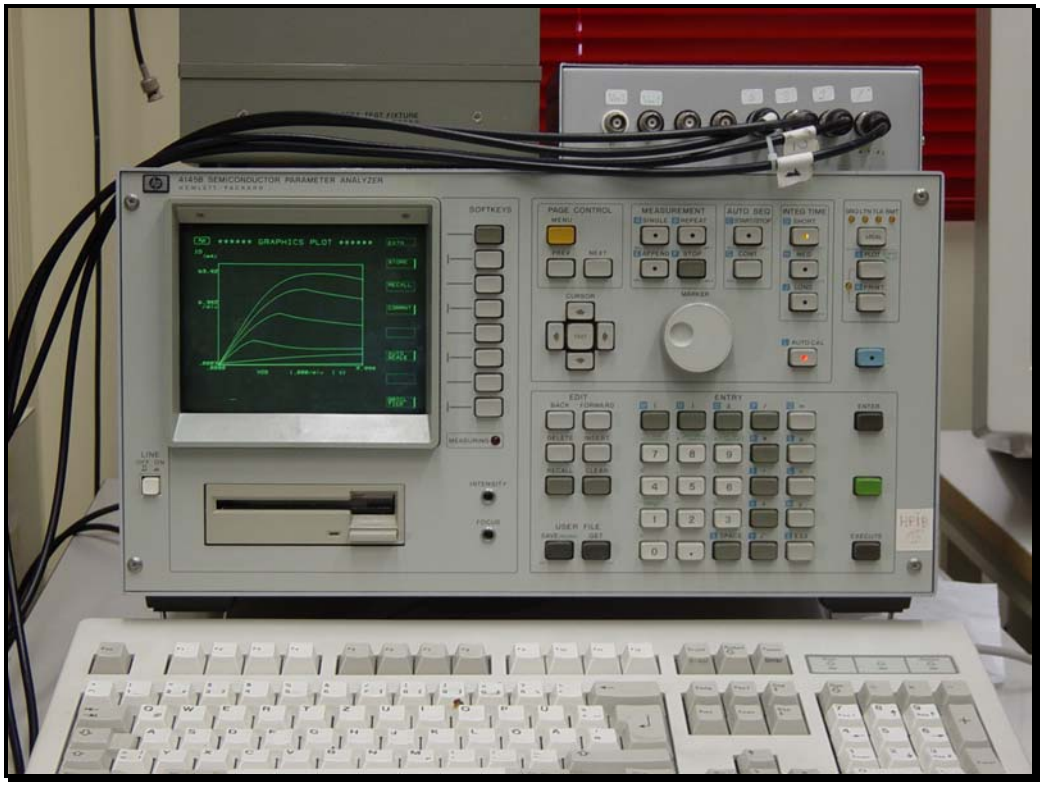
Sample driver

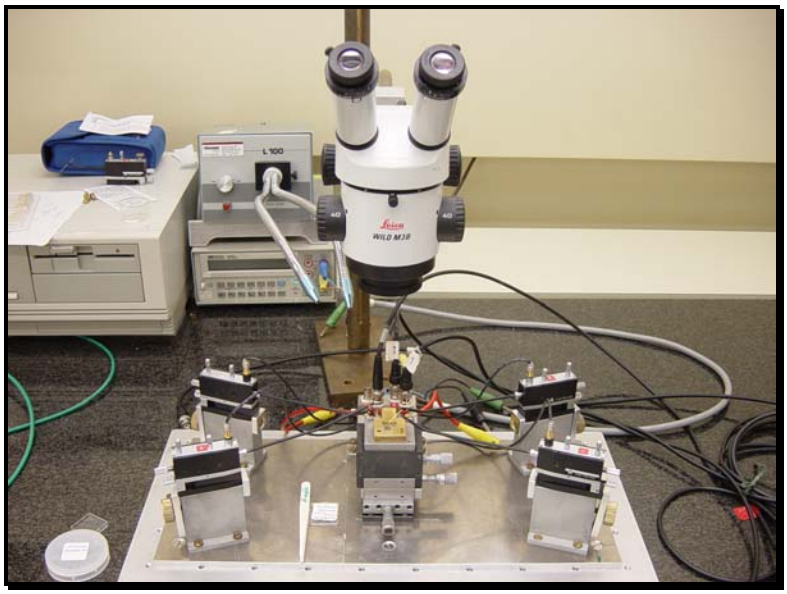
Orientation changers

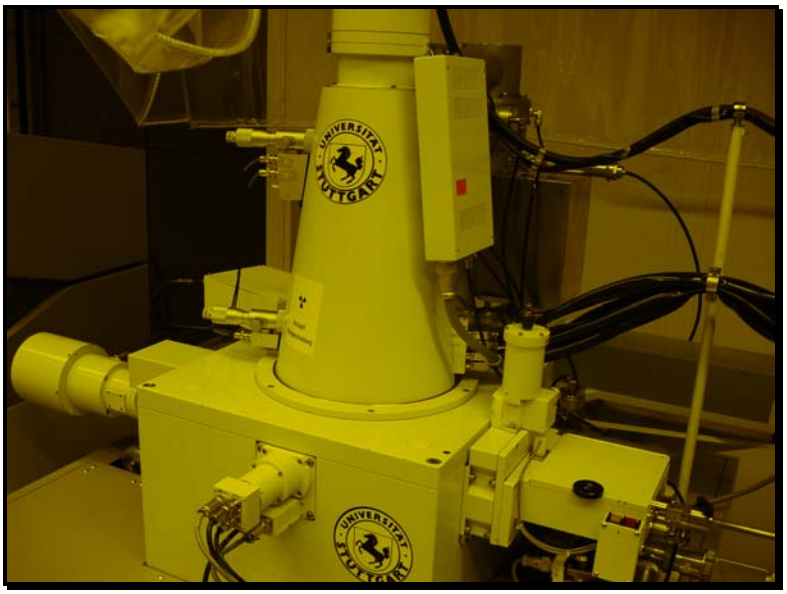
Controls for openings sample chamber and changing the sample



Semiconductor Parameter Analyzer HP 4145B, shown with 4 probe station set for the analysis of different device parameters.


4145B SEMICONDUCTOR PARAMETER ANALYZER
HEWLETT-PACKARD
SOFTKEYS
PAGE CONTROL
MEASUREMENT
AUTO SEQ
INTEG TIME
GRAPHICS PLOT
EDIT
ENTRY
USER FILE


L 100
Leica
WILD M3B



Electron Beam Lithography System JBX-5DII (U)

Photos: courtesy of Micro Structure Laboratory, 4th Physics institute, Stuttgart University.

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Chapter 5 Device Characterization of Gate recessed HFET

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Thanks

I completed my thesis in Microstructure Lab of 4th Physics Institute of Stuttgart University from 8th of Feb, 2002 to Feb, 2003. I worked on Gallium Nitride field effect transistors. The title of my MSc thesis is "Technology and Physics of gate recessed GaN/AlGaN HFET".

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