Institute of Computer Architecture and Computer Engineering

University of Stuttgart
Pfaffenwaldring 47
D–70569 Stuttgart

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Simulation-Based Analysis For NBTI Degradation In Combinational CMOS VLSI Circuits

Zdravko Georgiev

Course of Study:	Information Technology/InfoTECH
Examiner:	Prof. Dr. rer. nat. habil. Hans-Joachim Wunderlich
Supervisors:	Chang Liu, M.Sc., Michael Kochte, Dipl.-Inf.
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Abstract

The negative-bias temperature instability (NBTI) is one of the dominant aging degradation mechanism in today Very Large Scale Integration (VLSI) Integrated Circuits (IC). With the further decreasing of the transistor dimensions and reduction of supply voltage, the NBTI degradation may become a critical reliability threat. Nevertheless, most of the EDA tools lack in the ability to predict and analyse the impact of the NBTI. Other tools able to analyse the NBTI, are often on very low design level and requiring significant computational resources.

The purpose of this master work is to analyse the impact of the NBTI aging degradation in the combinational part of VLSI CMOS circuits. For that purpose, a gate-level NBTI simulation flow for estimating the degraded circuit performance parameters is proposed and implemented. The flow is NBTI model independent and tool independent. A particular implementation is made based on the Reaction-Diffusion NBTI model, and the tools: HotSpot 5.0, Candance Encounter, Synopsys Design Compiler, Synopsys Prime-Time. The results of the NBTI simulation are outputted in the format of statistical data of the gate delay degradation, the critical path delay degradation and length change, and the power consumption change. In addition, a heatmap visualizing the delay degradation is generated.

Finally, a set of simulations are performed on circuits from the ISCAS89 and NXP benchmark suits. The statistical data are presented, and the impact of the NBTI degradation is analysed.

1 Introduction

The electronic industry is one of the most quickly developing industry in the past five decades. One of the examples of how rapidly this industry is progressing is the Moor's law prediction that the number of transistors in integrated circuit (IC) doubles every two years (Figure 1.1).

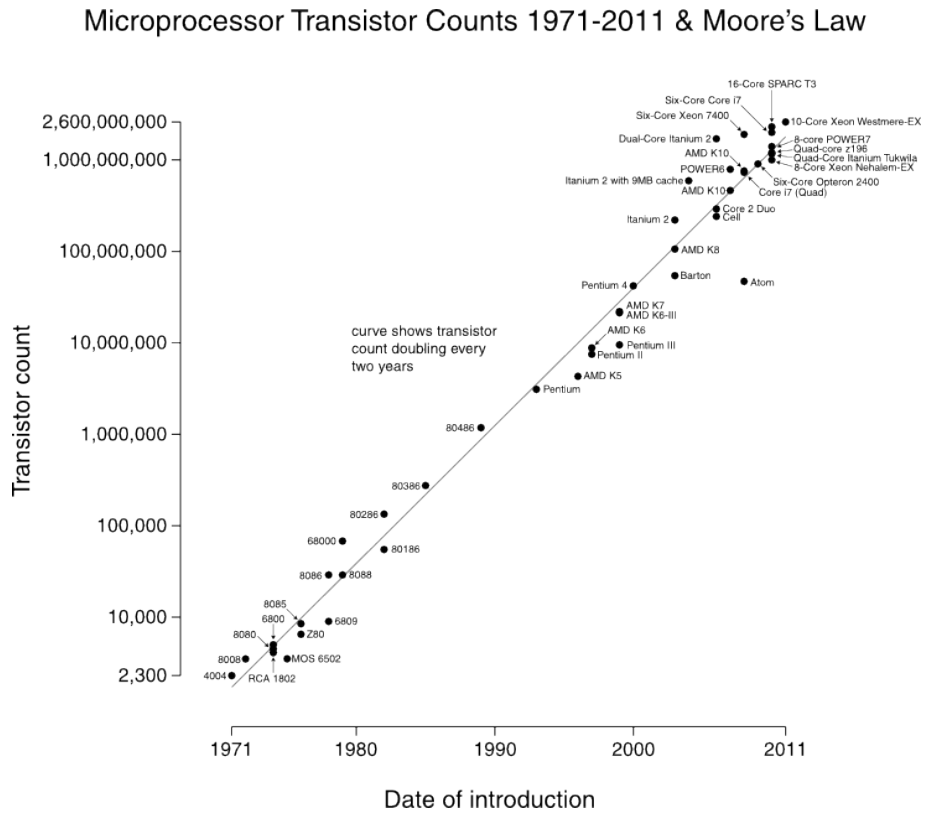


Figure 1.1: Moor's Law

When Gordon Moor issued his paper in 1965, the number of elements in a single IC was 50 [15]. At that time electronic devices such as home computers, automatic control for automobiles and personal portable communication equipment considered as basic attributes today, were called wonders. Almost five decades later, 22nm tri-gate transistor technology allows the incorporation of more than 2.9 billion transistors in a single IC [2]. The presence of so many elements integrated in a microscopic scale put some serious questions about the reliability of the IC even back in 1960. For a long period of time the idea of a circuit containing tens of elements was rejected even by major companies like Bell Labs. The inventor of the transistor

reasoned that in order to achieve 50% yield in an IC with 20 transistors, the manufacturing process must guarantee probability for functional transistor of at least $(0.5)^{1/20} \approx 0.966$ or 96.6%. In 1960, however, this was a rather optimistic percentage [4].

The invention of the lithographic process and planar-epitaxial technology allowed very high values of yield to be achieved. That made the mass production of IC electronics possible, but did not guarante the correct working of the device for the announced life-cycle. Even a perfectly manufactured IC with almost no defects is subject to different kind of failures. In 1960 such a failure - the electromigration - almost did not stop the emerging IC industry [19]. Other failures such as the hot carrier injection (HCI), time dependent dielectric breakdown (TDDB), and the negative bias temperature (NBTI) were later discovered and shown to effectively shorten the life-cycle of the MOSFET transistor.

Transistor failures can be divided into two different categories: metal and oxide failures (table 1.1).

Failure Category	***Failure Mechanism***	***Failure Result***
Metal Failures	Electromigration	Bridging or open defects
	Metal Stress Voiding	Open defects
Oxide Failures	Oxide Soft Breakdown	Higher Level of Noise
	Hot Carrier Injection	Decline in F_{max}
	Negative Bias Temperature Instability	Decline in F_{max}

Table 1.1: Most Frequent Failures in VLSI IC [19]

Most of the failures have progressive development which is connected with an altering of different transistor parameters. That change usually has negative impact on the circuit performance, and therefore is called degradation. The actual failure is revealed when the degradation of a transistor parameter goes beyond certain tolerance limit, contradicting with the system constraints.

Throught the past years a lot of research, work has been done to reduce the different degradation mechanisms both in design and manufacturing phase. Many design techniques to bypass failures and decrease degradations such as adding redundant hardware, clock and power gating, adding guard-band frequency have been developed. Most of the contemporary design tools have integrated design checks and rules for minimizing the parameters of the failures, and are able to automatically correct and optimize the design. In order they to be efficient, a precise information about the degradation progress through the time must be available. Without knowing precisely what is the effect of a failure in a particular circuit, it may be overestimated several times. That would increase the design efforts or even decrease the performance of the device. In the worst scenario the failure may be underestimated, leading to shorter life-cycle.

Degradation mechanisms like electromigration, TDDB, HCI and NBTI are highly dependant on parameters such as the voltage stress, temperature, and frequency. Therefore, the best way to estimate those parameters precisely in a large IC is to monitor them through a netlist simulation. In order to gain maximum benefit from such methodology, the simulation must be compatible with the existing IC development process, and executed relatively fast. Looking

at the Gajski Y-chart (Figure 1.2), which represent the various stages of the digital design, there are two levels at which netlist simulation is possible: gate-level and electrical level.

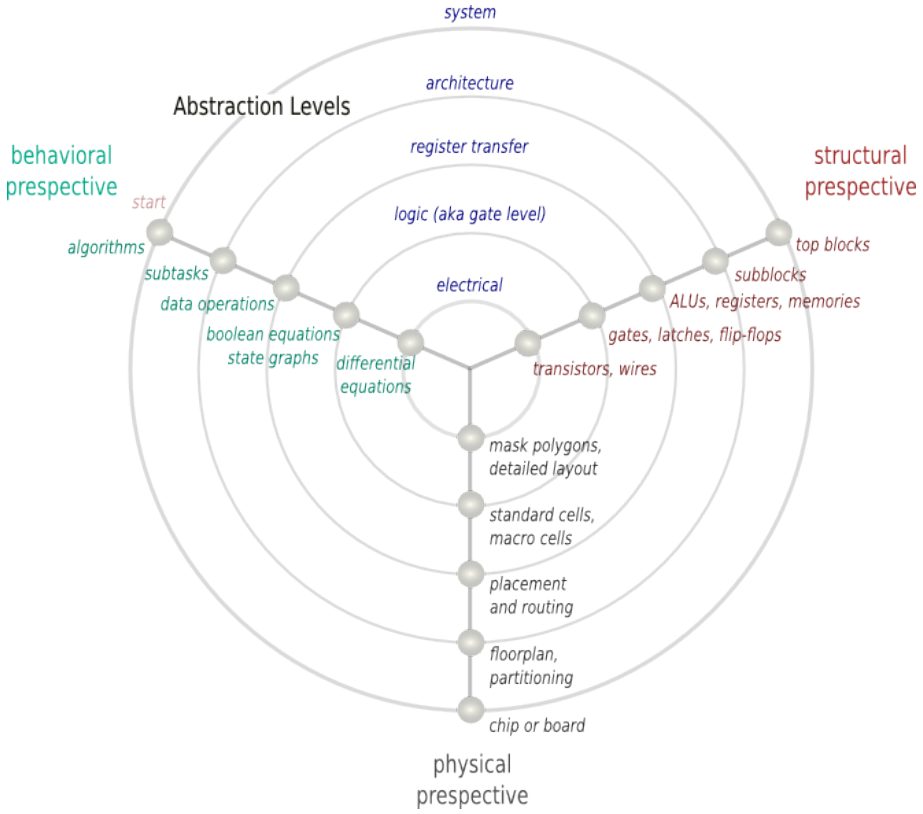


Figure 1.2: Gajski-Kuhn Y-chart. Source [17]

In general, the information needed to estimate the effect of a failure mechanism is transistor specific and technology dependent. Hence, the degradation can be estimated most precisely in the electrical level. Two problems are arising when such a simulation must be implemented:

1. Electrical level simulation is not a standard stage in the design flow,
2. Electrical level simulation requires significant amount of computational power.

In figure 1.3 is shown an exemplar design flow of a digital IC using an industrial tools for electronic design automation (EDA) provided by Synopsys and Cadence.

Among the simulation stages there are two gate-level simulations: functional simulation, which is on RTL level; and a fault simulation, which is also a type of gate-level simulation using circuit netist as input [21]. One of the main reasons that the electrical level simulation is not added to the design flow is the type of data processing required. If we look at the Y-chart, we may see that the behavioural description of the electrical abstract level is done by differential equations. In order to complete a circuit simulation the simulator must be capable to solve a system of non-linear differential equations. That is usually done by a SPICE simulator and takes significant amount of computational time [17].

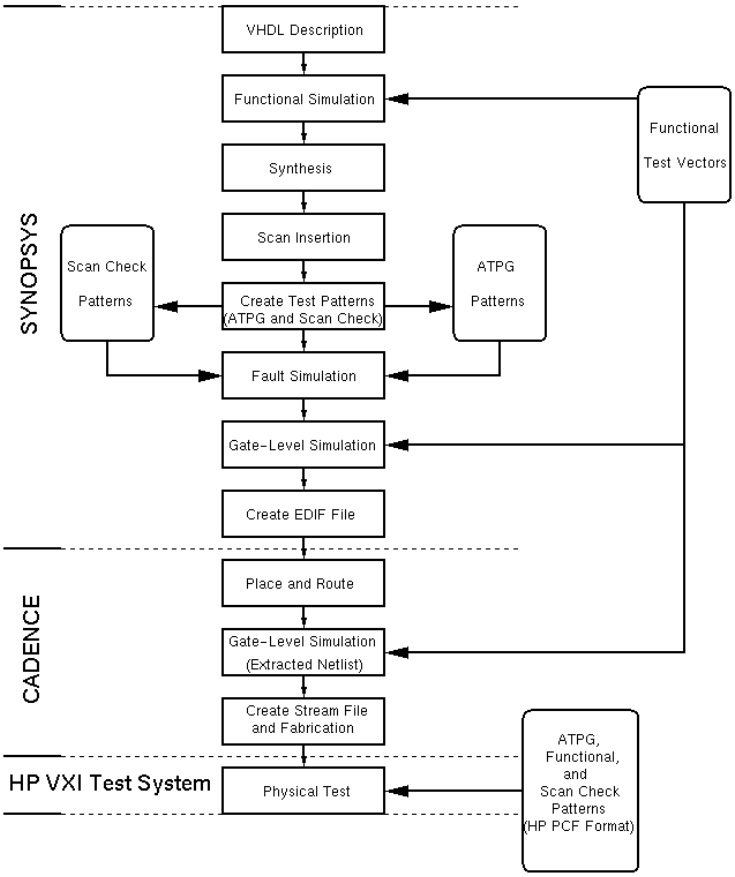


Figure 1.3: Design flow of a digial IC

http://www.ece.ubc.ca/ cad/local/html/test/design.html

Gate-level simulation, on the other hand, presents in the standard flow and is considerably faster. To obtain those parameters that are transistor specific, assumptions about the CMOS structures are made. In the presented master thesis gate-level simulation is selected, and is the subject of study throughout the paper.

In recent time NBTI is often considered to be the dominating degradation mechanism in VLSI IC. The total impact of NBTI on the time delay is about 15% for 65 nm technology process for the whole life-cycle. [7]. Therefore, it is selected as a degradation mechanism to be simulated and studied in the present master work.

The main challenges of the master work may be formulated as follows:

1. Performing simulation for a process that has no universally accepted model yet
2. Estimate transistor level operational parameters from gate-level simulation
3. Estimate long-term data based on short-term simulation

4. Implement simulation flow that is temperature aware
5. Integrate the simulation flow into an existing design flow of digital IC
6. Provide meaningful result data as an output of the simulation flow

NBTI is one of the few degradation mechanisms that have no universally accepted complete theory and model yet. There are several models published, however, non of them agrees completely with the experimental data [18]. That implies simulator implementation that is independent of the model and supports reconfiguration of the model.

As mentioned before, it is most appropriate to simulate the NBTI degradation at the gate abstraction level. However, in all models of NBTI there are some transistor specific parameters, such as the threshold voltage V_{th}, gate voltage V_g, gate voltage stress ratio α, oxide capacitance C_{ox}, etc. Some of them are constants and may be obtained from technology files, other are variables and need to be evaluated or approximated, based on certain assumptions. The most important assumption is the transistor structure of each used CMOS gates. In the presented work such assumptions have been made only or the basic CMOS gates: INV, NAND, NOR, AND, and OR.

Another serious challenge is the simulation duration. Degradation process is developing relatively slowly with time comparable to the life-cycle of the IC. Complete simulation of a such a complex process, that takes years, may not be feasible. Therefore, the simulation is performed for a much shorter time, and the data is extrapolated until the required period. In that methodology the selection of extrapolation methodology and the short-term simulation duration are fundamental for the accuracy of the final data. For devices working with periodic input patterns, it is reasonable to simulate one period, while for other circuits pseudo-random patterns are used for a configurable amount of time. In the literature, there are also long-term models, which are able to evaluate the future value of degraded parameter from a given sample. Such a model is used for the experimental part of the work.

NBTI is a process highly dependant on the temperature [7][18]. In the standard design flow, temperature is not estimated. Hence, a temperature simulation must also be integrated in the NBTI simulator. Another peculiarity is that the temperature distribution of the IC requires the physical layout of the circuit. Therefore, to evaluate the temperature, an additional stage in the flow is integrated after the layout generation. For small ICs, the temperature distribution is relatively universal and that stage could be avoided. In the particular implementation, the academic tool HotSpot 5.0 is used for temperature distribution estimation.

A simulation of NBTI degradation would not be so efficient if it cannot be integrated in the particular design flow. That requires synchronization with the input and output file formats of the different stages. Also, the output of the NBTI simulation must provide meaningful information and the possibility for further analysis. For large circuits with thousands of elements, statistical data is reasonable, such as bar diagrams, heat-map, maximum, minimum and average values of certain parameters.

The presented master work is organized in five chapters. Firstly, the NBTI ageing degradation process is briefly introduced. Several models are analysed, as well as the impact of the NBTI on the digital circuit performance. In the chapter "State-of-the-art", related works are discussed and the skeleton of the simulation methodology is built. Following is the chapter in which the simulation methodology and framework are presented. A chapter is also dedicated

to an implementation of the simulation, using popular EDA tools. The results are analysed and conclusions are drawn.

2 Negative Bias Temperature Instability

The negative bias temperature instability is a relatively recent reliability issue that is observed in p-channel MOSFET (p-MOSFET) transistors with negative bias between the gate and the source. It is worth mentioning that the bias temperature instability can be observed in all four bias combinations, however, it is most severe in the p-MOSFET with negative bias configuration [11]. NBTI has no universally accepted theory and model, therefore all information about it is based on confirmed and accepted experimental results.

So far it is generally accepted that the NBTI is a process of degradation of the:

- Absolute threshold voltage V_{th}
- Charge mobility μ
- Drain current I_{dd}
- Transconductance g_m

when a PMOS is stressed at elevated temperatures under a low and constant gate voltage [9].

One of the main reasons for the difficult studying of the NBTI is its property of fast recovering. During the recovery the stress voltage is removed and the transistor is recovering to some degree its original characteristics. Most scholars agree that there are actually two degradation components: permanent and recoverable, or also called reversible [10]. After that discovery, several very fast measurement techniques of the threshold voltage shift were developed including the on-the-fly technique, which allows independent measurement of the gate voltage. Now it is known that the permanent degradation depends on the following factors:

- Duration of applied gate voltage stress
- Amount of applied gate voltage stress
- Temperature
- Duty factor of stress and no stress
- Used technology
- Material of the gate dielectric

The physical background of NBTI is still a subject of scientific discussion and research. Most often it is attributed to two main events:

- Existence of interface charge traps

- Existence of charges in the oxide

Interface charge traps are formed in the border between the oxide and the substrate, called interface. The formation of the interface is highly technology depended, and it will be discussed in detail later on.

In addition to the interface charge traps, recently it was discovered that the oxide tends to charge positively during the operation of the p-MOSFET. The nature of that charge is yet not universally accepted, although some scholars attribute it to the trapped hydrogen ions, result of the broken apart Si-H bonds [11][23].

NBTI is a degradation mechanism of the gate insulator. The properties of the material used for insulator, the properties of the material used for substrate, and the technology used for their formation is of a high significance for the NBTI. Thus, a brief introduction of the p-MOSFET manufacturing process and gate insulator properties are discussed further on.

2.1 P-MOSFET Gate Insulator

The p-MOSFET is composed of (figure 2.1):

- n-substrate
- highly p-doped regions
- gate dielectric
- Metal plates

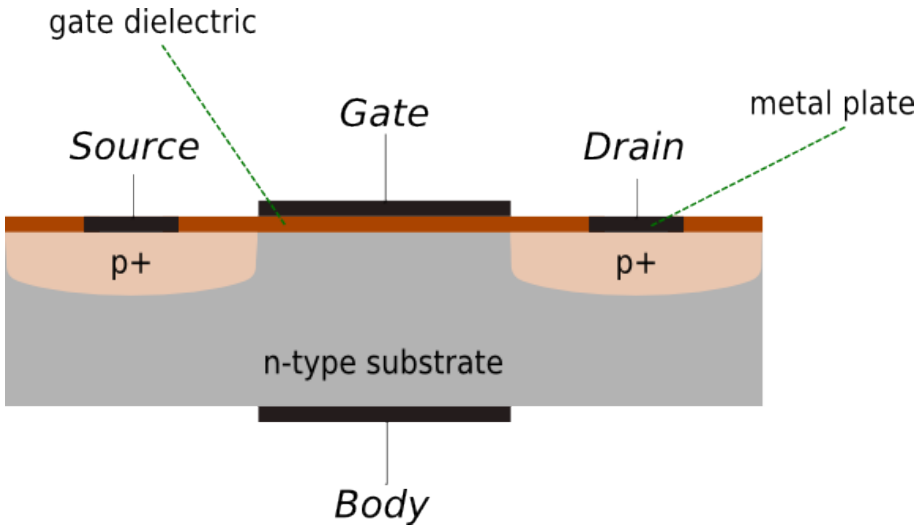


Figure 2.1: Ideal p-MOSFET

The basic steps in the process of fabrication are: lithography, thin film deposition, and etching [4]. Those three steps are supported by doping and cleaning. Considering the NBTI degradation, one of the most important role is played by the interface formed on the border

between the substrate and the gate dielectric. To understand its properties and how it is form, an overview of the manufacturing process of CMOS IC is presented.

2.1.1 IC Manufacturing Overview

Since their introduction in 1960, ICs are manufactured using a lithography process. Lithography is a method for creating relief structures on hard surfaces like stones, metals, silicon, glass, or gallium arsenide (GaAs). In IC fabrication lithography allows a computer-generated pattern to be transferred onto a silicon substrate. The typical lithographic flow is shown in figure 2.2.

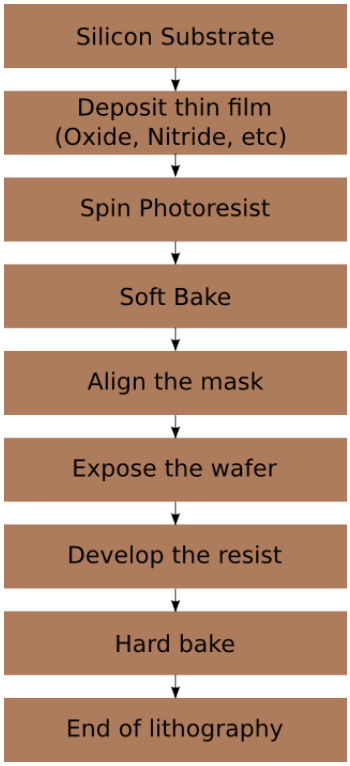
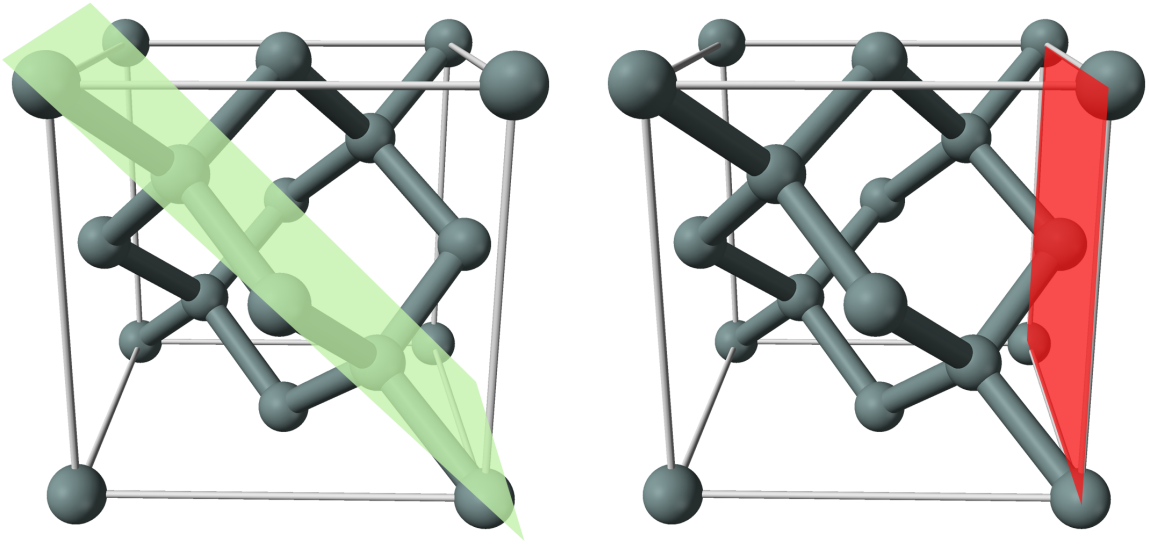


Figure 2.2: Lithography Process Flow. Source [26]

The gate dielectric is completed after the second step, therefore only the first two steps are discussed in details.

First is the manufacturing of the silicon substrate. The substrate or the wafer is highly pure, nearly defect free silicon crystal material, usually in the size of a large disk. The purity is not 100% pure, but during the growing process some initial impurity of boron, phosphorus, arsenic, or antimony is added with concentration of between 10^{13} and 10^{16} atoms per cm^3 [24]. An important characteristic of the substrate is the crystal orientation of the monocrystalline silicon. Silicon crystals are grown either in <100> orientation or in <111> shown in figure 2.3 [4].

On the top of the prepared wafer a thin film of insulator is deposited. Below are listed one of the most popular and widely used techniques for layer deposition [26]:



(a) <111> crystal plane (b) <100> crystal plane

Figure 2.3: Monocrystalline Silicon. Source [18][19]

- Thermal oxidation in a furnace
- Low Presure Chemical Vapor Deposition (LPCVD)
- Plasma Enhanced Chemical Vapor Deposition (PECVD)
- Atomic Layer Deposition (ALD)

Among them the most commonly used technique to produce a thin film of SiO_2 is the silicon oxidation. In fact it is not a deposition, but still produces the needed thin film of insulator with excellent quality. The process is performed in an oxidation furnace at temperatures between $900°C$ to $1200°C$. There are two types of oxidations: dry, in the presence of O_2; and wet, in the presence of H_2O. Dry oxidation achieves higher density of the SiO_2, but it is slower [26]. The reactions are described with the following equations:

$$Si_{(solid)} + O_{2(gas)} \Rightarrow SiO_{2(solid)} \tag{2.1}$$

and

$$Si_{(solid)} + 2H_2O_{(gas)} \Rightarrow SiO_{2(solid)} + 2H_{2(gas)} \tag{2.2}$$

The oxidation is crucial for the NBTI process because during it the interface region is formed. The formation and the properties of the interface region are discussed in details later on in the report. The key factor in this process is that in case of wet oxidation some Si atoms bond to hydrogen ions.

Chemical vapour deposition (CVD) is another widely used technique that allows achievement of good quality of deposited dielectric [26]. As the name suggest, it is based on chemical reactions with materials in gas or plasma phase. In the case of LPCVD, a low pressure,

achieved using pumps, increases the activation energy of the chemical in gas substance. The process goes under temperature between 550°C and 900°C and allows ultrathin dielectrics to be deposited including SiO_2, Si_3N_4, and polysilicon. The plasma enhanced CVD, on the other hand, uses radio frequency (RF) energy to create a highly reactive plasma substance which allows the deposition to be performed at low temperatures (150 to 300°C)[26].

Atomic layer deposition is a gaining popularity process in which the dielectric in gas substance is deposited in atomic thin layers. Although most often high-k dielectrics are deposited such as Al_2O_3 and HfO_2, other materials can also be deposited [26].

After the deposition of the dielectric layer the process goes as shown in figure 2.2. In them the highly doped regions for the source and the gate are formed and the metal plates are deposited where the source, drain, and gate are suppose to be.

Those are the manufacturing steps of the p-MOSFET. In the most common dielectric SiO_2 additional structure is formed between it and the substrate called interface. It is also reported that in other dielectrics like silicon nitride similar process is observed [9].

2.1.2 Oxide-Substrate Interface Region

After the deposition of the silicon oxide it has tetrahedron molecule with angle of 109° between each silicon and oxygen atoms (figure 2.4).

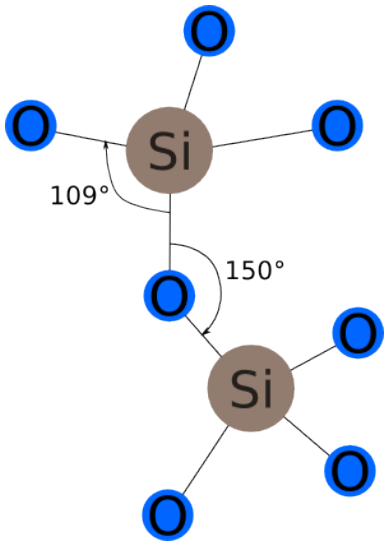


Figure 2.4: $Si0_2$ structure. Source [19].

The Si atom appears to be bond to four O atoms, but since each O atom is bond to another Si atom the ration is one Si to two O atoms. Between the different tetrahedrons the angle may vary between 120° and 180° with mean of 150°. When the angle deviate from the mean the bond is weakened [19].

In the border between the oxide and the substrate such weak bonds are created. The main reason for that is the lattice mismatch between those structures [9]. The weak bond tend to brake, leaving a trivalent Si atom with unsaturated valence electron, called an interface

trapped charge or just interface trap. As a result of this process a region with numerous dangling bonds is created. This region is very often called interface region or interface.

Depending on the substrate crystal orientation different types of interface traps are formed. In the case of a <111> lattice there is only one kind of interface traps called P_b centres, while in the case of <100> there are two: P_{b1} and P_{b2}. The difference between the two traps for the <100> substrate is in their spin momentum. In both cases interface traps have an amphoteric nature, meaning that the dangling bond can be unoccupied, occupied by one, or two electrons. Therefore, depending on the Fermi level of the interface the traps can be positively, neutrally, or negatively charged [9]. Whenever they are not neutralized, that creates an uncompensated charge, which shifts the threshold voltage [19].

During the process steps of the lithography, it is common that some amount of hydrogen atoms to be concentrated in the interface region. In such case the dangling bonds are absorbing those atoms forming SiH bonds. That process compensates the trap charge and improve the initial transistor characteristics. However, during the operation of the transistor it is possible the SiH bonds to be broken, creating again uncompensated charges. This process of SiH bonds braking lead to the NBTI degradation. What is happening after the SiH bond is broken is subject of different models. There is no universally accepted model and the topic of the presented work is not to prove or invent a particular model. Therefore only the most popular ones are briefly studied in the next section, even though some other models are mentioned for completeness.

2.2 Reaction-Diffusion Model

Reaction-diffusion (RD) is the classical, oldest, and most prevalent NBTI model in literature and industry [18]. As the name suggests, the model describes the NBTI in two phases. The first phase is the reaction. According to the model when a voltage stress is applied, the SiH bonds tend to brake with a linear dependence of the stress time. The outcome is holes and hydrogen atoms. Further on a diffusion process of the H or H_2 atoms into oxide or substrate is taking place. That phase is called diffusion. The hydrogen atoms penetrate into the oxide with time dependency t^n, where n is a neutral hydrogen species commonly given as 0.25 [18]. With much slower rates the H species may diffuse into the substrate. In the interface Si ions remain with uncompensated positive charge [19]. For p-MOSFET with negative bias, the positively charged interface decreases the threshold voltage, requiring more volts to be applied on the gate as a compensation.

The generation of traps is given by following equation [25]:

$$\Delta N_{it}(t) = \frac{2At}{1+\sqrt{1+4ABt^{3/2}}} = \frac{2k_F N_0 t}{1+\sqrt{1+4k_F N_0 k_R t^{3/2}(0.5\sqrt{D_H})}} \tag{2.3}$$

where k_F is the forward reaction rate, k_R is the reverse reaction rate, N_0 is the initial defect density, t is the time, and D_H is the hydrogen diffusion coefficient. Knowing all parameters in that equation the threshold voltage can be evaluated using the following formula [18]:

$$\Delta V_T = -\frac{\Delta Q_{it}}{C_{ox}} = -\frac{\Delta N_{it}}{K_{ox}\varepsilon_0} t_{ox} \tag{2.4}$$

where Q_{it} is the charge of the interface traps, C_{ox} is the oxide capacitance per unit area, t_ox is the oxide thickness, ε_0 is the vacuum permittivity, and K_{ox} is <unknown>.

The following issues in the RD model have been reported [18][1] :

- Poor alignment with experimental data
- Recovery is excluded from consideration
- The effect of the oxide charges is not considered
- The diffusion process assumes infinite oxide thickness

Recently it was found that after very short time the degraded threshold voltage is recovering some of its original value. We recognize two operation modes which affect the NBTI degradation due to the recovery: static, when the stress is constant; and dynamic, when there is stress followed by non-stress in a periodic or non-periodic sequence.

An enhancement of the RD model for static operation mode is proposed in [1]:

$$\Delta V_{th} = A\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)}\right)^{2n} \tag{2.5}$$

where n is the time exponent that can be 1/6 or 1/4, A is linearly proportional to the hole density and has an exponential dependence on the temperature (T) and the electric field E_{ox}.

$$A = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right)\sqrt[3]{K^3 C_{ox}(V_{gs}-V_{th})\left(\exp\frac{E_{ox}}{E_0}\right)^2} \tag{2.6}$$

In the case of dynamic operation, stress is followed by recovery. To describe that, separate models are proposed for each phase:

$$Stress : \Delta V_{th} = (K_v(t-t_0)^{1/2} + \sqrt[2n]{\Delta V_{th0}})^{2n} \tag{2.7}$$

$$Recovery : \Delta V_{th} = V_{th0}\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t-t_0)}}{2t_{ox} + \sqrt{Ct}}\right) \tag{2.8}$$

where t_{ox} is the oxide thickness, C_{ox} is the oxide capacitance per unit area, $(t-t_0)$ is the stress or recovery duration, and the rest of the parameters are given in table 2.1.

We distinguish two cases of dynamic NBTI degradation: with periodic stress, and with non-periodic stress. In the first case, each stress-recovery is repeated with a period T as shown in figure 2.5.

An important parameter for characterizing the periodic NBTI degradation is the alpha parameter, which is the stress ratio: $\alpha = t_{stress}/T$, where t_{stress} is the stress time in one period and T is the period. In case of simulation often for t_{stress} is taken the total time the gate voltage is active, while T is whole the simulation time. In the case of non-periodic stress, α is a function of the time t.

There are many other models in addition to the presented ones. Taking into account that there is no universally accepted one, further models are not considered here. The last presented

K_v	$\left(\frac{qt_{ox}}{\epsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs}-V_{th})\sqrt{C}exp\left(\frac{2E_{ox}}{E_o}\right)$		
C	$T_o^{-1}.exp\left(-E_a/kT\right)$		
t_e	t_{ox} $t_{ox}\sqrt{\frac{t-t_0}{t_1}} - \frac{\sqrt{\xi_2 C(t-t_0)}}{2\xi_2}$		$t-t_0 \geq t_1$ *otherwise*
$E_a(eV)$	0.49	$E_0(V/nm)$	0.335
δ	0.5	K $(s^{-0.25}C^{-0.5}nm^{-2})$	8×10^4
ξ_1	0.9	ξ_2	0.5
T_0	10^{-8}		

Table 2.1: Enhanced RD Model Parameters. Source [1]

model is used for performing experiments due to its complete form, good alignment with the experiment data, and convenient form for a simulator implementation.

Even a model perfectly aligned with the experimental results is not sufficient for simulation of the NBTI degradation for very long time periods such as the complete life-cycle. It is practical, the simulation to be limited between several minutes to a month, but it should not become a factor in the design flow. Therefore, the results of the simulation must be extrapolated to the needed time. Such methods for extrapolation or estimation of long-term models are presented in the next section.

2.3 Long-Term RD Model

Looking at equation 2.5 describing the static NBTI degradation, we see that it gives us the threshold voltage degradation for any t. Figure 2.6 shows the degradation due to static stress for 2000 seconds or about 33 minutes.

The problem arises when we need to estimate the threshold voltage degradation for dynamic V_{gs} stress. As before we consider two cases: periodic or random switching of V_{gs}.

In the case of periodic stress, let $\Delta V_{ths,m}$ and $\Delta V_{thr,m}$ be the threshold voltage change correspondingly in the end of the m-th stress and m-th recovery cycles. The initial threshold voltage in the beginning of the m-th stress is $\Delta V_{thr,m-1}$. The duration of the stress is αT_{clk}, where α is the stress ratio and T_{clk} is the stress-recovery period. Adding that to equation 2.7 we obtain:

$$\Delta V_{ths,m} = (K_v(\alpha T_{clk})^{1/2} + \sqrt[2n]{\Delta V_{thr,m-1}})^{2n} \tag{2.9}$$

The equation for $\Delta V_{thr,m}$ is derived analogically:

$$\Delta V_{thr,m} = V_{ths,m}\left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{CmT_{clk}}}\right) \tag{2.10}$$

Substituting:

$$\beta_j = \left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{CjT_{clk}}}\right) \tag{2.11}$$

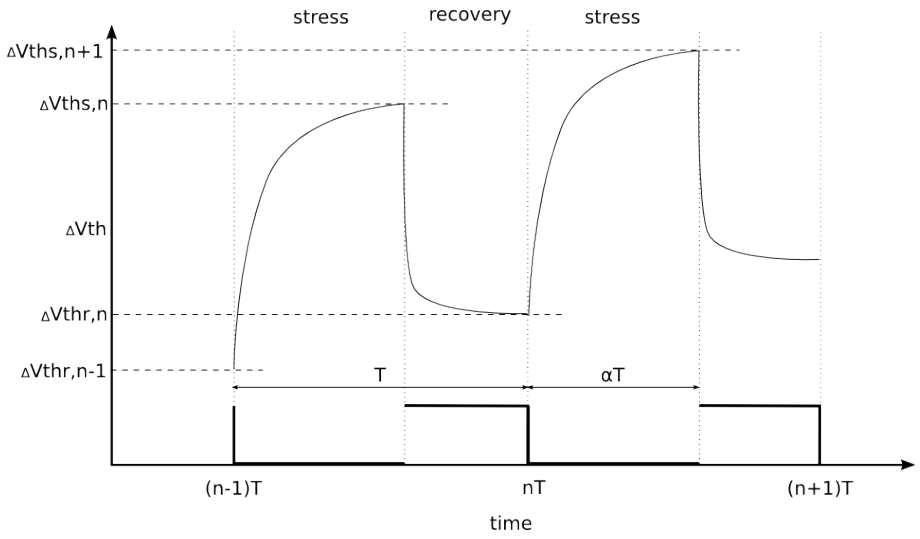


Figure 2.5: RD Model With Periodical Stress. Source [1].

it is possible to express $V_{ths,m+1}$ as a recursive formula of $V_{ths,m}$.

After simplification the following upper limit was derived in [1]:

$$\Delta V_{th} \leq \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_m^{1/2n}} \right)^{2n} \tag{2.12}$$

This solution gives the upper limit of NBTI degradation in the case of periodic V_{gs} stress. However there are large number of ICs that operate with a non-periodic sequence of gate voltage stress. In this case, a different approach must be applied. As mentioned earlier, there are two components of the NBTI degradation permanent component and reversible. According to the experimental data, the reversible degradation recovers very rapidly after the stress is removed, and after that it decays with a very slow rate to 0. Taking into account that Wang at [22] suggests to modify formula 2.12, using the term $[\alpha / min(\alpha, 1-\alpha)]$ instead of just α. This results in:

$$\Delta V_{th} \leq \left(\frac{\sqrt{K_v^2 \alpha T_{clk} / min(\alpha, 1-\alpha)}}{1 - \beta_m^{1/2n}} \right)^{2n} \tag{2.13}$$

This section presents approximations for estimating the long-term effect of NBTI. This topics remain open for research work and it is not closed, neither the provided equations are considered for the most accurate. However they do have complete form and description allowing to be implemented in gate-level simulation. The prove and searching for better models are not a subject of the presented work.

So far we considered different models of the NBTI degradation, but we don't know yet why the NBTI degradation is a reliability issue. In the next section that problem is studied.

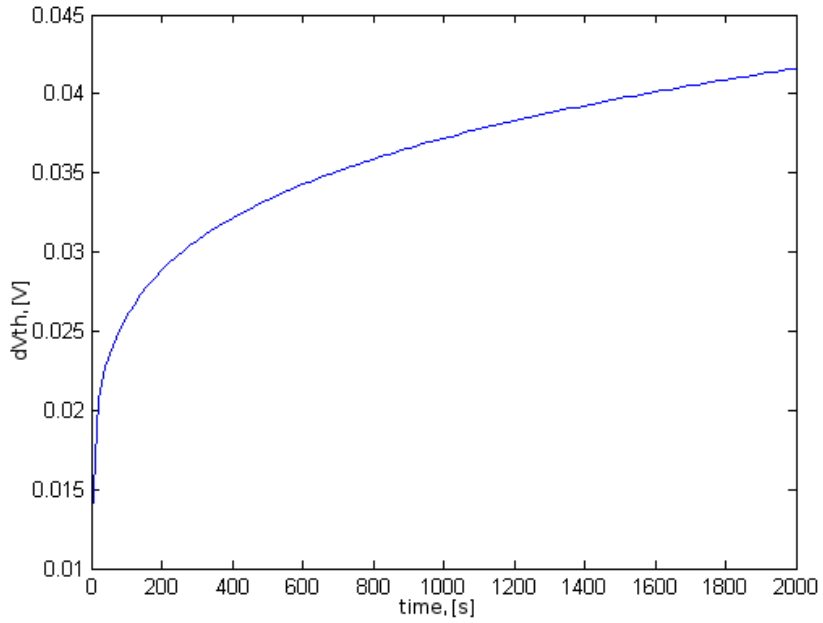


Figure 2.6: NBTI degradation with static V_{gs} stress

2.4 Impact of NBTI on the circuit

NBTI degrade the threshold voltage of a p-MOSFET. To understand how the NBTI degradation impacts the circuit performance it is enough to study how the threshold voltage shift of a p-MOSFET impacts it.

In figure 2.7 is depicted the simplest case - an inverter gate.

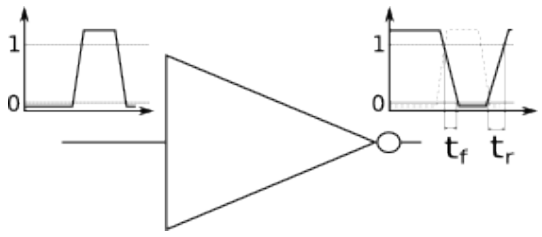


Figure 2.7: Inverter Gate

Except its logical function, a gate is characterized by the time delays of the output signal - rise delay t_r and fall delay t_f. The rise delay is the time for which the output signal rise from logical zero to logical 1, while the fall time is from logical 1 to logical 0. Those delays are implied by the output characteristics of the MOSFETs in the CMOS gate. In the case of inverter, there are two MOSFETs - a p-MOSFET and a n-MOSFET (figure 2.8). From them only the p-MOSFET is affected by the NBTI. The output characteristics of p-MOSFET are

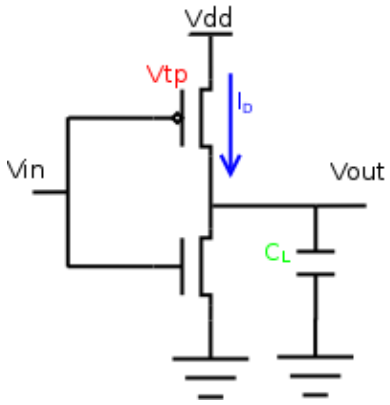


Figure 2.8: CMOS Inverter Transistor Circuit

described through the following equations [19]:

$$Saturation : I_D = -\frac{\mu\epsilon_{ox}}{2T_{ox}}\frac{W}{L}(V_{GS} - V_{tp})^2 \tag{2.14}$$

$$Ohmic : I_D = -\frac{\mu\epsilon_{ox}}{2T_{ox}}\frac{W}{L}[(V_{GS} - V_{tp})V_{DS} - V_{DS}^2] \tag{2.15}$$

where I_D is the drain current, μ is the holes mobility, ϵ_{ox} is the thin oxide (SiO_2) dielectric constant, T_{ox} is the oxide thickness, W and L are the transistor effective gate width and length, V_{tp} is the p-MOSFET threshold voltage, and V_{GS} and V_{DS} are the gate- and drain-source voltages. It is clear from the output characteristic plot (figure 2,9), that the threshold voltage shift will affect the slope of the p-MOSFET drain current.

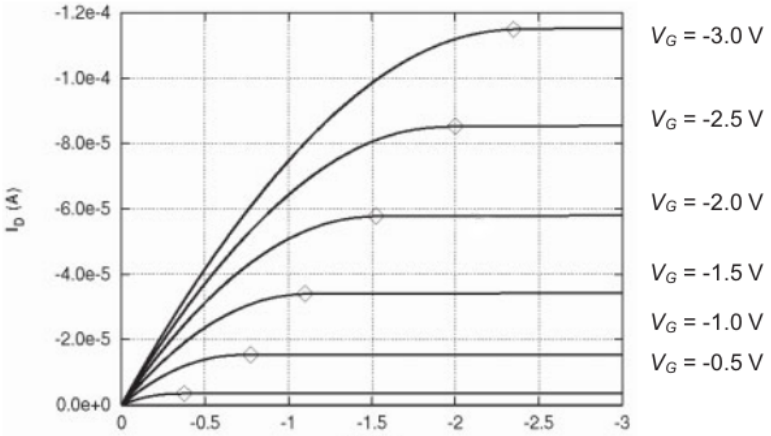


Figure 2.9: P-MOSFET Output Characteristic. Source [19]

Since in the case of NBTI, the threshold voltage is shifting to more negative, i.e. its absolute value is increasing, then the absolute value of $(V_{GS} - V_{tp})$ is decreasing, which for the value of I_D will be equivalent to a decreasing in V_{GS}. Therefore, if the p-MOSFET in the inverter CMOS gate is a victim of NBTI, then when it is switching on its I_D will increase slower. Since the p-MOSFET switch connect the power supply to the output, it will determine the rise delay t_r:

$$t_r = \frac{C_L V_{dd}}{I_D} = \frac{K_1}{(V_{GS} - V_{tp})^2} \tag{2.16}$$

where K_1 is a constant.

To get the delay change due to NBTI, we differentiate with respect to the time t. Since only the threshold voltage is affected by the NBTI, we obtain:

$$\Delta t_r = \frac{2K_1 \Delta V_{tp}}{(V_{GS} - V_{tp0})^3} \tag{2.17}$$

Taking into account that the initial rise time is known, a simplification can be made by dividing by t_{r0}:

$$\frac{\Delta t_r}{t_{r0}} = \frac{2\Delta V_{tp}}{(V_{GS} - V_{tp0})} \tag{2.18}$$

Equation 2.18 shows a linear relation between the Δt_r and ΔV_{th}. Considering the other gates, the situation is similar. The difference is in the number of inputs and the configuration of the p-MOSFET circuit. In that case it is not important only the output rise time, but rather the pin-to-pin rise delay. In gates with integrated inveter such as the AND, OR, NBTI is degrading both the rising and the falling delays. This is studied in detail in the chapter Implementation, where models for different CMOS circuit are implemented.

Once the gate suffered the delay degradation, it also influences the operation parameters of the whole integrated circuit. A very common result is decreasing of the operational frequency due to increased delay of the critical path. In addition, the critical path may change partially or completely.

Having described the NBTI degradation process, giving some of the models available in the literature, and studying the impact of NBTI on combinational digital circuits, we have the foundation to study the different approaches for NBTI simulation and analyse them.

3 State-of-the-art

The negative bias temperature instability is considered as one of the most critical reliability issues. A lot of research efforts has been dedicated to model the NBTI and simulate its impact on VLSI ICs. Considering the simulation of NBTI, the most common simulation methodologies are:

- Transistor level SPICE simulations
- Gate-level simulations

Transistor level NBTI simulations have the potential to be very accurate, and the model fits precisely with the measurements. Gate-level simulations, on the other hand, have the potential to simulate very large circuit logics composed of standard cells. Both of the approaches and related works are considered in the following sections.

3.1 SPICE Simulation of NBTI Degradation

Using the simulation program with integrated circuit emphasis (SPICE) is one of the first approaches used for NBTI simulation. SPICE is general-purpose and open source which makes it very popular, but at the same time powerful enough for very complex analog and digital circuit simulations. Initially, it started as an university project and later became an industry standard. The last version is the SPICE 3f.4, released in 1993. However, there are many industrial adoptions such as:

- ADVICE, from Bell Labs
- TISPICE, from Texas Instruments
- MCSpice, from Motorola
- HSPICE, from Meta Software

Other SPICE-level popular simulators are the Cadence Virtuoso Spectre and the Mentor Graphics Eldo.

The simulation flow using SPICE is similar to the gate-level simulation. As an input to the simulator, a SPICE-netlist text file, and SPICE models for each component of the netlist are provided. The simulation is at electrical level, and it is based on complex integro-differential equations. A positive feature of such methodology is the accuracy of the results, and the ability to calculate the total effect of all degradation mechanisms. However, as discussed earlier, due to the complexity of the transistor models, the simulation process requires huge amount of computational resources. Using clustering and powerful computers, that process may be accelerated significantly, therefore it is still subject of research and used in the industry.

Li et al. [13], proposed a SPICE based reliability simulation methodology for VLSI CMOS circuits. Except for NBTI other degradation mechanisms such as the hot-carrier injection and the time-dependent dielectric breakdown are also considered. Figure 3.1 shows the flowchart of the simulation.

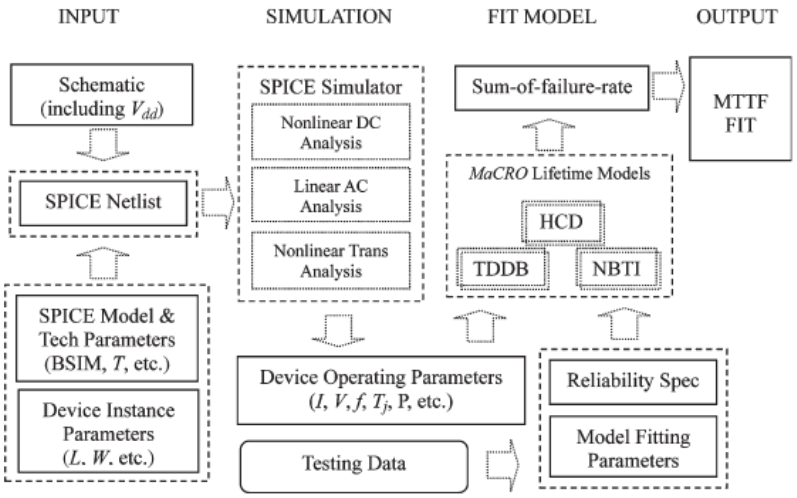


Figure 3.1: SPICE reliability simulation flow. Source [13]

The first step in the methodology is the evaluation of the device operating parameters, without considering degradation. That is done through a SPICE simulation of the whole circuit netlist. Once those parameters are known, a custom reliability simulation called MaCRO is executed. The MaCRO algorithm is based on accelerated lifetime models, and accepts the SPICE netlist and models, the calculated parameters, and reliability constraints as inputs. After the simulation, the outputs, based on testing data, such as the mean-time-to-failure (MTTF) and the failure-in-time (FIT) for each transistor in the netlist are generated.

The advantages of this methodology are improved reliability simulation speed, very accurate results, independence of the SPICE simulator, and meaningful output. However, the main limitation of the long SPICE simulation time still remains. Nevertheless, the idea of separate reliability simulation that uses estimated operating parameters may be applied in a higher level simulation as well.

The previous methodology proposed the implementation of a stand-alone degradation SPICE simulator. Some SPICE simulators support a user defined custom reliability model. This is a good feature for the purpose of NBTI simulation, which has no universally accepted model yet. Such simulation methodology was suggested by Mooraka at [14], who used such feature of Eldo simulator, called User Defined Reliability Model (UDRM). In this methodology, initially a fresh device simulation is performed for estimating the NBTI model parameters. Next, the degraded threshold voltage is calculated and transistor models are updated. A new simulation is executed and the resulting waveform is the output.

Compared with MaCRO, the simulation methodology proposed by Mooraka has a very simple implementation and flow. However, the SPICE simulation is performed twice, even though the output is not limited to MTTF and FIT.

Recovery is a characteristic of the NBTI that may have big impact on NBTI estimations. As discussed in chapter 2, it is a very fast process and in the case of random gate stress, it is very difficult to simulate. Kuflluoglu in [12] proposed an extensive and improved simulation methodology for NBTI recovery. The methodology reduces the computation efforts using a compact convolution-based model of the NBTI, rather than the detailed RD classical model. Figure 3.2 shows the simulation flow.

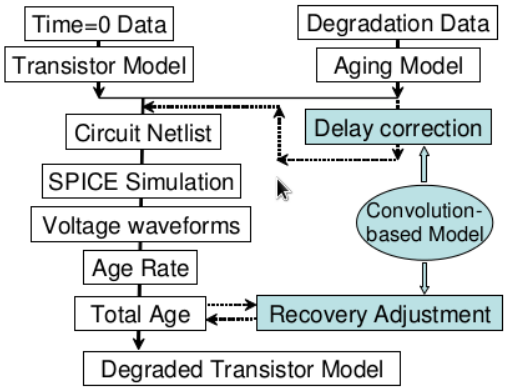


Figure 3.2: SPICE reliability simulation flow built into RELXPERT using URI equations. The solid lines show the default age calculation, while the dotted lines and shaded boxes stand for the delay correction due to NBTI. Source [13]

The implementation is based on RELXPERT SPICE simulator, using an Relxpert Ultrasim Reliability Interface (URI). Similar to the Eldo UDRM, URI provides interface for customization using equations. In contrast to the previous simulation methodology, this time the NBTI degradation calculation is integrated in the simulation and calculated during it. That allows to simulate each stress-recovery cycle achieving best matching with the NBTI model. Considering the simulation speed, we can expect a speed-up due to having only one SPICE simulation, and due to the simplified compact model. Having only one SPICE simulation may avoid over-simulating some parameters that are not affected by NBTI, as well as avoid doing initialization twice.

We can summarize that the NBTI simulations using SPICE simulators are very popular, accurate and highly potential for the future research and industrial projects. They can provide all necessary parameters for all NBTI models, and may be integrated in the SPICE simulator for cycle accurate simulation of the NBTI degradation. The main limitation of the SPICE simulation is their large amount of required computational resources, which makes them infeasible for complex circuits with a large number of elements. Since this is common for virtually all modern digital devices based on SoC or VLSI IC, SPICE based NBTI simulation methodologies remain limited for small circuits and analog or mixed mode ICs.

3.2 Gate-level Simulation of NBTI

Gate-level simulation has the potential to solve the main limitation of the SPICE model. Due to the simpler abstraction models used in the netlist, the simulation is significantly faster. However, the following problems arise:

1. Estimating the electrical level parameters of the NBTI model
2. Assuming transistor structure of each gate in the netlist

If we recall some of the equations describing the NBTI degradation, then we will find parameters such as the threshold voltage V_{th}, the gate-source voltage V_{gs}, and other technology parameters such as the gate oxide capacitance per unit area C_{ox}, the oxide thickness t_{ox}, etc. Those parameters are transistor specific, but on gate-level there are gates, flip-flops and latches which are viewed as black boxes from the transistor level perspective. One possible solution is to use a relation between a gate level parameter and the necessary transistor level parameters. Since the degradation of the p-MOSFET can be different depending on how they are connected to the inputs and in what configuration they are, it is necessary that information to be assumed or provided, in order to estimate the impact of the NBTI.

DeBole in [6] suggests a gate level simulation of NBTI using a first-order approximation for the propagation delay of the gate.

$$T_d = a_0 + a_1.\Delta V_{th} + a_2 C_1 \tag{3.1}$$

where T_d is the propagation delay, ΔV_{th} is the threshold voltage shift of the least-most degraded pMOS transistor due to the NBTI, a_0 is the intrisic delay of the gate without the NBTI degradation, a_1, a_2, and C_1 are constants obtained through HSPICE circuit simulations. The simulation framework is shown on figure 3.3.

Initially the parameters of the NBTI models are estimated. In the used model, the parameters are the operational conditions (temperature, gate voltage, initial time delay), the technology parameters (C_{ox}, t_{ox}), the design file as RTL or gate-level netlist, and the input value probabilities. The gate voltage and time delay are obtained through a cycle-accurate register transfer level (RTL) using the Illinois Verilog Model (IVM). Then using the switching activity a power analysis is performed for estimating the consumed power by each transistor. Having the power dissipation, the flow continues with Temperature Analysis using the academic tool HotSpot 4.0 to obtain the temperature for each cell in the layout. This methodology does not generate layout of the simulated IC, but instead uses the HotSpot floorplan feature for automatic generation of foorplan from a netlist and a power file.

Once all the operating conditions and input signal probabilities are ready, the NBTI simulator takes control to evaluate the maximum NBTI threshold voltage degradation for each gate. Using a long-term NBTI model the degradation is extrapolated until the necessary period. Next, the delay is calculated using formula 3.1 and used by the Synopsys Primetime tool to perform timing analysis of the degraded netlist. Having the degradation information, the impact of the NBTI is analysed and provided as output.

The "New Age" simulation methodology is a very promising solution for a NBTI degradation simulation. It solves very effectively the SPICE simulators large computational requirements. Instead of doing SPICE simulation of the whole circuit each time, only one SPICE simulation

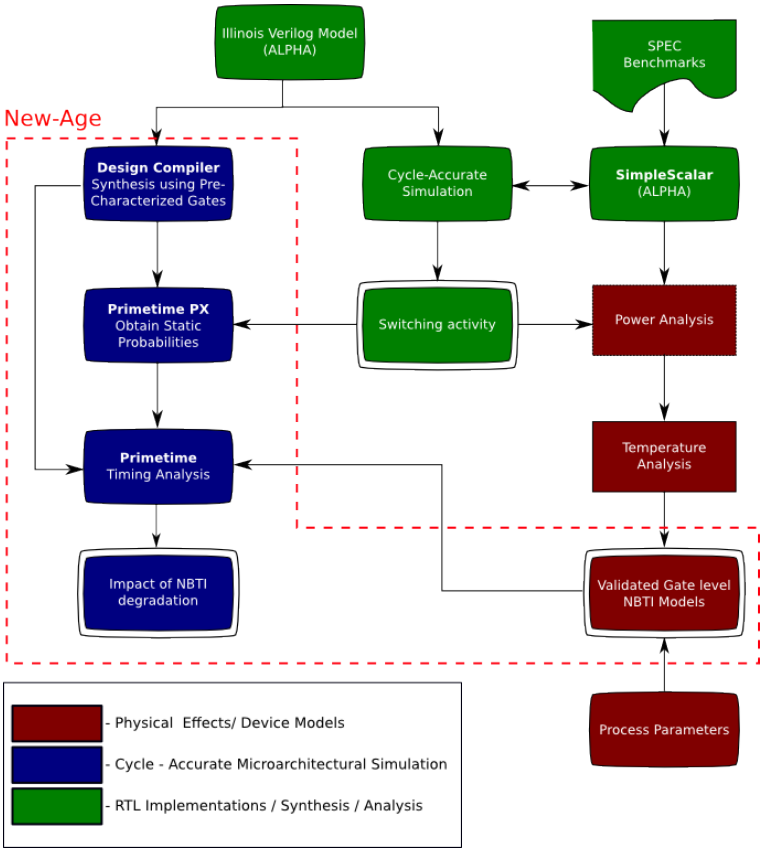


Figure 3.3: The "New-Age" NBTI Assessment Framework. Source [6]

is performed for each type of gate-level component (AND, NAND, DFF, etc). Once the SPICE simulation is done, a library is built and used directly by the NBTI simulator.

Wang at [22] improved the gate level NBTI model and proposed a simulation algorithm for NBTI simulation and obtaining the operational parameters. In the suggested methodology, the propagation delay t_p and the output slew rate t_o are modeled as functions of the threshold voltage degradation ΔV_{th}, the input slew rate t_i, and the load capacitance C_L. Considering the propagation delay two models are presented: t_p is a polynomial function of ΔV_{th} for fixing t_i and C_L; and t_p is a linear function of t_i and C_L for fixing V_{th}.

In the first model using Chebyshev polynomial for t_p the following equation was approximated:

$$t_{p1} = (a_0 - a_2) + (a_1 - 3a_3)(1 - 10\Delta V_{th}) + 2a_2(1 - 10\Delta V_{th})^2 + 4a_3(1 - 10\Delta V_{th})^3 \quad (3.2)$$

where a_0, a_1, a_2, and a_3 are obtained through SPICE simulations. According to the experiments published, this approximation gives results with maximum fitting error of only 0.38% [22].

The second model is given with the equation:

$$t_{p2} = b_0 + b_1\Delta t_i + c_0 + c_1\Delta C_L \quad (3.3)$$

where b_0, b_1, c_0 and c_1 are estimated with SPICE simulation. For specific ΔV_{th}, ΔC_L, and Δt_i the gate delay is the sum of the last two equations.

The algorithm (figure 3.4) requires as inputs the circuit netlist, the input signal probability and the slew rate. The output of the algorithm is the degraded delays due to NBTI. The first step is the levelizing of the netlist. This step is done to ensure that all input signals of a gate are valid and correct during the simulation. Once the netlist is levelized, the simulation starts sequentially from the first level, estimating the ΔV_{th}, ΔC_L, and Δt_i for each gate in the level. After that, the input signal characteristics of the next level are updated and the simulation goes on with the next level.

The advantage of this simulation methodology is the single gate-level simulation. That optimizes the NBTI degradation simulation flow. However, a SPICE simulation must be performed for each cell of the netlist, which requires additional efforts and time. In addition, the temperature is not considered, although it is universally accepted that NBTI is strongly dependant on temperature [18].

Both SPICE based transistor level simulations and gate level simulations have their positives and drawbacks. SPICE simulations allows very accurate cycle-by-cycle simulation taking into account the recovery of the NBTI. Gate level simulations are able to speed up the simulation saving computational resources and design time. They allow complex and large VLSI ICs, such as modern processors and system-on-a-chips, to be simulated and the NBTI degradation to be estimated. In addition, in contrast to SPICE simulators, the gate level simulators are integrated in virtually all modern digital VLSI IC EDA tools.

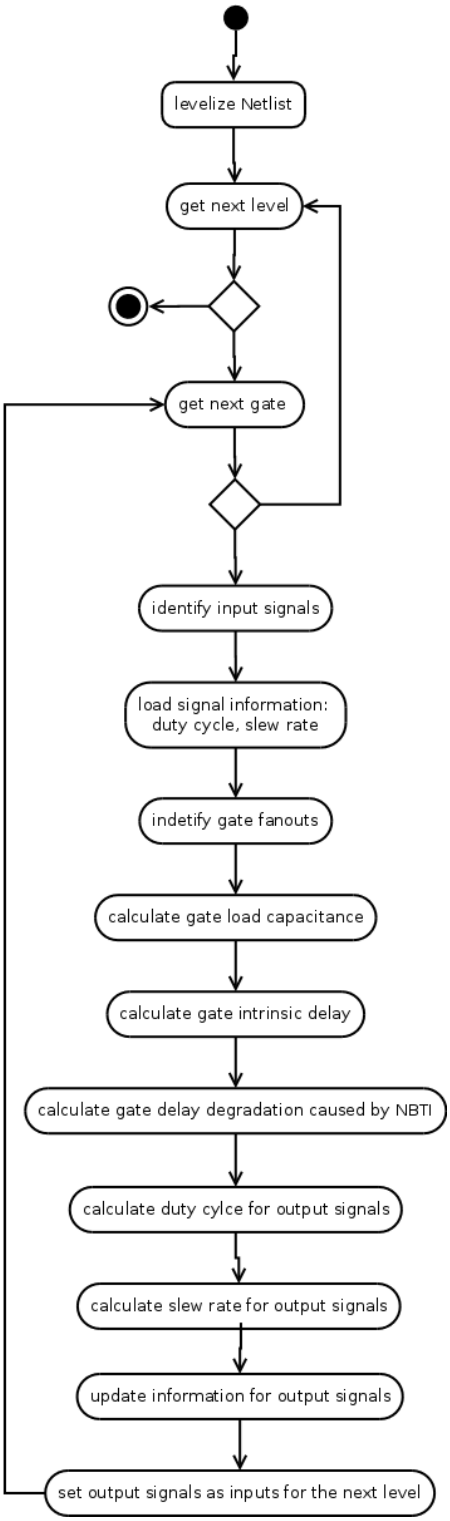


Figure 3.4: NBTI simulation algorithm. Source [22]

4 Simulation of Negative-Bias Temperature Instability

The first step of finding solution to any problem systematically is to choose an appropriate approach. A popular approach used in the system engineering is the v-model (figure 4.1).

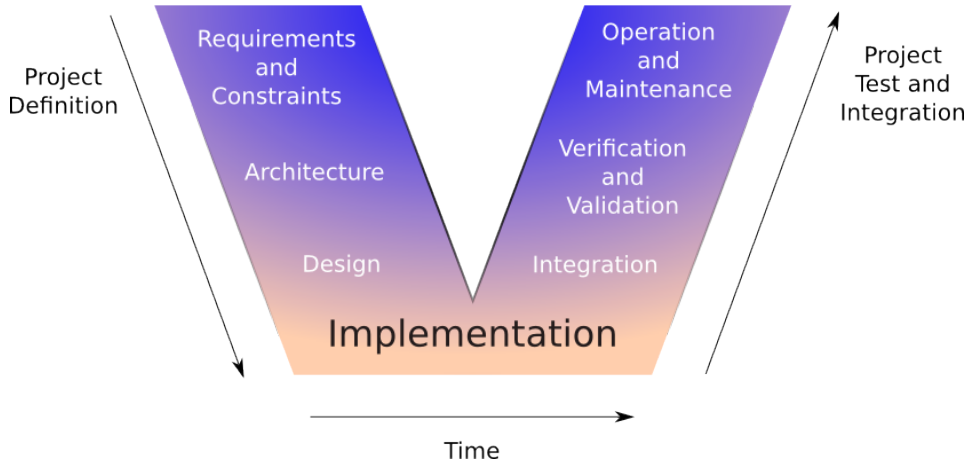


Figure 4.1: The V-model of System Engineering Process. Source [3]

The first step in the v-model is the definition of the system level requirements and constraints. Based on that, an architecture of the system satisfying all the system level requirements and constraints is selected. After this step, new set of architectural requirements and constraints is added. In the design step, all the platforms and frameworks are selected so that the system is completely defined for implementation of manufacturing. During this step, all high level functionalities are broken down to trivial functions.

Once the system design is done, it can be implemented or manufactured. The implementation begins from the lowest level functions or components. Next, all components are integrated into the subfuctional blocks until the whole system is built. The completed system is verified and validated against all the system requirements and constraints. Finally, the system is operated and maintained according to operational and maintenance manuals.

The first step of the simulation-based analysis of NBTI degradation in digital combinational circuits is the implementation of the NBTI simulator, which is a software system. Therefore, the v-model is appropriate and used as a solution approach.

This chapter is organized following the v-model. First the requirements of the NBTI simulator are defined, following the architecture or the simulation flow. Finally the design of the simulator design and implementation are presented and analysed, preparing the ground for

the next chapter - the simulation results and analysis.

4.1 Requirements and Constraints

The aim is to develop a NBTI simulator to estimate and analyse the impact of the NBTI degradation in CMOS VLSI digital combinational circuits manufactured with contemporary technology process. The simulation process has to be fast - in terms of several hours, but not more than a week.

Based on the aim the following system requirements are defined:

1. The simulation has to be performed on gate level
2. The NBTI simulator has to be integrable with available external EDA tools
3. The NBTI simulator shall be independent of the NBTI model
4. Transistor level models for each gate type have to be available prior to the simulation.
5. The NBTI simulator shall output a delay file containing the delay information for each gate and the statistical information about:
   a) Total number of gates affected by the NBTI degradation
   b) Statistical median and mean of the relative delay increase due to the NBTI degradation
   c) Critical path delay degradation
   d) Power dissipation of the degraded circuit
   e) Visualizing of the chip IC delay degradation due to the NBTI.

As discussed in the previous chapter, the transistor level SPICE simulation of VLSI circuits with large number of transistors requires serious computational resources and is very often not feasible. Therefore, the main interest of this master work is the NBTI simulation on gate level.

There are two possibilities for the NBTI simulator - to be stand-alone or integrable with the available EDA tools. The first possibility is, from one side, more flexible and specialized, but requires more efforts to be implemented. In addition, it will not optimize the process since EDA tools are used in any case during the design flow. Therefore, the second possibility is chosen.

The third requirement is due to the fact that there is no universally accepted NBTI model yet. The different models might require different parameters, some of which are at transistor level and require information about the MOSFET circuit structure inside the CMOS gates and cells. One solution, as discussed in the previous chapter, is to use gate level approximations with parameters estimated by additional SPICE simulation for each gate. To avoid SPICE simulations, it is also possible that the information of the p-MOSFET circuit is provided as an input to the NBTI simulator, which is the fourth requirements.

The last requirement concerns the output of the NBTI simulator. In order to analyse the effect of the NBTI degradation on a digital combinational circuit, statistical information

summaring the results is needed. In addition, a complete delay file is provided in a popular format, so that additional analysis could be possible by an external tool.

Based on those five requirements, it is possible to create a set of simulation flows satisfying them. One of the simulation flows is chosen, and the architecture of the simulator is determined by that flow.

4.2 Simulation Flow

The simulation high level flow diagram is shown of figure 4.2:

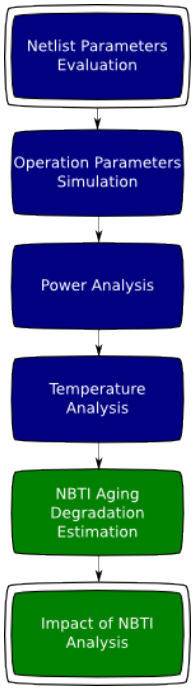


Figure 4.2: Simulation High Level Flow

The parameters needed for an NBTI model can be sorted into 3 groups:

1. Technology dependent constants $(t_{ox}, C_{ox}, \mu, \epsilon_{ox})$
2. Circuit static parameters $(V_{DD}, t_r, t_f, C_L, C_p, R_p, L_p)$
3. Operation parameters (T, V_{GS})

where C_p, L_p, and R_p are the parasitics of gate pins and wires. For those parameters the technology dependent constants can be obtained in a separate file and the rest of the parameters must be evaluated.

The first action is the evaluation of netlist parameters or the circuit static parameters such as the power supply voltage V_{DD}, the delays, and the parasitics. From them, the V_{DD} is

usually given as a circuit constraint in a separate file. The rest of the netlist parameters are obtained through static analysis of the netlist in the form of:

- Gate pin-to-pin initial delay
- Pin and wire parasitics capacitance, inductance and resistance

The gate pin-to-pin delay is needed for the delay degradation calculation according to formula 2.18. The gate parasitics are needed for the estimation of the switching activity.

Further on, the operation parameters are obtained through a simulation of the netlist. Such parameters are listed as following:

- Total time a signal has a value of logical "0", during the whole simulation
- Total time a signal has a value of logical "1" during the whole simulation
- Number of signal toggles in the whole simulation
- Total simulation time

Often, all those parameters are called the switching activity of a signal. Once that information is available, all parameters of the NBTI model are known, with exception of the technology dependant parameters and the temperature distribution. The technology dependent parameters are provided as a text file to the NBTI simulator. The temperature must be evaluated additionally. To do that, the temperature dependence of the the power dissipation is used. Also, it depends on the materials used for the chip manufacturing as well as the cooling methodology. Using the information from the first two phases of the flow, the power dissipation of the circuit is evaluated. After the temperature is available, the NBTI delay degradation is estimated for a given time. The degraded circuit is analysed and the impact of the NBTI is outputted in the format defined in the requirements.

The flow above is high-level and each of the activities may be broken down into activities according to the digital circuit design flow. In the following subsections each of the steps is defined as inputs and outputs and if necessary broken down into sub-steps.

4.2.1 Evaluation of Netlist Parameters

If we describe the evaluation of netlist parameters as a black box it looks as depicted in figure 4.3.

Figure 4.3: Evaluation of Netlist Parameters Black Box View

It accepts as an input the netlist file, the library files, and the design constraints; and outputs the parasitics and the initial pin-to-pin delay. Since one of the requirements is that

the simulation has to be integrable with EDA tools, for the parasitics and delay file we use the standard formats: the standard parasitics format (SPF), and the standard delay file (SDF).

The information about the parasitics is technology dependent and this it is not a part of the standard RTL or gate-level netlist. Very often the EDA tools provide library files, which contain this information. Using those library files, the netlist is recompiled and the parasitics for each gate and wire are generated in the SPF file format. In the compilation step, the circuit design constraints are taking into account. Such circuit design constraints could be the types of gates allowed. After the netlist is compiled, a static timing analysis is performed to generate the delay file. The complete data flow is shown in figure 4.4.

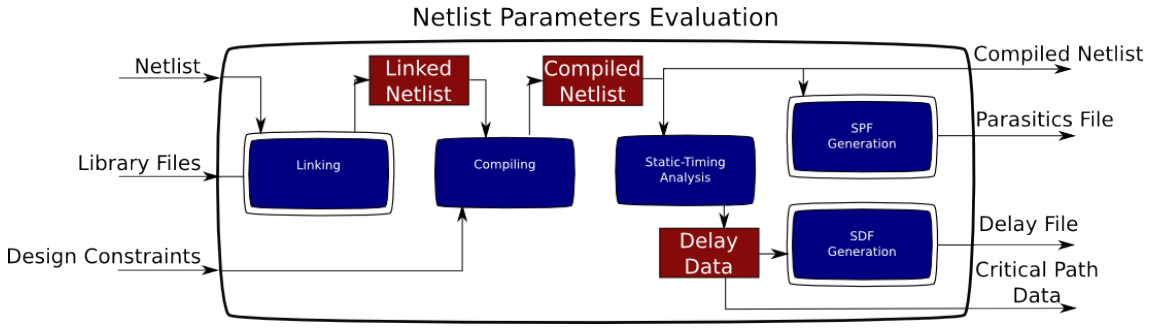


Figure 4.4: Evaluation of Netlist Parameters. White Box View

4.2.2 Simulation of Operation Parameters

The operational parameters needed for the NBTI model are the gate potential or the gate-source voltage (V_{GS}) and the operating temperature for each gate (T). Both of these parameters are functions of the time, and changing constantly depending on the signals provided at the inputs of the circuit. For the purpose of the long-term simulation, the amplitude of the gate-source voltage and the steady state temperature are taken. Possibly, there are other variants like the average of the gate-source voltage, which is the integral over the p-MOSFET on-time. We assumed that the gate-source voltage is approximately the same as the drain-source voltage suggested in [1]. For the purpose of temperature evaluation, the switching activity is required. It is obtained through simulation with pseudo random patterns. The black-box model of the operation parameters simulation is shown in figure 4.5:

Figure 4.5: Netlist Parameters Evaluation White Box View

The inputs are the compiled netlist that is about to be simulated and the library files. The output is the switching activity for each signal in the standard switching activity interchange format file - SAIF and a testbench file, to be reused further in the flow.

The internal white-box model of the operation parameter simulation is shown in the figure 4.6.

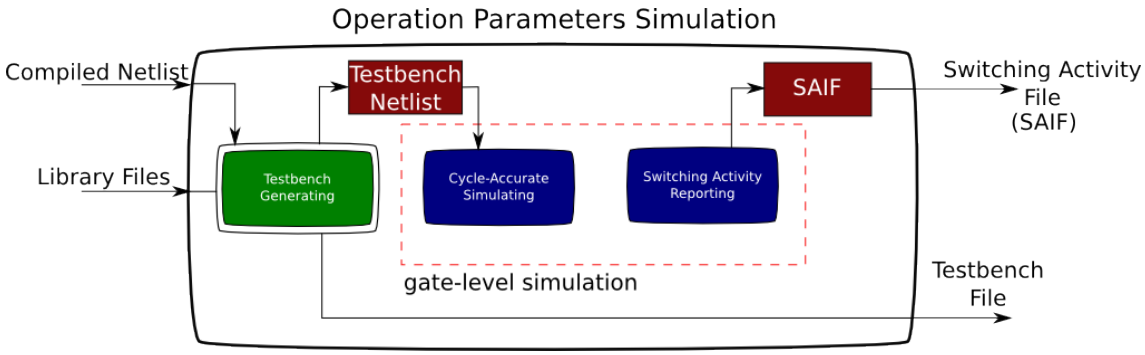


Figure 4.6: Netlist Parameters Evaluation White Box View

In order to simulate the gate-level netlist, a testbench is needed to provide pseudo-random signals to the inputs of the circuit under simulation. This is not a standard step in the design flow of the digital circuit design, thus it must be implemented additionally or an external tool must be used. After that, the gate-level simulation is performed. During each simulation cycle, the switching activity data for each signal is recorded. At the end of the simulation, it is generated and stored as a SAIF file.

The switching activity is used in the next step for the purpose of switching power dissipation evaluation.

4.2.3 Power Analysis

Generally, the power dissipated by a circuit can be classified into two broad categories:

- Leakage power
- Dynamic power

The leakage power is dissipated when the CMOS gate is not switching. Therefore it is also called static power. We distinguish two leakage power dissipation mechanisms:

- Intrinsic leakage power, caused by source-to-drain sub-threshold leakage
- Gate leakage power, caused by source-gate or gate-drain leakage

The leakage power depends on the technology and usually it is estimated using the power models defined the library files [16]. Models are also available for custom implementations. They are based on the technology parameters and voltage parameters - V_{DD} and V_{GS}.

In contrast to the leakage power, the dynamic power is dissipated during the switching of the CMOS gate. It is composed of two types of power:

- Internal power, or also known as short-circuit power

- Switching power

During the switching period there is a point of time when one or more p-MOSFET and one or more n-MOSFET are switched-on, establishing connection between the V_{DD} and the V_{SS} potentials. More often, this is observed whenever the p-MOSFET switches from on to off, and the n-MOSFET switches from off to on. The reason for that is the larger switching delay of the p-MOSFET. With the progressing of the NBTI degradation this delay is increasing and therefore the power dissipation increases as well.

The switching power is the power dissipated by the charging and discharging of the load capacitance. When the p-MOSFET is off, the load capacitance is charging, and when n-MOSFET is on, load capacitance is discharging. That is described by formula 4.1.

$$P_{sw} = \alpha C_L V_{DD}^2 f \tag{4.1}$$

where α is the switching activity of the CMOS gate, C_L is the load capacitance, and f is the operating frequency.

Having all the parameters obtained in the previous two steps, the power analysis can be performed. Figure 4.7 shows the black-box view.

Figure 4.7: Power Analysis Black Box View

In addition to the compiled netlist from where the gate names are fetched, for the static power dissipation the library files are needed. As mentioned before, the library contains parasitics and additional parameters concerning the static power model. Therefore, it is required for the static analysis. For the dynamic power the switching activity is used, as well as the library files, which are required for the internal power dissipation evaluation. This is because the internal power model depends on technological parameters as shown in figure 4.8.

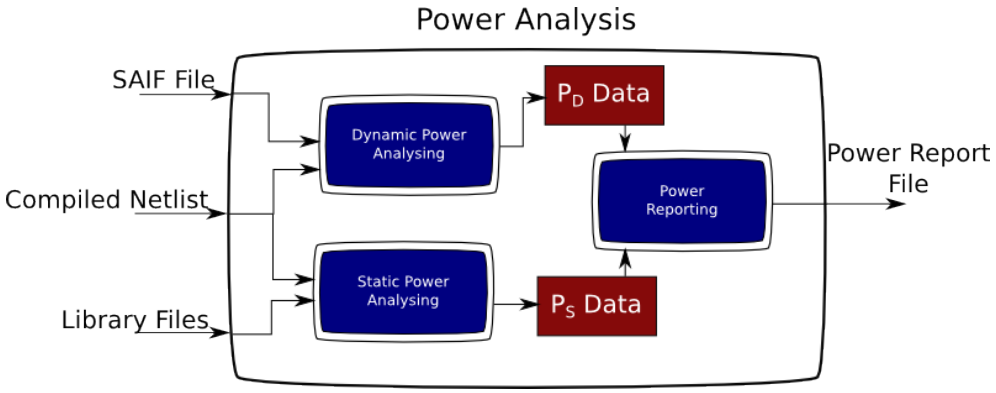


Figure 4.8: Power Analysis White Box View

The generated power report file contains information about the average power for each cell from the netlist. Having that information, it is possible to estimate the temperature distribution on the ICs.

4.2.4 Temperature Analysis

The temperature analysis is one of the most complex procedures in the simulation flow. Once it is generated from the power dissipation, the heat distributes over the IC chip area. Some portion of the heat interacts with the environment, or the thermal package, which may include heat sink, fan, etc. Therefore, to model the temperature dissipation in a precise way, information about the physical structure of the IC chip is required. Fortunately, many of those manufacturing parameters are standard and are assumed or configured before the temperature analysis. However, the geometrical information about the chip cannot be assumed. Commonly, the heat distribution modes are based on differential equations modelled with RC equivalent circuits [20]. Therefore, the physical information is high-level such as floor-plan, but rarely a detailed layout, is required.

In the presented master work, the Oil-Silicon model implemented by the HotSpot 5.0 thermal tool is selected. The temperature flow is modelled as an oil flow, distributed over the chip area with a structure shown on figure 4.9.

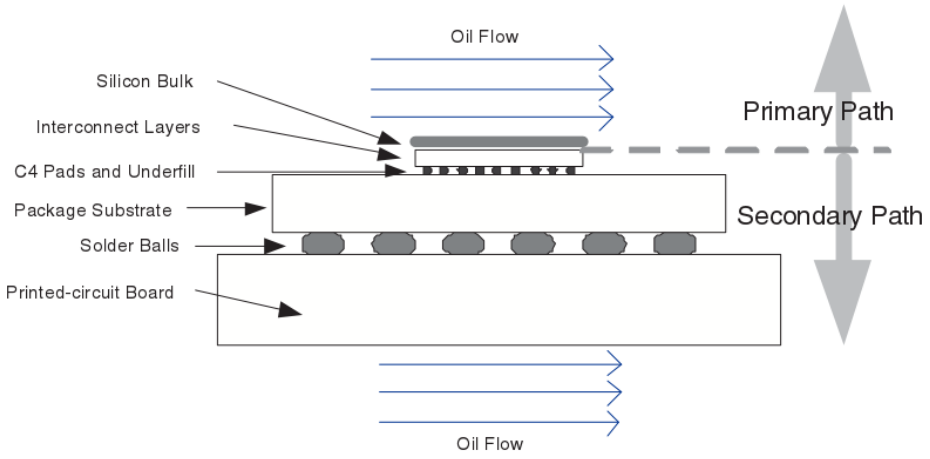


Figure 4.9: Oil-Silicon Thermal Model. Source [8]

The package configuration consists of silicon bulk, interconnect layers, pads and underfill, package substrate, solder balls and printed circuit board (PCB). The heat is transferred in two paths: primary and secondary. Through the primary path, the heat is released in the air, while through the secondary path the heat is removed through the interconnect layers down to the PCB. All those assumptions are made for achieving better results with the experimental

data of temperature distribution measured with infrared (IR) sensors [8].

To apply the model, the floorplan, the power dissipation for each floor and the configuration parameters of the heat model are required. The temperature analysis black-box view is shown in figure 4.10.

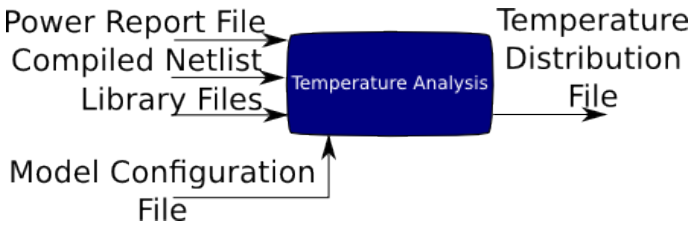


Figure 4.10: Temperature Analysis Black Box View

From the power analysis, the power dissipation for each gate is available. In addition, it is possible to generate the physical layout of the IC containing the geometric data for each cell from the netlist. The layout may be divided into big clusters for which the total power dissipation is calculated. The resulted clustered layout is parsed in the required floor-plan format. For each cluster, the total power is calculated and parsed to the required file format by the thermal analysis tool. Having the floorplan physical data and the power dissipation for each floor, a thermal simulation is performed, estimating the temperature for each floor. Finally, the temperature distribution is reported in a file (figure 4.11).

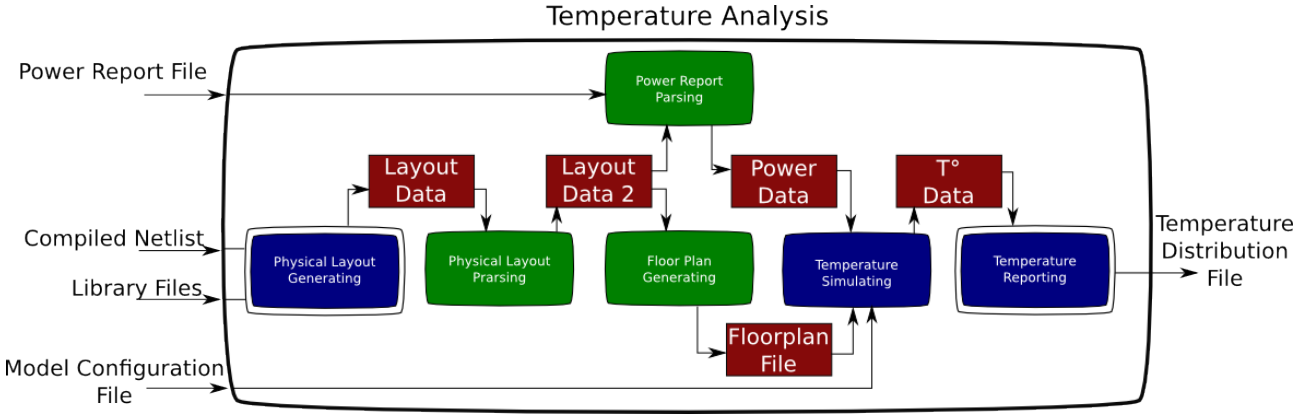


Figure 4.11: Temperature Analysis White Box View

The temperature analysis is the last step from the parameters acquiring. When it is completed, the NBTI degradation can be estimated by using the selected model.

4.2.5 NBTI aging degradation estimation

Once all parameters are approximated, the NBTI aging degradation can be estimated. The desired result of that estimation is the delay degradation for each cell in the netlist. Viewed

as a black box (figure 4.12), the process accept as inputs all data acquired in the previous steps.

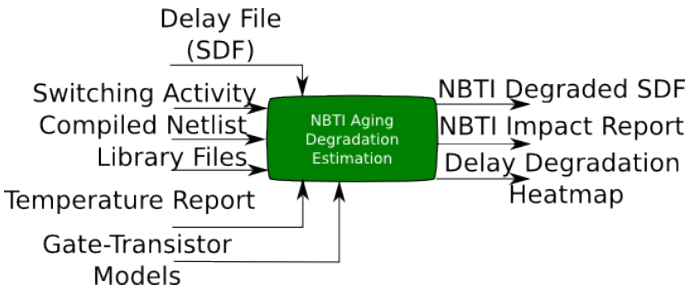


Figure 4.12: NBTI Aging Degradation Estimation Black Box View

That includes the temperature data, the switching activity, and the technology libraries. In addition to that, to estimate the NBTI degradation, transistor level models of the gates are needed. All other information such as gate names, input and output signals are fetched from the netlist. The delays are outputted in the SDF format, so they can be used for analysis by EDA tools in the further step. In addition, in that step a delay degradation heatmap is created to visualize the NBTI degradation, and the delay statistical data is evaluated - this is the statistical median and statistical mean of relative delay degradation of all cells in the netlist.

The white box view of the process is shown in figure 4.12.

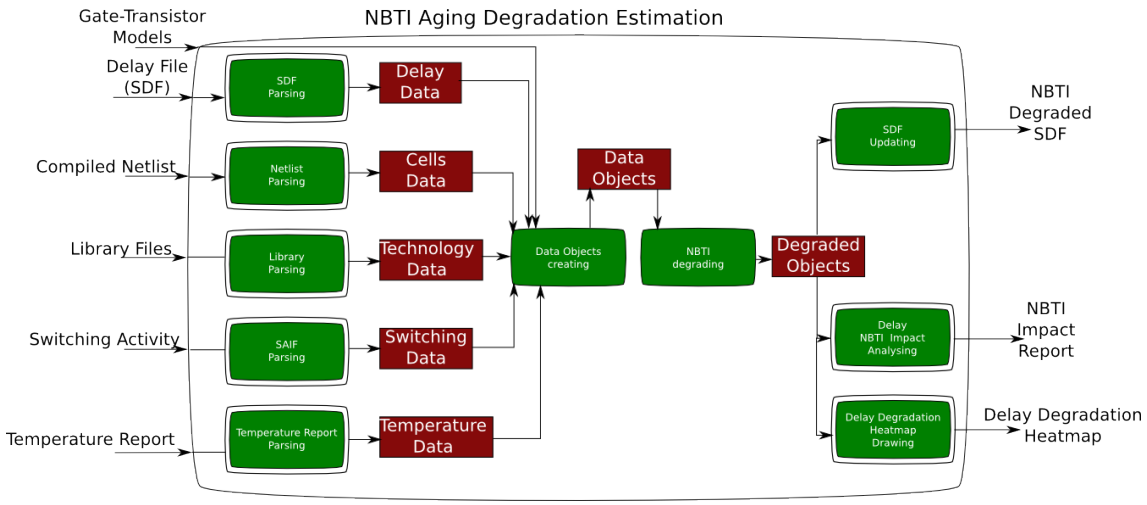


Figure 4.13: NBTI Aging Degradation Estimation White Box View

Since this process is not using EDA tools, and it is implemented as a program, the first step is to parse all the input files produced in the previous stages of the flow. The results are stored in data objects, which structure and hierarchy is determined during design time. Using the gate-transistor models, the objects encapsulate information about the p-MOSFET structure

of the CMOS gate. That allows the NBTI threshold voltage degradation to be estimated for each p-MOSFET of a gate. Knowing the threshold voltage degradation and p-MOSFET circuit, the gate delay degradation is calculated. It is then updated in the SDF file. Using the data stored in the objects, the mean values of the delay degradation and the number of cells with delay degradation larger than zero are calculated and stored in a file. Also, a heatmap is created, depicting every polygon of the physical layout with different colour depending on the value of the delay degradation.

Further on, the power dissipation and the critical path of the degraded circuit are required. This is done in the next step.

4.2.6 Impact of NBTI Analysis

The critical path and the power dissipation of the degraded circuit are obtained through static time analysis and power analysis, using the degraded SDF file. The black box view is depicted in figure 4.14.

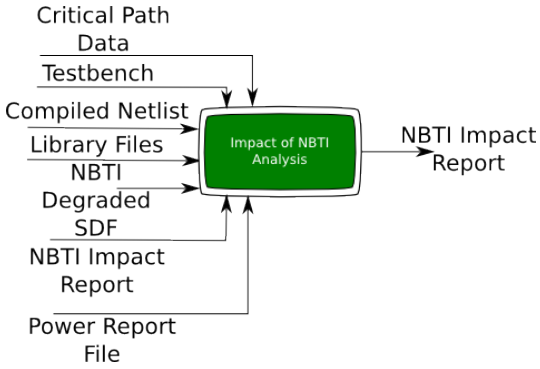


Figure 4.14: NBTI Aging Degradation Estimation Black Box View

For the purpose of the static time analysis, the compiled netlist, the library files, and the NBTI degraded SDF file are necessary. The power dissipation requires the switching activity, which is obtained through additional gate-level simulation. Therefore, in addition to the netlist, the delay file, and library files are needed in the testbench. The last input is the NBTI impact report generated in the previous step, containing the number of cells suffered NBTI degradation, and the statistical delay information from all the cells in the netlist.

Initially, the netlist is linked with the technology library. A static timing analysis is used for the evaluation of the critical path delay and cells. In parallel, a gate-level simulation can be performed, since both operations are independent. The evaluated switching activity is used for power analysis. The critical path and power data generated after NBTI degradation are compared with the nominal data and the impact of the NBTI is estimated. Finally, the NBTI impact report is updated with the power and critical path degradation analysis data in order to complete the output requirements. The internal data flow is depicted in figure 4.15.

This activity completes the simulation flow on architectural level. It is independent of the EDA tools and the programming framework, which are determined in the next phase - the design of the NBTI simulator.

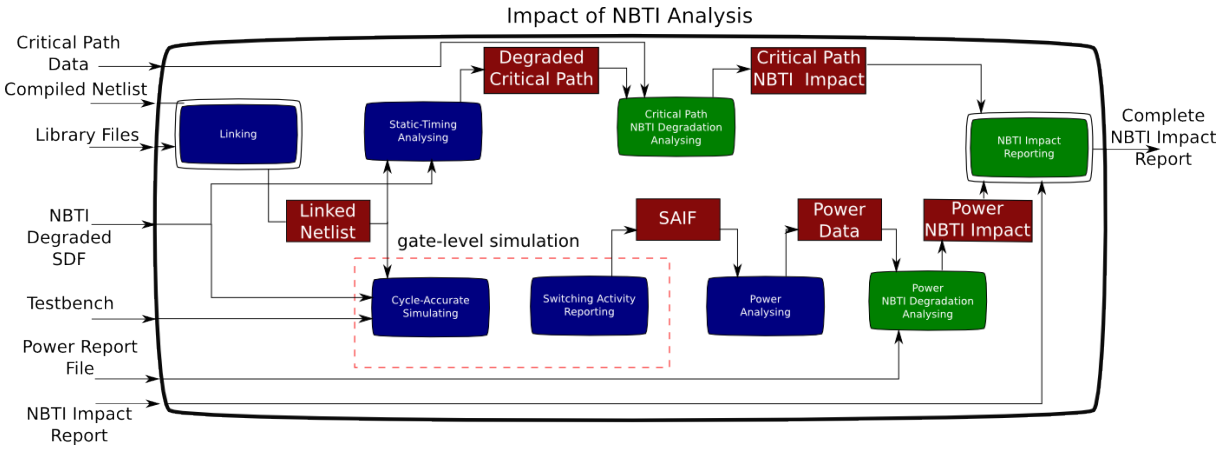


Figure 4.15: NBTI Aging Degradation Estimation White Box View

4.3 Simulator Design

The following design decisions are made:

1. Synopsys Desing Compiler is used for linking, compiling, static timing analysis, parasitics and delay reporting
2. Synopsys Verilog Compiler Simulator (VCS) is used for gate level simulation
3. Synopsys PrimeTime PX is used for power analysis
4. HotSpot 5.0 thermal tool is used for temperature analysis
5. Python 2.7 is used for implementation of the NBTI degradation analysis, and all supporting scripts.
6. Cadence Encounter is used for generation of physical layout of the circuit
7. The gate-transistor models are integrated in the NBTI degradation simulator

Taking into account the design decisions, the simulation flow graph is modified as shown in figure 4.16.

First, the circuit parameters are evaluated using the Synopsys Design Compiler. With this tool, the netlist is compiled and the standard delay format file, the standard parasitic format file are generated. Further on, a testbench is generated by a custom Python script for the purpose of the gate level simulation. The simulation is executed with the Synopsys VCS simulator, outputting the switching activity in a SAIF format. The SAIF and SPF files are used for the power analysis done by the Synopsys PrimeTime tool. The output of the power analysis is the power dissipation for each cell and the average power of the whole circuit, stored in the power report (PRT) format. Next, the physical layout is generated through the Cadence Encounter tool. The layout is stored as a graphical database system (GDS) file. This file is transformed into text file by the Java open source application - JGDSPARSER. After

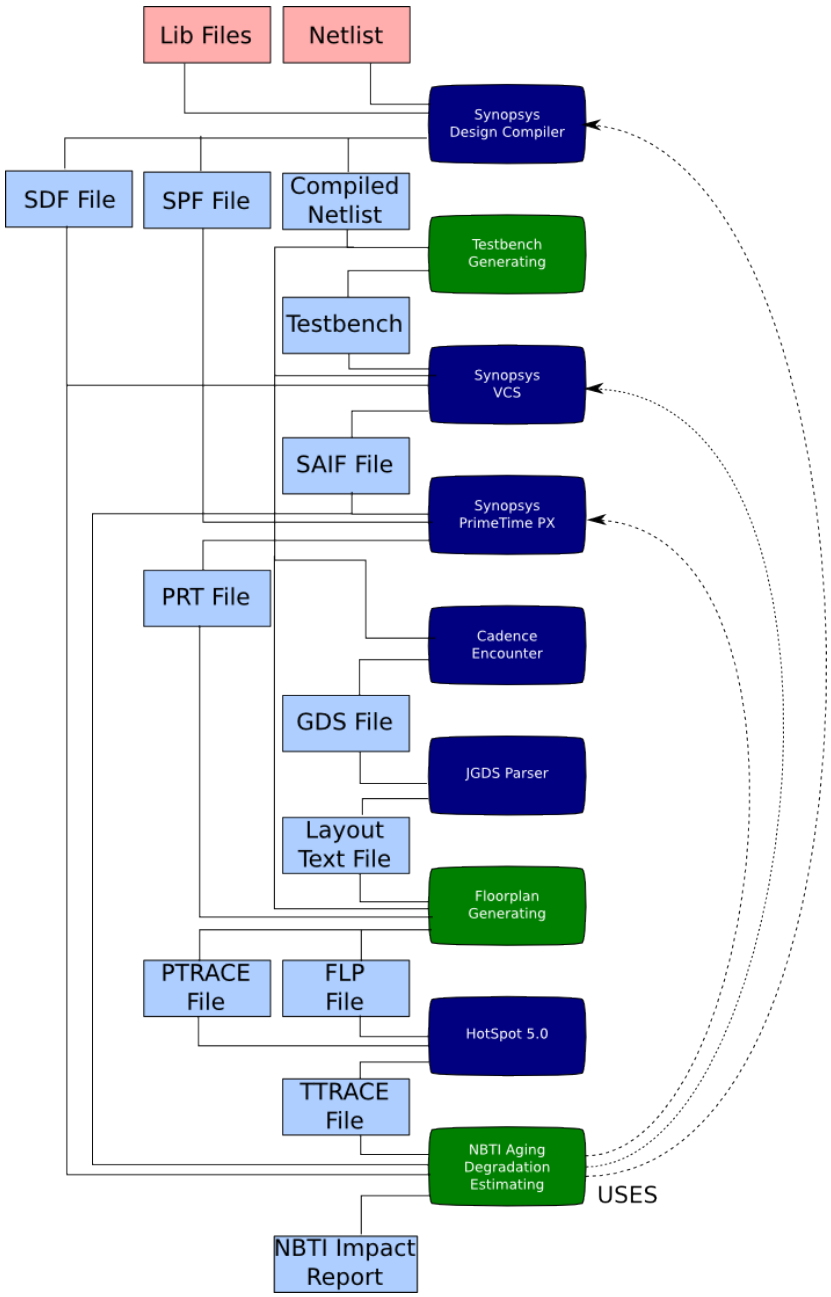


Figure 4.16: NBTI Degradation Simulator Design High Level View

the GDS parsing, the required by HotSpot floorplan layout and power report are created, by a custom Python script. The HotSpot tool evaluates the temperature and outputs it as temperature trace file (TTRACE). With the SAIF and the SDF files, the NBTI degradation is calculated according to the model, and a new SDF file with degraded delay information is created. With the new SDF file, the script calls again the Synopsys Design Compiler,VCS,

and PrimeTime to obtain the required statistical information about the impact of the NBTI degradation. Lastly, the impact report is generated for analysis.

In the diagram, the custom Python scripts are depicted with green. The detailed design is presented in the following subsections.

4.3.1 Testbench Generating

The purpose of the testbench is to provide pseudo-random input stimuli to each input of the circuit subject of NBTI degradation. Three parameters are configured prior to the generation of the testbench:

- number of random patterns N
- random stimuli time period T_{input}
- clock signal time period T_{clk}

Some circuits requires clock signal, even though they are entirely combinational. Therefore, in the testbench a clock signal is generated in addition to the input stimuli. The algorithm of the testbench stimuli inputting is shown in figure 4.17.

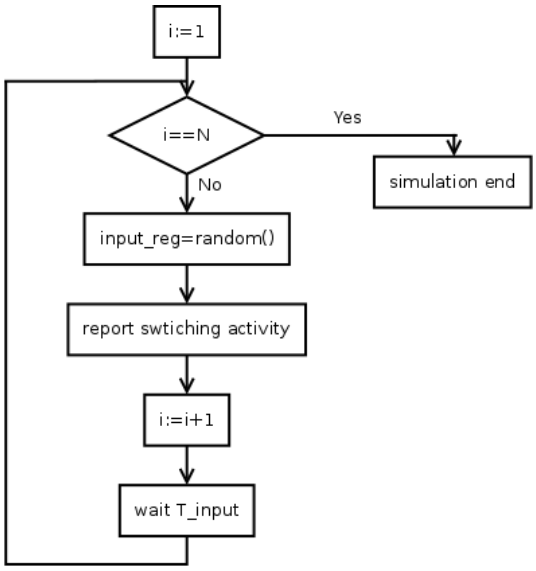


Figure 4.17: Testbench Stimuli Input Algorithm

For N iterations, pseudo-random stimulus are provided to the input register that forward them to the inputs. In each iteration, the switching activity is reported.

The testbench is created on the base of a template, that defines the structure of the Verilog file. The template is edited as follows:

1. from the given netlist the names of all inputs are recognized
2. an instance of the circuit defined in the netlist is added in the testbench

3. an input register array with the size of the inputs is added , with a single register size not larger than 32. The array is connected to the inputs of the circuit.

4. the parameters N, T_{input}, and T_{clk} are configured

5. the output file name for the SAIF is configured

The created testbench is a key factor of the gate level simulation, which main purpose is the estimation of the switching activity. Through it, the power is calculated. But before this power is used for temperature analysis, the required floorplan layout and power must be generated.

4.3.2 Floorplan Generating

The first task of this process is to create the floorplan file, containing the coordinates of each floor in the chip. This is done by dividing the chip area into a grid of equally sized rectangular floors. The floor size is defined by the grid number of rows (w) and grid number of columns (h).

Once the coordinates of each floor are determined, each cell is registered in the floor, inside which boundaries it is allocated. The cell which is allocated inside more than one floor is registered only with this portion of area that is inside the particular floor.

As it is shown in figure 4.18, only the part of the cell inside the floor is considered.

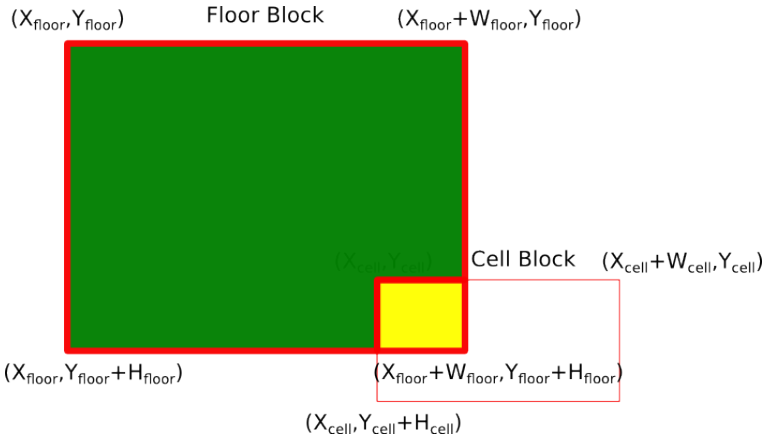


Figure 4.18: A cell partially inside a floor

If we transfer that on the X axis, only those points that are satisfying the condition $x \in [X_{floor}, X_{floor} + W_{floor}]$, and on the Y axis only points satisfying the condition $y \in [Y_{floor}, Y_{floor} + H_{floor}]$ are added.

Once the coordinates of the portion of the cell inside the floor is determined, its power is calculated. This is done by multiplying the power density of the whole cell to the cell area inside the floor. The complete algorithm for appending boundary cell is depicted in figure 4.19.

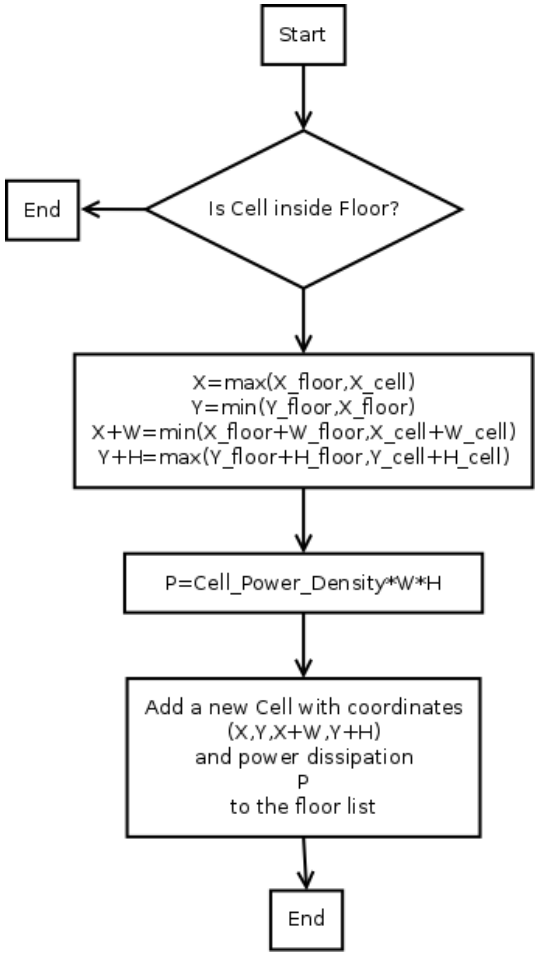


Figure 4.19: Boundary Cell division algorithm

With this approach the total estimation of the power is not affected by the way the chip is divided into floors. The floorplan data is used by the HotSpot tool to evaluate the temperature. Once that is done, the NBTI degradation is calculated using a given model.

4.3.3 NBTI Aging Degradation Estimation

The NBTI aging degradation is estimated using the long-term model described in chapter 2. Using formula 2.12, the absolute change of the threshold voltage due to NBTI degradation is estimated, and then using 2.18 the delay change is calculated.

The process is organized into four activities (figure 4.20).

The first is the fetching of all gates from the compiled netlist. The gates are stored in an object of type “gate” and organized into a Python dictionary data structure. The class “gate” contains objects of type “pmos”, in which the transistor level information is stored (V_{th}, α, rise and fall delays). Each "pmos" object is associated with its input signal by storing its name according to the netlist definition.

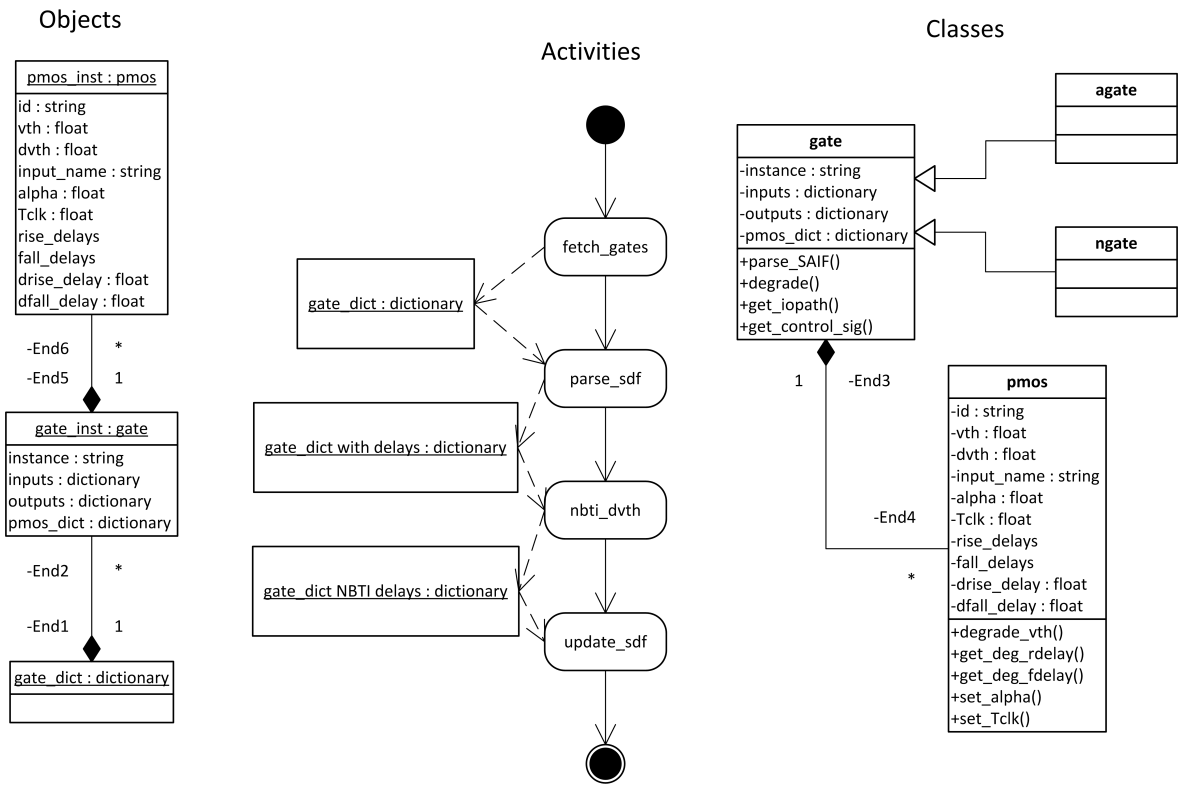


Figure 4.20: NBTI Aging Degradation Activities

After the initialization of all gate objects, there is no information about the delay of the gates. Therefore, the created by Synopsys design compiler SDF file is processed. The SDF file contains the input to output propagation delay for specified transitions. Depending on the type of the CMOS gate, the fetched delay is mapped to rise and fall delay of one of the "pmos" objects contained in the gate object. For this purpose, two types of gate class are specialized - ngate and agate. The "ngate" class corresponds to a native CMOS gate without integrated inverter, while the agate class corresponds to a CMOS gate with integrated inverter.

Once the delays are stored, the formulas 2.12 ad 2.18 are applied on each "pmos" object, calculating the NBTI threshold voltage and delay degradation for the whole circuit. Then, a new SDF file is created, updating the SDF file generated by the Synopsys design compiler with the NBTI degraded delay. Using this SDF file, the static timing analysis and power analysis are performed to obtain the required output.

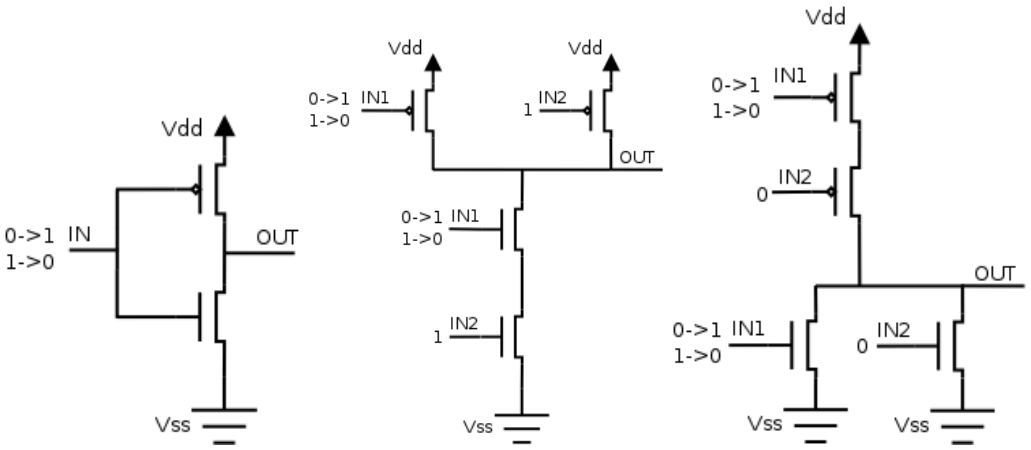
4.3.4 Processing the Standard Delay Format File

The SDF file consists of delay entries for each cell in the netlist. Each entry has the following syntax:

celltype ::= (**CELLLTYPE** QSTRING)
cell_instance ::= (**INSTANCE** PATH)
del_spec ::= (**DELAY** deltype+)
deltype ::= (**ABSOLUTE** *del_def*+)
del_def ::= (**IOPATH** *port_spec port_instance del_def*+)
(**RETAIN** deval_list)*deval_list)
deval_list ::=delval
||=deval deval

where, QSTRING is character string with quotes, PATH is the hierarchical name of the cell instance, *port_spec* is the particular input name, and *port_instance* is the output name of the gate. The delay value (de_val) can have one or two instances depending on the transitions of the gate output signal. The first delay value is determining the rising (01) transition, while the second is determining the falling (10) transition of the output signal.

The delay value specify the propagation delay from the *port_instance* input to the output, assuming that non-control values are assigned to all other inputs [5]. Therefore, the delay depends only on the delays of the MOSFETs along the propagation path. For the most basic set of gates only one or two p-MOSFETs can be met along any of the paths, assuming the transistor structure shown in figure 4.21 and 4.22.

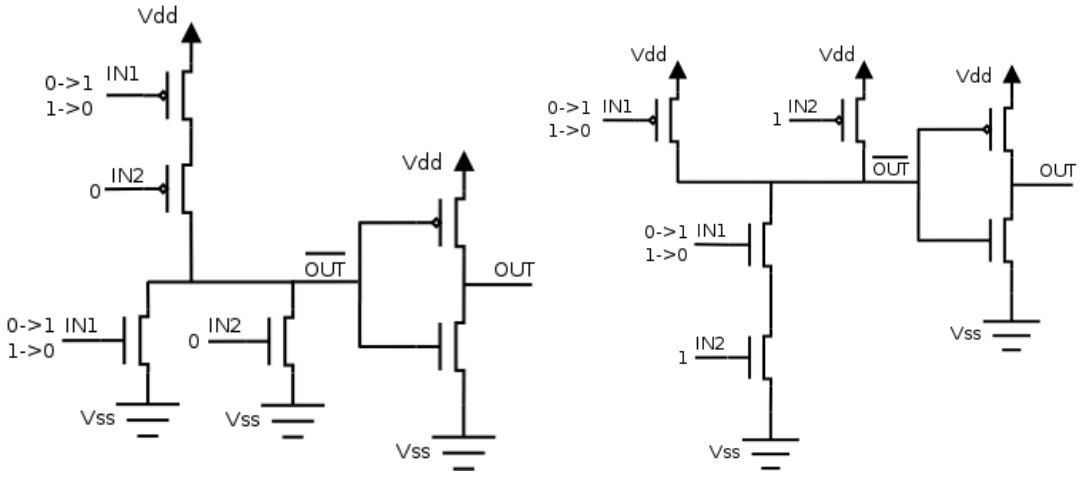


(a) INV CMOS Gate (b) NAND CMOS Gate (c) NOR CMOS Gate

Figure 4.21: Transistor Models of Basic CMOS Gates

Considering the CMOS gates NAND and NOR, each pin-to-pin delay will determine the delay of one pair p- and n-MOSFET delays. Knowing that the p-MOSFET switches several times slower due to the slower mobility of the holes [19], it is possible to associate the rise delay with the p-MOSFET delay and the fall delay with the n-MOSFET delay. Therefore, only the first de_val is changed due to the NBTI degradation.

In the case of CMOS gates AND and OR, assumed is integrated inverter at the output of the NAND and NOR CMOS gate respectively. In that case the propagation path includes two p-MOSFET - the one sharing the input and the additional p-MOSFET of the inverter.



(a) OR CMOS Gate (b) AND CMOS Gate

Figure 4.22: Transistor Models of Basic CMOS Gates with Integrated Invertor

The first p-MOSFET is determining the rise delay of the signal before it is inverted, and the second p-MOSFET is determining the rise delay of the inverted output signal. After the signal is inverted, the rise delay is transferred to the fall delay. Therefore, both the rise and the fall delays are degraded by the NBTI degradation. The rise delay is affected by the degradation of the integrated inverter p-MOSFET at the output, and the fall delay is affected by the degradation of the p-MOSFET connected directly to particular input pin.

The reading of the SDF file and storing the delay information to the created “gate” objects in the previous stage is done by referencing the cell instance value, which is unique for the whole netlist. The “gate” objects are specialized with the types “ngate” and “agate” for natural CMOS gates and CMOS gates with integrated inverter respectively. The second one contains additional “pmos” object related to the p-MOSFET of the input. Using the input name in the del_def the input “pmos” object is referenced, and using the output name the output “pmos” object is referenced.

After the SDF file is parsed, the delay change due to the NBTI degradation is calculated for each cell. Using that information, the SDF file is updated and stored under different name. The updated SDF file is used for static timing analysis, simulation, and power analysis.

4.4 Implementation

The whole NBTI simulator is implemented following the design described. It consists of Python, Shell and Tcl scripts. The main script named “nbtisim.sh” is written in Shell script and accept the following parameters:

- netlist file path
- target module
- number of patters

- input stimuli period
- clock half period
- floorplan grid height
- floorplan grid width
- saif file path
- NBTI simulation duration in years
- gate-source voltage V_{gs}

All files produced during the execution such as SDF, SPF, ptrace, ttrace, etc are stored in the project directory. Exception is the SAIF file, which is created during the gate level simulation. Its name is provided as input in order to provide the possibility to increase the file write time by accessing faster local storage.

The algorithm complexity of the NBTI simulator is linear O(N), where N is the cells in the netlist. However, the whole program including the external EDA tools depends also on the number of patterns. This tendency may be observed in the tables 4.1 and 4.2.

circuit	c432	c49	c1355	c3540	c5315	c6288	p45k	p100k
number of cells	58	487	485	879	1489	2332	22597	54198
total execution time, s	22	38	38	67	98	567	808	2796
Synopsys execution time,s	17	34	34	63	94	560	750	2631
Python execution time, s	5	4	4	4	4	7	58	165

Table 4.1: NBTI Simulator Execution Time for 100000 Patterns

number of patterns	10	100	1000	10000	25000	50000	100000	500000
total execution time, s	28	28	33	83	166	297	567	2739
Synopsys execution time,s	21	21	26	76	159	290	560	2732
Python execution time, s	7	7	7	7	7	7	7	7

Table 4.2: Simulator Execution Times for circuit c6288

Table 4.1 shows the execution times for several testbench circuit for the ISCAS and NXP packets. The total execution time is the time for which the whole NBTI simulation flow was executed. The Synopsys execution time is the time for executing the Synopsys DC static timing analysis script, the VCS gate level simulation, and the PrimeTime power analysis. The Python execution time refers to the execution of all Python scripts and the HotSpot thermal analysis tool. We can see that the with the increasing of the cells number the Synopsys execution time increases, as well as the Python execution time. For the smaller number of cells the increasing trend is almost unnoticeable, because the time for loading libraries,

linking and compiling dominate the simulation execution time. For circuits with more than 2000 cells the dependency between the number of cells and execution time is noticeable and approximately linear concerning the Python scripts execution. In addition, table 4.2 shows no dependency between the Python execution time and the number of patterns.

Having discussed the design and implementation of the proposed NBTI simulation flow, now the analysis of how NBTI affects the circuit performance can be presented.

5 Simulation Results

Using the implemented NBTI simulator, we simulate different benchmark circuits to analyse the effect of NBTI. The simulation are done changing one of the following parameters

1. the NBTI degradation time
2. the initial temperature
3. the drain to source voltage $V_{dd} - V_{ss}$

The target circuits are from the ISCAS89 benchmark packet and the NXP benchmark packet. Using the simulation data, we analyse the impact of the NBTI.

For NBTI aging degradation model, equations 2.13 and 2.18 are used with parameters determined according to the Synopsys 90nm technology library and [1]. All constant values are given in table 5.1 in SI units.

E_a,[eV]	0.49	k, [eV/K]	8.6173e-005
T_0, $[s/m^2]$	1e10	q, [C]	1.6e-19
t_{ox}, [m]	1.4e-9	t_e, [m]	2.15e-9
ϵ_0, $[A^2s^4kg^{-1}m^{-3}]$	8.8542e-12	ϵ_{rox}	3.9
ϵ_1	0.9e-9	ϵ_2	0.5e-4
E_{01}, $[V/m]$	3.35e+8	K_1, $[C^{-0.5}m^{-2.5}]$	9.4868e+25
n	1/6	δ	0.5
V_{th},[V]	-0.58	C_{ox},[F/m]	0.02466

Table 5.1: NBTI Aging Degradation Model Parameters

This chapter analyses the simulation results of NBTI aging degradation. We start from the simplest case - degradation of only one p-MOSFET is analysed applying static and dynamic stress. Then, analysis is presented for a selection of the ISCAS89 and NXP benchmark circuits.

5.1 NBTI Impact on a Single p-MOSFET

To understand how the NBTI aging degradation affects the circuit, we start from the simplest case - one p-MOSFET. To do that, the NBTI degradation model is implemented in MATLAB with all technology specifications of a p-MOSFET 90nm transistor, such as the one used in the CMOS gates. Important is the impact of the NBTI degradation of the threshold voltage V_{th} and the relative delay change $\Delta t/t_0$, where t_0 is the initial delay.

5.1.1 Time Dependance

The first set of simulations are done by fixing the drain-source voltage V_{ds} to 1.2 V and the temperature to $75°C$. The NBTI degradation time (t) is variable. According to the model, we expect to see increasing degradation throughout the years, which is the reason why the process is often related to the term "aging". Table 5.2 shows the impact of the NBTI aging degradation on the threshold voltage and the switching delay in the case of static gate voltage stress (α=1).

t, years	1	3	5	7	10	15	20
ΔV_{th},V	0.1585	0.1904	0.2073	0.2193	0.2327	0.249	0.2612
$\Delta t/t_0$	51%	61%	67%	71%	75%	80%	84%

Table 5.2: Statistical Mean of NBTI Delay Degradation With Respect to the Time in Years For Static Gate Voltage Stress

The results are showing that after an year of constant stress the threshold voltage shifts with about 158.5 mV, so that it becomes $-0.58 - 0.1585 = -0.7385V$. The switching delay increases with 51% for one year stress and with 75% over ten years stress. This a significant degradation, and shows how important is to avoid gates under constant stress and to make sure that there are no gates that constantly apply gate stress on their p-MOSFETs.

Due to the very fast recovery process, NBTI aging degradation with dynamic gate stress voltage has significantly smaller impact. Table 5.3 shows the threshold voltage absolute change in Volts, through the years, for different stress ratios.

α \ t, years	1	3	5	7	10	15	20
0.1	0.0103	0.0124	0.0135	0.0143	0.0151	0.0162	0.017
0.3	0.0129	0.0155	0.0169	0.0179	0.019	0.0203	0.0213
0.5	0.0149	0.0179	0.0195	0.0206	0.0218	0.0234	0.0245
0.7	0.0197	0.0237	0.0258	0.0273	0.029	0.031	0.0325
0.9	0.0309	0.0371	0.0404	0.0427	0.0454	0.0485	0.0509

Table 5.3: Statistical Mean of NBTI Threshold Voltage Degradation With Respect to the Time in Years For Dynamic Gate Voltage Stress

In the worst case, when α=0.9 the expected threshold voltage degrades to -0.6254 V for 10 years, which is a common period for a life-cycle. The degraded threshold voltage is expected, when applied random signal can reach -0.6018 V. The best case is observed when α=0.1, and the expected new value of the threshold voltage is -0.5951 V. This is a 6.7 mV difference from the case α=0.5.

The impact of the NBTI degradation on the switching delay is presented in table 5.4.

According to the results, in the worst scenario NBTI degradation may change the switching

t, years / α	1	3	5	7	10	15	20
0.1	2.30%	3.09%	3.96%	4.89%	5.47%	6.06%	6.67%
0.3	2.88%	3.87%	4.95%	6.12%	6.85%	7.59%	8.36%
0.5	4.80%	5.76%	6.28%	6.64%	7.04%	7.54%	7.91%
0.7	6.36%	7.64%	8.32%	8.80%	9.34%	9.99%	10.48%
0.9	9.97%	11.97%	13.04%	13.79%	14.63%	15.66%	16.43%

Table 5.4: Statistical Mean of NBTI Delay Degradation With Respect to the Time in Years For Dynamic Gate Voltage Stress

delay up to about 15% for 10 years. That means that a guardband of 10% is not sufficient any more. In the average case, α=0.5, the degradation is 7%, which is almost 1.3 times more than the best case (α=0.1), and about 2.1 times less than the worst case scenario.

The simulated results, approve our expectation for increasing impact of the NBTI aging degradation throughout the time. It is also noticeable that the major degradation process occurs for a relatively short period of time, and then there is a slow down. Also, a very important factor is the stress ratio α. The results shows that a stress ration of 0.9 is leading to potential reliability risk, while a 0.7 stress ration is still above the 10% limit of delay change.

We have seen the strong dependence of NBTI degradation from the time. The results shows that NBTI is progressing significantly fast, and can be observed even in the first year. Also, as the name suggests, we may expect strong temperature dependence. Therefore, a set of simulations with T as a variable is performed.

5.1.2 Temperature Dependence

To analyse the temperature dependence, we fix the time to 10 years, the supply voltage to 1.2 V, while the temperature is changing. Table 5.5 shows the results for the case of static gate voltage stress.

T,[°C]	0°	25°	50°	75°	90°	105°	120°
ΔVth,V	0.1102	0.1474	0.1885	0.2327	0.2604	0.2888	0.3178
Δt/t0	35.55%	47.56%	60.81%	75.07%	84.00%	93.16%	102.51%

Table 5.5: Static Gate Stress NBTI Aging Degradation Temperature Dependence

As it is expected, there is a strong temperature dependence of the NBTI degradation. Most of the ICs are designed to work on lower temperature than 90°C. The results show decay behaviour, which means that in the operating range of 30-50°C, the delay degradation is more sensitive to temperature changes.

Considering the dynamic gate stress, similar tendency can be observed in tables 5.6 and 5.7.

α \ T,[°C]	0°	25°	50°	75°	90°	105°	120°
0.1	0.0071	0.0096	0.0123	0.0151	0.0169	0.0188	0.0207
0.3	0.0089	0.012	0.0154	0.019	0.0212	0.0235	0.0259
0.5	0.0103	0.0138	0.0177	0.0218	0.0244	0.0271	0.0298
0.7	0.0136	0.0183	0.0234	0.029	0.0324	0.036	0.0396
0.9	0.0211	0.0286	0.0367	0.0454	0.0508	0.0564	0.062

Table 5.6: NBTI threshold voltage degradation dynamic stress temperature dependance

α \ T,[°C]	0°	25°	50°	75°	90°	105°	120°
0.1	2.30%	3.09%	3.96%	4.89%	5.47%	6.06%	6.67%
0.3	2.88%	3.87%	4.95%	6.12%	6.85%	7.59%	8.36%
0.5	3.31%	4.45%	5.70%	7.04%	7.88%	8.75%	9.62%
0.7	4.38%	5.90%	7.56%	9.34%	10.46%	11.60%	12.76%
0.9	6.81%	9.21%	11.83%	14.63%	16.39%	18.18%	20.01%

Table 5.7: NBTI delay degradation dynamic stress temperature dependence

The threshold voltage degradation in the worst case reaches -0.63V for 90°C and about -0.62V for 50°C. In the best case, the threshold voltage degrades to -0.5969 for 90°C and -0.5959 for 50°C. In the case of random input, the expected stress ratio is about 0.5, and therefore we can expect degradation of about 7.88% for hot IC, and 4.45% relative delay change for cool IC chip. We can also see, that the slope of the temperature dependence is decreasing with α, meaning that the importance of the temperature decreases when the p-MOSFET switches more.

Finally, the dependence of the supply voltage V_{ds} is presented and analysed.

5.1.3 Supply Voltage Dependence

One may suggest that increasing the supply voltage leads to greater degradation of the switching delay, since it increases the electric filed applied on the dielectric layer. Nevertheless, the experiments show the contrary - NBTI degradation increases with the degreasing of the supply voltage. That means that in the future the impact of NBTI will increases, since the trend is to decrease the supply voltage.

The simulation experiments are done fixing the temperature to $75°C$, the time to 10 years, while varying the supply voltage V_{ds}. Table 5.8 shows the results for the case of static gate voltage applied

Simulation shows that the NBTI degradation strongly depends on the V_{gs} value. The weaker negative electric field applied on the gate oxide generates more traps in the transistor interface region, which decreases the effective threshold voltage. For the case of 0.9 V stress, the value of the threshold voltage becomes about 0.84 V.

V_{ds},[V]	5.0	3.3	2.5	1.2	0.9
ΔVth,V	0.1102	0.1474	0.1885	0.2327	0.2604
Δt/t0	1%	4%	11%	75%	154%

Table 5.8: NBTI aging degradation static stress temperature dependence

In the cases of dynamic stress, the supply voltage importance is lower but still a factor. For 0.9 stress ratio, in the worst case, the delay degradation may reach 30%, while for 2.5 V, it is only 2.08%. In the best case, the delay degradation may reach 10.02% for 0.9 V, but for 2.5 V it i only 0.69%.

α \ V_{ds},[V]	5.0	3.3	2.5	1.2	0.9
0.1	0.0009	0.0035	0.0066	0.0151	0.016
0.3	0.0011	0.0044	0.0083	0.019	0.0201
0.5	0.0012	0.0051	0.0096	0.0218	0.0231
0.7	0.0017	0.0068	0.0127	0.029	0.0307
0.9	0.0026	0.0106	0.0199	0.0454	0.048

Table 5.9: NBTI delay degradation dynamic stress temperature dependence

α \ V_{ds},[V]	5.0	3.3	2.5	1.2	0.9
0.1	0.04%	0.26%	0.69%	4.89%	10.02%
0.3	0.05%	0.33%	0.86%	6.12%	12.55%
0.5	0.06%	0.38%	1.00%	7.04%	14.45%
0.7	0.07%	0.50%	1.32%	9.34%	19.16%
0.9	0.12%	0.78%	2.07%	14.63%	30.02%

Table 5.10: NBTI delay degradation dynamic stress temperature dependence

Using the results of the single p-MOSFET NBTI degradation, it is possible to analyse the impact of NBTI on CMOS circuits.

5.2 NBTI Impact on CMOS Combinational Circuits

To analyse the impact of NBTI degradation on CMOS combinational circuits, set of simulations is performed with eleven circuits from the ISCS89 benchmark circuits, and two from the NXP benchmark circuits. The input stimuli applied during the simulation were pseudo-random with seed, meaning that for the generated stimulus of two different execution are

the same. This allows comparison of the power dissipation between the fresh and degraded circuit.

Like the analysis of one p-MOSFET, the simulation are performed with respect to three different variables: time, temperature, and drain-source voltage V_{ds}. For each of those cases, the gate delay , the critical path, and the power dissipation of each circuit are analysed.

The gate delay results are given as statistical mean, median, minimum, and maximum. The statistical mean or average is calculated as the sum of each gate relative change due to NBTI degradation in the circuit and divided by the total number of the gates. The statistical median is evaluated by sorting the gates by relative delay degradation value and taking the value in the middle of the list. The statistical minimum and maximum are the first and the last value respectively, of the sorted list of relative delay degradation due to the NBTI.

The critical path degradation is analysed by the values of the critical path average delay degradation, relative length degradation and relative number of cells changed in the degraded critical path comparing them to the cells of the original one.

Finally, the power dissipation is analysed by presenting the average value for the relative total power dissipation degradation.

The first set of simulations performed is with respect to the time.

5.2.1 Time Dependence

To analyse the time dependence, the drain-source voltage is fixed to 1.2 V, the temperature is fixed to $75°C$, and the time is varying over years. Since the results of some circuits were very close to other, the results are presented for three circuits from the ISCAS89 benchmark packet - c880, c1908, and c6288; and one from the NXP benchmark packet - p45k. The number of patterns used for gate-level simulations is 10000 for all circuits.

Knowing that the stimuli are random, we expect to see results very close to the results of single p-MOSFET delay degradation for α=0.5. However, depending on the circuit logic, it is possible to have gates with low switching probability. This may increase the α for a particular group of gates increasing the average delay.

The gate delay statistical results are shown in the tables 5.11, 5.12, 5.13, 5.14.

t, years / circuit	1	3	5	7	10	15	20
c880	6.14%	7.38%	8.03%	8.50%	9.02%	9.65%	10.12%
c1908	8.83%	10.61%	11.55%	12.22%	12.97%	13.87%	14.56%
c6288	4.77%	5.73%	6.24%	6.60%	7.01%	7.50%	7.86%
p45k	10.34%	12.41%	13.52%	14.30%	15.17%	16.23%	17.03%

Table 5.11: Statistical Mean of NBTI Delay Degradation With Respect to the Time in Years

We can see from table 5.11 that the average values of the delay degradation are rather high for the circuits c1908 and p45k. C1908 average delay reaches the 10% for 3 years, while the p45k reaches 10% for less than an year. On the other hand, the statistical median results show results very close to the single p-MOSFET with α=0.5. The reason for the high values of the

circuit \ t, years	1	3	5	7	10	15	20
c880	4.81%	5.77%	6.29%	6.65%	7.06%	7.55%	7.92%
c1908	4.79%	5.75%	6.26%	6.63%	7.03%	7.52%	7.89%
c6288	4.78%	5.74%	6.25%	6.61%	7.02%	7.51%	7.88%
p45k	4.88%	5.86%	6.38%	6.74%	7.16%	7.66%	8.03%

Table 5.12: Statistical Median of NBTI Delay Degradation With Respect to the Time in Years

circuit \ t, years	1	3	5	7	10	15	20
c880	1.61%	1.93%	2.10%	2.22%	2.36%	2.53%	2.65%
c1908	1.48%	1.78%	1.94%	2.05%	2.18%	2.33%	2.44%
c6288	3.61%	4.33%	4.72%	4.99%	5.30%	5.67%	5.94%
p45k	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

Table 5.13: Statistical Minimum of NBTI Delay Degradation With Respect to the Time in Years

circuit \ t, years	1	3	5	7	10	15	20
c880	50.96%	61.20%	66.64%	70.48%	74.80%	80.03%	83.96%
c1908	50.96%	61.20%	66.64%	70.48%	74.80%	80.03%	83.96%
c6288	8.44%	10.14%	11.04%	11.68%	12.39%	13.26%	13.91%
p45k	50.96%	61.20%	66.64%	70.48%	74.80%	80.03%	83.96%

Table 5.14: Statistical Maximim of NBTI Delay Degradation With Respect to the Time in Years

average delay degradation is explained by the results in table 5.14, showing the maximum delay degradation. As we can see, the delay degradation values for c880, c1908, and p45k are the same values as for p-MOSFET with α=1. This means that in those circuits there is a group of gates that were under constant stress during the simulation of the particular patterns. In p45k the number of those cells is the largest, since it has the biggest impact on the average delay, while the number of the cells under constant stress is the smallest for c880. This is due to the fact that p45k is considerably large circuit, and therefore 10000 patterns are not enough to switch all 22597 cells.

The minimum delays, depicted in figure 5.13, show that in the circuits c1908 and c880 there were cells with very high switching activity, less than 0.1. Circuit c6288 is characterized with the minimum switching activity of more than 0.3. For p45k the zeros mean that there were cells not covered by the input stimuli. Indeed, the achieved coverage was 96%, therefore this results are reasonable.

The impact data of NBTI degradation on the critical path is presented in the tables 5.15, 5.16, and 5.17.

t, years / circuit	1	3	5	7	10	15	20
c880	5.15%	5.88%	6.62%	6.95%	7.35%	8.09%	8.82%
c1908	7.14%	8.57%	10.00%	10.32%	10.71%	11.43%	12.14%
c6288	4.37%	5.37%	5.77%	6.16%	6.56%	6.96%	7.36%
p45k	5.84%	7.00%	7.78%	8.17%	8.56%	9.34%	9.73%

Table 5.15: Statistical Mean of Critical Path NBTI Delay Degradation With Respect to the Time

t, years / circuit	1	3	5	7	10	15	20
c880	0.00%	0.00%	2.86%	2.86%	2.86%	2.86%	2.86%
c1908	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
c6288	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
p45k	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

Table 5.16: Statistical Mean of Critical Path NBTI Length Degradation With Respect to the Time

t, years / circuit	1	3	5	7	10	15	20
c880	0.00%	0.00%	8.57%	8.57%	8.57%	8.57%	8.57%
c1908	5.56%	5.56%	5.56%	5.56%	5.56%	5.56%	5.56%
c6288	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%
p45k	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

Table 5.17: Relative Change of Old Cells in the Degraded Critical Path

Considering the results showing the critical path delay, only the circuit c908 degrade above the 10%. The event occurs after the fifth year of operation. The results are close to the average delay degradation of the circuit and are following the same tendency of increase with the time.

Table 5.16, shows that although unlikely, the critical path may become longer in terms of number of the cells. Circuit c880 increases the number of cells in the critical path with 0.0286 times, and at the same time removing 8.57% of gates in the not degraded critical path (table 5.17). Circuit c1908, on the other hand, has not increased the number of the cells, but substituted 5.56% of the gates in the original not degraded critical path. It is also noticeable

that the length degradation is a steady parameter changing only once and remaining the same through the years. Therefore, the degradation length and number of changed cells are not considered further in the report.

The last analysed parameter is the power dissipation presented in table 5.18.

t, years / circuit	1	3	5	7	10	15	20
c880	3.97%	4.30%	4.30%	3.97%	3.97%	3.97%	3.97%
c1908	-5.85%	-6.25%	-6.25%	-6.25%	-6.05%	-6.25%	-6.05%
c6288	2.70%	2.70%	2.91%	2.91%	2.91%	2.70%	2.91%
p45k	7.65%	7.65%	7.65%	7.65%	7.65%	7.65%	7.65%

Table 5.18: Statistical Mean of Total Power NBTI Degradation With Respect to the Time

The results of the power dissipation are obtained after PrimeTime analysis based on the netlist file and the updated SDF file containing the NBTI degraded delay values. On the contrary to the initial expectation that the power will increase with the progress of NBTI degradation, results show steady power change. It is not clear what is the particular power model used by PrimeTime and how exactly the information of the delay file is used.

Interestingly, circuit c1908, although with the largest average delay have negative power dissipation change. The reason for that is the change in the switching activity. Other explanation are the hazards that may occurs in the combinational asynchronous circuits. That may change the switching activity due to slowed propagation of a signal.

Overall, except the results of the power dissipation, all other results hold the time dependency of the single p-MOSFET. In the first year occurs the most significant degradation and after that a degradation of roughly 1% is observed every two years.

The next subsection presents the results of NBTI simulation varying the ambient temperature of the chip.

5.2.2 Temperature Dependence

The simulations are done with supply voltage 1.2 V, over the period of 10 years. The information is presented for the delay degradation of gates and the impact on the critical path delay.

Expectations are that the dependence of temperature for the single p-MOSFET will be hold, with close results for α about 0.5 will be observed. Tables 5.19 to 5.22 show the statistical data for NBTI delay degradation of the whole circuit.

The results show that the temperature dependency follows the single p-MOSFET tendency. The average delay degradation for the circuit c1908 changes with approximately 2% every 25°C, in the range 25°C - 75°C, reaching the 10% for 90°C. For the circuit p45k, the degradation increases with approximately 3% every 25°C, in the range 25°C - 75°C, reaching the 10% at 60°C.

The critical path average delay degradation data due to the NBTI is show in table 5.23.

We can see that for the given circuits up to temperature values of 90°C, the critical path delay degradation is below 10% relative change. Compared with the average cell delay, the

T,[°C] / circuit	25°	50°	75°	90°	105°	120°
c880	3.94%	5.34%	6.60%	7.39%	8.20%	9.02%
c1908	5.67%	7.68%	9.49%	10.62%	11.78%	12.97%
c6288	3.06%	4.15%	5.13%	5.74%	6.37%	7.01%
p45k	6.65%	8.99%	11.11%	12.43%	13.79%	15.17%

Table 5.19: Statistical Mean of NBTI Delay Degradation With Respect to the Temperature

T,[°C] / circuit	25°	50°	75°	90°	105°	120°
c880	3.09%	4.18%	5.16%	5.78%	6.41%	7.06%
c1908	3.07%	4.16%	5.15%	5.76%	6.39%	7.03%
c6288	3.06%	4.15%	5.13%	5.75%	6.38%	7.02%
p45k	3.13%	4.24%	5.24%	5.86%	6.50%	7.16%

Table 5.20: Statistical Median of NBTI Delay Degradation With Respect to the Temperature

T,[°C] / circuit	25°	50°	75°	90°	105°	120°
c880	1.04%	1.40%	1.73%	1.93%	2.15%	2.36%
c1908	0.96%	1.29%	1.59%	1.78%	1.98%	2.18%
c6288	2.31%	3.13%	3.87%	4.34%	4.81%	5.30%
p45k	0.00%	0.00%	0.00%	0.00%	0.00%	0.00%

Table 5.21: Statistical Minimum of NBTI Delay Degradation With Respect to the Temperature

T,[°C] / circuit	25°	50°	75°	90°	105°	120°
c880	32.87%	44.37%	54.77%	61.29%	67.98%	74.80%
c1908	32.87%	44.37%	54.77%	61.29%	67.98%	74.80%
c6288	5.43%	7.34%	9.07%	10.15%	11.26%	12.39%
p45k	32.87%	44.37%	54.77%	61.29%	67.98%	74.80%

Table 5.22: Statistical Maximum of NBTI Delay Degradation With Respect to the Temperature

critical path delay of the circuit c1908 degrades with about 2% every 25°C. Similar comparison can be done for other circuits, showing comparable temperature dependency with the average delay degradation.

T,[°C] / circuit	25°	50°	75°	90°	105°	120°
c880	2.94%	4.41%	5.15%	5.88%	6.62%	7.35%
c1908	4.29%	6.43%	7.86%	8.57%	10.00%	10.71%
c6288	2.78%	3.78%	4.77%	5.37%	5.96%	6.56%
p45k	3.50%	5.06%	6.23%	7.00%	7.78%	8.56%

Table 5.23: Critical Path NBTI Delay Degradation With Respect to the Temperature

Finally, the supply voltage dependence is presented and analysed.

5.2.3 Supply Voltage Dependence

To analyse the voltage dependence, the ambient temperature is fixed to 75°C, the time is fixed to 10 year, and the V_{ds} voltage is changing to 3.3 V, 2.5 V, 1.2 V, and 0.9.

Expectations are as in the previous simulations to have results close to the single p-MOSFET with α=0.5.

Statistical mean and maximum results from the simulations are shown in tables 5.24 and 5.25.

V_{ds},[V] / circuit	3.3	2.5	1.2	0.9
c880	0.18%	0.70%	9.02%	20.34%
c1908	0.26%	1.00%	12.97%	29.24%
c6288	0.14%	0.54%	7.01%	15.80%
p45k	0.30%	1.17%	15.17%	34.21%

Table 5.24: Statistical Mean of NBTI Delay Degradation With Respect to the V_{ds}

V_{ds},[V] / circuit	3.3	2.5	1.2	0.9
c880	1.48%	5.79%	74.80%	168.67%
c1908	1.48%	5.79%	74.80%	168.67%
c6288	0.25%	0.96%	12.39%	27.95%
p45k	1.48%	5.79%	74.80%	168.67%

Table 5.25: Statistical Maximum of NBTI Delay Degradation With Respect to the V_{ds}

In all circuits, the average delay degradation due to the NBTI goes beyond 15% for supply voltage of 0.9 V. In the same time, for 2.5 V, the delay degradation cannot reach even 2%. The maximum delay degradation for 2.5 V is below the 10% as well. The dependency is the same

circuit \ V_{ds},[V]	3.3	2.5	1.2	0.9
c880	0.00%	0.74%	7.35%	19.85%
c1908	0.00%	0.71%	10.71%	24.29%
c6288	0.00%	0.40%	6.56%	14.71%
p45k	0.00%	0.39%	8.56%	19.84%

Table 5.26: Statistical Mean of Critical Path NBTI Delay Degradation With Respect to the V_{ds}

as for the single p-MOSFET and shows nearly exponential increase of the delay degradation with the decrease of the supply voltage.

Considering the critical path, the results are showing less than 15% delay degradation for circuit c6288 with supply voltage 0.9 V. For the rest of the circuits, the delay degradation is close to 20% for 0.9 V supply voltage. For 2.5 V, the impact of NBTI is almost unnoticeable with maximum value of 0.74% for the circuit c880. Surprisingly, p45k supplied with 2.5 has the smallest value for critical path delay degradation, although the average degradation was the highest. This may be because of the large number of cells with high stress ratio in the critical path.

The results of the simulations show that the impact of the NBTI degradation depends highly on the supply voltage. The results show that for 0.9 V supply voltage, the degradation delay goes beyond the 15% for temperature 75°C over ten years. The critical path degradation also reaches 15% for the selected circuits.

5.2.4 Visualisation of NBTI Delay Degradation

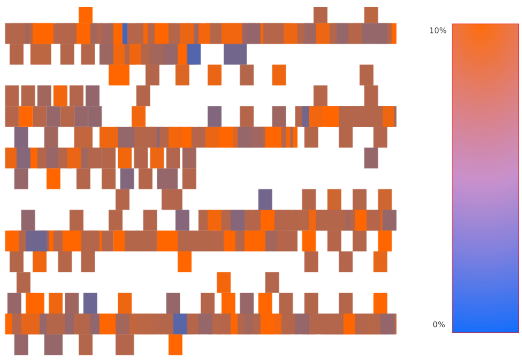


Figure 5.1: C880 HeatMap Graphic

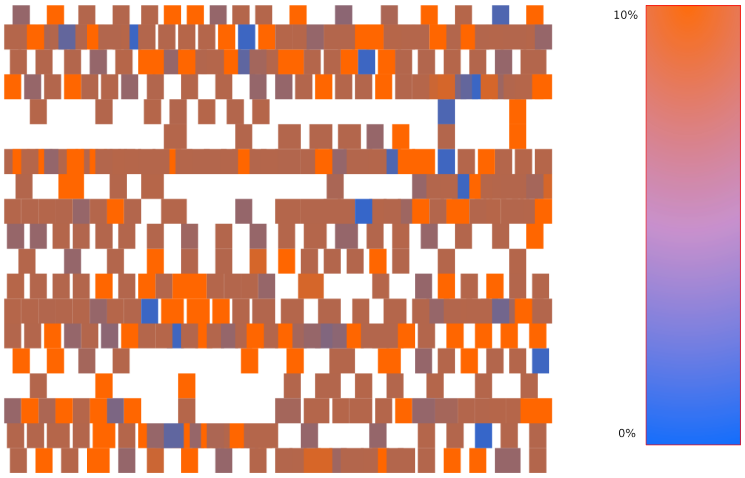


Figure 5.2: c1908 HeatMap Graphic

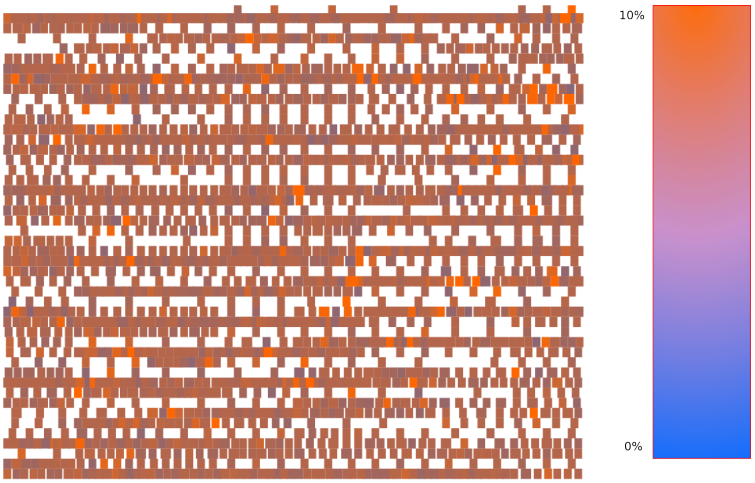


Figure 5.3: c6288 HeatMap Graphic

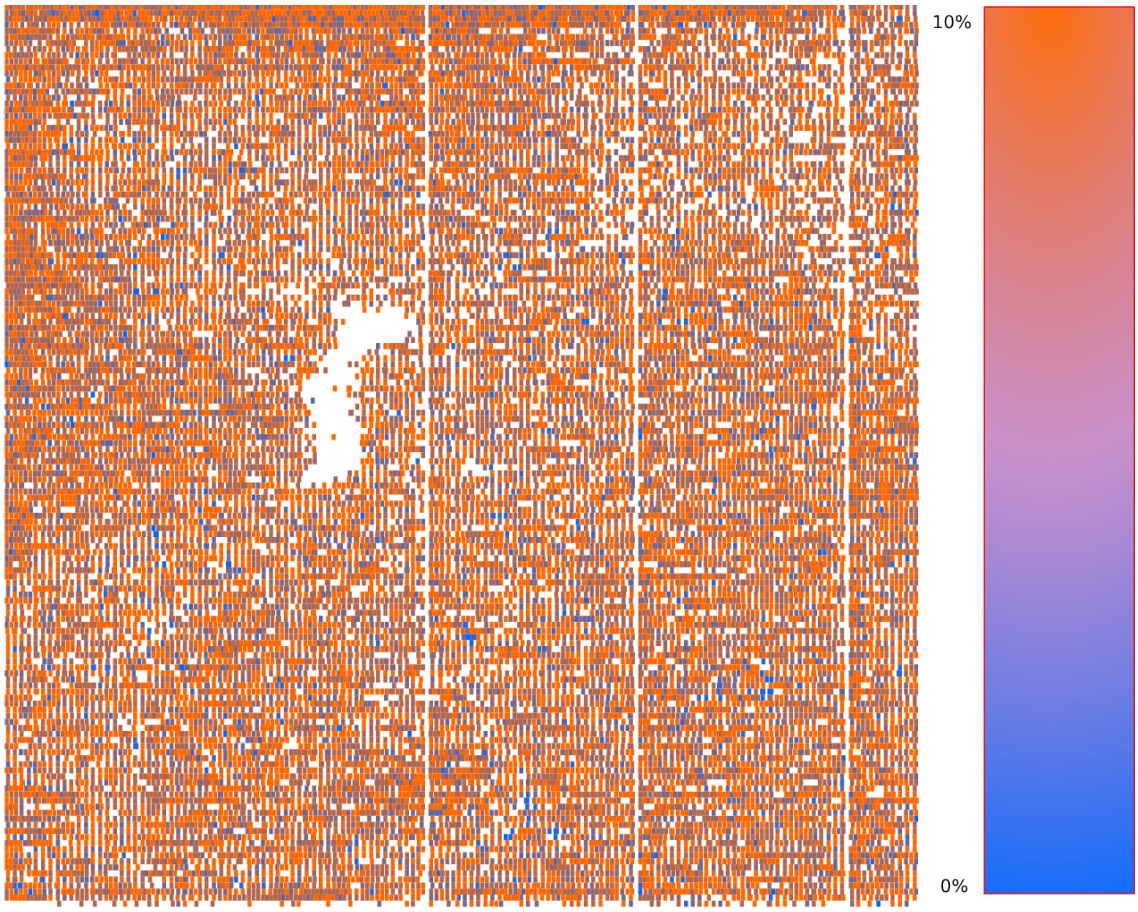


Figure 5.4: p45k HeatMap Graphic

6 Conclusion

In the presented master work the simulation based analysis of the NBTI was considered, and it was used to evaluate the NBTI impact on combinational CMOS circuits. For this purpose, a simulation flow independent of the NBTI model and EDA tools was proposed. Based on it, a NBTI simulator was implemented using the EDA tools: Synopsys Design Compiler, Synopsys PrimeTime, Synopsys VCS simulator, Cadance Encounter, and HotSpot 5.0. A research for NBTI long-term models was done, and the model suggested in [22] was selected and implemented. The simulation flow was successfully built into the VLSI digital CMOS circuits design flow using scripts written in Python, Tcl and Shell script. As an output of the NBTI simulation, statistical data are generated such as the average, median, minimum and maximum of gate delay. In addition, a heatmap showing the average delay of the layout is generated. Finally, numerous simulations on combinational part of the ISCAS89 and NXP benchmark circuits were performed.

The results of the NBTI simulation estimations show that the impact of the NBTI on combinational CMOS VLSI circuits is significant. The average gate delay degradation and critical path delay degradation can reach 10% for 10 years, with 75°C operating temperature and 1.2 V supply voltage.

NBTI depends on the temperature and supply voltage. Results show that for 0.9 V the average circuit and critical path NBTI delay degradation can reach 15% for 10 years. The results shown a high dependency between the gate stress time and the NBTI degradation. Gates under constant stress can reach 52% delay degradation for one year, while the delay degradation for 0.9 stress ration is 19%. Based on that, it was concluded that it is critical for the reliability of the device to remove any possibility for constant gate stress to be applied on any gate in the circuit.

The results also shown that the NBTI aging degradation is progressing significantly over the first operational months. The results shown that for one year the delay degradation can reach 10% in the worst case and 5% in the best case of the simulated circuits.

Using the heatmap graphics, which illustrate the average gate delay degradation for each cell in the layout, it was shown how to recognize the potential aging hotspots in the IC. Based on that, the areas with higher degradation can be localized, and later the circuit can be redesigned to decrease the stress time of the particular group of gates.

Finally, it can be stated that the NBTI aging degradation is a serious threat to the reliability of VLSI CMOS combinational circuits. In the future, with continued technology scaling and supply voltage reduction the impact of the NBTI degradation will likely increase or remain as serious as before. Using NBTI prediction and analysis tools in early level of the design flow can increase the performance of the circuit and ensure reliability for the specified life-cycle time.

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Decleration

I hereby declare that the work presented in this thesis is entirely my own and that I did not use any other sources and references than the listed ones. I have marked all direct or indirect statements from other sources contained therein as quotations. Neither this work nor significant parts of it were part of another examination procedure. I have not published this work in whole or in part before. The electronic copy is consistent with all submitted copies.

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