Low Noise Amplifiers for MetOp-SG

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***Abstract*—We present low-noise amplifiers (LNA) that have been developed in the framework of two pre-qualification ESA projects for frequencies between 54 and 229 GHz for the METOP-SG satellite program. The main goal of these satellites is water vapor detection in atmospheric science and weather forecasting which advances the current state of the art for the metamorphic high electron mobility transistor (mHEMT) technology. The MMIC amplifiers are based on the $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ heterostructure and utilize transistors with a gate length of 50 nm. On-wafer measurements will be presented for all frequency bands as well as results of packaged LNAs.**

***Index Terms*—Low noise amplifier (LNA), metamorphic high electron mobility transistor (mHEMT), monolithic microwave integrated circuit (MMIC).**

I. INTRODUCTION

Providing measurements of atmosphere is of critical importance for accurate weather forecast and climate change. Weather conditions are studied by measuring for instance the concentration of water vapor and temperature in the atmosphere. Therefore, the interest in electronics operating at frequencies above 50 GHz is pushed by the potential of this frequency regime for manifold applications like meteorology, but also astronomy, reconnaissance and surveillance as well as quality control and high data rate wireless communication. Due to tremendous advances in device scaling, today's monolithic integrated circuits can be deployed in the millimeter and submillimeter-wave frequency regime. In this work, we present the design and characterization of LNAs at 54, 89, 118, 165, 183 [1] and 229 GHz which are aimed to be employed in the next generation of ESA/EUMETSAT meteorology satellites for earth and atmosphere monitoring.

II. MMIC DESIGN

The LNAs were fabricated using the in-house 50 nm $In_{0.52}Al_{0.48}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As$ metamorphic HEMT heterostructure grown using molecular beam epitaxy (MBE) on 4-inch semi-insulating GaAs substrates. Details on the epitaxial growth and fabrication process are reported in [2]. This technology features peak transconductance g_m of about 1800 mS/mm and typical extrinsic values of f_T and f_{max} of about 370 GHz and 670 GHz, respectively, in a 2×15 µm gate width device. The passive components of the MMICs includes 50 Ω/sq thin film resistors in NiCr, 225 pF/mm^2 SiN based metal-insulator-metal (MIM) capacitors and two metal layers for interconnection with 2.7 µm thick Au plated air bridge technology. The technology features also backside processing with the substrate thinned down to 50 µm and a back plane metal layer for suppression of the substrate modes, allowing either grounded coplanar waveguide (GCWG) or microstrip transmission lines. Fig. 1 shows a 165 GHz LNA MMIC

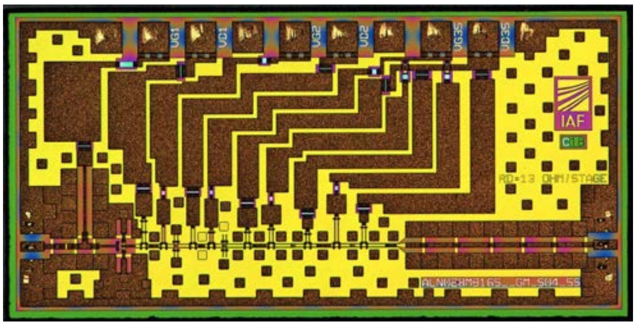

Fig. 1. Photograph of a MMIC LNA operating at 165 GHz (1 x 2 mm^2).

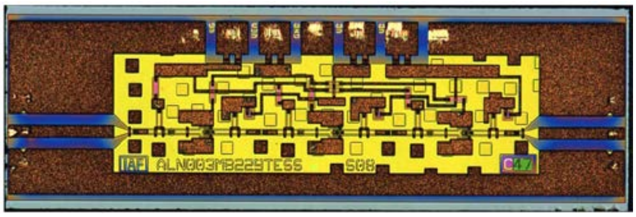

Fig. 2. Photograph of a LNA operating at 229 GHz (0.5x1.5 mm^2)

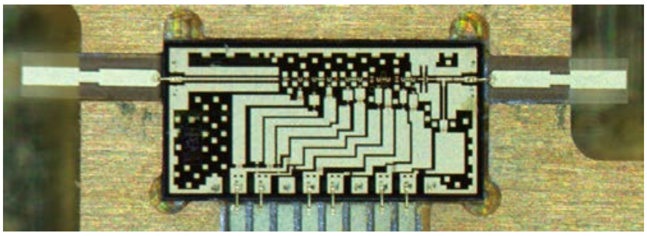

Fig. 3. Photograph of a packaged LNA operating at 165 GHz. The MMIC is connected via bond wires to quartz based waveguide transitions.

consisting of a five-stage common-source topology. Fig. 2, the photograph of a 229 GHz LNA with a three-stage cascade design is presented.

III. PACKAGING

The packaging of these LNAs is realized in reliable and compact split block modules using gold plated brass housings with a size of only $12 \times 30 \times 36$ mm^3. As an example, Fig. 3 shows the photograph of a packaged 165 GHz LNA. The MMIC is glued with silver epoxy into the cavity and connected via bond wires to quartz based waveguide transitions reaching into the rectangular waveguide of the housing. All packages presented here use quartz transitions, except the 229 GHz LNA. Here, the waveguide transition is already integrated in the chip in order to reduce losses due to bond wires [3]. So far, no effort has been put into the optimization of an impedance matching network for any LNA between the quartz waveguide transition and the coplanar input of the MMIC.

IV. MEASUREMENT RESULRS

The 54 GHZ LNA developed during the ESA pre-qualification project has been assembled by two other groups [4, 5]. Therefore we present here the on-wafer measurements of this amplifier which are shown in Fig. 4. A gain more than 30 dB and a noise figure better than 2 dB was hereby achieved. It is a microstrip design in common source topology using 4×15 µm gate width transistors resulting in a total gate width of 60 µm. The measurement was done with a drain voltage of Vd = 0.8 V and a total drain current of Id = 72 mA (id = 300 mA/mm). The LNA for 89 GHz has not been characterized on module level but on-wafer measurements have been performed. These are shown in Fig. 5, where a gain of 25 dB and a noise figure of 2.5 dB were measured. This LNA is also a common source design with four stages. The first three stages contain 2×20 µm gate width devices whereas the fourth stage uses a 4×15 µm gate width transistor giving a total gate width of 40 µm and 60 µm, respectively. This LNA is biased with Vd = 0.8 V and the total drain current is controlled to Id = 54 mA. LNA modules at frequencies of 118, 165, 183 and 229 GHz have been assembled and characterized by s-parameter and noise figure measurements. Fig. 6 shows the results of the D-band LNA with a band of interest for MetOp-SG from114 to 124 GHz where a gain of around 22 dB and a noise figure of 3.1 dB was achieved. This common source LNA design consists of four stages with a gate width of 4×15 µm each. The LNA is biased with Vd = 0.8 V where the drain current is set to Id = 18 mA at each stage. For the LNA at 163 to 167 GHz (see Fig. 7) a gain > 20 dB and an average noise figure of 5 dB was measured. The measurement results of the amplifier aimed for the band from 174 to 192 GHz is demonstrated in Fig. 8 with an average gain of 22 dB and an average noise figure of 5.3 dB. Both designs consist of a common source topology using 5 stages and two finger transistors with a total gate width of 20 µm (see Fig. 1). They are biased with Vd = 0.8 V and the

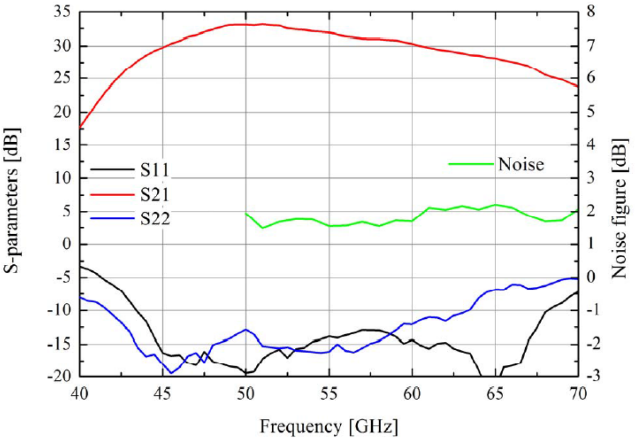

Fig. 4. On-wafer measurement S-parameters and noise figure of a 54 GHz LNA.

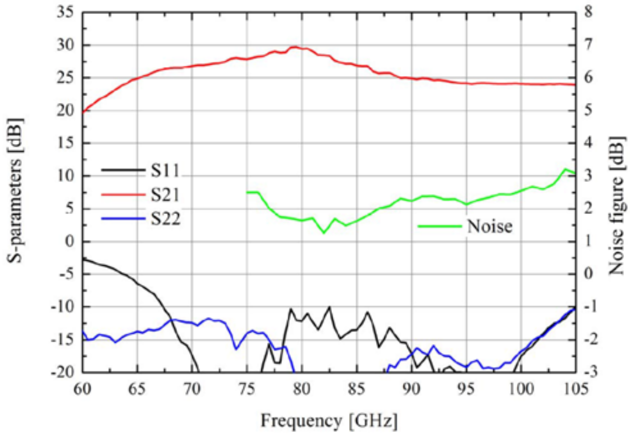

Fig. 5. On-wafer mesurement S-parameters and noise figure of a 89 GHz LNA.

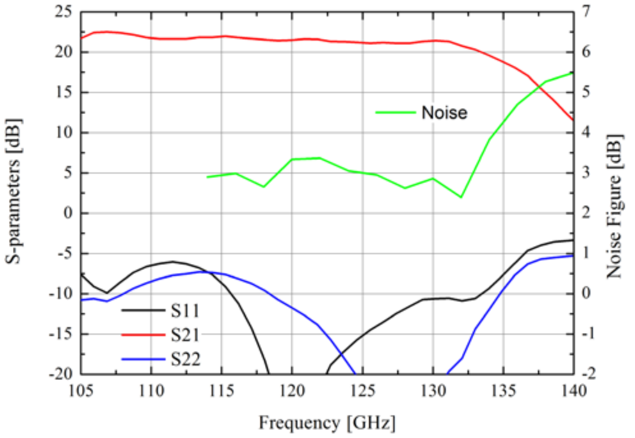

Fig. 6. Measured S-parameters and noise figure of a packaged 118 GHz LNA.

total drain current is set to Id = 30 mA (id = 300 mA/mm at each stage).

The highest frequency band and therefore the most challenging in terms of packaging is the band from 228 to 245 GHz. Fig. 9 shows the measured data of this module with an average gain of 21 dB and an average noise figure of 6 dB.

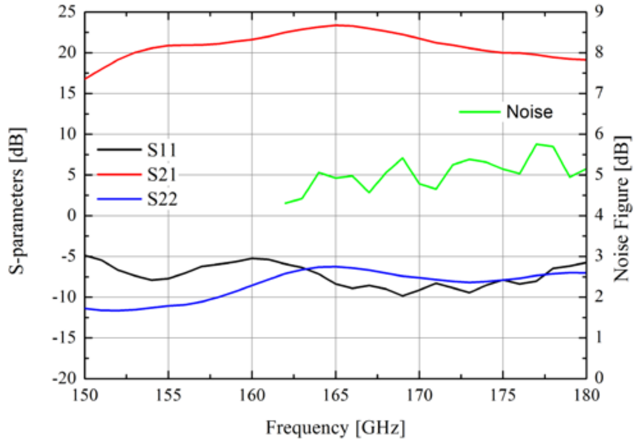

Fig. 7. Mesured S-parameters and noise figure of a packaged 165 GHz LNA.

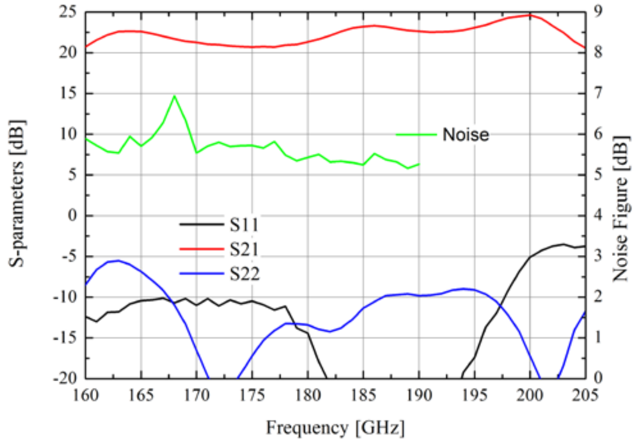

Fig. 8. Measured S-parameters and noise figure of a packaged 183 GHz LNA.

The design is three stages cascode circuit using two-finger transistors with total gate width of 20 µm. The drain voltage of this LNA is Vd = 1.6 V where the drain current is controlled to Id = 24 mA.

V. CONCLUSION

We have demonstrated MMIC LNAs at six different frequencies from 54 to 229 GHz at wafer and at module level, showing excellent performances in terms of gain and noise figure. Table 1 summarizes the achieved results and compares them to the MetOp-SG requirements on module level. Based on the achieved results, MetOp-SG receiver suppliers decided to select these LNAs, developed at Fraunhofer IAF, for the MetOp-SG satellite program.

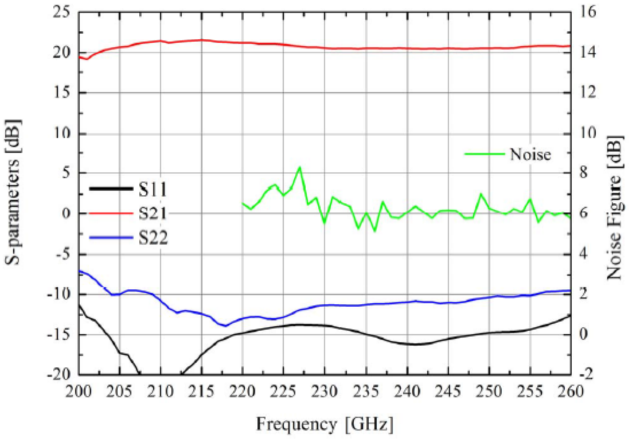

Fig. 9. Measured S-parameters and noise figure of a packaged 229 GHz LNA.

TABLE I. METOP-SG REQUIREMENTS VS. MEASURED DATA

Frequency [GHz]	Requirements[b]		Measurements	
	Gain [dB]	NF [dB]	Gain [dB]	NF [dB]
54	> 28	< 2.5	> 28[a]	< 2[a]
89	> 24	< 3	> 24[a]	< 2.5[a]
118	> 20	< 4	> 20	< 3
165	> 20	< 4.8	> 20	< 5
183	> 20	< 5.1	> 20	< 5.2
229	> 20	< 6.1	> 20	< 6.2

[a] On-wafer data, these LNAs have not been packaged yet.

[b] Packaged

TABLE II. COMPARISON TO REPORTED MMIC LNAS

Ref.	Frequency[GHz]	Gain [dB]	NF [dB]	
[6]	43 - 90	25	< 2.5	On-wafer
[7]	65 - 92	>26	3	Packaged
[8]	160 - 170	12 - 16	3.7	Packaged
[9]	170 - 185	17	3.4	Packaged
[10]	230 - 280	16 - 24	10	On-wafer

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