

# Cryogenic Broadband Q-Band MMIC Low-Noise Amplifier

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**Abstract**—The design of a broad-band monolithic cryogenic low-noise amplifier (MMIC LNA) in the Q band, aimed to be used in radio-astronomy receiver front-end modules is presented. A 70 nm gate-length GaAs mHEMT process from OMMIC foundry is used to manufacture the amplifier. An accurate model for the minimum noise bias point of the transistor has been obtained at room temperature. The amplifier design is based on a four stage monolithic common source transistor configuration. At 300 K, the amplifier shows an associated gain of  $28 \pm 1.1$  dB and an average noise temperature of 145 K with a minimum noise temperature of 101 K at 45 GHz tested on wafer. When cooled down at 15 K, the average noise temperature is 18.4 K with a minimum of 13.5 K and 27.3 dB of associated gain. The DC power consumption is extremely low, 4.1 mW, at cryogenic temperature.

**Keywords**—Monolithic Microwave Integrated Circuit (MMIC); Low Noise Amplifier (LNA); broadband amplifiers; cryogenic; GaAs mHEMT

## I. INTRODUCTION

In the field of radio-astronomy, the scientist community demands high sensitivity receivers in order to detect very weak signals from the sky. Cryogenic low noise amplifiers (LNAs) are placed in the front-end of these receivers to amplify these weak input signals with a very low contribution to the overall noise [1]-[3].

Research activity in new materials has led to the development of HEMT on indium phosphide (InP) semiconductor technology, which allows to have amplifiers with very high gain and ultra-low noise [4]. However a low stability, fragility and limited access to this technology, have pushed the development of metamorphic HEMTs (mHEMT) on gallium arsenide (GaAs) semiconductor substrates with a high content of InP in the channel, leading to high performance semiconductors. Many works based on mHEMT structures have been presented with excellent results [5]-[9].

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The monolithic technology can be a better option for high frequency designs since the element sizes and their interconnections can be more accurately controlled and higher yield is achieved. However, this technology has the handicap of the costs associated with its production (for low quantities) and sometimes it is not affordable.

This paper describes the design of a cryogenic MMIC LNA in the 33-50 GHz frequency band with very low noise and DC power consumption. The technology used for the design is briefly presented in section II. The design of the low noise amplifier is described in section III as well as the small signal model of the transistor. The noise and scattering characterization of the amplifier at room and cryogenic temperature is shown in section IV. Finally, the conclusions of this work are summarized in section V.

## II. TECHNOLOGY

Transistors are built in metamorphic HEMT technology with 70 nm gate length process from OMMIC foundry (France). The active component is based on a GaInAs-InAlAs-GaInAs-InAlAs heterostructure and a conductive channel with 52% and 70% of indium content respectively. It provides a transition extrinsic frequency  $f_T = 300$  GHz and a maximum oscillation frequency  $f_{max} = 350$  GHz. The wafer is thinned down to 100  $\mu\text{m}$ .

For the amplifier design the transistor size is chosen to have a  $4 \times 15$   $\mu\text{m}$  gate periphery for all the stages of the amplifier. Fig. 1 shows a picture of a  $4 \times 15$   $\mu\text{m}$  OMMIC mHEMT transistor.

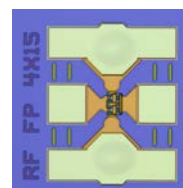


Fig. 1.  $4 \times 15$   $\mu\text{m}$  OMMIC mHEMT transistor.

### III. MMIC LNA DESIGN

#### A. Transistor Small-Signal and Noise Models

Accurate small signal and noise transistor models are very important for a successful LNA design. Using discrete transistors with the same gate periphery and same technology that those used in the amplifier design, DC and S-parameter measurements have been made to extract the small signal model. In order to get the model, the approach followed in [10]-[11] is used to get an estimation of the suitable bias point for low noise. From DC measurements, the minimum of the function (1) can be calculated providing the optimum bias point to minimize  $T_{\min}$ .

$$f(V_{ds}, V_{gs}) \approx \sqrt{I_{ds}} / g_m \quad (1)$$

Fig. 2 shows the small signal model. The numerical values for  $V_d = 0.6$  V and  $I_d = 6.7$  mA are shown in Table I.

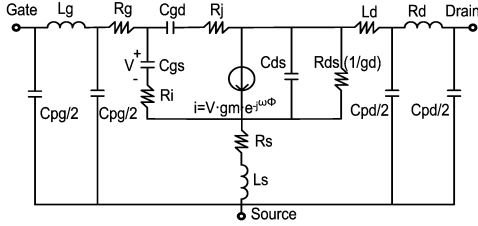


Fig. 2. 4x15  $\mu\text{m}$  mHEMT transistor small signal model.

TABLE I. SMALL SIGNAL PARAMETERS VALUES FOR A 4x15  $\mu\text{m}$  OMMIC MHEMT TRANSISTOR.  $V_D = 0.6$  V,  $I_D = 6.7$  mA

Intrinsic Parameter	Value	Extrinsic Parameter	Value
Cgs	38 fF	Cpg/2	14.75 fF
Ri	7.5 $\Omega$	Lg	38.31 pH
Cgd	13.7 fF	Rg	0.5 $\Omega$
Rj	19 $\Omega$	Cpd/2	14.75 fF
gm	71 mS	Ld	40.75 pH
$\Phi$	0 ps	Rd	4.19 $\Omega$
Cds	17.5 fF	Rs	2.75 $\Omega$
gd	6.9 mS	Ls	4.84 pH

For the noise model, the Pospieszalski model [10] has been used and the two additional temperatures  $T_d$  and  $T_g$  have been obtained.  $T_g$  is assumed to be equal to the ambient temperature and 50  $\Omega$  noise figure measurements of the transistor have been made in order to get  $T_d$ . The results of these measurements for  $V_d = 0.6$  V and  $I_d = 6.7$  mA are shown in Fig. 3, where the ripple is due to mismatching between the transistor and the source. The value obtained for  $T_d$  is 3200 K, while the remaining resistors of the small signal model are set to an ambient temperature  $T_g = 300$  K.

#### B. LNA Design

The MMIC LNA is a four stage design with transistors in common source configuration. All the stages have the same transistor size of 4x15  $\mu\text{m}$  and the same bias point. Source feedback technique for the two first stages has been used to get good noise performance as well as input matching and stability.

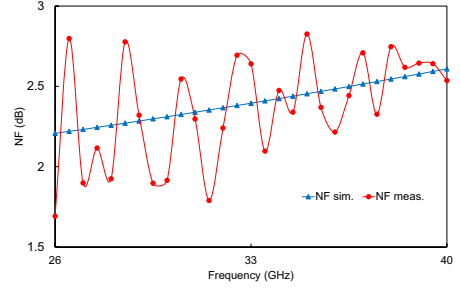


Fig. 3. Noise performance of a 4x15  $\mu\text{m}$  OMMIC mHEMT transistor at room temperature for  $V_d = 0.6$  V and  $I_d = 6.7$  mA.

Since the first stage is the most important in terms of noise, the design should rely on simple microstrip lines for the input stage. Matching networks for the last two stages are designed to achieve flat gain keeping the noise of the amplifier as low as possible. Design and optimization processes are carried out using ADS Momentum simulator from Keysight. Bias networks are kept independent for each stage and they are made up of a combination of resistors and capacitors providing filtering networks. Fig. 4 shows the schematic of the LNA.

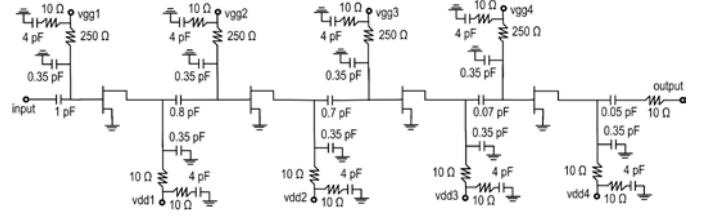


Fig. 4. Schematic of the 4 stage MMIC LNA.

A detailed picture of the MMIC LNA is shown in Fig. 5.

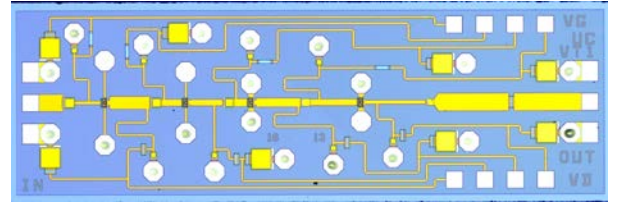


Fig. 5. Photograph of the fabricated MMIC LNA (3 x 1 mm<sup>2</sup>).

### IV. LNA MEASUREMENTS AND CHARACTERIZATION

#### A. Measurements on Wafer at Room Temperature

Firstly the LNA is characterized on wafer at room temperature. These measurements are made in a coplanar probe station from Cascade Microtech. Radio Frequency (RF) characterization is performed using a Keysight E8364A network analyser. Noise measurements are performed using the Y-factor method with a Keysight N8975A noise figure analyser. An external down-converter is used to measure in the 33-50 GHz frequency band. A 6 dB attenuator at the output of the noise source (346C\_K01) is used to lower the ENR in order to improve the noise measurement accuracy [12].

Fig. 6 shows the S-parameters results, while noise temperature and insertion gain are shown in Fig. 7. The mean

gain in the 33-50 GHz frequency band is 28.2 dB. Input return loss is better than 4 dB and output return loss is better than 11 dB within the whole band. The mean noise temperature is 145 K in the 33-50 GHz frequency band, and the minimum noise temperature is 101 K at 45 GHz.

The bias point for getting the lowest noise in the amplifier at room temperature is  $Vd = 0.61$  V and  $Id = 24.9$  mA, with a DC power consumption of 15.2 mW. These values are very close to the bias point for lowest noise provided by (1), validating this expression for the design.

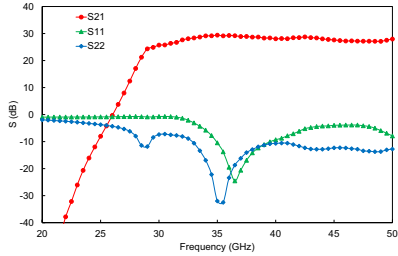


Fig. 6. Measured Scattering parameters for on wafer MMIC LNA at room temperature,  $Vd = 0.61$  V and  $Id = 24.9$  mA.

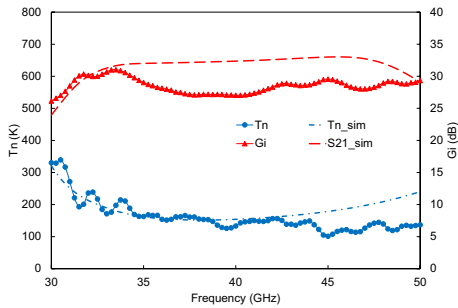


Fig. 7. Measured Noise temperature for on wafer MMIC LNA at room temperature,  $Vd = 0.61$  V and  $Id = 24.9$  mA.

The figure of merit ( $FOM$ ) in (2), defined in [6], has been used in order to evaluate the performance of the LNA in radio-astronomy receivers. This  $FOM$  (2) includes linear gain ( $G$ ), bandwidth ( $BW$  (GHz)), noise factor ( $F$ ), and power consumption ( $P_{dc}$  (mW)). The results of the MMIC LNA presented in this paper are compared in Table II with other published works.

$$FOM = (G \cdot BW) / ((F-1) \cdot P_{dc}) \quad (2)$$

### B. Amplifier Characterization at Cryogenic Temperature

For the characterization of the MMIC LNA at cryogenic temperatures a suitable module has been machined. This module is made of aluminium in order to improve the thermal conductivity and to reduce the total weight. Afterwards, the chassis is nickel and gold plated.

The chassis has two cavities: one for the chip and the high frequency access lines with 1.2 mm width, whereas the other houses the biasing networks as shown in Fig. 8. DC bias accesses are narrow channels in order to avoid resonances in the cavity. The chassis is equipped with 1.85 mm coaxial connectors, and the transition between these connectors and

the microstrip lines is made using sliding contacts to allow flexibility in the joints during cryogenic tests. The off-chip bias networks are made up of capacitors, resistors and, protection diodes to prevent potential low frequency instabilities.

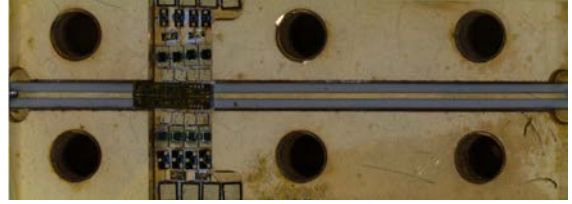


Fig. 8. Detail of the MMIC LNA assembly inside the chassis.

At cryogenic temperature the noise measurement was performed using the cold-attenuator technique [13] with a 20 dB attenuator module [14] inside the cryostat. The noise source is connected directly to the cryostat input line. In Fig. 9 the MMIC LNA chassis is presented clamped to the cold base inside the cryostat, just before a cooling cycle.

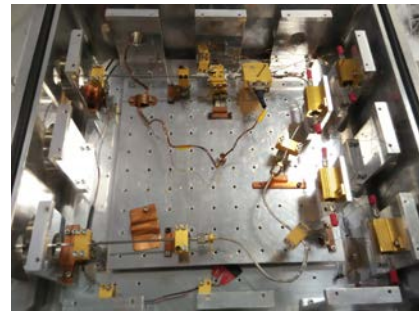


Fig. 9. Photo of the MMIC LNA inside the cryostat.

Fig. 10 shows the measured noise temperature and associated gain for the LNA module at 15 K. The amplifier achieves an average gain of 27.3 dB and an average temperature of 18.4 K in the whole 33-50 GHz frequency band, with a minimum of 13.5 K at 45 GHz. The DC power consumption is only 4.1 mW,  $Vd = 0.37$  V and  $Id = 11.2$  mA.

The decrease of gain and increase of noise at 47 GHz, seems to be due to the bonding wires and microstrip to coaxial transition effects, since it has not been observed in on wafer measurements. These effects could be minimized using rectangular waveguide to microstrip transitions, because better return loss could be achieved.

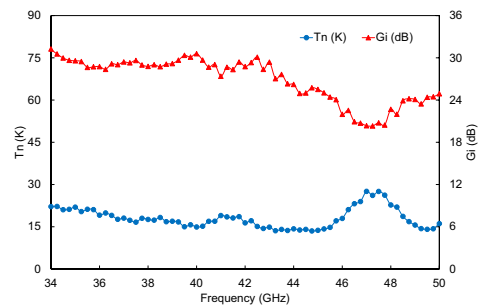


Fig. 10. Measured insertion gain and noise temperature for the LNA assembled at physical temperature of 15 K.  $Vd = 0.37$  V and  $Id = 11.2$  mA.

TABLE II. COMPARISON OF PREVIOUSLY REPORTED LNA AND THIS WORK

Ref.	BW (GHz)	G (dB)	NF (dB)	T <sub>n</sub> (K)	P <sub>dc</sub> (mW)	FOM	Process
[4]	24 – 40	28	0.19	13.2 module @ 15 K	10.8	832	130 nm InP HEMT
[5]	27.3 – 50.7	23.1	3.7	390 on wafer @ RT	88	2.8	150 nm GaAs mHEMT
	30-50	19.5	0.62	44.8 module @ 28 K	21.4	57.5	100 nm GaAs pHEMT
[6]	27-45	25	3.1	302 on wafer @ RT	9	34	150 nm GaAs mHEMT
[7]	30-50	19.8	3.4	345 on wafer @ RT	46	3.6	150 nm GaAs mHEMT
		23	0.34	23.4 module @ 16 K	10	347	150 nm mHEMT
[8]	37-53.2	32.5	3.2	316 on wafer @ RT	152	4.1	150 nm mHEMT
	32-50	29.5	2.8	263 on wafer @ RT	140	4.2	70 nm GaAs mHEMT
This work	33-50	28.2	1.8	145 on wafer @ RT	15.2	55.6	70 nm GaAs mHEMT
		27.3	0.27	18.4 module @ 15 K	4.1	1504	

Three units, shown in Fig. 11, have been assembled with similar results in terms of noise and gain at cryogenic temperature.

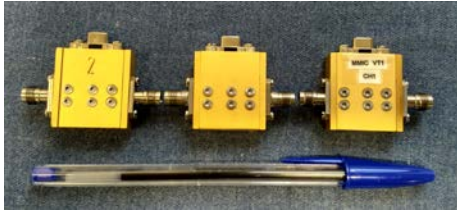


Fig. 11. Three chassis with the MMIC LNA assembled.

## V. CONCLUSION

The design and characterization of a broad-band monolithic cryogenic low-noise amplifier developed for radio-astronomy applications in the 33-50 GHz frequency band have been presented. The LNA is a four-stage common source configuration manufactured on 70 nm GaAs metamorphic technology from OMMIC foundry.

The amplifier exhibits a gain of 28 dB and a noise temperature of 145 K in the 33-50 GHz frequency band for on wafer measurements at room temperature. When the amplifier is cooled down to 15 K, the gain is 27.3 dB and the noise temperature is 18.4 K. The DC power consumption at cryogenic temperatures is only 4.1 mW.

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