Performance Analysis of 1ϕ T/4 PLLs with Secondary Control Path in Current Sensorless Bridgeless PFCs

P. Lamo[1], F. López[2], A. Pigazo[1], F. J. Azcondo[2]
[1]University of Cantabria. Computer Science and Electronics Dept., School of Nautical Studies.
[2]University of Cantabria. TEISA Dept., ETS II y T.
Santander, Spain
{lamop, lopezf, pigazoa, azcondof}@unican.es

***Abstract*— New power factor correction (PFC) stages such as bridgeless converters and the associated current shaping techniques require grid synchronization to ensure unity Displacement Power Factor (DPF). Sensorless line current rebuilding algorithms also need synchronization with the line voltage to compensate at least for part of the current estimation error. The application of a secondary control path to reach faster and more robustly the proper operation point previously applied in single/three-phase PLLs in grid connected converters is here proposed for the current sensorless bridgeless PFCs. This work analyzes the performance of three single-phase T/4 PLL structures, first without secondary control path, and later with feedforward and feedback secondary control paths, both in simulation and experimentally, and evaluates their applicability to current sensorless digitally controlled single phase bridgeless PFCs based on the current rebuilding technique.**

Keywords—converter; current sensorless; PLL; bridgeless; power factor conversion; FPGA

I. INTRODUCTION

Front-end PFC stages supply the DC loads with the appropriate voltage/current levels under diverse grid operation conditions and ensure a high efficiency and power density [1]. At the same time, the PFC is responsible for impressing the current waveform according with the applicable standards and grid codes [2].

PFC stages have evolved from diode bridges, plus a DC/DC stage, with the last one processing the current to force unity PF, to diode bridgeless topologies, where the functionalities of both stages are combined, reducing the number of power devices along the current paths and, hence, increasing the overall efficiency [3]. A drawback of this evolution is the more difficult current and voltage sensing [5], [6] which may limit the operation power range and the more complex implementation of the controller due to the elimination of the voltage reference and the natural grid synchronization [4]. The PFC circuit becomes more sensitive to voltage phase and switching noise around the zero voltage crossing. Signal conditioning and isolation circuit are usually required, along with a filter to increase noise immunity. Current estimation is an alternative to overcome the limitation linked to the direct current measurement. In this case, an observer emulates the power converter operation and the computed line current is the input to the current controller [7], [8]. But low immunity to grid noise is even more critical in current sensorless solutions, since the phase of the input voltage is utilized to rebuild the input current [9], so that synchronization mismatches results in large current estimation errors in algorithms that use the current rebuilding or pre-calculated duty-cycle techniques. Zero-voltage detectors can be utilized to provide grid synchronization, but exhibit poor noise immunity, being quite sensitive to grid disturbances [10], and, as a consequence, PLLs are preferred [11]. In [12], the PLLs is used in current sensorless PFCs to obtain the duty cycle sequence within the utility period without estimating the current, requiring a large inductance and additional compensation for the line voltage distortion and parasitic resistances [13].

PLL algorithms have been employed to track the grid voltage phase for synchronization of grid-connected power converters [11]. The simplest structure consists of a phase detector (PD), which compares the input signal and the generated one providing an error signal, whose DC component corresponds to the phase error. Other frequency components of the error signal are filtered out by means of a low pass filtering (LF) stage, implemented in most cases as a PI controller to obtain a correction signal to be added to the central frequency of the PLL, which sets the initial operation point. After that, a voltage controlled oscillator (VCO) generates the PLL output signal with zero phase-error in steady-state. When the PFC is connected to a strong grid, small frequency variations would occur and the conventional approach can be fast enough to track phase changes with good dynamics and providing stability. However, in weak grids, the operation point of the PLL would not match the operating conditions and the PLL performance would be deteriorated, requiring a synchronization system with greater complexity. This is the case of PLLs with a secondary control path (SCP),

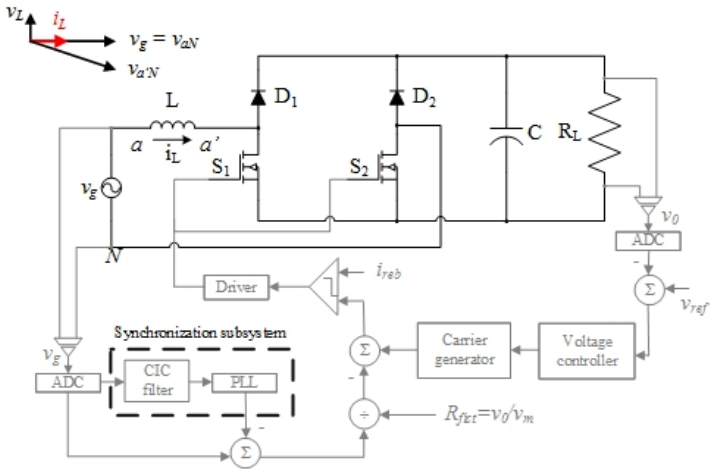

Fig 1. Bridgeless with the proposed controller using PLL synchronization.

with feedback or feedforward control structures to adjust the PLL central frequency, analyzed in [14], where the *dq* components resulting from the Park transformation in three-phase systems are employed. These structures have also been utilized in the case of single phase PLLs, as it is done in [15] and [16], where a quadrature signal is generated to obtain the *dq* components by means of a T/4 delay block. Frequency variations introduce errors within the generation of the quadrature signal by a delay of T/4, which deteriorates the PLL performance. There are alternatives such as inverse transformation of Park or a second-order generalized integrator, SOGI, which would lead to a better overall performance of the PLL [17]. According to [18], despite the helping by the grid side filter, the buffer length which depends on the sampling frequency must be large enough to minimize the effect of the current ripple caused by the PFC.

This paper studies the performance of single phase T/4 PLL structures, with and without SCP, applied to a current sensorless digitally controlled single phase bridgeless PFCs, according to the structure shown in Fig. 1. The PFC performance applying three different PLL structures is compared in both, simulation and experimentally.

II. Single Phase T/4 PLL Structures Under Analysis

The conventional 1-phase T/4 PLL structure, which is shown in Fig. 2, employs the central frequency (ω_c) to provide the initial operation point. Gains k_p and T_i must be adjusted considering the linearized PLL model around ω_c, resulting in a second order system, where the gains are related to the settling time (T_{set}) and the damping coefficient (ξ). These parameters can be determined by applying diverse design strategies, such as ITAE [19] or minimum symmetrical optimum [11]:

$$k_p = \frac{9.2}{T_{set}} \qquad (1)$$

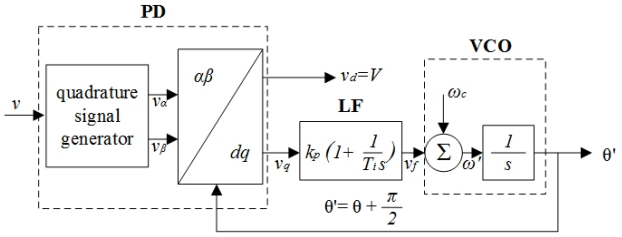

Fig. 2. Conventional T/4 PLL.

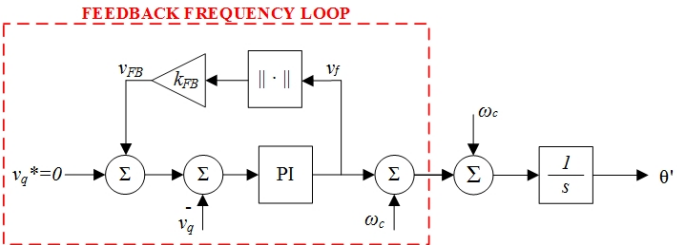

Fig. 3. T/4 PLL with feedback frequency loop with detail of the implementation.

$$T_i = \frac{T_{set} \cdot \xi^2}{2.3} \qquad (2)$$

The T/4 delay single phase PLL has been widely applied for synchronization of grid-connected power converters due to its simplicity and reasonable performance under normal grid operation conditions [11], [20]–[22]. However, grid disturbances and frequency variations in weak electrical grids deteriorates its performance.

To get a faster response to frequency variations, the above structure can be modified including a secondary control path [14]. Fig. 3.a shows a positive feedback structure applied to the input frequency of the low pass filter with the aim of correcting the error signal when the frequency of the input signal undergoes variations.

In this structure, the Frequency Feedback (FFB) gain is [15]

$$v_{FB} = \min(abs(v_f \cdot k_{\mathrm{FB}}), 5) \qquad (3)$$

with $abs(v_f \cdot k_{\mathrm{FB}})$ ensuring the system stability and k_{FB} adjusting the dynamics. FFB presents a zero steady state phase error during slope frequency variations due to the FFB action resulting in a faster reference signal tracking with a small steady-state error.

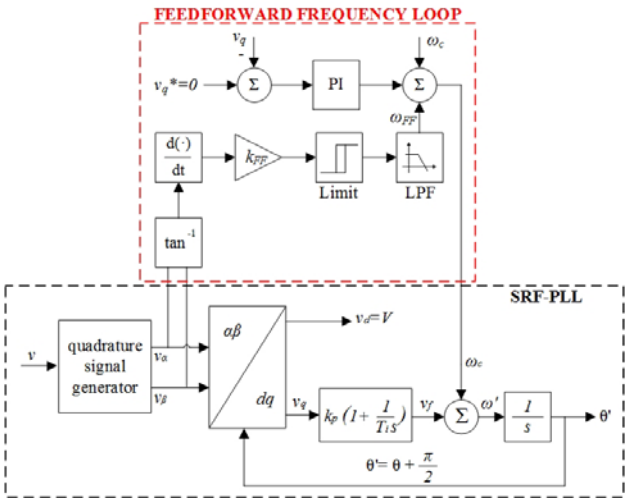

Fig. 5. T/4 PLL with feedforward frequency loop with detail of the implementation.

A different approach for a SCP in single-phase T/4 delay PLLs is due to the Frequency Feedforward (FFF), which can be applied to T/4 PLL, as shown in Fig. 4 [23], wherein the frequency correction is performed based on the phasorial representation of the line voltage into a stationary reference frame, which is employed to generate a fast correction action on the central PLL frequency especially in the case of large frequency deviations at the PLL input. It is a simple design that includes a low-pass FIR filter tuned for fast dynamic and stable operation. The tuning procedure is described in [23]. According to [14], in this case, SCP increases the PLL closed-loop bandwidth, so it improves too its dynamic performance. However, it too increases the type of PLL control loop by one, and it increases the problem of the stability.

The feedback controller achieve a good performance in reducing the phase error but the feedforward controller eliminates the frequency error.

III. Simulation Results

The sensorless and bridgeless PFC depicted in Fig. 3 has been modeled and its performance due to the synchronization subsystem structure evaluated in simulation. The three PLLs described in Section II have been applied with the same PI controller parameters, designed according to [11]. The employed simulation parameters are included in Table I.

TABLE I. SIMULATION PARAMETRES

PARAMETER	VALUE
Nominal frequency	50 Hz
K_p	46
K_i	23
K_{FB}	80000
K_{FF}	48828.125
T_s	$2.48 \cdot 10^{-5}$ s

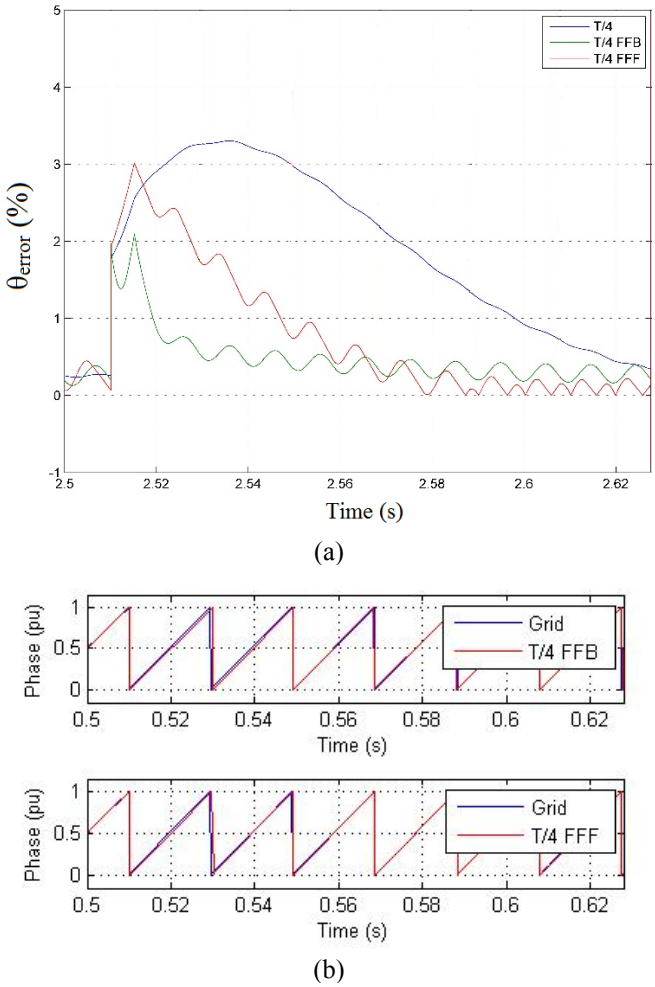

Fig. 4. a) Monitoring the phase angle of the T/4 PLL with feedforward and feedback secondary control paths. b) Phase error due to a frequency step from 49 Hz to 51 Hz.

The tracking capabilities of the PLLs under sinusoidal conditions and applying a frequency step from 49 Hz to 51 Hz are shown in Fig. 5. The measured tracking error is depicted in Fig. 5.a. Initially, all the PLLs are locked to 49 Hz and track the grid voltage phase with an average error equal to 0.24 %. The FFF PLL results on the worst steady state response due to a 0.22 % ripple. At t=0.5 s, a +2 Hz frequency step is applied and the grid frequency changes suddenly to 51 Hz. The FFF PLL achieves the fastest response time and reaches the steady state within 0.19 s. Moreover, the FFF PLL results in the minimum deviation of all the evaluated PLLs, with a maximum 3 % error during the transient. The FFB PLL response is faster than the conventional T/4 delay PLL one but exhibits a higher overshoot. Per unit phases of line voltage and SCP PLLs are compared in Fig. 5.b, where the slow response of FFB, in comparison to FFF, is depicted.

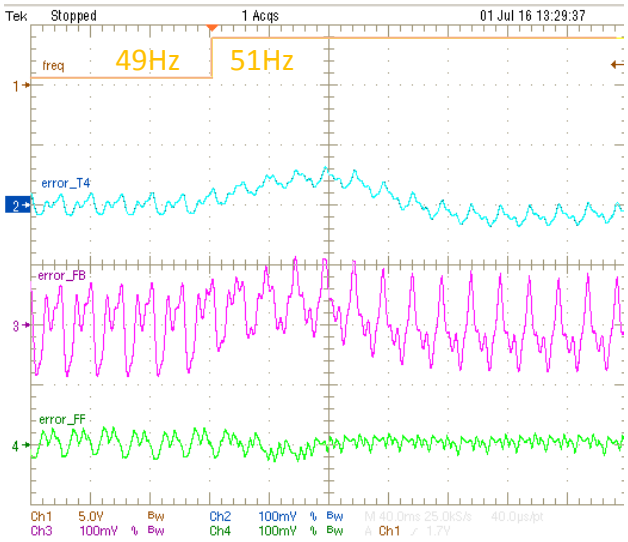

Fig. 6. Output of the phase detectors for the standard T/4 (channel 2), FFB (channel 3) and FFF (channel 4) PLLs under a frequency step from 49 Hz to 51 Hz (channel 1) with the parameters adjusted with Table I.

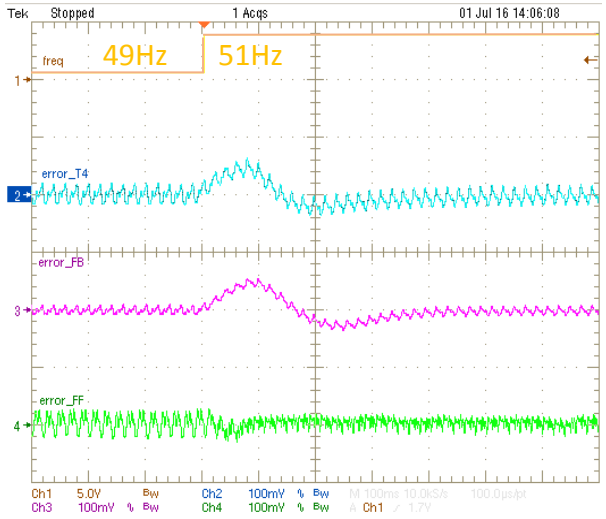

Fig. 7. Output of the phase detectors for the standard T/4 (channel 2), FFB (channel 3) and FFF (channel 4) PLLs under a frequency step from 49 Hz to 51 Hz (channel 1) with KFB= 50 and the saturation value is 0.5 to obtained a good dynamic response without amplifying the noise.

IV. Experimental Results

The performance of a bridgeless PFC with a current sensorless controller when the synchronization subsystem is implemented using a conventional T/4 PLL, and the described variations with secondary control loop, has been evaluated in a laboratory prototype of bridgeless PFC. The digital controller has been implemented in a FPGA (a XC7A100T-1CSG324C from Xilinx) and both the inner control signals and the measured grid current and voltage signals are measured in order to stablish the PFC performance in each case. The laboratory prototype is fed by programmable AC source from Pacific (AC Power Source 345-AMX).

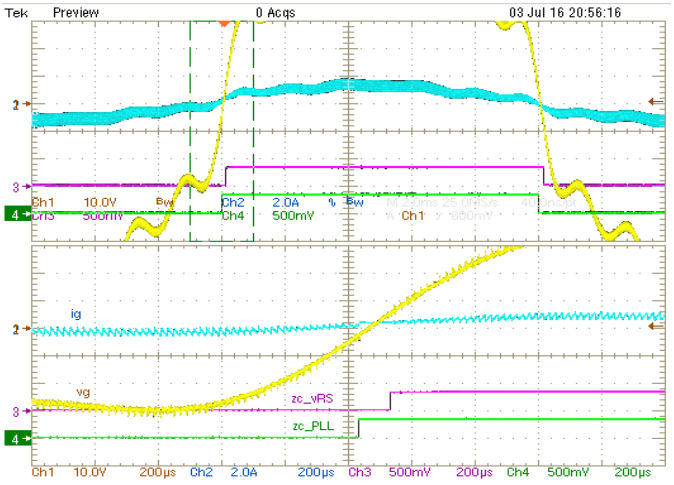

Fig. 8. Behavior of the Zero-Crossing Detector (Channel 3) and the conventional T/4 PLL (Channel 4) in case of converter operating thougth the zero crossing instant where voltage line (Channel 2) and current line (Channel 3) are presented.

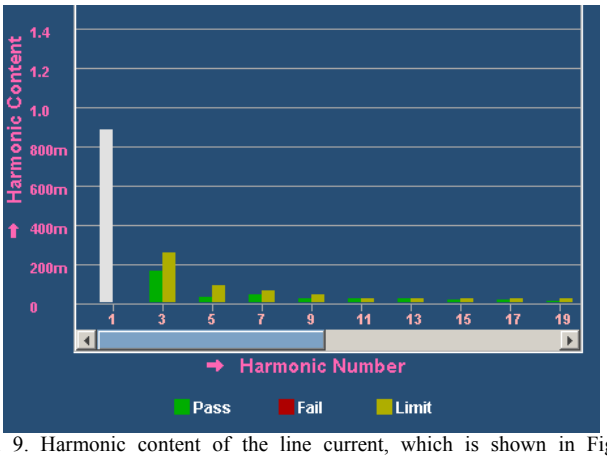

Fig. 9. Harmonic content of the line current, which is shown in Fig.8. compared with the limits set by the standard IEC 61000-3-2 Class C.

Firstly, the PLLs have been parallelized within the digital controller and only the synchronization subsystem was enabled. This allowed the PLLs' dynamics to be compared under the same operation conditions. The obtained results are shown in Fig. 6 and 7, where the inner error signals, the PI controller inputs, for each PLL during a frequency step from 49 Hz to 51 Hz. The best results in terms of rate adaptation and noise immunity are obtained with the FFB PLL. Then, the FFF PLL takes 0.08 ms to adapt to the new situation. Finally, the conventional PLL got the worst performance (its response time is 0.3 s). In Fig. 6, the results are obtained with the same values of simulation where it is shown the amplified value of the frequency feedback output in order to the expectation explained in [15]. To correct it, the values of k_{FB} and the saturation are modified to eliminate the phenomenon of amplification in the frequency feedback and improve its dynamics performance.

The effect of the synchronization subsystem on the bridgeless PFC performance is shown in Fig. 8. As it can be

seen, the zero –crossing detection approach results in a worst line current waveform around zero crossing instants due to the noise and its effect on the current rebuilding algorithm. These waveforms can be improved with the adoption of PLLs for synchronization as shown in Fig. 8.

Finally, Fig. 9 shows the harmonic content of the mains current obtained with the PLL, which shows that complies with the standard IEC 61000-3-2 Class C.

V. Conclusion

PLL circuits are an effective addition to digital control circuits in bridgeless PFCs. Simple PLL structures, such as a T/4 delay PLL, can be employed to improve the PFC performance. However, frequency variations in weak electrical grids can deteriorate the synchronization subsystem performance and more complicated approaches must be employed. This is the case of PLLs with a secondary control path. The obtained results show that both the frequency feedback and feedforward approaches improve the synchronization and, as a result, the harmonic content of the line current is kept within the IEC 61000-3-2 class C limits.

Acknowledgment

This work has been supported by the Spanish Ministry of Economy and Competitiveness under grant TEC2014-52316-R ECOTREND Estimation and Optimal Control for Energy Conversion with Digital Devices.

References

[1] L. H. Dixon, "High power factor switching preregulator design optimization," *Unitrode Power Supply Des. Semin. Man. SEM700*, 1990.

[2] I. E. Commission and others, *Electromagnetic Compatibility EMC—Part 3-2: Limits for Harmonic Current Emissions (Equipment Input Current⩽ 16 A per phase)*, vol. 2. Edition, 2005.

[3] L. Huber, Y. Jang, and M. M. Jovanovic, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, 2008.

[4] U. Moriconi, "A bridgeless PFC configuration based on L4981 PFC controller," *Appl. Note AN*, vol. 1606, pp. 18–18, 2002.

[5] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005.*, 2005, vol. 2, p. 812–817 Vol. 2.

[6] L. XueChao and W. ZhiHao, "UCC28070 implement bridgeless power factor correction (PFC) pre-regulator design," *Appl. Rep. SLUA517-JULY*, 2009.

[7] J. W. Kimball and P. T. Krein, "A current-sensorless digital controller for active power factor correction control based on Kalman filters," in *Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE*, 2008, pp. 1328–1333.

[8] M. Pahlevani, S. Pan, S. Eren, A. Bakhshai, and P. Jain, "An Adaptive Nonlinear Current Observer for Boost PFC AC/DC Converters," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6720–6729, Dec. 2014.

[9] V. M. Lopez, F. J. Azcondo, A. de Castro, and R. Zane, "Universal digital controller for boost CCM power factor correction stages based on current rebuilding concept," *Power Electron. IEEE Trans. On*, vol. 29, no. 7, pp. 3818–3829, 2014.

[10] F. D. Freijedo, "Contributions to grid-synchronization techniques for power electronic converters," *Vigo Univ. Dep. Electron. Technol.*, 2009.

[11] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid converters for photovoltaic and wind power systems*, vol. 29. John Wiley & Sons, 2011.

[12] H. C. Chen, Z. H. Wu, and J. Y. Liao, "Modeling and Small-Signal Analysis of a Switch-Mode Rectifier With Single-Loop Current Sensorless Control," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 75–84, Jan. 2010.

[13] H. C. Chen, C. C. Lin, and J. Y. Liao, "Modified Single-Loop Current Sensorless Control for Single-Phase Boost-Type SMR With Distorted Input Voltage," *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1322–1328, May 2011.

[14] S. Golestan, M. Ramezani, and J. M. Guerrero, "An analysis of the PLLs with secondary control path," *Ind. Electron. IEEE Trans. On*, vol. 61, no. 9, pp. 4824–4828, 2014.

[15] T. Thacker, D. Boroyevich, R. Burgos, and F. Wang, "Phase-locked loop noise reduction via phase detector implementation for single-phase systems," *Ind. Electron. IEEE Trans. On*, vol. 58, no. 6, pp. 2482–2490, 2011.

[16] M. S. Reza, M. Ciobotaru, and V. G. Agelidis, "A Modified Demodulation Technique for Single-Phase Grid Voltage Fundamental Parameter Estimation," *Ind. Electron. IEEE Trans. On*, vol. 62, no. 6, pp. 3705–3713, 2015.

[17] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics Assessment of Advanced Single-Phase PLL Structures," *IEEE Trans. Ind. Electron.*, vol. 60, no. 6, pp. 2167–2177, Jun. 2013.

[18] P. Lamo, F. Lopez, A. Pigazo, and F. Azcondo, "An Efficient FPGA Implementation of a Quadrature Signal Generation Subsystem in SRF PLLs in Single-Phase PFCs," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2016.

[19] R. Peña-Alzola, M. A. Bianchi, and M. Ordonez, "Control Design of a PFC With Harmonic Mitigation Function for Small Hybrid AC/DC Buildings," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6607–6620, Sep. 2016.

[20] Y. Yang, L. Hadjidemetriou, F. Blaabjerg, and E. Kyriakides, "Benchmarking of phase locked loop based synchronization techniques for grid-connected inverter systems," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, 2015, pp. 2167–2174.

[21] Y. Yang, F. Blaabjerg, and Z. Zou, "Benchmarking of Grid Fault Modes in Single-Phase Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5, pp. 2167–2176, Sep. 2013.

[22] Y. Yang and F. Blaabjerg, "Synchronization in single-phase grid-connected photovoltaic systems under grid faults," in *2012 3rd IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 476–482.

[23] B. I. Rani, C. K. Aravind, G. S. Ilango, and C. Nagamani, "A three phase PLL with a dynamic feed forward frequency estimator for synchronization of grid connected converters under wide frequency variations," *Int. J. Electr. Power Energy Syst.*, vol. 41, no. 1, pp. 63–70, 2012.