Broadband Low-Noise GaN HEMT TWAs Using an Active Distributed Drain Bias Circuit

Friedbert van Raay, Rüdiger Quay, Beatriz Aja, Giuseppe Moschetti, Matthias Seelmann-Eggebert, Michael Schlechtweg, and Oliver Ambacher
Fraunhofer Institute of Applied Solid-State Physics (IAF)
Tullastr. 72, D-79108 Freiburg, Germany
friedbert.van.raay@iaf.fraunhofer.de

***Abstract* — Modern communication and radar systems show an increasing demand for robust ultra-broadband amplifiers for low-noise applications. A set of three different 0.5 GHz to 20 GHz MMIC LNAs using a GaN HEMT technology with a gate length of 0.25 µm was designed and fabricated, each with a noise figure between 3 dB and 7 dB over frequency. Two designs with four and five FET cells feature approx. 10 dB and 11 dB broadband gain, while a third MMIC with a chain connection of both figures more than 20 dB of gain. A distributed active drain bias circuit substitutes large area or off-chip inductor structures and enables a full-MMIC chain connection of both TWA stages.**

Keywords— Low-Noise Amplifiers, AlGaN/GaN HEMTs, Active Biasing Circuits, Distributed Amplifiers.

I. INTRODUCTION

GaN HEMTs have proven reasonable noise figure (NF) performance compared to e.g. GaAs pHEMT processes of comparable transient frequency [1, 2]. In a first step, this applies to narrowband amplifiers, e.g., at X-band frequencies [3]. For different modern communication system and radar applications, it is interesting to investigate the broadband noise performance of GaN HEMT technologies, as is done e.g. in [4, 5]. This leads to the scientific goal to explore the limits of the noise figure performance of broadband travelling-wave amplifiers (TWAs) using GaN HEMT technologies, e.g. in the frequency range from nearly zero to around two thirds of the unity gain current transition frequency. For broadband applications, the TWA concept is often used because of its inherent gain flatness and good input and output matching. One key issue of using broadband TWAs down to very low frequencies is the realization of the drain biasing, especially in MMIC integration. For this purpose, an active distributed drain bias circuit is proposed which uses a reactance circuit and therefore has no influence on the noise performance. This subcircuit concept enables a purely monolithic integration of a chain of ultra-broadband TWAs without using any external biasing circuitry. In this paper, a set of three 0.5 GHz – 20 GHz TWAs with gains of 10 dB and 20 dB and a noise figure of 3.5 dB at X-band frequencies using a GaN HEMT technology with a gate length of 0.25 µm is presented.

II. CIRCUIT CONCEPT

The primary design goal for the TWA is 20 dB of gain up to 20 GHz. A preliminary assessment of the required total gate width(s) and a loss consideration for the corresponding number of cells [6] shows that a chain of two TWAs is more feasible than a single-stage TWA. Herewith, the determination of the maximum size of the individual FET cells in the TWA(s) is derived from the intended maximum frequency. The most efficient case of building e.g. the artificial gate transmission line is to use the discrete input capacitances (C_{gs}) of the individual FET cells and add discrete spiral inductors instead of microstrip transmission lines, while adding a minimum amount of capacitive loading besides the input capacitances of the FET cells and enabling a rather compact design compared to using transmission lines. From the given input capacitance per gate width for the 0.25 µm GaN HEMT technology, and an input return loss specification of -10 dB, a maximum cell size of 180 µm is found. Typically, the output capacitance per cell is less critical than the input capacitance and the latter is the limiting factor here.

III. DISTRIBUTED DRAIN FET BIASING

The key aspect in ultra-wideband TWAs is the realization and especially the monolithic integration of the drain biasing of the TWA. Spiral inductors for low frequency coverage require more and more chip area with lower minimum frequency and avoiding resonances and increasing loss towards the upper frequency limit gets more and more challenging. Therefore, the proposed solution is a FET biasing circuit based on a bootstrap – reactance circuit principle [7]. For DC, this circuit acts as a current drain, and for RF it shows high-impedance inductive behavior, and high capacitive impedance beyond the eigen-resonance with the output capacitance of the FET. For eliminating this capacitive effect, a distributed biasing is used, i.e., each active FET cell in the TWA has its own biasing FET. The drain-source capacitance of the biasing FET and the drain-source capacitance of the active cell which is in cascode configuration are hidden in the output artificial transmission line of the TWA. The cell size of the bias FET can be chosen so that the total output capacitance of the bias FET and the active FET are identical to the input capacitance of the active FET. This means that the characteristic impedance and travelling time on input and output line are matched without any additional capacitors in the output line.

The reactance bias circuit between the drain line and the DC supply rail is a FET for each cell which has the gate-source input shorted by a rather large MIM capacitor, see fig. 1. The applied DC gate voltage of the bias FET(s) determines the DC drain voltage at the output line of the TWA. This DC-gate

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voltage is applied via a high-resistive voltage divider between the V_{DD} DC supply and ground potential. The high resistance of the voltage divider at the gate and the gate-source MIM capacitor allow to realize very large time constants “on chip”, e.g., 5kΩ times 5 pF or 25ns, i.e. the 3 dB low-frequency cut-off frequency is 6.37 MHz in this example. The equivalent inductance of the FET bias circuit is

$$L_{Bias} = R\,C / G_{m,eff} \quad \text{with } R = R_1 R_2 /(R_1+R_2) \qquad (1)$$

where R_1 and R_2 are the resistances of the voltage divider, and C is the MIM capacitance between gate and source. $G_{m,eff}$ is the effective transconductance of the FET which is reduced by a source resistor formed by an increased gate-to-source spacing of the electrodes of the bias FET, resulting in a value of approx. 160 mS/mm in our case. For a TWA with a total gate width of 0.72 mm (4 cells with 4 gatefingers of 45 µm length), this results in an effective inductance value of L_{Bias}=434 nH. In our example, the capacitor is realized as a MIMIM structure using three metallization and two dielectric layers with a total area of approx. (100 × 100) µm^2.

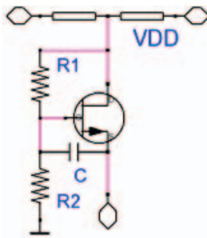

Fig. 1: Principle schematic of active drain bias cell.

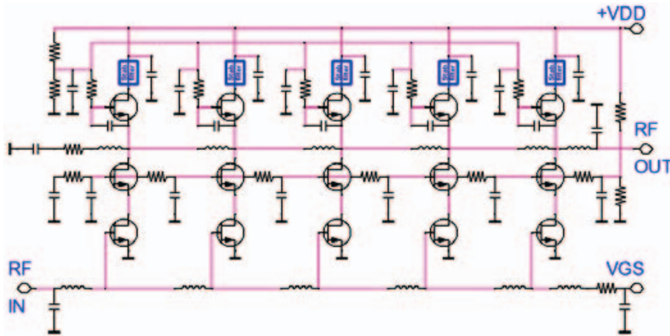

Fig. 2: Principle schematic of the TWA stage 1 with five FET cells.

IV. Design of TWA stage 1

Fig. 2 shows the schematic diagram of the first stage of the distributed amplifier chain. Five FET cells (4x45 µm each) are connected in parallel, the artificial transmission lines are formed using the input and output capacitances of the individual FET cells, respectively, and spiral inductors in between. The active FET cells are in cascode configuration to achieve a nearly frequency-independent gain and a good isolation between input and output transmission lines. On top of each active cell, the corresponding drain bias cell is located which returns the DC current of the active cell to the V_{DD} DC supply. The gate biasing of the active common-source (CS) FET cells is done through the internal load resistor of the RF input line. The common-gate (CG) FETs of the cascode structure are stabilized with RC low-pass filters in the gate bias rail. For increasing flexibility in application, the DC decoupling capacitors on the gate input and drain output line are omitted in the single-stage design. The stability investigation of the entire circuit shows an instability between 30 GHz and 40 GHz which requires an additional LC - bandstop filter stabilization circuit in the drain path of the biasing FET. The design of this stabilization subcircuit is discussed below in section VI. The common-gate cells are oversized in comparison to the common-source ones to maintain proper gain flatness and stability of the entire TWA. The main supply voltage is V_{DD} = 30 V, which is subdivided to the CS, CG and bias cells via resistive dividers for the gate voltages of the CG and CS bias stages. In the design procedure, the first step is the choice of the FET cell sizes for the CS, CG, and bias FET cells as described above. The main degrees of freedom are the inductances of the input and output artificial transmission lines, which are set to maintain the characteristic impedance of approx. 40 Ω fitting to the internal termination resistances and equal travelling times.

The LC compensation networks at the beginning and the end of these both transmission lines (see fig. 2) are used for fine-tuning the input and output reflection coefficients. A final residual mismatch due to the deviation of the characteristic impedances being somewhat smaller than 50 Ω is accepted. This eases better broadband matching up to approx. 2/3 f_T and gives a slightly improved noise performance. Starting from the optimized schematic, the layout is performed step-wise based on the FET cell columns of the TWA structure, mainly using the automatic layout generation feature for these columns in ADS.

V. Design of Second stage and TWA Chain

The second stage is designed using the same procedure as is described for the first stage. The main difference is that four FET cells are used in this case instead of five. The simulated performance of both stages is rather similar: Broadband gain of 12.5 (11.5) dB at 0.5 GHz, in both cases with a slight slope down to 11.0 (10.5) dB at 18 GHz and less than ± 0.5 dB ripple in both cases. The simulated noise figure (NF) has a wide minimum at approx. 6 GHz, and rises up to 6.5 dB at 20 GHz. The NF of the second stage is about 0.5 dB to 1 dB worse from low to high frequencies, respectively. This difference in noise figure is confirmed by the on-wafer measurements on the fabricated MMICs, see below.

It is important to emphasize that the FET reactance biasing configuration enables a chain connection to a two-stage TWA without any off-chip elements, i.e. realized on a single, compact MMIC. The chip areas of the MMICs for stage 1, stage 2, and the chain are 4.25 mm × 1.75 mm, 3.75 mm × 1.75 mm, and 4.25 mm × 3.0 mm, respectively. The chain connection of both TWAs is done with a short 50 Ω interconnect line and a 100 µm × 100 µm capacitor, which is again realized as a MIMIM structure. In the chain of both stages, the gain ripple is reduced by the combination of the five-cell and the four-cell TWA, which have gain ripples with a certain frequency offset. Figs. 3a, b show the layouts of the TWA stages 1 and 2, respectively. Fig. 4 depicts a chip photograph of the TWA chain MMIC.

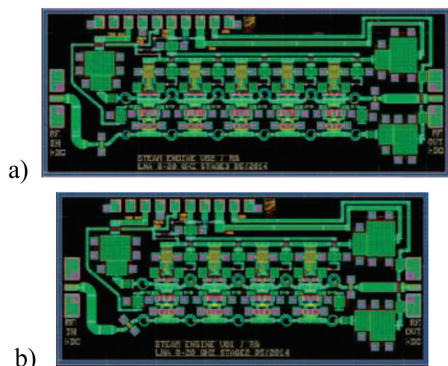

Fig 3: Layouts of TWA stages 1 and 2. a) stage 1, chip area 4.25 mm × 1.75 mm. b) stage 2, chip area 3.75 × 1.75 mm.

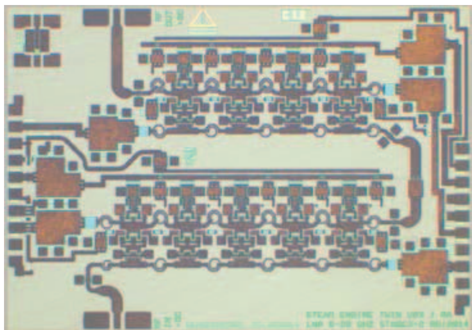

Fig. 4: Chip photograph of TWA chain of stages 1 and 2. Chip area: 4.25 mm × 3.0 mm.

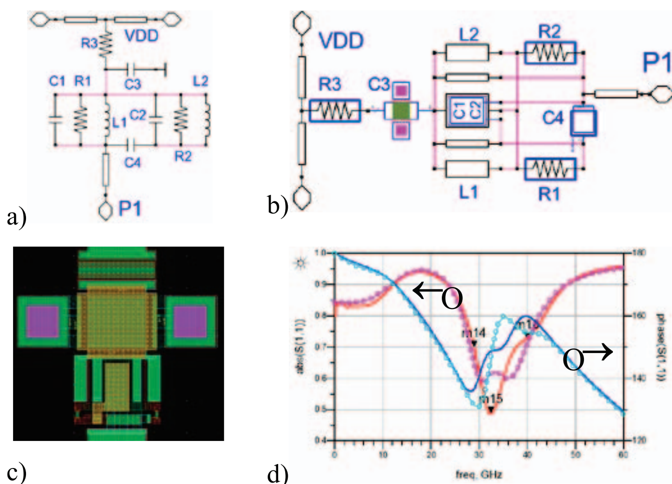

Fig. 5: Drain bias stabilization network. a) Simplified LCR schematic. b) Equivalent distributed circuit. c) Final layout. d) S(1,1) at port P1. MOM Simulation vs. LCR design goal. Magnitude (red: MOM, magenta/circles: LCR) and phase (blue: MOM, light blue/circles: LCR).

VI. DRAIN BIAS STABILIZATION NETWORK

For the drain bias stabilization network, a rather broadband but lossy parallel resonance structure turned out to be required. From the VDD drain DC supply rail, the DC supply for each column is taken via a RC low-pass filter (which is realized by a NiCr resistor and a MIM capacitor to ground) and then fed through the LCR distributed bandstop filter which is centered between 30 GHz and 40 GHz. The LCR equivalent schematic is shown in fig. 5a. It is a classical two-tank LC resonator with capacitive head coupling via capacitor C_4. The above-mentioned low-pass filter $R_3 - C_3$ separates the adjacent FET columns from each other. The resistors R_1, R_2 realize the necessary damping of the parallel resonators L_1, C_1 and L_2, C_2, respectively. P1 is the connection point to the drain of the bias FET cell. In a first design step, the lumped-element equivalent circuit schematic (fig. 5a) was used to adjust the LCR values to the desired damping and oscillation suppression performance vs. frequency and finally the entire TWA circuit was checked for internal stability. Subsequently, the discrete schematic was transferred to the distributed schematic shown in fig. 5b which comprises coupled CPW lines and MIM capacitor structures and NiCr sheet resistors instead of the ideal LCR elements. With this distributed schematic, the geometry values of the distributed elements were pre-adjusted towards the two-port S-parameter performance of the lumped-element LCR schematic of fig. 5a. Finally, the corresponding layout structure and geometry were optimized in several iterations of ADS Momentum simulations. One critical requirement during this design process was to squeeze the filter into the limited layout area which was available in the already partly finished subcells of the entire TWA circuit. The final area of the filter structure was only 135 µm × 132 µm. Fig. 5d shows the critical reflection coefficient S_{11} at port P1 of the filter as given by the final Momentum simulation of the layout structure in comparison to the goal defined by the ideal LCR network. Measured data are not available here, because this filter structure does not exist as a separate subcircuit pull-out on the fabricated wafer.

VII. MEASUREMENT RESULTS

The small-signal measurement and simulation results are illustrated in the figs. 6, 7, and 8 for the TWA stages 1 and 2 and the TWA chain, respectively. In each bottom graph, the magnitude of the reflection coefficients S_{11} and S_{22} is depicted in dB, and compared to an on-wafer mapping on a 3" wafer comprising 21 reticles. In each top diagram, the gain S_{21} and the noise figure are given in dB, and are again compared to the mapping measurement on the 3" wafer. A wide gain bandwidth of 0.5 GHz to at least 18 GHz is achieved in simulation and measurement. In the frequency range from 0.5 GHz to 20 GHz, the measured and simulated reflection coefficients are below - 10 dB. In the simulation, a gain bandwidth of approx. 2/3 $f_{T,ext}$ (extrinsic unity current gain transition frequency) has been accomplished. The small deviations in S-parameters and NF between simulation and measurement are due to a slightly reduced FET performance (gain and transient frequency) on the measured wafer, which is confirmed by the FET performance mapping results on the PCM RF test FETs on this individual wafer. It should be noted that even the trend between the noise figures of both the TWAs stage 1 and 2 (TWA stage 1 is better in simulated NF) is precisely confirmed in the measurement, while the NF mappings are very homogeneous and show a small sample deviation of ±0.1 dB. Taking into account the ratio of the maximum operating frequency to the unity current gain transition frequency of the used technology, the achieved noise performance is comparable to other state-of-the-art GaN and GaAs broadband TWAs [5, 8].

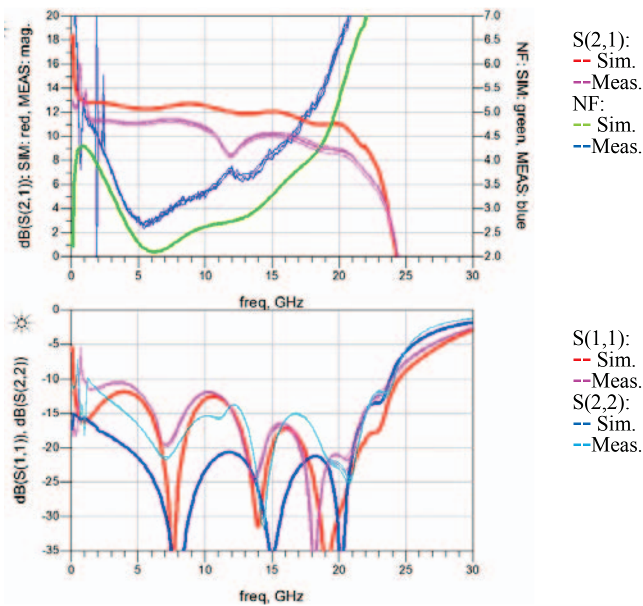

Fig. 6: Measured (wafer map) and simulated S-parameters and NF of TWA stage 1. Top: S(2,1) in dB and NF in dB. Bottom: S(1,1) and S(2,2) in dB.

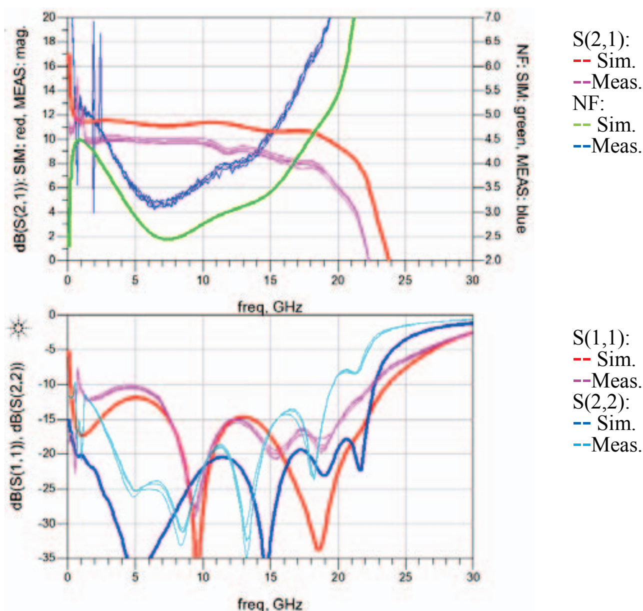

Fig. 7: Measured (wafer map) and simulated S-parameters and NF of TWA stage 2. Top: S(2,1) in dB and NF in dB. Bottom: S(1,1) and S(2,2) in dB.

VIII. Conclusion and Outlook

Two different ultra-broadband four-cell and five-cell cascode TWAs using a 0.25 µm GaN HEMT technology have been designed for low-noise applications. A new distributed FET current source drain biasing using a bootstrap–reactance circuit principle avoids area-consuming or even off-chip hybrid inductors with inherent eigenresonance problems at high frequencies. This enables a full – MMIC and area – saving chain connection of both TWAs. The design procedure emphasizes the subcircuit for FET drain biasing. A bandwidth of 2/3 f_T (transient frequency) was experimentally validated for both TWAs and their chain connection as a third MMIC in on-wafer measurements. The achieved noise figure values are comparable to state-of-the-art GaN and GaAs broadband TWAs. A future re-design will address even better gain flatness and a DC level shifter using common-drain FET(s) in the interstage of the TWA chain instead of using a simple capacitive decoupling.

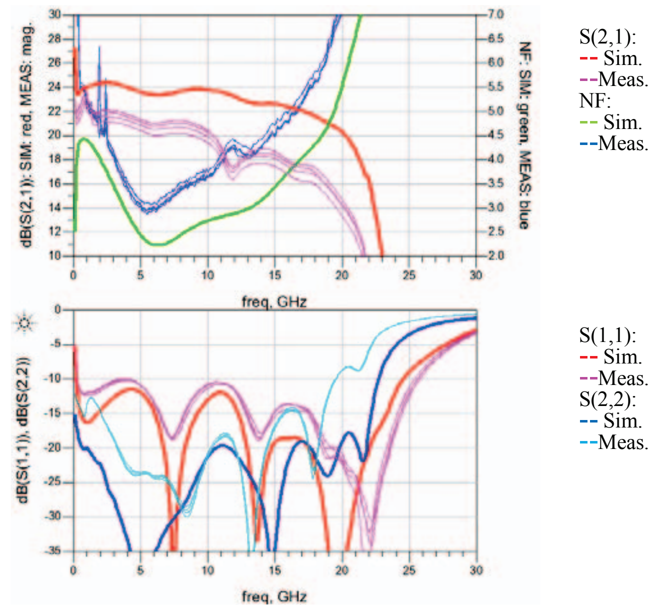

Fig. 8: Measured (wafer map) and simulated S-parameters and NF of TWA chain. Top: S(2,1) in dB and NF in dB. Bottom: S(1,1) and S(2,2) in dB.

Acknowledgment

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