A Planar 75 % Efficient GaN 1.2-GHz DC-DC Converter With Self-Synchronous Rectifier

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***Abstract*—This paper presents the design and characterization of a DC-DC converter operating at 1.2 GHz with a maximum efficiency of 75 % at 4.6 W output power, and with a maximum output power of 13 W at 58 % efficiency. The microwave converter consists of a GaN class-E power amplifier coupled to a GaN class-E rectifier. The circuit is planar and exhibits a power density of approximately 0.65 W/cm^3 at the 75 % efficiency point. The rectifier can be operated with input gate drive or self-synchronously with a single RF input.**

***Index Terms*—DC-DC converters, high efficiency power amplifiers, rectifiers, harmonic terminations.**

I. Introduction

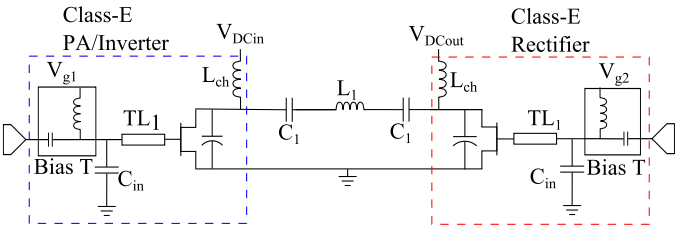
THE increase in switching frequency in DC-DC converters can considerably reduce the value and size of passive components used for decoupling filters and energy storage, leading to higher power density, reduced size, and faster transient response. An additional benefit is the potential for monolithically integrated miniaturized supplies with higher current densities, since magnetics are eliminated or greatly reduced [1]. These benefits can be observed in applications such as envelope tracking (ET) and integration of power supply on chip [2]. Increasing the frequency of the converter, however, presents an additional set of challenges, such as higher losses in the active device as well as in passive components, and high-frequency parasitics which limit switching frequency and power as summarized in [3].

Table I compares recently published DC-DC converters with switching frequencies approaching the GHz range.

Table I
High frequency DC-DC converters comparison

Ref.	Year	f (GHz)	Technology	P_{out} (W)	η (%)
[4]	2008	0.030	MOSFET	220	87
[5]	2009	0.110	LDMOS	25	86
[6]	2005	0.233	CMOS	0.55	82
[7]	2012	0.780	GaN	11.5	72
[8]	2013	1	GaN	8.5	77
This work	2014	1.2	GaN	5.0	75
[9]	1999	4.5	GaAs	0.02	64

In this paper, a 1.2 GHz DC-DC converter with an efficiency of more than 70 % and a maximum output power of 7.6 W is introduced. The design is based on a class-E^2 converter first introduced in [10] and recently scaled to a 0.994 GHz 8.5-W, 77 % efficiency design [8] shown in Fig. 1. The RF output of the class-E PA (inverter) operated with the drain supply V_{DCin} is connected to the drain RF input of a class-E transistor rectifier through a filter. The rectifier is then driven with an RF input at the gate producing a V_{DCout} output voltage at



C_{in}	3.9 pF	C_1	12 pF
L_{ch}	24 nH	TL_1	4 mm
L_1	1.8 nH	Bias T	28 nH 33 pF

Fig. 1. Circuit schematic for class-E^2 converter consisting of a class-E PA and rectifier coupled through a resonant network.

the DC load connected to the rectifier drain. The RF input at the rectifer gate can be eliminated by connecting a specific impedance to ground, resulting in self-synchronous operation [11].

II. Design and Characterization of the Converter

Detailed analysis of the converter from Fig. 1 has previously been published in e.g.[10], [12]. The goal of the work presented in this paper is to demonstrate an efficient DC-DC converter switching in the GHz range with 5-10 W of output power and as low profile as possible, leading to high volume power density. The two transistors are GaN on SiC pHEMTs T2G6001528-Q3 from TriQuint. The estimated output capacitance is $C_{out} \approx 2.7$ pF and the series resistance is $R_{ON} \approx 0.5\,\Omega$. The breakdown voltage and maximum current are specified as 100 V and 5 A, however a operational peak drain current of 1.4 A is recommended.

Well known class-E design equations for the maximum frequency of operation and the class-E load presented at the virtual drain of the device are given by [13]

$$f_{max} = \frac{I_{DS}}{2\pi^2 C_{out} V_{DS}} \tag{1}$$

$$Z_{net} = \frac{0.28015 e^{j49.0524^\circ}}{\omega_s C_{out}} \tag{2}$$

Using the estimated value of C_{out}, V_{DS}= 18 V and I_{DS}=1.4 A in (1), a maximum switching frequency of ≈1.5 GHz is obtained. In order to account for additional parasitic capacitance while maintaining a high switching frequency, a more conservative operating frequency of 1.2 GHz is chosen. The impedance to be synthesized by the matching

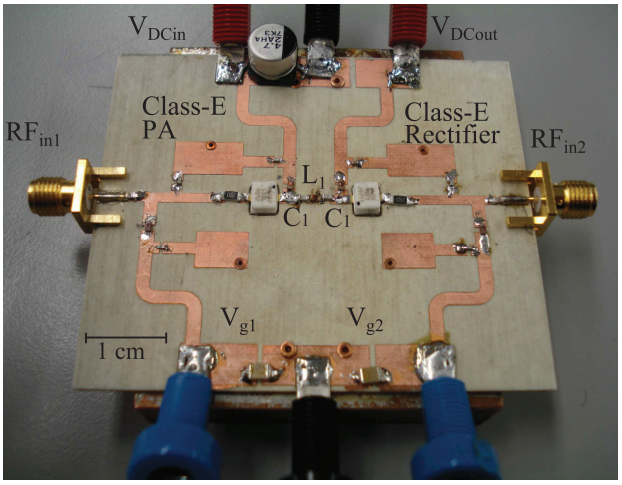


Fig. 2. Photograph of class-E^2 synchronous converter corresponding to the block diagram in Fig. 1. The DC-AC conversion is performed by the class-E PA, and the AC-DC conversion by a synchronous rectifier with the same circuit architecture as the PA. Both gates are RF-driven. The DC output V_{DCout} is connected to a variable load.

network is calculated to be Z_{net}= 9 + j10.4 Ω from [13]. As described in [12], the rectifier provides the correct value of $\Re\{Z_{net}\}$ and the reactances presented to the amplifier and the rectifier can be combined into one, resulting in 9 + j20.8 Ω. To synthesize Z_{net} at f_0 and provide an open circuit at $2f_0$ and $3f_0$, the approach of [7] is adopted. The parasitic capacitance of a series inductor L_1 in Fig. 1 provides an approximately open circuit at $2f_0$ and $3f_0$ when the inductor's self resonance frequency (SRF) is between the two harmonics, while a series capacitor C_1 tunes the impedance at the fundamental.

To maintain low circuit profile, only passive components with a maximum thickness of 2 mm are used. With this restriction, inductors from Coilcraft's 0603HP series, and capacitors from ATC's 600L and 600S series are chosen. The inter-stage network is simulated using NI/AWR MWO with high frequency models for the passive components provided by Modelithics. The design is implemented on a 30-mil Rogers RO4350B substrate, and a photograph of the prototype is shown in Fig. 2.

A. Measurements and results

The converter is characterized using the setup shown in Fig. 3. The PA is biased at a quiescent current of 10 mA for input voltages ranging from 12-27 V, and the rectifier transistor is pinched-off. R_{DC} is implemented using a BK Precision 8500 electronic DC load in a constant voltage mode enforcing output voltages ranging from 10-27 V. All the measurements are performed with P_{in}= 23 dBm. The phase shift is adjusted for synchronous operation. Fig. 4 shows the efficiency and output power as a function of output voltage for 13, 17 and 27 V. The efficiency of the converter is defined as

$$\eta_{DC-DC} = \frac{V_{DCout} I_{DCout}}{V_{DCin} I_{DCin}} \quad (3)$$

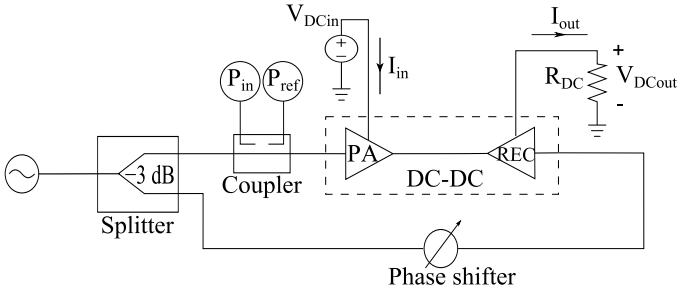


Fig. 3. Setup used to characterize E^2 converter prototype. The output voltage is enforced by the electronic load while the current is allowed to be set by the converter itself.

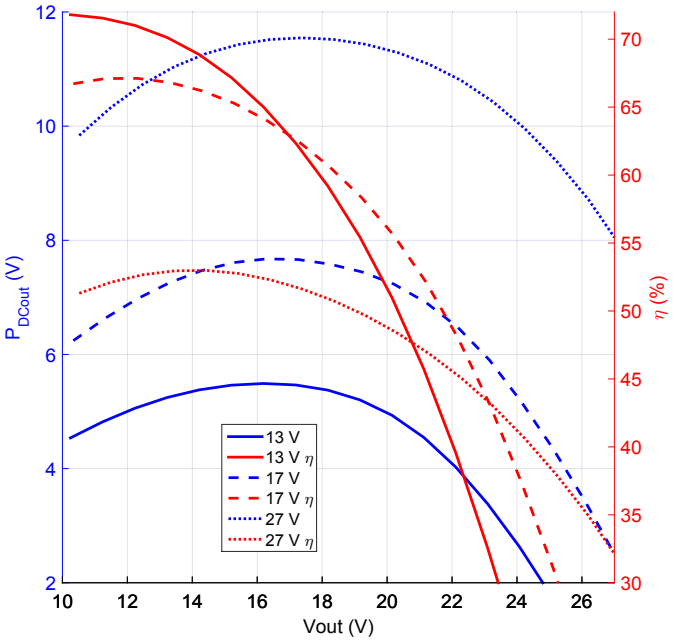


Fig. 4. Measured converter efficiency (red) and output power (blue) plotted as a function of output voltage for an input voltage of 13, 17 and 27 V.

As expected, output power increases with input voltage, while the efficiency of the converter decreases with increasing input and output voltage.

III. Self-Synchronous Operation

It is shown in [11] that at microwave frequencies a transistor rectifier can be operated in self-synchronous mode without the need of an RF input, enabled by gate to drain feedback capacitance. The feedback power at higher frequencies is sufficient to drive the rectifier; hence, if an appropriate impedance is connected at the gate, the rectifier does not require a separate RF input. A prototype of a self-synchronous converter is shown in Fig. 6.

A load-pull measurement is performed to determine the optimum impedance at the gate port of the rectifier for maximum efficiency at an input voltage of 13, 17 and 27 V. The results for 17 V are plotted in Fig. 5, with the optimum

impedance of approximately 3.7 + j44.3 Ω at the connector reference plane. The efficiency contours clearly show the area of the Smith chart where the gate impedance nees to be for efficienct self-synchronous operation.

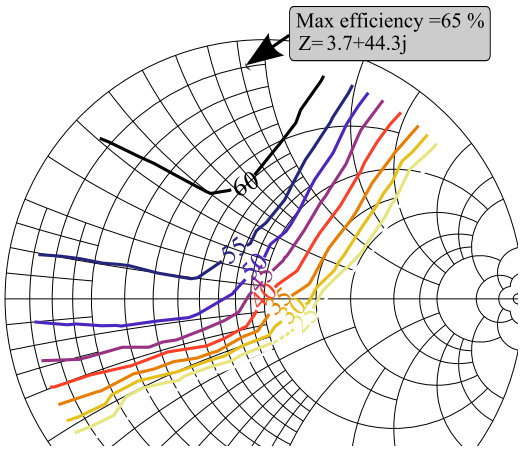


Fig. 5. Impedance constellation and efficiency contours produced by a load pull performed at the gate port of the rectifier for maximum efficiency for a DC output voltage of 17 V. The Smith chart is normalized to 50 Ω.

The rectifier input matching network and the connector are de-embedded and the impedance presented at the reference plane of the transistor gate is estimated to be 0.15 + j2 Ω. A single 8 pF shunt capacitor to ground is used to present the impedance to the transistor.

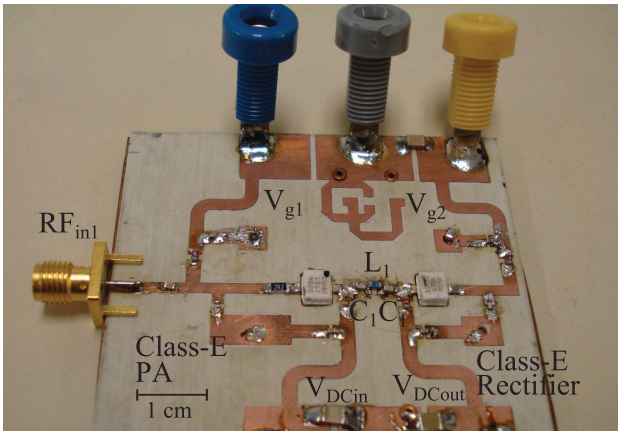


Fig. 6. Photograph of class-E^2 converter with the rectifier operating self-synchronously. The RF port at the gate of the rectifier is removed and the input matching network is modified to present the optimum impedance to the rectifier. The size of the circuit board is 5.6 cm by 6 cm.

The converter is then characterized following the previously described procedure without the need of a second RF driver for the rectifier. Fig. 7 shows the efficiency and output power as a function of output voltage for 13, 17, and 27 V. The results are improved compared to those of Fig. 4 . The converter is the most efficient at 13 V input voltage and at lower output voltages in general, achieving an efficiency above 70 % for output voltages ranging from 11-17 V, with a maximum efficiency of 75 % and 4.6 W.

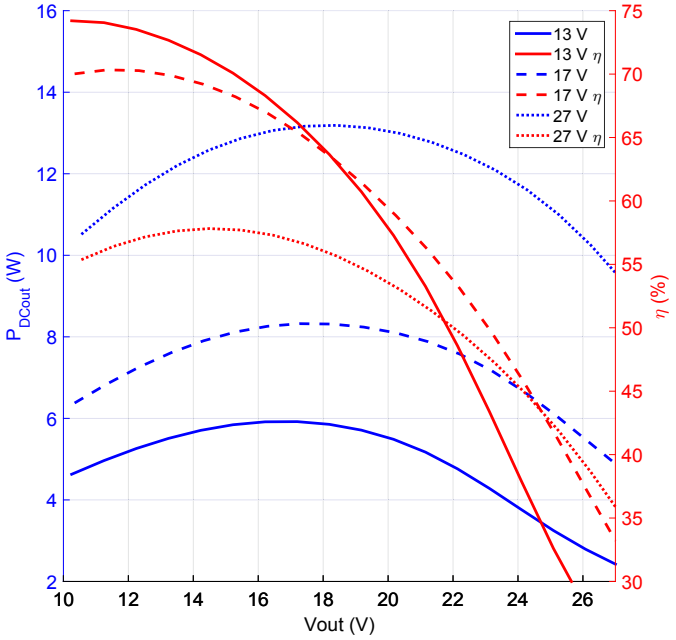


Fig. 7. Self-synchronous class E^2 measured converter efficiency (red) and output power (blue) plotted as a function of output voltage for an input voltage of 13, 17 and 27 V.

IV. Conclusion

Two microwave DC-DC converters that operate at a switching frequency of 1.2 GHz with efficiencies of approximately 70 % at greater than 5 W are presented. The thickness of the passive elements in the converter is maintained below 2 mm in favor of increasing power density and integration. The operation of the rectifier in self-synchronous mode provides an important step in the implementation of a resonant DC-DC converter with no RF driving signals. Although the efficiency of the converter is lower compared to low-frequency alternatives, the converter is planar, contains no bulky magnetic components and is amenable to monolithic integration.

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