An E-pHEMT S[illegible]biased and Self-synchronous Class E Rectifier

M. N. Ruiz and J. A. García.

Dept. of Commun[illegible]s Engineering, University of Cantabria, 39005 Santander, SPAIN

Abstract — In this paper, the[illegible] a self-biased and self-synchronous class E rectifier, ba[illegible]n Enhancement-mode Pseudomorphic High Electron M[illegible]ransistor (E-pHEMT), is proposed. Characterized by a [illegible]ue of the switch-mode time-constant (the on-state [illegible] times the output capacitance), high power effici[illegible]res may be obtained when forcing zero-voltage and z[illegible]e-derivative switching conditions (ZVS and ZVDS). T[illegible]ynchronous operation, made possible by the device gate[illegible] coupling capacitance, leads to a compact design, whi[illegible]ate-to-source Schottky junction allows self-biasing the ga[illegible]al in order to improve the efficiency versus input power profile. Simulations, based on an extracted simplified non-linear model, are combined with measured results for implementations at 900 MHz and 2.45 GHz. Efficiency values as high as 76% and 64% have been estimated at power levels of -4 dBm and -1 dBm, respectively, with peak figures of 88% and 77%.

Index Terms — Class E, E-pHEMT, nonlinear model, rectifiers, rectennas, wireless powering.

I. Introduction

During the last years, the interest on the design of high-efficiency RF-to-DC rectifying circuits has increased significantly, conceived in this case as part of the rectifying antenna or rectenna [1], to be employed in the receiving end of a far-field wireless power transmission link or in an high frequency electromagnetic energy harvester [2]. Although usually designed over Schottky diodes, due to their benefits in terms of simplicity, compactness and cost, some efforts have also appeared in the introduction of synchronous or transistor-based rectifiers [3]. Using E-pHEMT commercial devices, high efficiency figures were reported for relatively high power levels, more typical of power beaming applications, without requiring an auxiliary bias source for the gate terminal. A low power density topology resulted, associated to the use of a complex multi-harmonic drain terminating network and the introduction of an external path for properly synchronizing the gate-to-source and drain-to-source voltage waveforms. The performance also deteriorated at lower power values, as the excitation signal amplitude was far from forcing the desired device operation as a switch.

In this paper, simple lumped element drain and gate terminating networks are employed, based the first on a self-resonant coil [4], while aimed the second to take full advantage of the device intrinsic drain-to-gate reactive signal path [5]. A gate self-biasing mechanism is also added to maximize the output conductance variation, and consequently the rectifier efficiency, along a significant input power range.

II. E-pHEMT Characterization and Modeling

As power should be delivered to the DC load resistor, a rectifying transistor operates in the third quadrant of its I/V characteristics when in the conduction or on-state [6]. Most available non-linear models for MESFETs and HEMTs have been conceived for their use as current-source mode amplifiers, reason why their prediction capabilities are far from being the best in the linear region and sometimes fail reproducing the inverse operation (V_{ds} and $I_{ds} < 0$). Some alternatives were proposed nearly 15 years ago, as [7] and [8], motivated by a great interest in the design of highly linear controlled attenuators, switches and resistive mixers. The real symmetry of the device behavior suggested the use of V_{gd} instead of V_{ds} as a control voltage. In more recent papers, the case of [9], a slightly different strategy has been followed with very good fitting of the device global characteristics.

Based on those works, a simple non-linear model, whose equivalent circuit appears in Fig. 1, has been extracted for the selected device, the VMMK-1218, a 0.25 µm gate E-pHEMT in a GaAsCap wafer-scale sub-miniature leadless package from Avago Semiconductors. While the C_{gs}, C_{gd} and C_{ds} capacitances have been assumed to be linear and extracted from [S] parameter measurements in off-state, the $I_{gs}(V_{gs})$ and $I_{gd}(V_{gd})$ nonlinearities have been adjusted to the widely accepted Schottky junction equation.

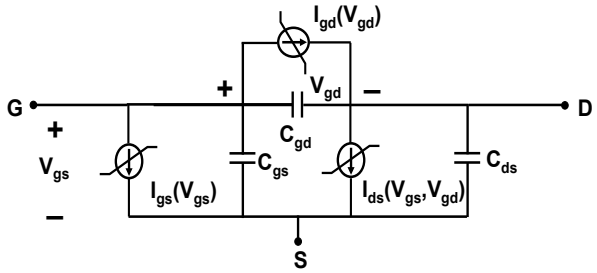


Fig. 1 Electrical equivalent circuit of the extracted model.

The $I_{ds}(V_{gs},V_{gd})$ main nonlinearity, modeled through eq. (1), includes continuous and continuously derivable functions for accurately describing the exponential nature of the sub-threshold device behavior. Special attention was also put in the reproduction of the linear regions in normal and inverse operation (first and third quadrant).

$$Ids(V_{gs},V_{gd}) = \beta[1+\lambda(V_{gs}-V_{gd})]\ \{[\alpha(V_{gs}-V_{th}) + \ln(2\cosh(\alpha(V_{gs}-V_{th})))](1+\mu V_{gs}) - [\alpha(V_{gd}-V_{th}) + \ln(2\cosh(\alpha(V_{gd}-V_{th})))](1+\mu V_{gd})\} \quad (1)$$

where β = 15 mS, α = 7 V^{-1}, μ = 0.25 V^{-1}, V_{th} = 0.6 V and λ = 0.135 V^{-1}.

As it may be appreciated from Fig. 2, a good agreement exists between the measured and modeled characteristics, despite the relative simplicity of the adjusted equation.

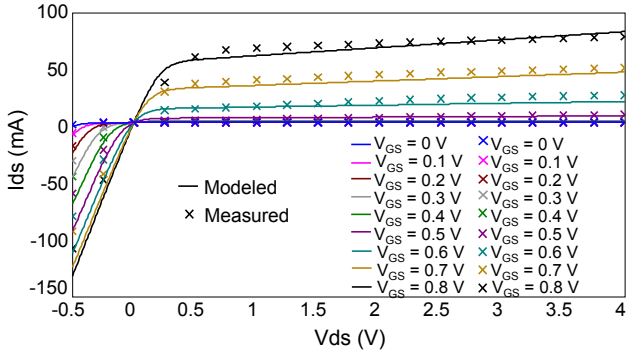


Fig. 2 Comparison of I/V measured and modeled characteristics.

III. Drain and Gate Terminating Impedances

The nominal drain termination at the fundamental, theoretically derived for assuring ZVS/ZVDS operation, $Z_{opt}(f) = [0.1836+j\cdot0.2116]/(\omega\cdot C_{out})$, was estimated from the extracted device capacitances. Using the above presented model, a load-pull simulation with the VMMK-1218 operating in inverting mode and open conditions to the second and third harmonic showed that the maximum efficiency appeared very close the theoretical value, 170+j·196 Ω.

After fixing this value at the drain terminal, load-pull simulations at gate side, following the procedure employed in [5], were carried out for different power levels and V_{GS} values. The output DC resistance, R_{DC} = 380 Ω, was derived from the inverter simulations and approximately fitted the theoretical $R_{DC} = V_{DD}/I_{DD} = 1/(\pi\cdot\omega\cdot C_{out})$ equation. As it may be appreciated from Fig. 3, for two different power levels and the V_{GS} voltage where maximum efficiency was estimated (a value decreasing with the RF power), the optimum reflection coefficient at gate side was nearly the same.

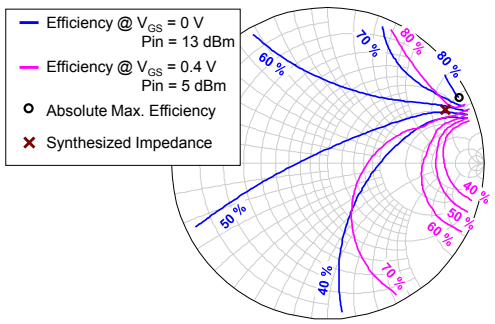
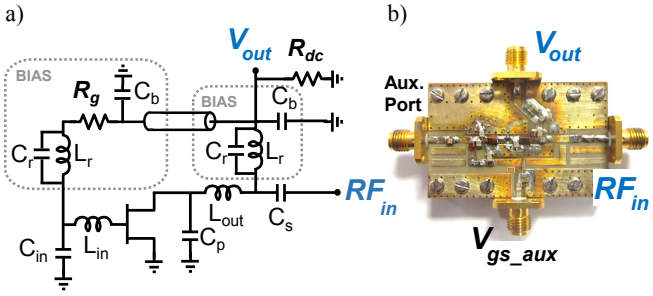


Fig. 3 Load-pull simulation results in self-synchronous mode.

Evaluating the PI reactive part of the model (C_{gs}, C_{gd} and C_{ds}) in Fig. 1 with such a termination at gate side, the drain-to-gate voltage transfer function was estimated to be 0.19·exp(-j·180º), which means optimum self-synchronous operation occurs when the fundamental components of $V_{gs}(t)$ and $V_{ds}(t)$ are opposite phase, while their absolute values are related by $1/G_v$, with $G_v = |V_{ds}(f)/V_{gs}(f)|$ the voltage gain (14 dB) estimated from the simulations of the class E amplifier, its time-reversal dual.

IV. Rectifier Topology and Measured Results

The proposed lumped-element circuit topology for the class E rectifier appears in Fig. 4a, together with details of the implementation in Fig. 4b. A table with the values is also provided. Ultra-miniature high current air core inductors from Coilcraft and 100A multilayer ceramic capacitors from ATC have been employed.



L.E.	C_{in}	L_{in}	C_p	L_{out}	C_s	L_r	C_r	C_b	R_g
Value	3.3 pF	25 nH	0.1 pF	25 nH	6.8 pF	11 nH	2.7 pF	100 pF	10 kΩ

Fig 4 a) Class E rectifier schematic and b) implementation at 900 MHz.

The L_{out} coil at drain side was selected with a self-resonant frequency between the second and third harmonic [4]. The series capacitance C_s, resonating L_{out}, provides the required inductive termination at the fundamental, while C_p allowed adjusting the real part of the optimum impedance. Parallel resonant circuits (L_rC_r) were used instead of chokes at the gate and drain DC paths to force an open condition at the fundamental. The $C_{in}L_{in}$ gate network was designed for approximating the optimum gate termination. The synthesized gate impedance has been also included in Fig. 3.

The rectifier performance was then characterized versus input power for different gate-to-source biasing voltages, as represented in Fig. 5a. The efficiency profile may peak at different power levels if such a voltage were conveniently adjusted following the represented optimum law, also derived from the load-pull simulations in section III. For very low power levels, the best conversion efficiency appears at V_{GS} = 0.37 V, relatively close to V_{th}. Describing the threshold voltage the point where the device output conductance has a maximum variation with V_{gs}, the greatest difference between the off-state and on-state resistances may be forced at this point for small available gate driving amplitudes. When the input power level increases, the desired device performance as

a switch is better approximated if lowering such a voltage below threshold.

The proposed self-biased topology is based on the connection of the output DC voltage port (drain side) to the gate biasing path. In this way, when increasing the input power, the rectified voltage allows increasing V_{GS} up to close the threshold value (see blue trace in Fig. 5b, for P_{in} < -4 dBm). As observed from Fig. 5a, the efficiency suddenly grows thanks to this self-biased effect.

Above this power value, keeping a high efficiency would demand decreasing V_{GS} along the optimum path (gray dashed trace in Fig. 5b). Advantage may be taken from the small value of the rectified current appearing at gate terminal, associated to the $I_{gs}(V_{gs})$ Schottky junction nonlinearity (see model schematic in Fig. 1). A properly dimensioned resistor, R_g= 10 kΩ, introduced in the gate biasing path, allows reducing the gate-to-source DC voltage, following $V_{GS} = V_{out} - R_g \cdot I_{GS}$, close to the optimum trajectory.

As it may be appreciated in Fig. 5a, a peak value of 88% was obtained at 16 dBm (V_{GS}=-0.36 V), while the efficiency was as high as 76% at a power value of -4 dBm (V_{GS}=0.31 V).

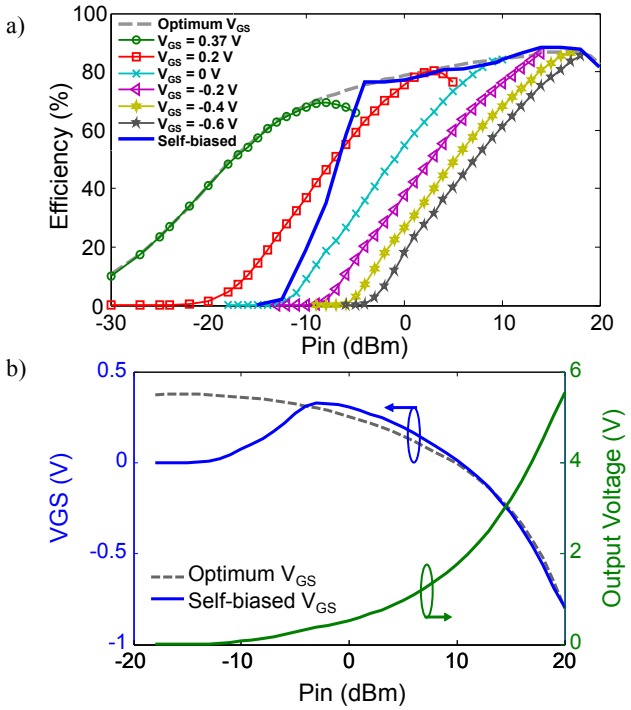


Fig. 5. Measured profiles with input power for the a) efficiency, b) the output and the V_{GS} voltage.

A similar design procedure was followed for a 2.45 GHz rectifier, based on the same VMMK-1218 device. In Fig. 6, the measured evolution of output voltage and efficiency are plotted versus input power. The estimated peak was in this case of 77% at 13 dBm, with a 64% value at -1 dBm.

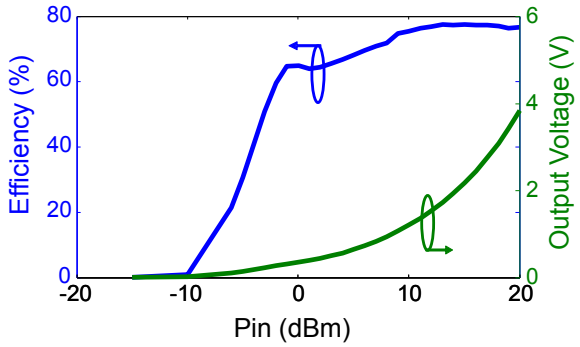


Fig. 6. Measured output voltage and efficiency profiles versus input power for a 2.45 GHz implementation.

These results, at a higher frequency band, support the validity of the proposed design methodology, the accuracy of the extracted device nonlinear model for rectifier simulation, as well as the potential of the employed E-pHEMT technology. If interested in a broadband operation, attention should be put to the quality factor of the drain terminating network at the fundamental as well as to the evolution of the best gate side impedance condition. Employing a transistor instead of a diode, besides the flexibility associated to the auxiliary control provided by the gate voltage, the circuit may be reconfigured for operation in an inverse rectenna mode (class E oscillator) [10].

V. Conclusion

The design of a self-biased and self-synchronous class E rectifier, based on an Enhancement-mode Pseudomorphic High Electron Mobility Transistor (E-pHEMT), has been presented. A dedicated and simple device nonlinear model, combining linear capacitances and a symmetrical $I_{ds}(V_{gs}, V_{gd})$ equation, has been proposed and employed for simulating the device performance in this mode of operation, overcoming the limitations associated to most widespread solutions. Combining a simple drain terminating network, based on a self-resonant coil, a self-synchronous operation and a gate self-biasing strategy, the efficiency may be kept high for a significant power range.

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