A linear assisted switching envelope amplifier for a UHF Polar Transmitter

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***Abstract*—Spectrally efficient wireless communication standards impose stringent linearity specifications, which would require traditional IQ transmitters to operate with back-offed and power inefficient linear RF power amplifiers (PAs). In order to overcome such a significant limitation, alternative architectures have been proposed, as those based on the Envelope Elimination and Restoration (EER) technique. An example of the application of this technique is the Polar Transmitter. In this paper, a UHF Polar Transmitter is presented, combining switching and linear stages in the envelope amplifier as to achieve both wide bandwidth and high efficiency, when drain modulating a GaN HEMT Class E RF PA. Several tests, using EDGE, TETRA, and WCDMA standards have been performed with good results.**

I. Introduction

THE simultaneous phase and envelope variations, typical of spectrally efficient wireless communication standards, require using linear Radio Frequency Power Amplifiers (RF PAs) that operate in power backoff, resulting in low energetic efficiency. In order to increase the efficiency of these systems, techniques derived from *Envelope Elimination and Restoration- (EER)*, formerly proposed by L.R. Kahn in [1] can be employed [2], [3]. Several implementations and theoretical analysis of Kahn-technique transmitters can be found in the literature [4]–[9]. Modern versions of these EER-based techniques, where the amplitude and phase components are digitally generated at base band, are often known as Polar Transmitters.

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In order to explain how a Polar Transmitter works, a brief introduction will be done here. In Fig. 1a its basic architecture is presented. The Signal Source block generates the reference to the Envelope Modulator and to the RF PA from the IQ baseband components. Therefore, the communication signal is digitally split into its amplitude and angular components, labelled E(t) and $\phi(t)$ in Fig. 1a. This task is done according to the following equations:

$$E(t) = \sqrt{I^2(t) + Q^2(t)} \tag{1}$$

$$\phi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right) \tag{2}$$

The information contained in the angle of the complex envelope, labelled $\phi(t)$, is used to phase modulate the carrier signal at frequency $\omega_{carrier}$. This task is performed by the PM Modulator block. The resulting constant-envelope RF signal may be efficiently amplified by a switched-mode or saturated RF PA, such as a Class E amplifier. The desired envelope variations, $E(t)$, are introduced through the Envelope Modulator (EM), which provides a dynamic bias for high level amplitude modulating the RF PA. As the voltage in the drain of the transistor in the final stage RF PA is varying along the envelope signal by means of the output voltage of the envelope modulator, the resulting RF signal is both phase and envelope modulated. This process is known as *drain modulation*. Sometimes the input signal of the RF PA is amplitude modulated when the output RF power is very low in order to reduce distortion ([6], [8], [9]) due to *feed-through* effects. This process is known as *drive modulation*. This leads to an architecture known as Hybrid Modulator, represented in Fig. 1b. In this case drain modulation is provided for output amplitudes above a certain level, let us say 50% of the maximum output amplitude. For output amplitudes below this level, the modulation is carried out by means of drive modulation. Therefore, the input signal of the RF PA is a phase and amplitude modulated RF signal, clipped to a certain amplitude level. The envelope signal processed by the

Envelope Amplifier has a constant value in the places where the RF input signal is amplitude modulated, and follows the communications envelope in the rest of the signal. The following equation describes how signal $E_H(t)$ is obtained:

$$E_H(t) = \begin{cases} E(t) & \text{if } E(t) \geq E_{min} \\ E_{min} & \text{otherwise} \end{cases} \quad (3)$$

where $E(t)$ is the signal described in (1). Once $E_H(t)$ is obtained, the IQ components $I_d(t)$ and $Q_d(t)$, that will determine the signal processed by the RF PA V_{RF_in}, are calculated as follows:

$$I_d(t) = \begin{cases} k \cdot E_{min} \cdot \cos(\phi(t)) & \text{if } E_H(t) \geq E_{min} \\ k \cdot E(t) \cdot \cos(\phi(t)) & \text{otherwise} \end{cases} \quad (4)$$

$$Q_d(t) = \begin{cases} k \cdot E_{min} \cdot \sin(\phi(t)) & \text{if } E_H(t) \geq E_{min} \\ k \cdot E(t) \cdot \sin(\phi(t)) & \text{otherwise} \end{cases} \quad (5)$$

where k is a constant chosen in such a way that the minimum value of V_{out} in Fig.1b, V_{out_min}, coincides with $k \cdot E_{min}$ multiplied by the RF PA gain at V_{out_min}. In order to reduce the bandwidth of the envelope and the RF signal, determined by these hard clipping functions, a soft clipping is usually preferred as suggested by several authors [8], [9]. In these conditions all the system behaves correctly and the output signal is the desired one. Signals $I_d(t)$ and $Q_d(t)$ are sent to an IQ modulator which generates the signal V_{RF_In} (see Fig.1b). In both cases, the Polar and the Hybrid Transmitter, the envelope and the RF signal must be synchronized to correctly generate the desired final RF signal with minimum distortion. It should be noted that the hybrid architecture is less stringent concerning this fact than the Polar Transmitter. Moreover, pre-distortion of the RF signal can be employed to further linearise the complete system.

Regarding the overall efficiency, one of the most critical parts is the Envelope Amplifier, also known in literature as Envelope Modulator. In order to keep its efficiency high, a switching-mode DC/DC converter is often used [10]–[14]. However, the bandwidth and *slew-rate* requirements imposed by the communications signals usually surpass the capabilities of these DC/DC converters. In order to solve that, combination of switching mode DC/DC converters with linear stages have been proposed [15]–[19]. The efficiency of these systems remains high, because the switching stage provides most of the power (concentrated at frequencies up to several hundreds of kHz), while the linear stage

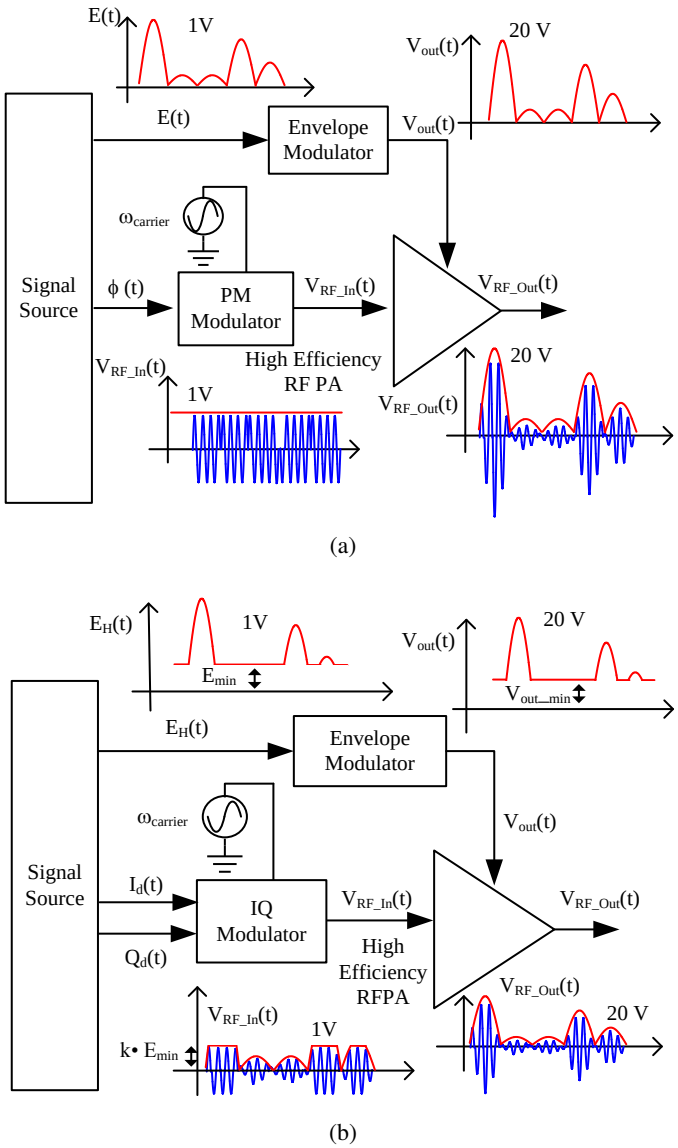


Fig. 1: Diagrams of the proposed architectures: (a) Polar Transmitter Architecture and (b) Hybrid Transmitter Architecture

provides the power associated with the fast variations in the output voltage of the EM. The higher the bandwidth of the switching stage, the more efficient the overall system, since the switching stage can reproduce faster variations, reducing the power provided by the linear stage.

This paper presents an improved version of the system presented in [19]. The bandwidth of the switching stage is enhanced by means of an improved output filter design. The Envelope Modulator is also properly combined with an RF PA to build a Polar Transmitter for the UHF band. The RF PA is a GaN HEMT Class E amplifier, operating at 770 MHz. The operation has been

tested using EDGE, TETRA and WCDMA standards.

This paper is organized as follows: Section II expounds the operation of the Envelope Modulator. A brief explanation on the RF PA design is given in section III. Experimental results are shown in section IV. Finally, conclusions are addressed in section V.

II. Operation of the Envelope Modulator

A. Principle of Operation

The Envelope Modulator, which is represented in Fig. 2, is based on a combination of a Multiple Input Buck Converter, formerly presented in [14], with a linear stage based in wideband Op-Amps. Power sharing between the linear and the switching stage is carried out by the combiner, which is just a pair of Schottky diodes in anti-parallel [19]. In Fig.2 the load resistor R represents the RF PA.

The principle of operation is simple. The switching stage and the linear stage try to set the same voltage across the load. If this happens, the combiner disconnects the linear stage from the load and all the power is provided by the switching stage, with high efficiency. During fast transients, the dynamic of the switching stage is not fast enough, so one of the diodes will become forward biased, allowing the linear stage to provide the current necessary to maintain the desired voltage. If the linear stage is setting the output voltage, there will be an error equal to the knee voltage of the diodes, V_γ.

The switching stage is a Multiple Input Buck converter, as in [14]. In this paper an improved version

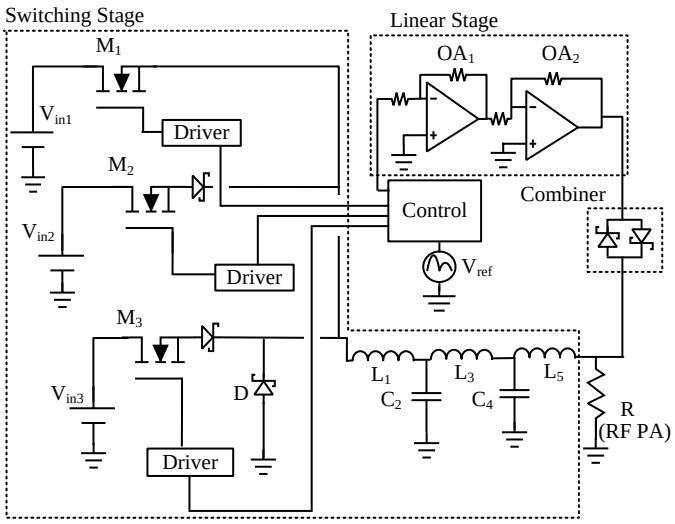


Fig. 2: Schematic of the Envelope Modulator

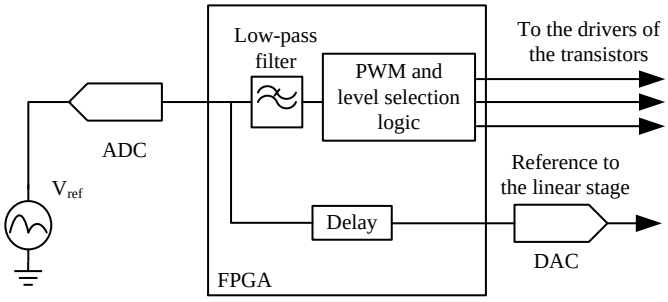


Fig. 3: Control system of the Envelope modulator

with a fifth order output filter is presented. The filter is designed to maximize the bandwidth of the switching stage, while maintaining a low output voltage ripple. An odd order filter is mandatory to make the switching stage behaves as a current source, just as in [19]. The study of higher order filters for the MIBuck converter was done in [20]. A brief summary of this study will be presented in section II-B.

The control system provides the PWM signals which are necessary to generate the output voltage. The control stage also provides the reference voltage (i.e. the envelope waveform to reproduce) to the linear stage. This reference is properly delayed, so both stages try to set the same voltage at the same time. The linear stage operates in closed loop, with a gain equal to the one of the switching stage, thus forcing the output voltage to follow the reference. This control system is fully explained in [19] and summarized in Fig.3. The low pass filter shown in it has a cut-off frequency slightly lower than the cut-off frequency of the output filter of the switching stage (see Fig.2). Since PWM modulation can be seen as a form of sampling with a sampling frequency equal to the switching frequency, this filter avoids the aliasing effects caused when trying to reproduce a signal with a bandwidth higher than half the sampling, thus complying with the Nyquist criterion. The delay is used to synchronize the output voltage of the linear and switching stages.

The strong point of this topology relies in its simplicity. The switching stage operates in open loop in order to maximize its bandwidth. It is supposed that the input voltages are tightly regulated and that the load does not change so much during operation, which seems to be the case of an RF PA operating in saturation or switched-mode. A constant switching frequency eases the task of designing the filter. Precision on the output voltage, up to the knee voltage of the diodes of the combiner, is

obtained via the feedback of the linear stage.

B. Filter design

In a DC/DC converter intended to work as an envelope modulator the role of the output filter is slightly different from the one in a traditional DC/DC converter. Since the latter only has to keep a constant DC voltage at the output of the converter, there are no considerations about the transfer function of the filter, apart from the ones concerning the converter stability when it is working in closed loop. Usually a second order filter is used with the inductor setting the conduction mode (either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM)) and the capacitor is chosen according to the output ripple requirements. However, if a switching DC/DC converter is used as an envelope modulator, the output voltage will be not a constant DC quantity, but a strongly time-varying envelope, with frequency content from the DC to a certain bandwidth ω_{h_max}. Therefore, the role of the filter will be to reject the switching frequency components and the intermodulation products of the switching frequency ω_s and the signal to reproduce [21]. This task has to be performed while keeping the distortion of the signal to reproduce as low as possible. This situation is depicted in Fig. 4. Therefore, a filter with a pass-band with a flat gain response and a flat group delay (in figure 4 the variation of the group delay has been represented) has to be chosen. This filter must also exhibit a good rejection at the switching frequency. In [20] the Butterworth, Legendre, and Bessel filters were studied using a criteria based on the distortion of the signal to reproduce and the step response of the filter. However, here the criteria will be different: it will be the amount of current (and therefore the power) processed by the linear stage during a transient. This will be shown in section II-C.

The switching-stage operates in open-loop and, therefore, the filter has to be designed to remain the operation in CCM in order to maintain the linearity between the duty cycle and the output voltage. The CCM operation of the MIBuck has been fully explained in [14] following the approach presented in [22]. Basically there is a minimum value of L_1 which is:

$$L_{1\_min} = \frac{R}{2 \cdot f_s} \cdot \frac{\left(\sqrt{\lambda_{ij}} - 1\right)^2}{\lambda_{ij} - 1} \tag{6}$$

The parameter λ_{ij} is the ratio between the input voltages V_{ini} and V_{inj} ($\lambda_{ij} = V_{ini}/V_{inj}$). These are the input voltages that are being switched in the MIBuck converter.

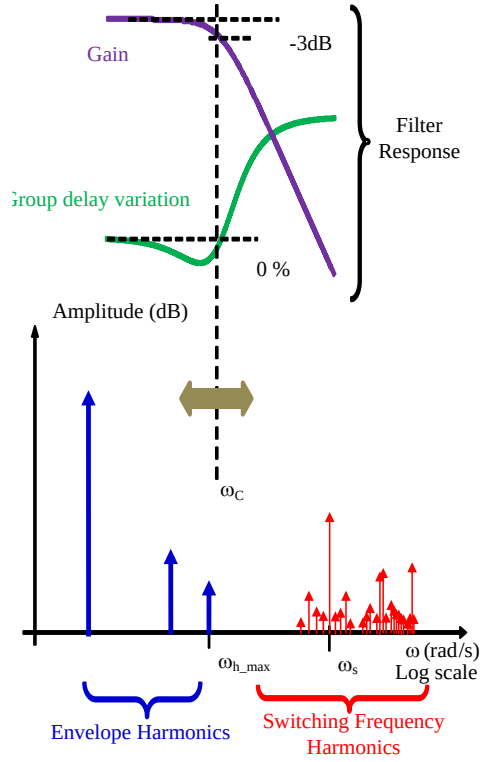


Fig. 4: Role of the filter in an envelope modulator

Parameter R is the load of the converter and f_s the switching frequency. The validity of equation (6) with filters with an order greater then two was discussed in [20]. For values of L_1 above L_{1_min}, $L_1 \geq L_{1\_min}$, the converter will always operate in CCM. However L_1 is determined by the normalization equations of the elements of the filter. These equations relates the elements (inductors and capacitors) of the normalized filter, with a cut-off frequency of 1 rad/s and a load of 1 Ω, with the desired cut-off frequency and load:

$$L_x = \frac{l_x \cdot R}{2\pi \cdot f_c},\ C_x = \frac{c_x}{2\pi \cdot f_c \cdot R} \tag{7}$$

where the l_x and c_x are the inductor and capacitor values found in tables, R the load of the filter and f_c is the cut-off frequency. It is important to note that the filter must be designed to have a null input impedance. This impedance is set by the ON resistance of the MOSFETs and diodes of the switching network. Therefore, proper tables have to be used [23]. In some filters, such as the Bessel filter, the tables sometimes are written for cut-off frequencies different from 1 rad/s so a normalization has to be done. The inductor that will determine the CCM boundary is the first one, L_1. Then, applying equation (7):

$$L_1 = \frac{l_1 \cdot R}{2\pi \cdot f_c}, \tag{8}$$

where l_1 is the normalized value of the first inductor of the filter. By merging equations (6) and (8), rearranging terms and applying that $L_1 \geq L_{1\_min}$ the following expression is obtained:

$$\frac{f_s}{f_c} \geq \frac{\pi}{l_1} \frac{\left(\sqrt{\lambda_{ij}} - 1\right)^2}{\lambda_{ij} - 1}, \tag{9}$$

This equation establishes a ratio between the switching frequency of the converter, f_s and the cut-off frequency of the filter f_c. While the condition represented in 9 is fulfilled the converter will operate in CCM. The worst situation takes place when the converter switches between the lowest input voltage and zero, leading to an infinite value for λ_{ij}. In this case, equation (9) yields:

$$\frac{f_s}{f_c} \geq \frac{\pi}{l_1}. \tag{10}$$

Figure 5 shows the rejection ratio and the CCM/DCM boundary versus the ratio f_s/f_c for the Bessel, Butterworth and Legendre filters. It can be seen how for a ratio f_s/f_c above 2 all the filters guarantee the CCM operation of the converter. Therefore, for rejection ratios above 40 dB, which guarantee a good rejection of the switching frequency, the converter will operate in CCM. The lower the ratio f_s/f_c the lower the switching frequency for a given signal bandwidth, and therefore, the lower the switching losses in the converter. A more detailed analysis on the use of filters with an order higher than two can be found in [24] for the the Buck converter. The results presented in the aforementioned paper are applicable here.

As in [19] the converter must operate as a current source. This can be accomplished by choosing an odd order filter, thus the output element will be an inductor. A fifth order filter will guarantee this current source behaviour while maintaining a low value of f_s/f_c for a given rejection ratio.

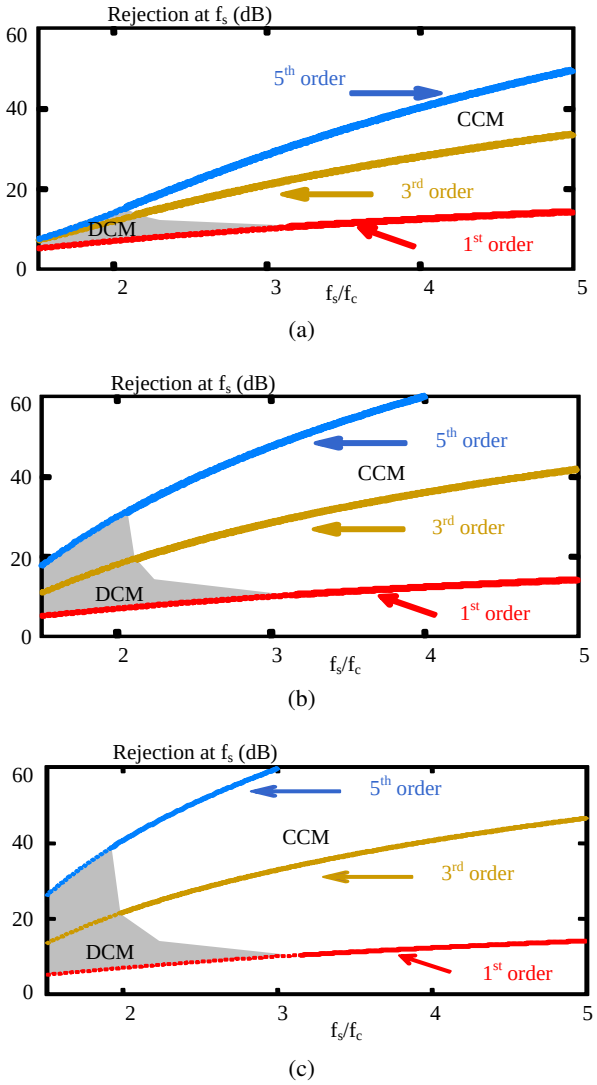


Fig. 5: Rejection Ratio and CCM/DCM boundary for: (a) Bessel filter, (b) Butterworth filter and (c) Legendre filter transfer function

C. Operation and simulations

Figure 6 shows the equivalent circuits for the Envelope Modulator presented in this paper. Figure 6a represents the switching equivalent. The control generates the PWM signals so V_{node} is a square signal that swings between V_{ini} and V_{inj}. The width of the pulses guarantees that:

$$\langle V_{node} \rangle_{switching} = V_{ref}. \tag{11}$$

Therefore an averaged equivalent is shown in Fig. 6b equivalent. The Schottky diodes shown in Fig. 6b has been replaced with their equivalent circuits based on the knee voltage V_γ and ideal diodes in Fig. 6c. The voltage sources V_{ref} represents the desired voltage at the load.

As stated in section II-A, the main idea is that both the switching and the linear stages try to set the same output voltage at the same time. Therefore, the control system generates the adequate PWM pulses at the input of the MIBuck filter so its averaged value in a switching period equals the output voltage of the linear stage. The actual averaging is carried out by the filter of the switching stage. Therefore, if the output voltage of the switching stage equals the one of the linear stage, the latter becomes disconnected from the output and processes no power. This is the situation represented in Fig. 6d. The system will remain in this situation while

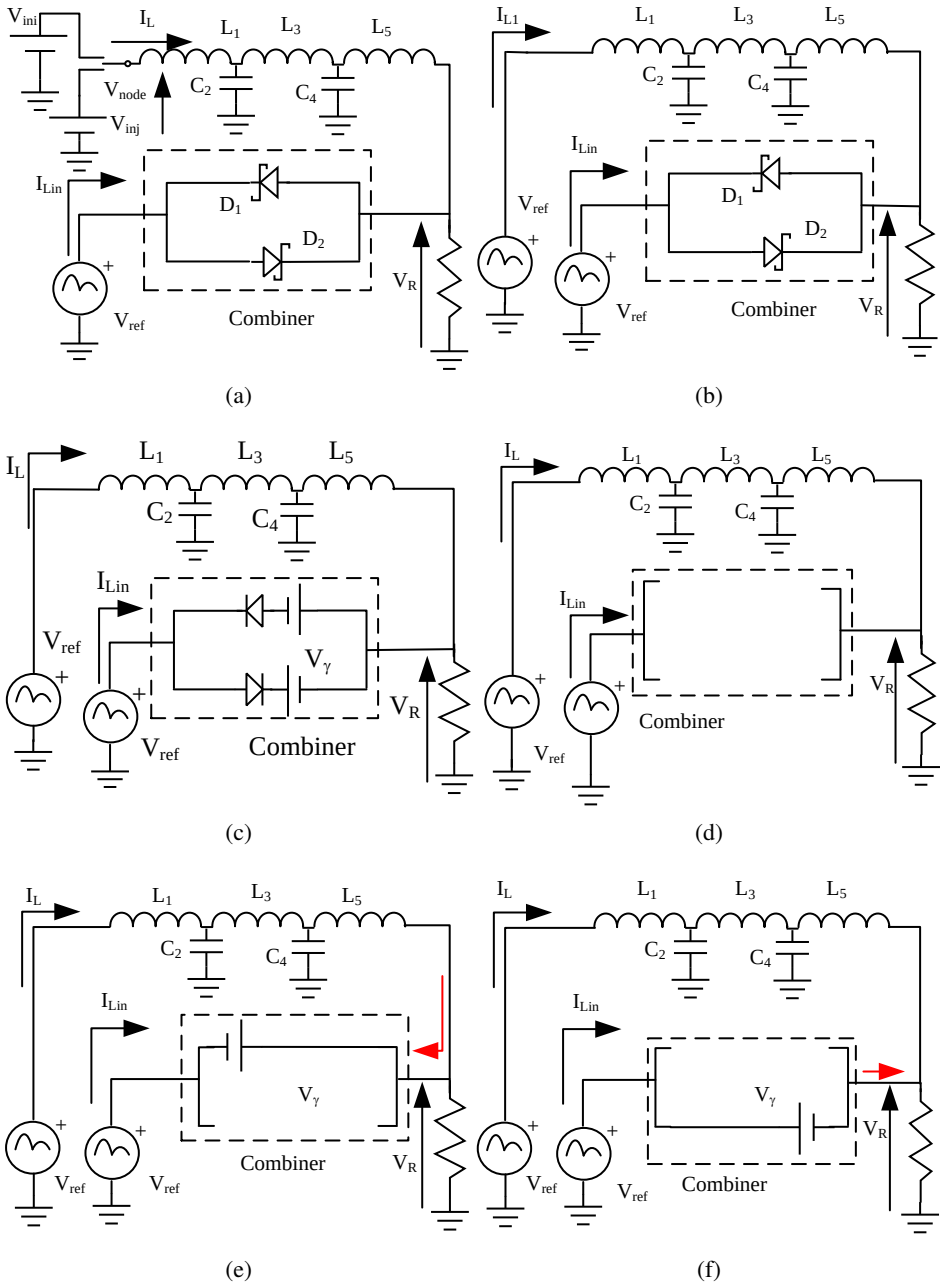


Fig. 6: Equivalent circuits for the combination with the linear stage being: (a) Switching equivalent (b), averaged equivalent with the real Schottky Diodes, (c) the general averaged equivalent (d) disconnected from the load, (e) absorbing the excess of current, (f) providing the necessary current to maintain the desired voltage at the output

the voltage difference between the linear and switching stages is below the knee voltage of the diodes V_γ. Then, the maximum allowable difference between these voltages will be V_γ. This is the desired state, where the switching stage processes all the power and the efficiency will be the highest. This state can only be achieved when the Envelope Modulator is in steady state, reproducing a waveform with a harmonic content well below the cut-off frequency of the output filter. In other cases, such as in fast transients, one of the diodes will become forward biased and the linear stage will set the output voltage. As a consequence, there are two possible situations. The first one is depicted in Fig. 6e. Here, the output voltage of the filter would be higher than the desired one if the linear stage did not exist. Therefore, diode D_1 becomes forward biased and the linear stage sets the voltage on the load to $V_{ref} + V_\gamma$ by absorbing the necessary current. The opposite situation

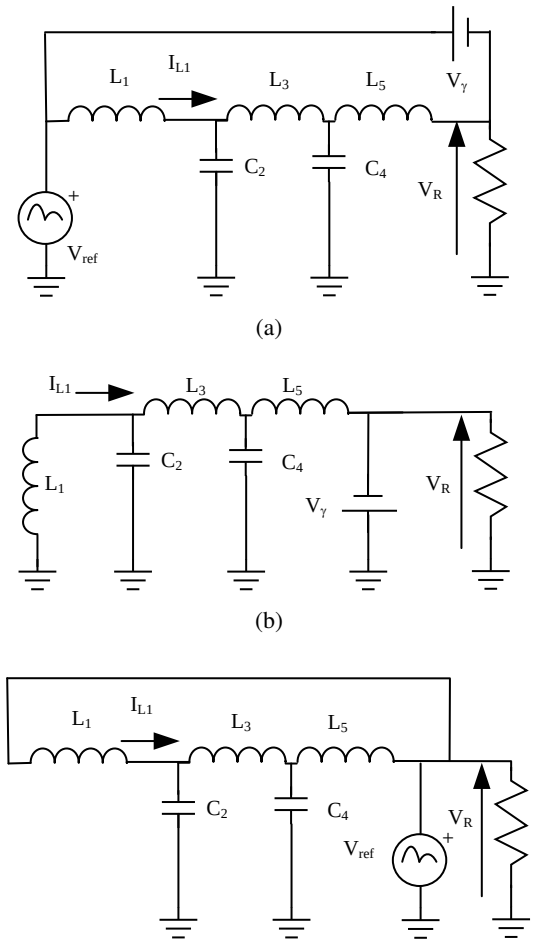


Fig. 7: Equivalent circuit to study the system in the situation depicted in Fig. 6f: (a) Overall circuit, (b) Role of source V_γ and (c) Role of source V_{ref}

is shown in Fig. 6f. In this case the output voltage of the filter would be lower than the desired one if the linear stage did not exist and the linear stage will provide the current necessary to set the voltage $V_{ref} - V_\gamma$ across the load.

In the situations where the linear stage fixes the output voltage, the evolution of voltages and currents on the reactive elements of the filter will be determined by the voltage drop V_γ, and the objective voltage V_{ref}. The equivalent circuit to study how this circuit evolves when the linear stage provides current is shown in Fig.7a. Applying superposition theorem the role of voltages V_{ref} and V_γ can be seen in Fig. 7b and 7c. By reversing the voltage V_γ, this circuit can also represent the situation described by the equivalent in Fig.6e where the linear stage absorbs current.

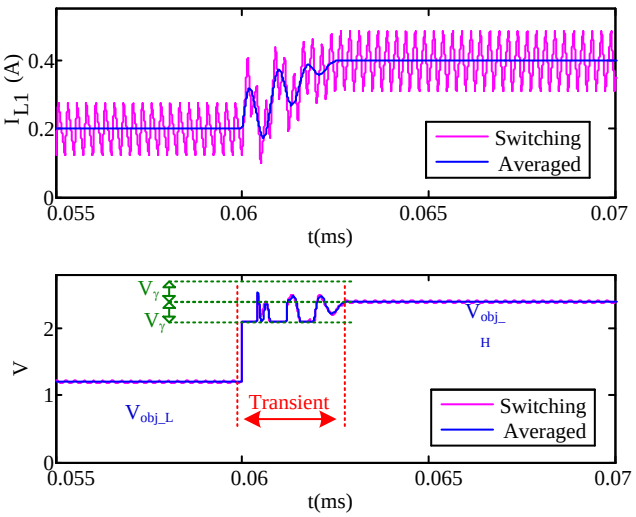


Fig. 8: Operation during a step from V_{obj_L} to V_{obj_H}

In order to clarify the behaviour of the system, an example will be presented using a voltage step in the envelope reference signal V_{ref}. This voltage step will be generated in such a way that the output voltage will swing from V_{obj_L} to V_{obj_H}, as it is represented in Fig.8. In this figure, the waveforms corresponding to both averaged and switched models are represented. The switching frequency being $4\ MHz$ and the filter being a 5^{th}-order Bessel filter with a cut-off frequency of $1\ MHz$. At the beginning of the step the dynamics of the low-pass filter avoids the output voltage of the switching stage to reach the desired value, V_{obj_H}. Therefore, one of the diodes of the combiner (in this case D_2) allows the linear stage to provide enough current to set an output voltage equal to $V_{obj\_H} - V_\gamma$. The evolution of the currents and voltages in the reactive elements of the filter forces the combiner to connect and disconnect the linear stage from the output during the transient (shown as the ripple of the output voltage during the transient period in Fig. 8). During this period the output voltage is limited around $V_{obj\_H} \pm V_\gamma$. Finally, the transient is finished when the average value of the current through the inductor reaches V_{obj_H}/R. In this instant the switching stage sets the output voltage, with a very low output voltage ripple. This simulation and all the simulations presented in this paper were carried out using MATLAB/Simulink models.

The filter chosen for this simulation is a fifth order Bessel filter. In order to determine which filter fits better to this application, the same simulation was carried out using Legendre and Butterworth filters with the same cut-off frequency. Regarding the efficiency, the goal of the system is to minimize the amount of current

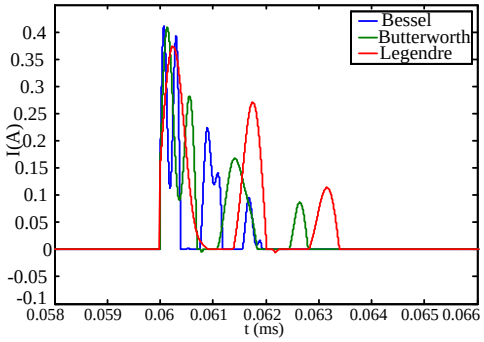


Fig. 9: Current through the linear stage during a step from V_{obj_L} to V_{obj_H}

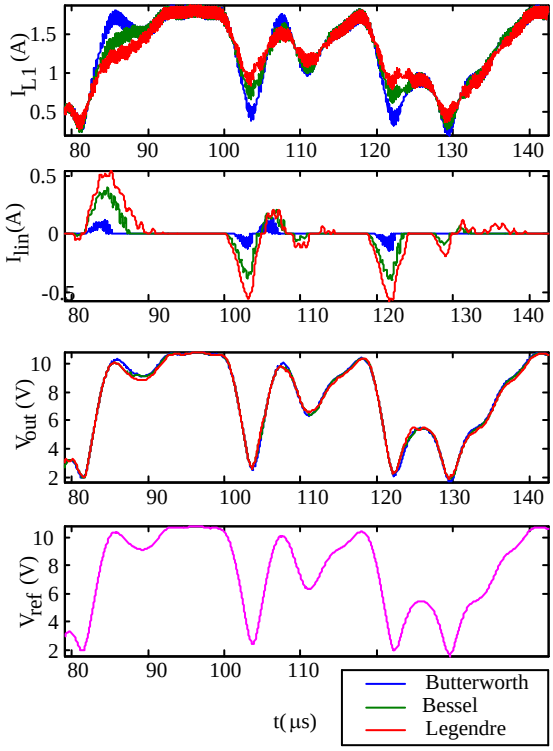


Fig. 10: Simulation of the system with EDGE standard envelope signal

processed by the linear stage. Therefore, the lower the average current processed by the linear stage during the transient, the better the filter. Figure 9 shows the current through the linear stage in the rising edge of the step. It can be seen how the transient is shorter with the Bessel filter than with the other ones.

For this kind of filter the value of f_s/f_c to maintain CCM is 2.0771. The filter has to be adapted to the value of the load, which will be determined by the current demanded from the RF PA to its drain power supply. This behaviour is explained in section III.

The operation of the systems has been simulated with more complex waveforms. The envelope corresponding to the EDGE cell telephony standard is shown in Fig.10. The reference signal, amplified to a similar value to the one of the one of the output signal, is labelled V_{ref} and the output voltage with the different filters is labelled V_{out}. It is apparent how similar they are. However, there are minor differences between the different filters employed (Bessel, Butterworth, Legendre). It can be seen how the current through the linear stage, labelled I_{Lin}, is different to zero in the fast transients. With every filter type, the current through the linear stage is much more lower than the current through the switching stage (labelled I_{L1}), being the power processed by the latter higher as was intended to be. It is easy to see how the minimum current through the linear stage is achieved through the use of a Bessel filter in the switching stage, which is according to the step simulation, as depicted in Fig.9.

III. RF Stage

The RF PA is a Class E amplifier, formerly proposed by the Sokals in [25]. This switched-mode RF power amplifier is able to provide a high efficiency because the transistor turns on at a zero value of its voltage and time-derivative (Zero Voltage Switching, ZVS, and Zero Voltage Derivative Switching, ZVDS, conditions). It has been conceived using a 30 W GaN HEMT device, grown over a SiC substrate, and has been designed to operate in the 770 MHz band. Its bias point is set to $V_{DS} = 28V$ and $V_{GS} = -3.5V$. The resonant network that guarantees Class E operation is adapted to the parasitics of the transistor at this bias point. Following [26], [27], a lumped-element multi-harmonic termination network has been employed, being an open circuit condition presented at the device drain terminal to the second and third harmonic of the excitation frequency. Its schematic is shown in Fig.11. The necessary impedance needed by the Class E operation is synthesized by the network formed by inductor L_{fun} and capacitor C_{fun}. The short circuits at the second and third harmonic, that provide isolation between the synthesized impedance values, are performed by the networks formed by L_{2s} and C_{2s} for the second harmonic and L_{3s} and C_{3s} for the third one. The open circuit termination at the drain is obtained at the third harmonic by the tank formed by L_{3p} and C_{3p}, and at the second harmonic thanks to the introduction of a small inductor L_{2p}. The Envelope Modulator takes the place of the voltage source V_{DS} in Fig.11. In order to improve its dynamic response of it, the capacitors C_{bias2} and C_{bias3} placed in parallel with the source V_{DS} have

been removed. Undesired long-term memory effects due the chokes (L_{bias}) may be reduced if selecting appropriate coils, self-resonating at or close to the carrier frequency, in such a way their reactance to the envelope frequency content may be neglected. L_{in} and C_{in} are used for input matching at the fundamental. The capacitor bank and the resistor, employed in the gate biasing path, help assuring the desired circuit stability, while also providing some protection to the GaN HEMT gate-to-channel junction.

The Class E RF PA is built around the GaN HEMT Transistor CGH35030 from Cree Inc. All the inductors of this RF PA are from the Air Core series, Coilcraft, and the capacitors from the 100A and 100B series, ATC. All the values of inductors and capacitors used in this design are shown in Table I.

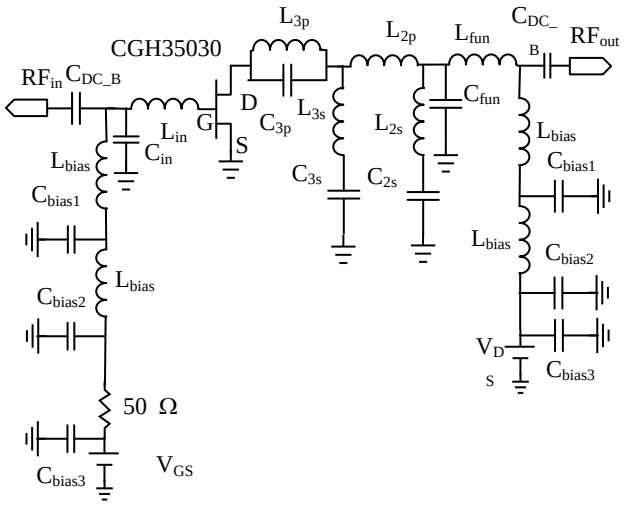


Fig. 11: Schematic of Class E RF PA

TABLE I: Component values in the Class E RF PA schematic (Fig. 11)

Component	Value	Description
C_{DC_B}, C_{bias1}, C_{bias2}	82 pF	ATC 100B
L_{bias}	43 nH	Coilcraft Mini Series
C_{bias3}	10 μF	50 V electrolitic
C_{in}	8.2 pF	ATC 100A
L_{in}	3.85 nH	Coilcraft Micro Series
C_{3p}	0.5 pF	ATC 100A
L_{3p}	5.6 nH	Coilcraft Micro Series
L_{3s}	2.5 nH	Coilcraft Mini Series
C_{3s}	0.4 pF	ATC 100A
L_{2s}	8 nH	Coilcraft Mini Series
C_{2s}	0.5 pF	ATC 100A
L_{2p}	12 ^{o}	Microstrip Tx-line
L_{fun}	8.8 nH	Coilcraft Micro series
C_{fun}	3 pF	ATC 100 A

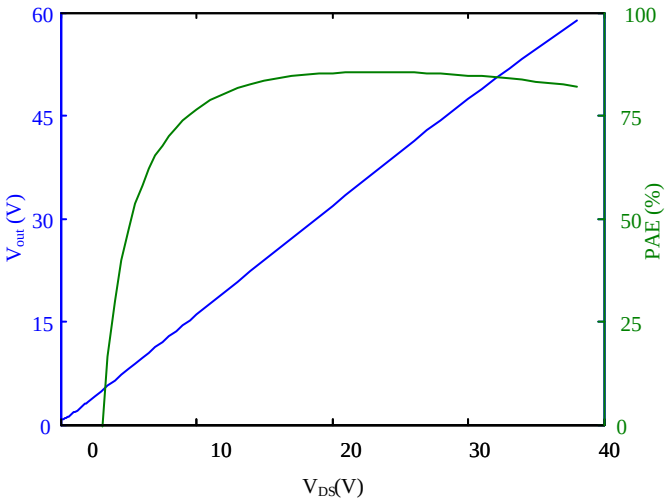


Fig. 12: Measured evolution of output RF amplitude, V_{out}, and PAE versus V_{DS}

Power Added Efficiency (PAE) is a figure of merit in power amplifiers, defining the use of the consumed DC power for creating difference between the input and output power values, It is defined as:

$$PAE = \frac{(P_{RF\_Out} - P_{RF\_In})}{P_{DC}} \tag{12}$$

where P_{RF_Out} is the RF output power, P_{RF_In} the RF input power and P_{DC} the DC power consumed by the RF PA. Its measured evolution with V_{DS} is shown in Fig.12, together with the amplitude of the output RF voltage. A high value of PAE, over 80% for the 12 to 38 V range, has been obtained, together with a nearly linear $V_{DS} - to - AM$ conversion characteristic. Both features would lead to a high average efficiency and low intermodulation products when using this RF PA in a Polar Transmitter.

In order to check how the RF PA behaves as a load to the DC/DC converter, the current demanded by the RF PA was measured while the drain to source voltage V_{DS} was being changed from 0 to 40 V. Voltage V_{GS} was set to $-3.5\,V$ and the RF input power was 24 dBm. Results can be seen in Fig.13, where it can be observed how it is very similar to a resistance of 33 Ω. As this operating point is the desired one for the operation of the RF PA, the filter of the switching stage was designed with this value of load. If a different input power were processed by the RF PA, then the filter would have to be redesigned. In the case of the Hybrid Transmitter, the load presented to the Envelope Modulator does not keep constant when the envelope is clipped to its minimum value, E_{min}, and the RF input signal is amplitude modulated. However,

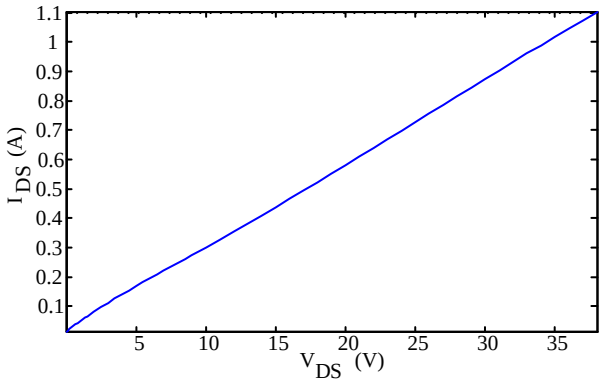


Fig. 13: Behaviour of the RF PA as load to the DC/DC converter

as the most significant envelope variations were handled through the EM, its averaged value did not vary so much from the aforementioned value (41 Ω).

IV. Experimental Results

A prototype of the proposed Envelope Modulator has been built. The switching stage is a MIBuck converter, whose main semiconductors are IPD135 MOSFETs from Infineon and B360 diodes from Diodes Inc. Input voltages to the MIBuck were set to 28, 14 and 7 V. The drivers of the MOSFETs are the EL7156 from Fairchild Semiconductor. Controls signals are transferred from the FPGA to the drivers using IL610 isolators from NVE Corporation. The linear stage was designed using the op-amps THS3001 from Texas Instruments for OA_1 in Fig.2 and LT1230 from Linear Technologies for OA_2 also in Fig.2. The first one provides voltage gain and the second one exhibit a lower voltage gain but provides the current amplification. As both are current feedback amplifiers the resistors selected are chosen to provide the maximum bandwidth with the proper gain, which mean that both of them are configured as inverting amplifiers, as can be seen in Fig.2. The first one, OA_1, has a gain of 24.6 dB with 560 Ω and 33 Ω resistors. The second one OA_2 shows a gain of 9 dB with 620 Ω and 220 Ω. More details about this configuration can be found in [19]. The linear stage voltages were 28 and -1.8 V. The diodes of the combiner were the MBRA130 from On Semiconductor.

The switching frequency of the switching stage was set to 4 MHz, while the cut-off frequency of the filter was set to 1 MHz, thus it complies with (9) keeping the converter operating in CCM. The values of the elements of the filter can be found in table II.

TABLE II: Elements of the filter

L_1 (μH)	C_2(nF)	L_3(μH)	C_4(nF)	L_5(μH)
7,94	4,3	3,95	2,28	0,85

All the control system was implemented in a Virtex-4 FPGA from Xilinx. The necessary ADC was the THS1230 and the DAC was de THS5651 both from Texas Instruments.

Figure 14 shows the response of the Envelope Modulator to a step in its reference voltage. It can be seen the similarities between its output voltage response and the simulation shown in Fig. 8. In this case, the test was done with a 33 Ω resistor in the place of the RF PA. Figure 14 shows how the linear stage handles all the current at the beginning of the waveform. This current decreases while the switching current increases, presenting oscillations due to the evolution of currents and voltages in the elements of the filter. When the system reaches a steady state, all the current is provided by the switching stage, and the linear stage becomes disconnected. The slew-rate achieved is around 300 $V/\mu s$. It is important to remark that with the LT1210, the slew-rate and bandwidth varies with the gain and the load. In this application, the load and the bias are different to the one used in the datasheet [28] and, therefore, the values for the bandwidth and the slew-rate may differ. Measuring the bandwidth of a system used as an Envelope Modulator is a difficult task. The envelopes of the communication signals tend to have a long tail of harmonics which carry very little power. Fortunately, the bandwidth limitations exhibited by the

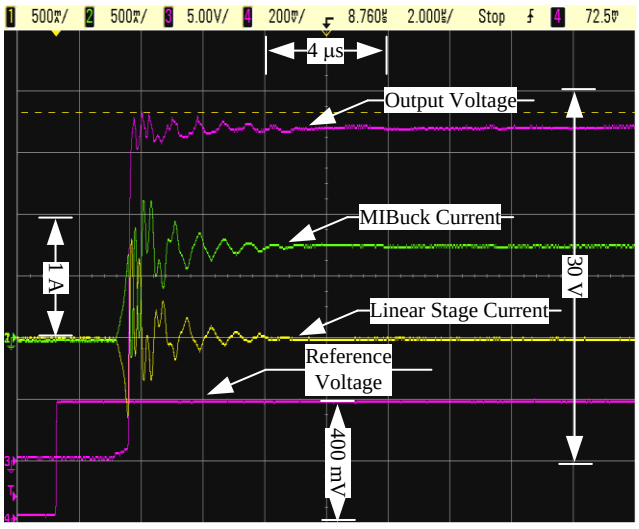


Fig. 14: Step response of the Envelope Modulator

LT1210 match very well with this requirements because the LT1210 bandwidth is higher for lower output power signals. For this reason the best way to verify that the system is capable to work with real communication signals are the tests with the whole system.

The EM and the RF PA were integrated in a test bench to measure various communication standards. This test bench is represented in Fig.15. The envelope and phase signals are generated in a PC running MATLAB and then transferred to two Agilent E4428 ESG vector signal generators. One of them will reproduce the envelope signal, while the other will modulate the RF signal with the phase information. The latter will be pre-amplified by the driver and amplified by the RF PA. The EM will provide the proper voltage to the RF PA according to the envelope generated by the corresponding signal generator. Both generators are synchronized by means of their external trigger functionalities and digitally implemented delays, so the envelope and phase variations take place at the correct time to reconstruct the desired output signal with minimum distortion. The output of the RF PA is then attenuated, downconverted by the E4407B Spectrum Analyzer from Agilent and digitized by the Agilent's VSA 89600 digitizers. The output of these digitizers is sent to the PC, which is running the software VSA 89600. This software is used to analyse the RF output signal.

Cell communications EDGE standard and TETRA emergency communications standard were tested in a pure EER configuration, as their complex envelopes

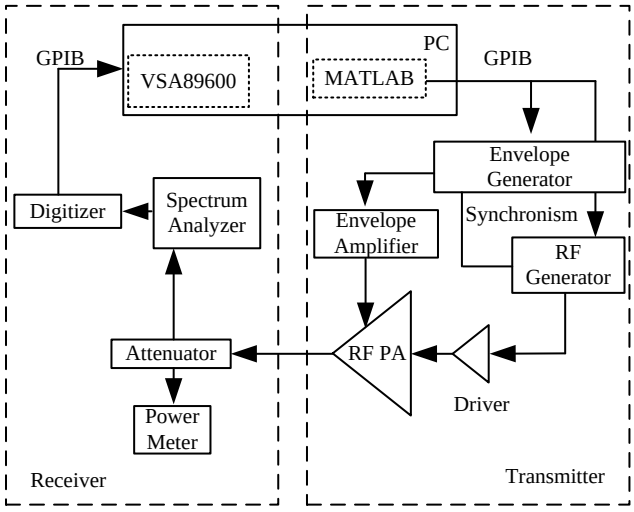
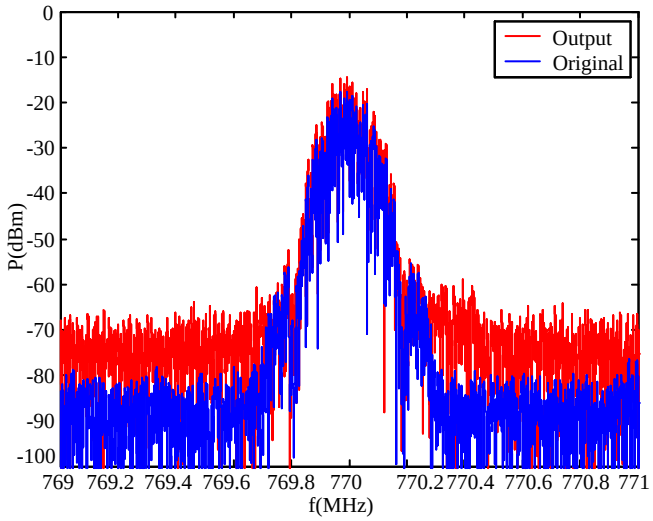
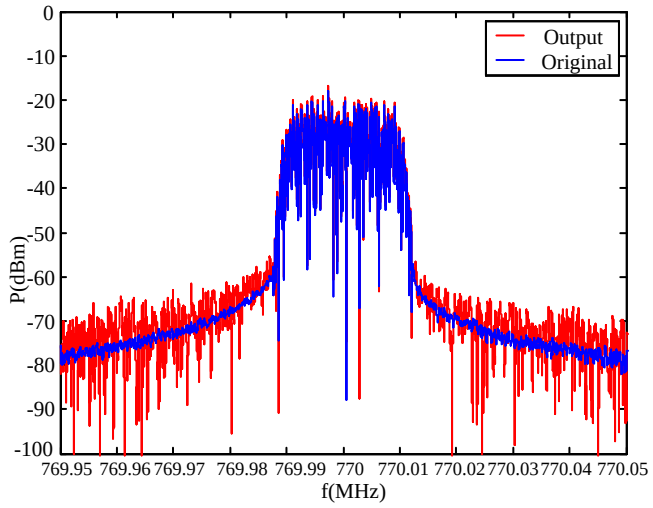


Fig. 15: Experimental set-up for the tests with the RF PA



(a)



(b)

Fig. 16: Experimental results: Spectrum of the (a) EDGE, (b) TETRA standard signal compared to the original

have a hole in the IQ diagram (no nulls). In this way, not only the feed-through effect (associated to the GaN HEMT feedback capacitance, C_{gd}) is circumvented, but also the undesired reduction in average PAE (due to the device low gain when operated close to 0 V) is avoided. Figure 16a shows how the output spectrum using the EDGE standard is very close to the original, almost complying with the regulations (the output signal does not comply with the strict regulations about Adjacent Channel Power Ratio (ACPR) by 6 dBc or 7 dBc, the requirement establishes a -60 dBc margin). By using a more complex predistortion the requirements of the standard can be accomplished, however is a good example from an efficiency point of view. A better result can be seen in Fig. 16b for the TETRA standard.

The spectra were performed using FFT instead of using an Spectrum Analyzer, hence the noisy aspect. Figure 17 shows different waveforms in the system using the TETRA standard signal. It can be seen how the current through the linear stage is around zero most of the time, only processing power in fast transients. Although some glitches in the output voltage appear (see Fig.17) the results in the spectral domain (see Fig.16b) show a good correspondence between the input and the output spectra, which is a good indicator of the quality of the system.

Regarding the efficiency, using the EDGE and TETRA signals the PAE of the system (from DC to RF output power) is around 66.7% and 66.5% respectively, with an RF output power of 9.5 W over a RF load of 50Ω, which is the standard value for RF applications. The input power to the RF PA was 24 dBm (0.25 W). The envelope modulator provides the RF PA with a power of 10.4 W for the EDGE standard operation and 10.3 W for the TETRA standard, with an efficiency (from DC to DC) around 74.7% and 75.2% respectively. The efficiency of the EM strongly depends on the harmonic content of the signal that processes, which is related to the ratio of the power processed by the linear stage. Using the EDGE standard signal, 19.5% of the input power to the EM is demanded by the linear stage while, the remaining 80.5% is demanded by the switching stage. These ratios are slightly different with the TETRA signal, 15.7% and 84.3% being the ratio of the power demanded by the linear stage and the ratio of the power demanded by the switching stage, respectively.

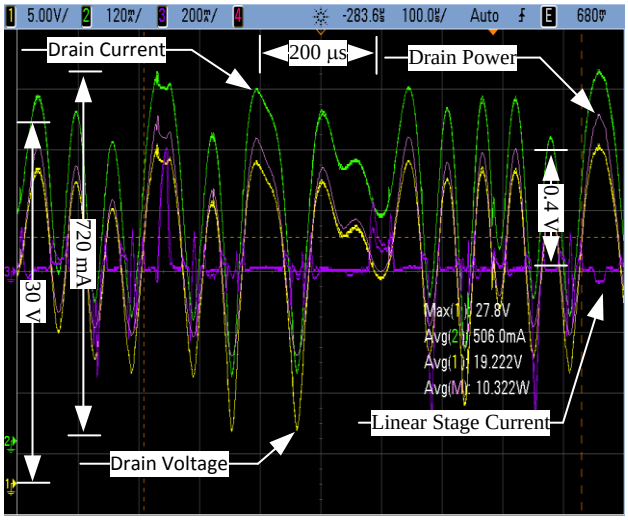


Fig. 17: Waveforms corresponding to TETRA standard signal

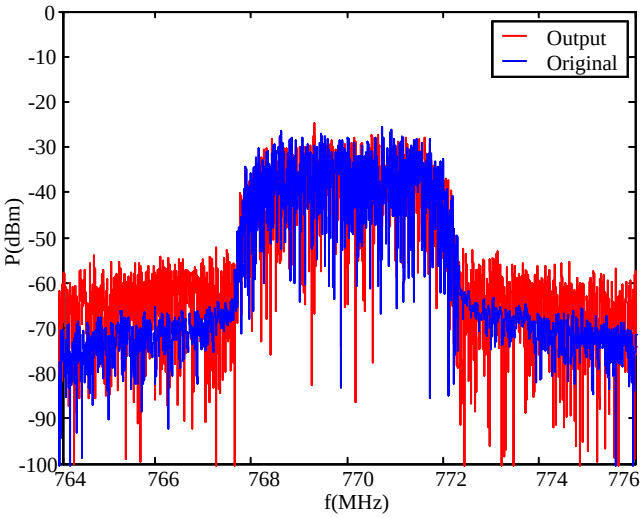


Fig. 18: Spectrum of the WCDMA standard signal compared to the original

The results of the Hybrid Transmitter with one carrier WCDMA cell communication standard signal are shown in Fig.18, where the input and output spectra are compared. As in the other cases, these spectra were performed using FFT instead of an spectrum analyser, hence its noisy aspect. Measurements of the ACPR (*Adjacent Channel Power Ratio*) were carried out using the VSA 89600 software (direct measurements from Fig.18 cannot be used due to the noise provided by the use of the FFT to obtain this plot). This measure was taken according to the requirements regarding WCDMA standard. The value obtained was -50 dBc, while the standard requires -45 dBc. The PAE in this case is lower, around 34.4%, with an output RF power of 2.33 W over a 50 Ω RF load. The average input power to the RF PA is 21 dBm (0.125 W). The EM provides the RF PA with a power of 3.2 W and an efficiency of 49.9%. The linear stage demands 65.8% of the input power to the EM. The remaining 34.2% is demanded by the switching stage. Hence the efficiency is lower than the one corresponding to the EDGE and TETRA examples (the linear stage has to process more power).

V. Conclusions

This paper presents results of a complete high efficiency transmitter based on EER techniques. This transmitter is formed by a switching linear assisted Envelope Modulator and a high efficiency Class E RF Power Amplifier operating at 770 MHz. The presented system can operate in Polar Mode for communication standards like EDGE and TETRA with a PAE around 66%. For signals with a wider bandwidth and more

complex statistics (a higher PAPR value and nulls in the envelope), like WCDMA, the system has to operate in hybrid mode. In this case, as the linear stage has to process more power, the PAE is reduced to a 34.2%. Both of the configurations comply, or are close to comply, with the ACPR requirements imposed by the corresponding standards.

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