Title: **Universal digital controller for Boost CCM power factor correction stages based on current rebuilding concept.**

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Abstract— Continuous conduction mode power factor correction (PFC) without input current measurement is a step forward with respect to previously proposed PFC digital controllers. Inductor volt-second (vs_L) measurement in each switching period enables digital estimation of the input current, but an accurate compensation of the small errors in the measured vs_L is required for the estimation to match the actual current. Otherwise, they are accumulated every switching period over the half line cycle, leading to an appreciable current distortion. A vs_L estimation is proposed, measuring the input (v_g) and the output voltage (v_o). Discontinuous conduction mode (DCM) occurs near input line zero crossings, and is also detected by measuring the drain-to-source MOSFET voltage, v_{ds}. Parasitic elements also cause a small difference between the estimated voltage across the inductor based on input and output voltage

measurements and the actual one, which must be taken into account to estimate the input current in the proposed sensorless PFC digital controller. This article analyzes the current estimation error caused by errors in the on-time estimation, voltage measurements, and the parasitic elements. A new digital feedback control with high resolution is also proposed. It cancels the difference between DCM operation time of the real input current, (T_{DCM}^{g}) and the estimated DCM time (T_{DCM}^{reb}.). Therefore, the current estimation is calibrated using digital signals during operation in DCM. A fast feedforward coarse time error compensation is carried out with the measured delay of the drive signal, and then a fine compensation is achieved with a feedback loop that matches the estimated and real DCM time. Experimental results are shown for a 1 kW boost PFC converter over a wide power and voltage range.

Index Terms— Digital control, Power factor correction, Digital error compensation, Sensorless controller, Boost converter, Continuous conduction mode.

I. INTRODUCTION

Some advantages that motivate the use of digital control in PFC stages include: reduction of discrete components, reduction of size, reduction of sensitivity to parameter tolerances, ease of controller implementation and extension of its performance limits. A resistive sensor is the most commonly used solution for current sampling. The power dissipated by this resistor causes a hot spot in the converter, as is shown in Fig. 1. The first criterion to determine the value of the resistor is often the gain of the amplifier stage (Fig. 2) [1]. Furthermore, the current analog-to-digital converter (ADC) must have a wide bandwidth, increasing the cost in comparison with voltage ADCs. Focused on proposing cost-effective solutions without losing performance, current estimation techniques based on voltage measurements are presented in [2]-[4] and [5] for single-phase and multiphase converter applications, respectively. For PFC applications, several works have been presented to avoid sensors or ADC chips in the converter, simplifying the control circuit. Approaches such as [6], [7] eliminate the voltage sensor in the input or output voltage, [8] uses the diode current as a variable to compute the duty cycle, and [9] and [10] avoid the use of an ADC chip in the

current acquisition, but a current sensor is used. In [11], the current sensor is avoided to detect zero current in a critical mode (CRM) Boost converter.

In continuous conduction mode (CCM) Boost PFC converters, the most recent works proposing current sensorless solutions to obtain power factor correction are [12]-[17]. A PFC without any ADC, using analog comparisons is presented in [12], while a predictive duty-cycle is presented in [13] and [14] with an implementation in a DSP and in an FPGA, respectively. In [15] and [16], the current loop is avoided with a sinusoidal input voltage, while the same approach is improved in [17] under distorted input voltage.

With the above mentioned controllers, high power factor value and low THD of the input current (*THDi*) is achieved in the voltage and power ranges presented for each reference in Fig 3 (according to the experimental results presented in each work). Furthermore, the influence of the parasitic elements and the effects of the non-idealities are not analyzed in detail. The green area represents the goal of this work, that corresponds with the typical range of commercial analog ICs [18] for CCM PFC controllers (universal input voltage range and wide output power range).

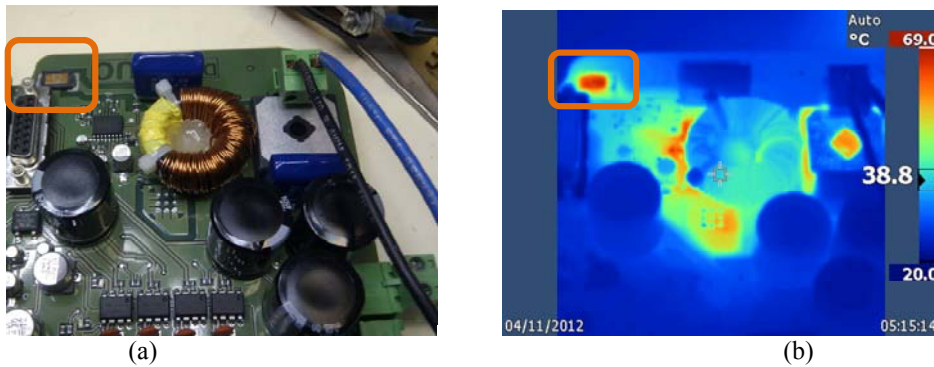(a)   (b)

Fig 1. (a) Traditional PFC converter with current sensor. (b) Thermal image at full load
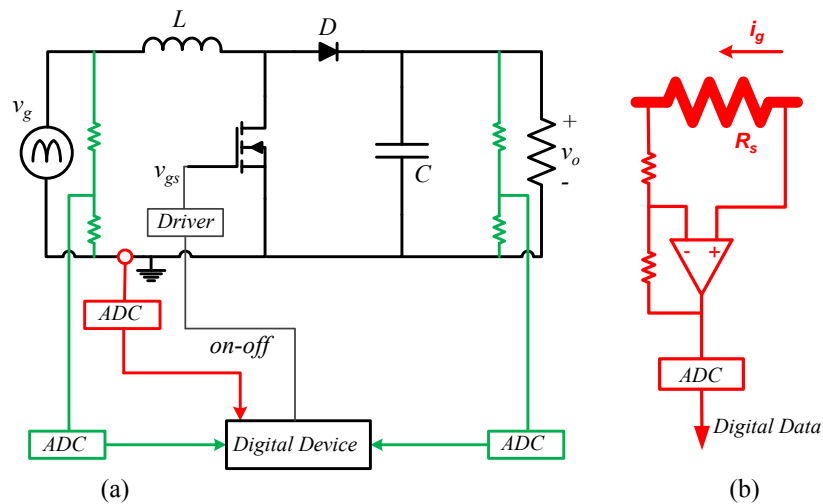
Fig. 2 (a) Typical PFC scheme with digital control and a current sensor. (b) Analog to digital conversion circuit of the input current.
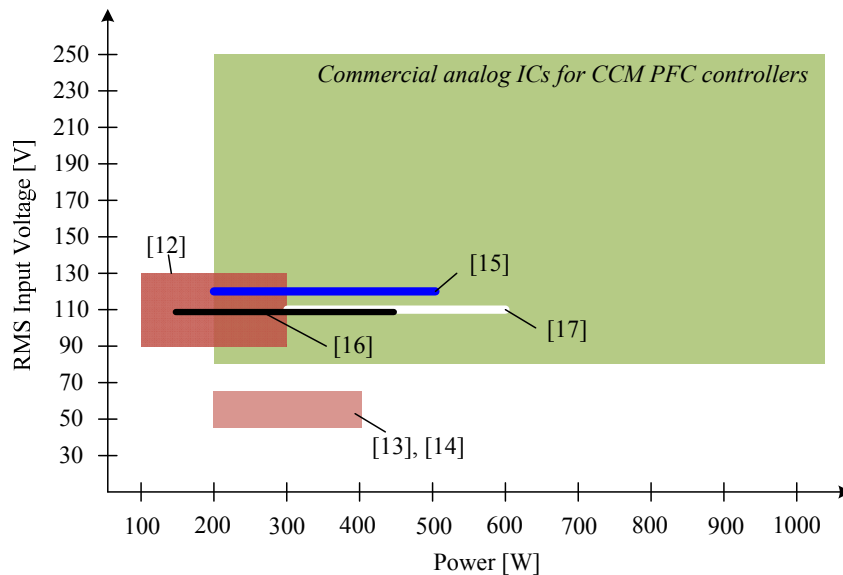

Fig. 3. Input voltage and power range of the recent works in sensorless PFC controllers. The green area represents the goal of this work.

This work is based on the previous ones [19]-[22] where the input current rebuilding concept is used. The variable volt-seconds (vs_L) across the inductor is estimated in each switching period, and the small error (current estimation error) accumulated per switching period over the half line cycle causes current distortion. The effect of the switching delays is presented in [19]. The aim of this work is to:

- Present a fast and coarse feedfoward control to compensate automatically the effect of the switching delays, presented in the previous work [19], measuring these delays every switching period.

- Study and model the influence of the different sources of current estimation error: parasitic elements and errors in the voltage acquisition data.

- Propose a fine low frequency feedback control, with high resolution, to compensate automatically the current estimation error.

This paper is organized as follows. A brief overview is provided in Section II on input current estimation without a current sensor. Section III shows estimation errors due to errors in data capture voltage, which are caused due to tolerances and offsets in the voltage measurement circuits (resistors, ADC, etc.), the differences between the estimated inductance and the real one, the influence of the parasitic elements, and delay in the drive signal. Digital compensation of the errors is described in Section IV, supported with simulation results. An auxiliary circuit for DCM detection is presented in Section V and applied to a new approach for feedback correction of the estimation error in Section VI. Experimental results are presented in Section VII for a 1 kW Boost converter operated over a wide range of input voltages and load power levels.

II. DIGITAL CURRENT ESTIMATION WITHOUT CURRENT SENSOR

Figure 4 shows the simulation block diagram of the current estimator implemented in the digital device, which represents a behavioral model of the boost converter shown at the top of the figure. The input and output voltages of the converter (v_g and v_o) are applied to the inductance L, and define the value of the real input current (i_g), so they have to be measured and quantized to estimate the current value in the digital controller. The hardware scheme of the current estimator is presented in [19]. Digital input and output voltage data (v_g^* and v_o^*) have a LSB resolution (expressed in volts per bit) represented by q_g and q_o, respectively, and given by

$$q_g = \frac{v_g}{v_g^*}\left(\frac{Volts}{bits}\right); \quad q_o = \frac{v_o}{v_o^*}\left(\frac{Volts}{bits}\right) \quad . \tag{1}$$

The inductor voltage is defined by the power converter state (ON-state or OFF-state), being emulated in the current estimator by the signal *on-off,* which drives the power switch Q giving a digital estimated inductor voltage, v_L^*, and a rebuilt inductor voltage, $v_{L,reb}$. Ideally, the ON and OFF times are known because they are generated by the controller. The value of q represents the LSB resolution defined by the

designer. Ideally, $q=q_g=q_o$, but a real analog-to-digital conversion causes a small difference between them:

$$q_g = q(1 - \varepsilon_g), \quad q_o = q(1 - \varepsilon_o) \tag{2}$$

being ε_g and ε_o the percentage error of the input and output analog-to-digital conversions, respectively.
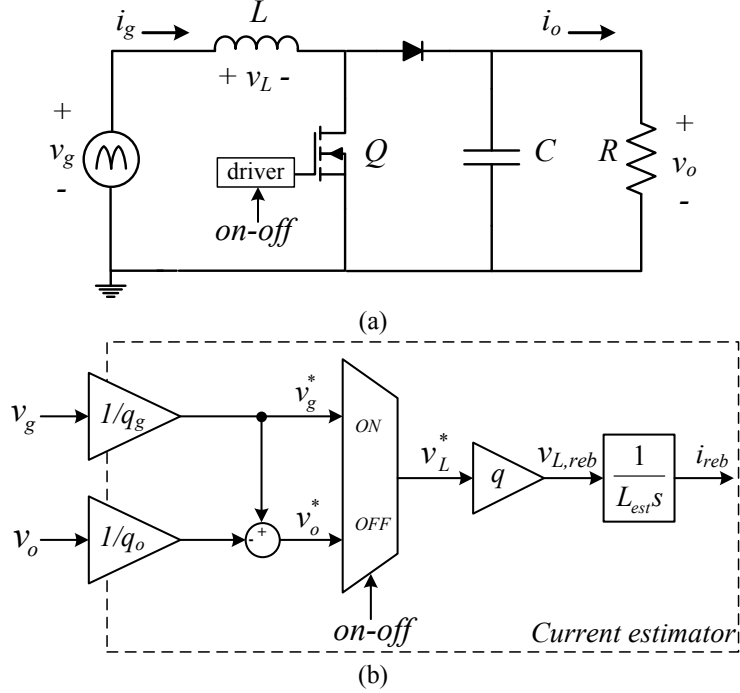

(a)

(b)

Fig 4. (a) Basic model of the boost converter (b) Boost converter current estimator

Theoretically, the inductance L, is known, but tolerances, temperature, switching frequency and the inductor current value depending on the core material cause a difference between the estimated value of the inductance (L_{est}) and the real one. The inductor is modeled as an integrator with a gain equal to the inverse of its inductance, whose output is the digitally rebuilt (estimated) input current i_{reb}. This signal, i_{reb}, is used in the PFC current loop instead of the real i_g.

TABLE I. LIST OF CORRESPONDENCE BETWEEN THE ANALOG AND THE DIGITAL VARIABLES

		Real	Estimated	Units
Inductor voltage	ON	$v_L = v_g$	$v_{L,reb} = \dfrac{v_g}{q_g}q$	[V]
	OFF	$v_L = v_g - v_o$	$v_{L,reb} = \left(\dfrac{v_g}{q_g} - \dfrac{v_o}{q_o}\right)q$	[V]
Inductance value		L	L_{est}	[mH]
ON-time		t_{on}	t_{on}^*	[seconds]
Input current		i_g	i_{reb}	[A]

	ON-state	OFF-state
Real input current (i_g [A])	$\Delta i_g = \dfrac{v_g}{L} t_{on}$	$\Delta i_g = \dfrac{v_g - v_o}{L}(T_{sw} - t_{on})$
Rebuilt input current (i_{reb} [A])	$\Delta i_{reb} = \dfrac{v_g q}{L_{est}} t_{on}^*$	$\Delta i_{reb} = \dfrac{(v_g^* - v_o^*)q}{L_{est}}(T_{sw} - t_{on}^*)$

Table I shows the correspondence between the analog variables (real variables in the converter) and their corresponding digitally estimated variables expressed in the same units. These variables define the value of i_g and i_{reb} according to the expressions presented in Table II, where Δi_g and Δi_{reb} are the peak-to-peak current ripple of the real and rebuilt input current, respectively.

If analog and digital variables are equivalent, with $v_g = v_g^* q$, $v_o = v_o^* q$ with $q = q_g = q_o$, $L = L_{est}$ and $t_{on} = t_{on}^*$, both currents agree ($i_{reb} = i_g$), and the waveforms are as presented in Fig. 5, where $i_{reb}[k]$ represents the estimated current in the clock cycle k, and $i_{reb}^-[j]$ and $i_g^-(jT_{sw})$ the estimated and real current at the end of the switching cycle j (valley values), respectively. In this situation, there is no current estimation error, defined as the difference between i_g and i_{reb} expressed in amps $i_{error} = i_g - i_{reb}$, and therefore i_{reb} corresponds with an accurate quantization of i_g in this case.
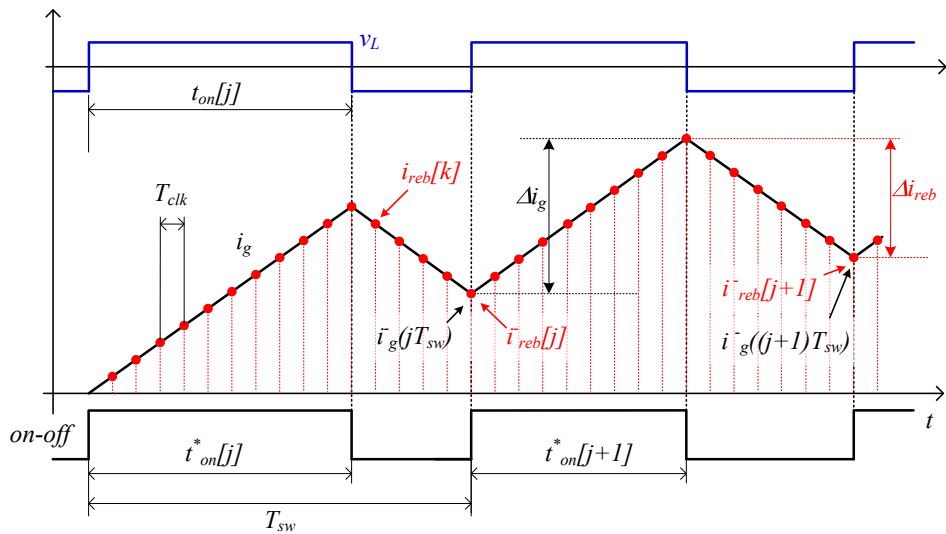

Fig. 5. Digital signal $i_{reb}[k]$, compared with the analog real input current i_{in}, under ideal conditions. The *on-off* signal is the output of the digital device and v_L the analog inductor voltage.

At the beginning of the half line cycle, it is fulfilled that $i_{reb}=i_g=0$. Since the input current is not measured, the line zero-crossings are the only points where the real current is known.

Small errors in the digital variables compared with the analog (Table I) cause a current estimation error in each switching period j. Main current estimation errors are due to:

- Voltage data errors due to the tolerances of the voltage dividers, noise, offset, quantization process or non-linearity of the ADCs ($v_g \neq v_g^* q$ and/or $v_o \neq v_o^* q$ and/or $q_g \neq q_o \neq q$),

- the difference between the estimated inductance (L_{est}) and the real one (L), so in this case ($L \neq L_{est}$),

- the influence of the parasitic elements (R_L, R_{on}, R_D, V_D)

- the drive signals' delays ($t_{on} \neq t_{on}^*$)

All of these errors are described separately in Section III, where the current estimation error caused by these different situations is modeled.

III. MODELING THE CURRENT ESTIMATION ERRORS

To simulate the effect of the different causes of error, and make a first validation of the model, the block presented in Fig. 4 has been built in MATLAB/Simulink® and PLECS®. In this work only the switching converter has been carried out with PLECS®, and a behavioral control algorithm has been described in Simulink, as is shown in Fig. 6.
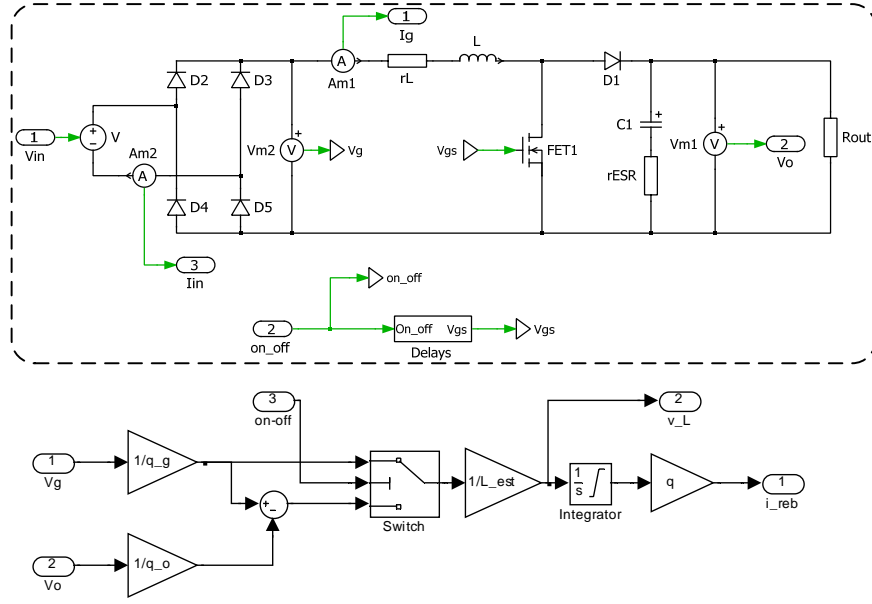
Fig. 6. Simulations Blocks in Simulink with PLECS toolbox. Bottom: PLECS subcircuit in Simulink with the current estimator. Top: Boost converter in PLECS with a block to simulate the drive signal delays

The values of the real input current i_g and the estimated input current i_{reb}, in CCM at the end of a switching period j, $i_{in}^-(jT_{sw})$ and $i_{reb}^-[j]$ respectively, are defined by expressions (3) and (4) according to Fig. 7 and the current estimator (Fig. 4 and 6)

$$i_g^-(jT_{sw}) = i_g^-((j-1)T_{sw}) + \frac{T_{sw}}{L}\{v_g[j] - v_o[j]d'[j]\} \quad , \quad (3)$$

$$i_{reb}^-[j] = i_{reb}^-[j-1] + \frac{T_{sw}}{L}\left\{\frac{v_g[j]q}{q_g} - \frac{v_o[j]q}{q_o}d'[j]\right\} \quad , \quad (4)$$

where ($1-d[j]$) is notated as $d'[j]$, and constant voltage values are assumed over the switching period j. Therefore, the current estimation error, defined as $i_{error} = i_g - i_{reb}$, is evaluated at the end of the switching period, being the difference between (3) and (4), and given by (5) for a switching period n

$$i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_g[j]\left(1 - \frac{q}{q_g}\right) - v_o[j]\left(1 - \frac{q}{q_o}\right)d'[j]\right\} \quad . \quad (5)$$

The error from (5) can be expressed in function of i_{reb}

$$i_{error}[n] = i_{reb}[n] \times \left(\frac{q_g}{q} - 1 \right) + \frac{T_{sw}}{L} \sum_{j=0}^{j=n} \left\{ v_o[j]d'[j]\left(\frac{q_g}{q_o} - 1 \right) \right\} \quad , \tag{6}$$

and it is possible to define the value of the real input current in the switching cycle *n*, as

$$i_g[n] = i_{reb}[n] \times \frac{q_g}{q} + \frac{T_{sw}}{L} \sum_{j=0}^{j=n} \left\{ v_o[j]d'[j]\left(\frac{q_g}{q_o} - 1 \right) \right\} \quad . \tag{7}$$

Both expressions, (6) and (7) have two different terms, the first one defines a current proportional to i_{reb}, which is the variable controlled by the PFC controller, so it has a sinusoidal shape. Therefore, the first term does not create distortion (harmonics) in i_g. The second term is not sinusoidal, causing a current distortion and decreasing the power factor value. It can be seen how this current is non-zero when $q_g \neq q_o$. Figure 8 shows the simulated waveforms of the currents i_{reb} and i_g at the top of the figure, and the simulated current error $i_{error,sim}$ compared with the modeled error defined by (6), i_{error}, when $q_g \neq q_o \neq q$,
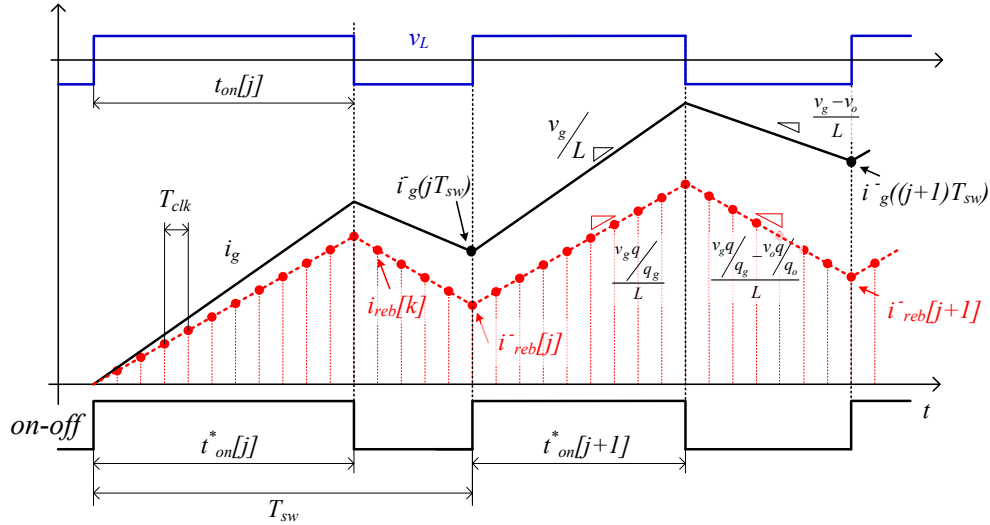

Fig. 7. Digital estimated current $i_{reb}[k]$ compared with the analog real input current i_{in} under errors in data capture voltage across the inductance when $q_g \neq q_o \neq q$. The *on-off* signal is the output of the digital device and v_L the analog inductance voltage.
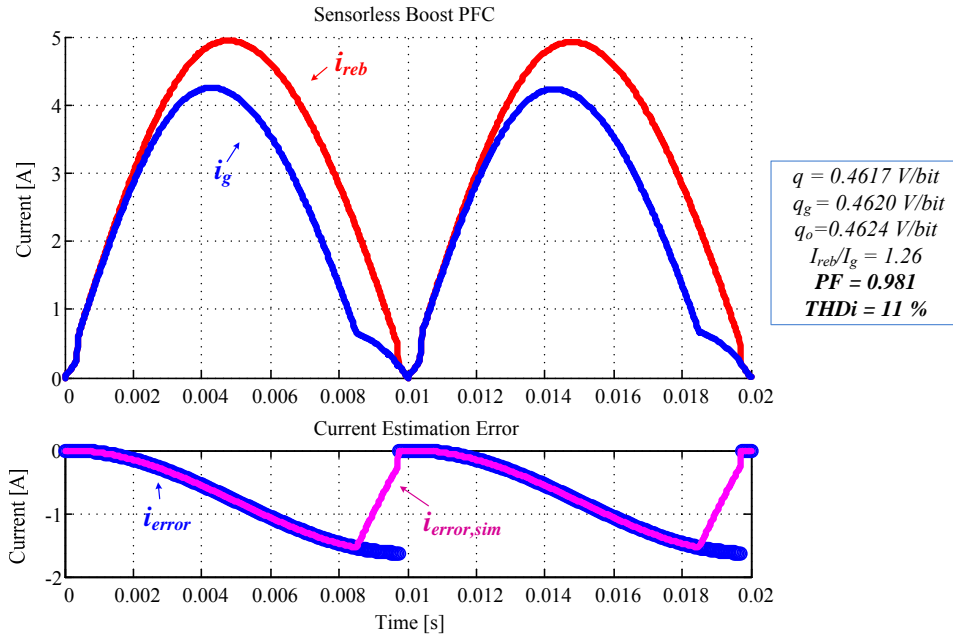
Fig. 8. Steady state simulated waveforms with the Simulink/PLECs model of the system with V_g=230 V_{rms}, V_o=400 V_{dc}, P_o=640 W, f_{sw}=72 kHz, L=1mH and C=220 μF when q=0.4617 V/bit, q_g=0.4620 V/bit, q_o=0.4624 V/bit

The second cause of error analyzed in this work is the current estimation that appears due to the difference between the real inductance (L) and the estimated L_{est}, ($L \neq L_{est}$). The behavior of the sensorless boost converter is shown in Fig. 9 in the switching periods j and $j+1$ when $L \neq L_{est}$ and $q_g = q_o = q$, i.e. considering the inductance error only.
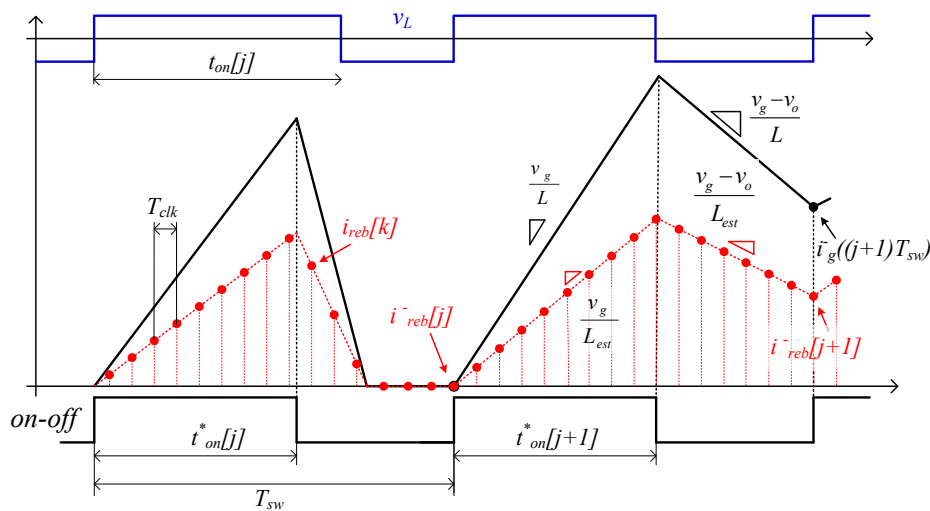

Fig. 9. Digital estimated current i_{reb} compared with the analog real input current i_{in}, when the estimated inductance value L_{est} is higher than the real L. The on-off signal is the output of the digital device, and v_L the inductance voltage.

According to Fig. 9, the current values are defined at the end of the switching period j, by

$$i_g^-(jT_{sw}) = i_g^-((j-1)T_{sw}) + \frac{T_{sw}}{L}\{v_g[j] - v_o[j]d'[j]\} \quad , \tag{8}$$

$$i_{reb}^-[j] = i_{reb}^-[j-1] + \frac{T_{sw}}{L_{est}}\{v_g[j] - v_o[j]d'[j]\} \quad . \tag{9}$$

Comparing (8) and (9), the relation between i_{reb} and i_g yields to expressions (10) and (11) for i_{in} and i_{error}, respectively. As it has been addressed before, i_{reb} is the variable controlled by the PFC control algorithm, so it has a sinusoidal shape (proportional to the input voltage). Considering L constant over the line cycle, i_{in} is sinusoidal too, and no current distortion appears despite the current estimation error

$$i_g = i_{reb} \times \frac{L_{est}}{L} \quad , \tag{10}$$

$$i_{error} = i_{reb} \times \left(\frac{L_{est}}{L} - 1\right) \quad . \tag{11}$$
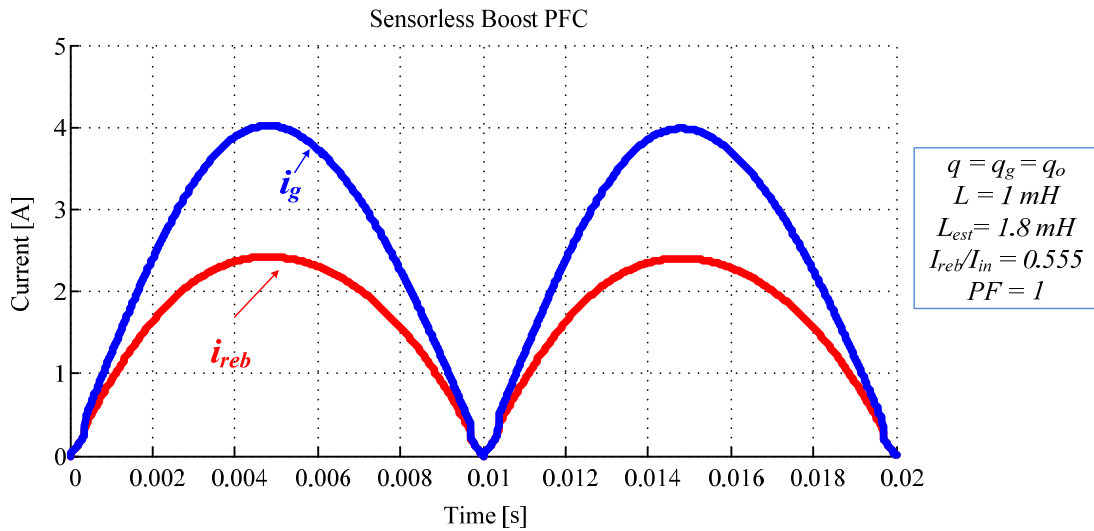

Fig. 10. Steady state simulated waveforms with the Simulink/PLECS model of the system with V_g=230 V$_{rms}$, V_o=400 V$_{dc}$, P_o=640 W, f_{sw}=72 kHz, L=1mH and C=220 µF when L_{est}=1.8 mH V/bit, $q=q_g=q_o$

At this point, it can be seen that the difference between q_o and q_g causes current distortion and decreases the PF value because it means a difference between the V/bit resolution in the ON-state and in the OFF-state, and consequently, a difference in the A/bit also. So, to analyze the behavior of the PFC

controller with the current estimator it can be considered $q=q_g$ and $L_{est}=L$, and the current error, accumulated in the n switching period, is defined by

$$i_{error}[n] = \frac{T_{sw}}{L} \sum_{j=0}^{j=n} \left\{ v_o[j]d'[j]\left(\frac{q_g}{q_o}-1\right)\right\} \qquad .$$

(12)

The last cause of current distortion analyzed in this work is the influence of the parasitic elements. Figure 11 shows the model of the boost converter with parasitic elements, being R_L the effective series resistor of the inductor, V_D and R_D the forward voltage at zero current and the ON-state resistor of the power diode, and R_{on} the MOSFET on-resistance.
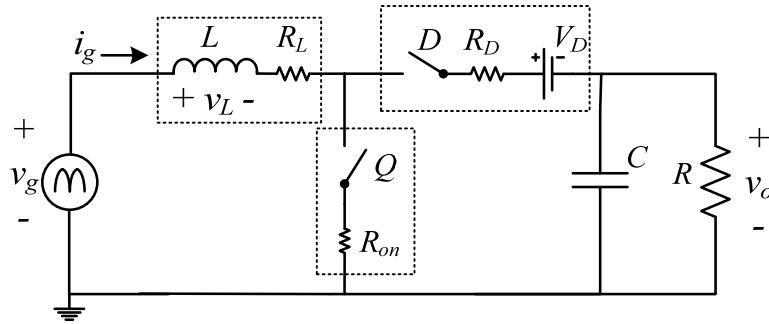

Fig. 11. Boost converter diagram with parasitic elements.

$$v_L = \left| \begin{array}{ll} v_g - \left(R_L + R_{on}\right)i_g & \text{if } ON-state \\ v_g - \left(R_L + R_D\right)i_g - V_D - v_o & \text{if } OFF-state \end{array} \right.$$

(13)

The controller varies the duty cycle d such that the average input current over the switching period, $\langle i_g \rangle = v_g / R_e$, where the emulated resistance R_e is chosen by the controller to obtain the desired dc output voltage. By solving the volt-second balance in L, assuming the small ripple approximation,

$$\langle v_g \rangle - \langle v_o \rangle (1-d) = R_L \langle i_g \rangle + R_{on} \langle i_g \rangle d + R_D \langle i_g \rangle (1-d) + V_D (1-d) \qquad .$$

(14)

Substituting $\langle i_g \rangle = v_g / R_e$ in (14), it is possible to solve the command d given by the PFC controller to obtain a sinusoidal current [23]

$$d = \frac{v_g - (R_L + R_D)\dfrac{v_g}{R_e} - V_D - v_o}{(R_{on} - R_D)\dfrac{v_g}{R_e} - V_D - v_o} \quad . \tag{15}$$

Defining $\langle v_{par} \rangle$ as the average voltage drop across the parasitic elements, in each switching period,

$$\langle v_{par} \rangle = -R_L \langle i_g \rangle - R_{on} \langle i_g \rangle d - R_D \langle i_g \rangle (1-d) - V_D(1-d) = v_o(1-d) - v_g \quad , \tag{16}$$

and substituting (15) in (16),

$$\langle v_{par} \rangle = v_g \left(\frac{v_o(R_{on} + R_L - R_e)}{v_g(R_{on} - R_D) - (V_D + v_o)R_e} - 1 \right) \quad . \tag{17}$$

Figure 12 shows the $\langle i_g \rangle$ and $\langle i_{reb} \rangle$ waveforms when the estimated volt-seconds across the inductor are less than the actual ones due to the non-compensation of the parasitic effects with $V_g = 230$ V$_{rms}$, $V_o = 400$ V$_{dc}$, $P_o = 640$ W, $f_{sw} = 72$ kHz and reactive components $L = 1$ mH, and $C = 220$ μF. The parasitic elements are $R_L = 0.3$ Ω, $R_D = 0.08$ Ω, $V_D = 1.8$ V, $R_{on} = 0.18$ Ω. These values are obtained in the datasheets of the RHRP860 Fairchild Power Diode and the IRFP27N60K International Rectifier Power MOSFET, the switching devices used in the laboratory prototype. It can be observed how due to the current estimation error, i_g is not sinusoidal, with PF=0.728 and $THDi$=49 %.
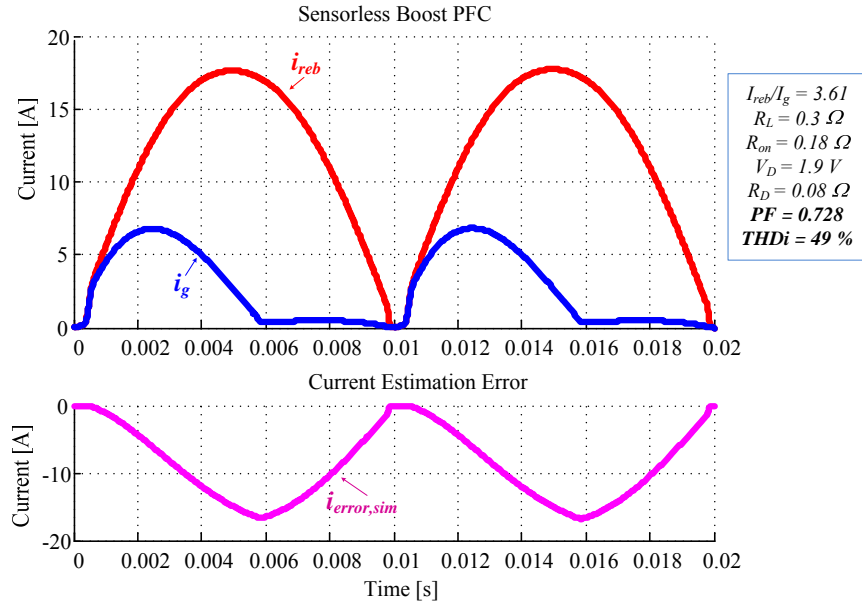
Fig. 12. Simulated current waveforms without consideration of the parasitic elements influence. Top: Real and rebuilt input current. Bottom: Simulated current estimation error

An additional error in the estimated volt-seconds applied to the inductor is caused by time errors and is addressed in [19], where it is concluded that they are mainly due to the difference between the ON-time applied in the real converter (t_{on}) and the estimated ON-time, t_{on}^*. The effect of this time error is shown in Fig. 13, defining $\Delta t_{on}[j] = t_{on}[j] - t_{on}^*[j]$ as the on-time modification in the switching period j,

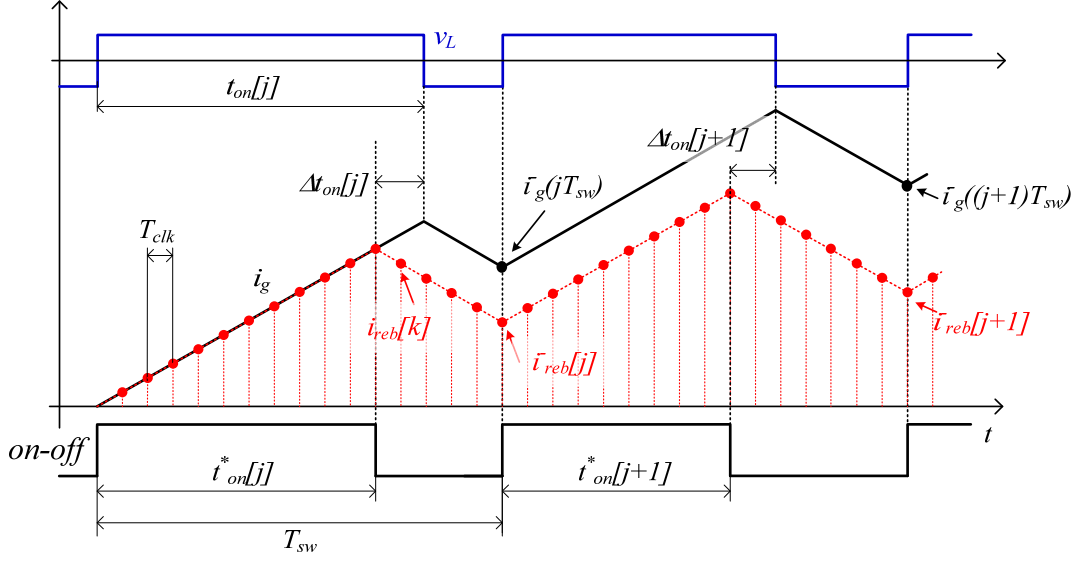$$i_{error}[n] = \sum_{j=1}^{j=n} \frac{v_o[j]}{L} \Delta t_{on}[j] \quad . \tag{18}$$

Fig. 13. Digital signals estimated current $i_{reb}[k]$ compared with the analog real input current i_g, with a on-time modification Δt_{on} for the switching periods j and $j+1$. The *on-off* signal is the output of the digital device and the inductor voltage, v_L

IV. DIGITAL CORRECTION OF THE CURRENT ESTIMATION ERRORS

Two compensation strategies, working at the same time, are presented in this section. The first one is time compensation, presenting an improvement in comparison with the previous work [19]. The on-time error $\Delta t_{on}[j]$ is measured every switching period and it is compensated by accounting for it when the digital circuit calculates the required on-time in every switching period. In this case, as is presented in [20], an auxiliary circuit, which includes a resistor divider and a signal diode, is used to detect the drain-to-source voltage drop across the power MOSFET and obtain the digital signal (v_{ds}^{dig}) which indicates the real ON-OFF transitions in the boost converter, as is presented in Fig. 14.

The digital controller compares the *on-off* with v_{ds}^{dig} to measure the ON-time modification every switching period ($\Delta t_{on}[j] = \Delta t_{on-off}[j] - \Delta t_{off-on}[j]$) in terms of clock periods of the digital circuit.
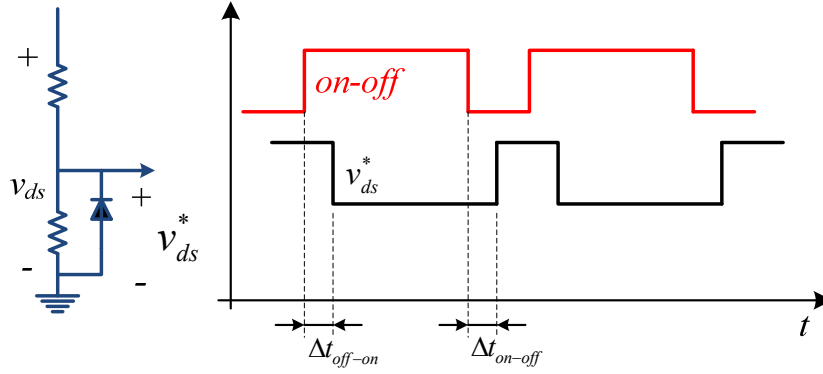
Fig. 14. Auxiliary circuit to adapt the drain-to-source voltage as a digital signal. Comparison with the *on-off* signal and the drive signal's delays $\Delta t_{on\text{-}off}$ and $\Delta t_{on\text{-}off}$

This strategy constitutes a coarse and fast feedforward compensation of the volt-second/current errors caused due to time errors. The resolution of the Δt_{on} measurement depends on the clock period of the digital device and the minimum error is $\pm T_{clk}/2$ [22]. For the Boost parameter presented before and a clock period of 10 ns, ($\pm T_{clk}/2 = \pm 5$ ns) causes a current error accumulated in the last switching period n_u of the half line cycle of, $i_{error}[n_u] = \pm 1.40$ A, where $n_u = f_{sw}/(2f_u)$.

The second error compensation strategy is based on the estimation of the inductor voltage drop by modifying the current estimator block presented in Fig. 4. The new approach is presented in Fig. 15, introducing the digital signal v_{dig} which modifies the output voltage data in the current rebuilding algorithm.
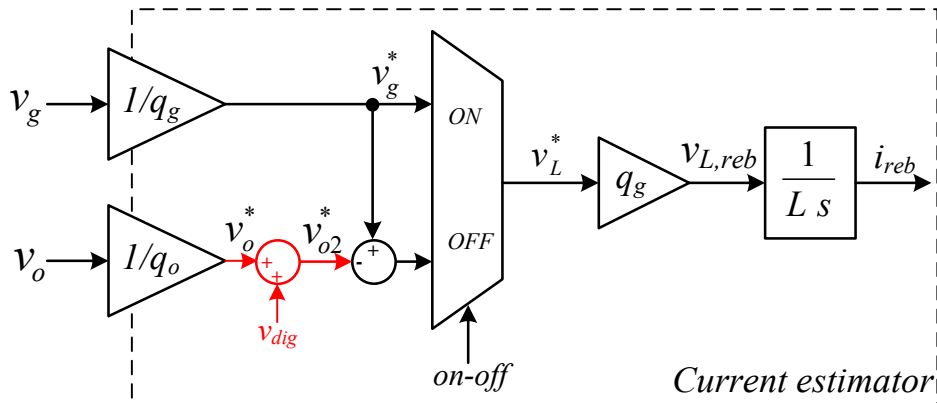

Fig. 15. Behavioral model of the current estimator when the current estimator error is compensated modifying only the output voltage data.

The signal v_{dig} adds to v_o an average value in each switching period expressed in volts ($q=q_g$), given by

(19):

$$\left\langle v_{dig} \right\rangle = -v_{dig} q_g (1-d) \tag{19}$$

If it is considered only the effect of the parasitic elements, the value of v_{dig} that compensates this effect is obtained comparing (16) and (18) to assure $\left\langle v_{par} \right\rangle = \left\langle v_{dig} \right\rangle$, obtaining:

$$v_{dig} = \frac{1}{q_g} \frac{v_o (R_{on} + R_L) + V_D R_e - v_g (R_{on} - R_D)}{R_e - (R_{on} + R_L)} \tag{20}$$

It can be observed how expression (20) describes a waveform almost constant over the line cycle, neglecting the output voltage ripple $v_o \approx V_o$, and approximating $R_{on} \approx R_D$. Figure 16 shows the simulation result with $V_g = 230$ V$_{rms}$, $V_o = 400$ V$_{dc}$, $P_o = 640$ W, $f_{sw} = 72$ kHz and reactive components $L = 1$ mH, and $C = 220$ μF. The values of the parasitic elements are $R_L = 0.3$ Ω, $R_D = 0.08$ Ω, $V_D = 1.8$ V and $R_{on}=0.18$ Ω. The resulting power factor, with this first approximation, is 0.991 with a *THDi* = 5.41 % improving the results obtained in Fig. 12).
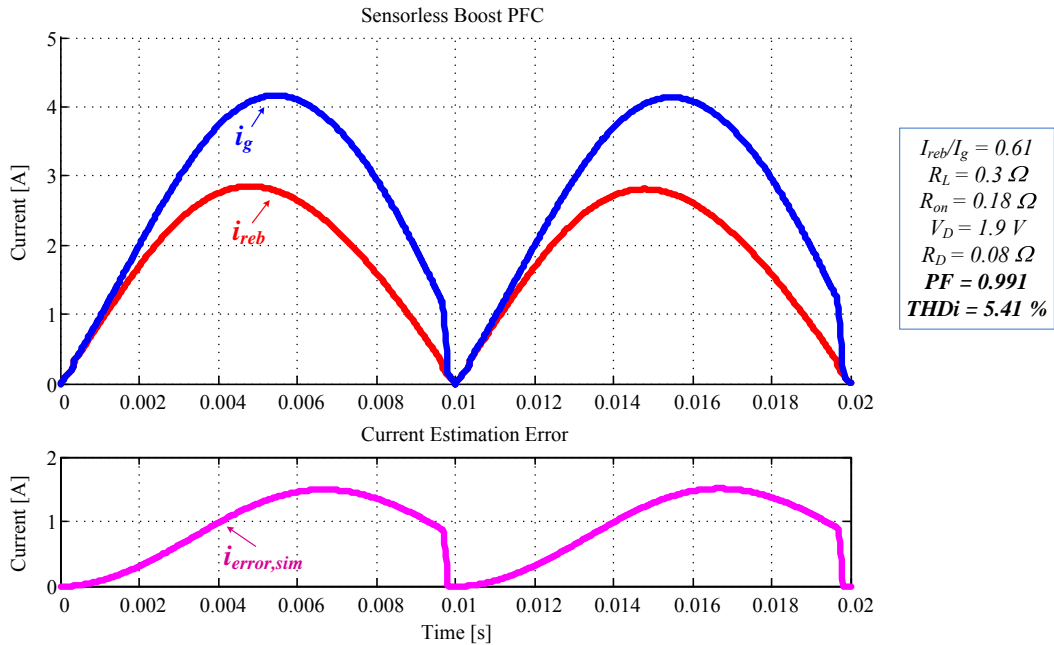

Fig. 16. Simulation results with the proposed compensation assuming $v_o \approx V_o$ and $R_{on} \approx R_D$ with V_g=230 V$_{rms}$, V_o=400 V$_{dc}$, P_o=640 W, f_{sw}=72 kHz and reactive components L=1 mH, and $C = 220$ μF. The values of the parasitic elements are $R_L = 0.3$ Ω, $R_D = 0.08$ Ω, $V_D = 1.8$ V, R_{on}=0.18 Ω.

With v_{dig} signal added to the current estimator, the influence of the parasitic elements is compensated. The current error due to $q_g \neq q_o$ is also compensated at the same time, note that both sources of error cause equivalent i_{error} shape. Considering now, no influence of the parasitic elements, a new LSB resolution (function of v_{dig}) in the output voltage data q_{o2} and the current estimation error are redefined as:

$$q_{o2} = \frac{v_o}{\dfrac{v_o}{q_o} + v_{dig}}\left(\frac{Volts}{bits}\right); \quad i_{error}[n] = \frac{T_{sw}}{L}\sum_{j=0}^{j=n}\left\{v_o[j]d'[j]\left(\frac{q_g}{q_{o2}}-1\right)\right\} \tag{21}$$

V. DISCONTINUOUS CONDUCTION AUXILIARY DETECTION CIRCUIT

Accumulated current estimation error over the half-line cycle causes input current distortion, decreasing the power factor value. As it has been shown in Fig. 8, 12 or 14, when it happens, the time in which discontinuous conduction mode (DCM) occurs is a parameter that enables the detection of discrepancy between i_{reb} and i_{in}.

An auxiliary circuit, capable of detecting the converter mode of operation (CCM or DCM) is presented in this work. Figure 16 shows the hardware architecture (Fig. 17a) and the circuit behavior (Fig. 17b). A digital signal $DCMi_g$, indicates the converter operation mode by its logic level (e.g., $DCMi_g$ = '0' for CCM operation and $DCMi_g$ = '1' for DCM operation). This circuit, similar to the one described in [24] and [25], compares the output voltage v_o, with the MOSFET drain-to-source voltage v_{ds} (used to measure the drive signal's delays), adapted with two equal resistor dividers ($R_{ds1} = R_a$, $R_{ds2} = R_b$), with an analog comparator. In CCM operation $v_{ds} > v_o$ (due to the influence of the parasitic elements) during the whole OFF time, but this is not true in DCM operation. Drain-to-source voltage v_{ds}, adopts a value close to the input voltage as soon as input current i_g reaches zero. But the inherited parasitic elements of the power switches cause oscillations in the drain-to-source voltage around v_g [26].

The analog comparator output signal x_1, is registered at the beginning of the switching period using the *on-off* signal rising edge, that is internally available in the digital device. If x_1 is high at this sample instant, the boost converter is operating in DCM ($DCMi_g$ = '1'). Conversely, if sampled x_1 is low, the

converter is operating in CCM ($DCMi_g$ = '0').

In the case of the digitally rebuilt input current i_{reb}, the signal, $DCMi_{reb}$, indicates if i_{reb}=0 at the beginning of the switching period (DCM operation is estimated and $DCMi_{reb}$ = '1') or not (CCM operation is estimated and $DCMi_{reb}$ = '0').
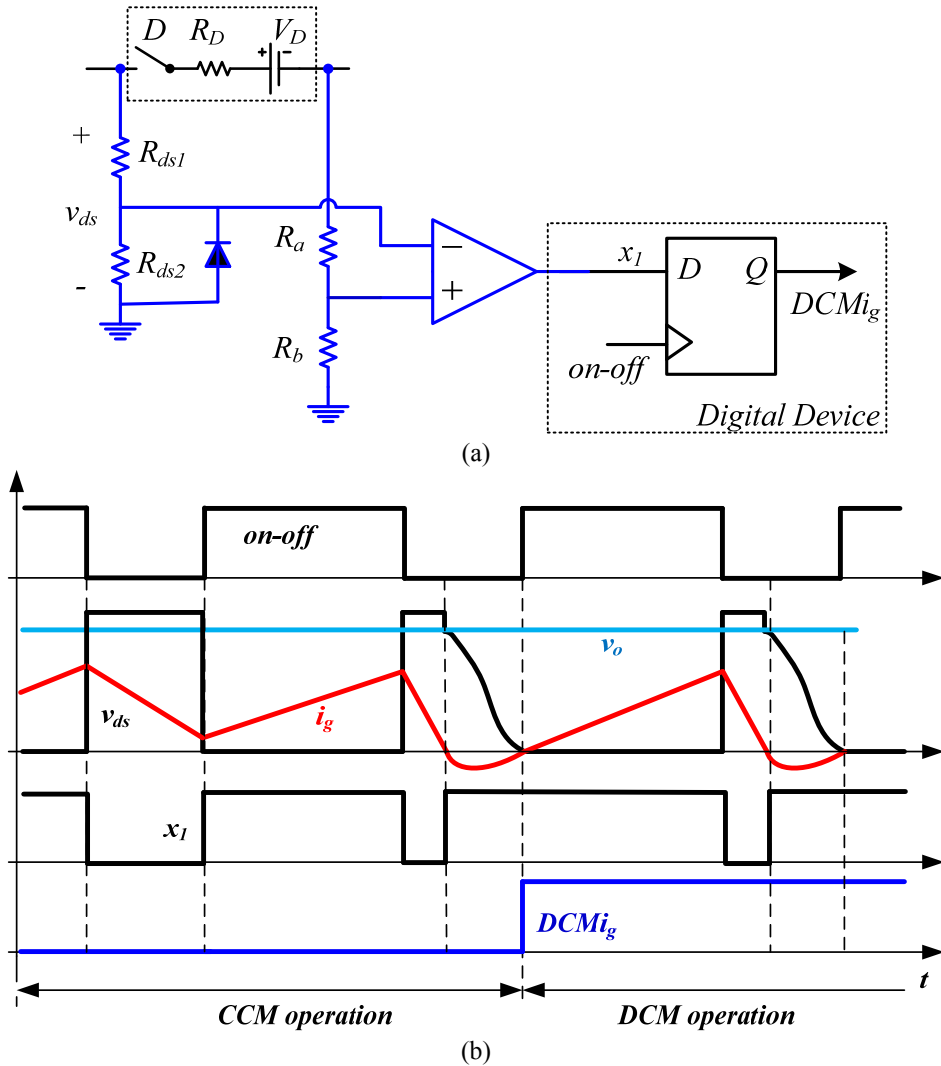

(a)

(b)

Fig. 17. DCM condition detection auxiliary circuit for the real input current. (a): Hardware architecture. (b): Circuit waveforms.

VI. HIGH RESOLUTION FEEDBACK LOOP

Recent works [19]-[22] avoid the input current measurement and propose a PFC digital control that includes the measurement of the parasitic elements (R_L, V_D, R_D, R_{on}) and applies a duty cycle command d, according to these elements, or simply neglects their influence. But parasitic elements influence change with the temperature, frequency and the components used in the PFC converter. It can be observed that in

these previously proposed solutions for sensorless PFCs use high inductance values and low switching frequencies in comparison with the state-of-the-art of CCM PFCs that include a current sensor.

The estimated input current i_{reb}, has a DCM time defined as T_{DCM}^{reb}, and i_g has a different DCM time T_{DCM}^g. A distortion in i_g leads to $T_{DCM}^g \neq T_{DCM}^{reb}$ reducing the power factor value. The i_{reb} controller captures $DCMi_g$ and $DCMi_{reb}$ and, measures and compares T_{DCM}^g and T_{DCM}^{reb}. DCM time error e_{DCM}, is expressed in equation (22):

$$e_{DCM} = T_{DCM}^{reb} - T_{DCM}^g \tag{22}$$

Thus, an indirect measurement of the current estimation error is obtained by e_{DCM}. The output voltage loop assures the desired output voltage v_o, and depending of the v_{dig} value, two different situations, shown in Fig. 18, can occur. If $e_{DCM} < 0$ (Fig. 18a), then $i_g < i_{reb}$, and it is necessary to increase v_{dig} to decrease i_{reb} to match DCM times. On the other hand, in Fig. 18b, it is presented the situation with $e_{DCM} > 0$, being $i_g > i_{reb}$, in which it is necessary to decrease v_{dig} to increase i_{reb}.
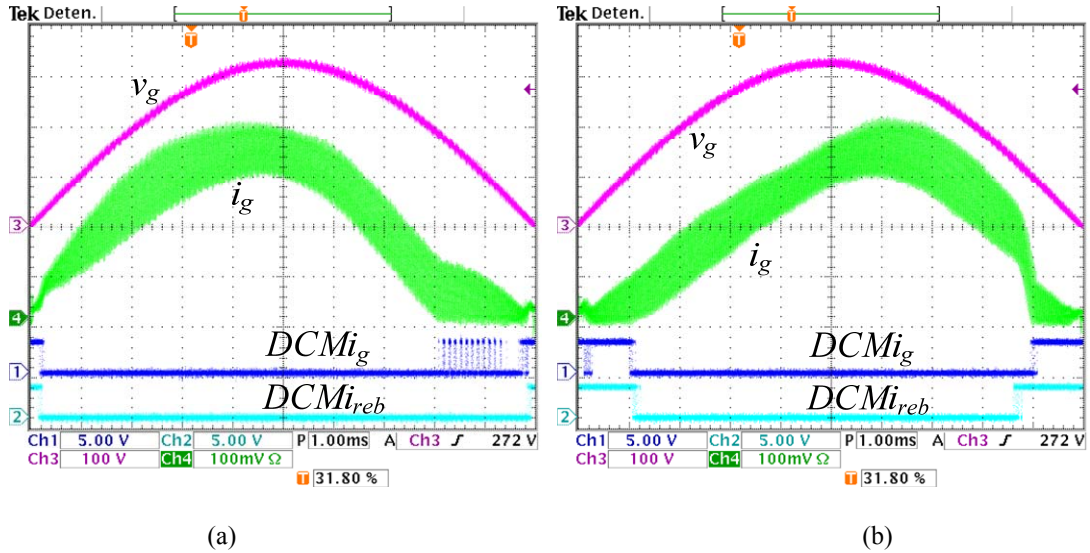

Fig. 18. Real waveforms. Input voltage v_g, real input current i_g waveforms and digital signals $DCMi_g$ and $DCMi_{reb}$ for: (a) $T_{DCM}^{error} < 0$, then $i_{reb} > i_g$; and (b) for $T_{DCM}^{error} > 0$ and then $i_{reb} < i_g$

To obtain an universal PFC controller that compensates all the current estimation errors, the proposed the new feedback loop adjusts v_{dig} to match $T_{DCM}^{reb} = T_{DCM}^g$. A block diagram of the proposed control loop

is presented in Fig. 19. The DCM time error e_{DCM} is the input of a PID compensator, which adjusts internally the value of the signal v_{dig} until DCM times match, i.e. $e_{DCM}=0$.
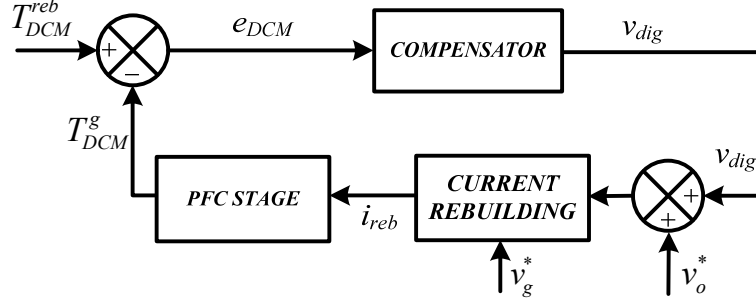

Fig. 19. Block diagram of the proposed controller.

At the same time, this new feedback loop compensates with high resolution for the estimation errors not compensated by the feedforward strategy, due to the $\pm T_{clk}/2$ resolution of the Δt_{on} measurement (addressed in Section IV). In this work 10-bit ADCs are used and v_{dig} is a 14-bit signal. Therefore, the output voltage value used to estimate the input current (v_o^*) has 14 bits (4 LSB added). A variation of ±1 LSB of v_{dig} represents an accumulated current error in the last switching period n_u of the half line cycle of, $i_{error}[n_u] = \pm0.15$ A (with the parameters previously presented). So this new feedback loop has a resolution in the current estimation error of one order magnitude higher that the feedforward compensation, whose resolution is limited by the digital device clock period (resulting in $i_{error}[n_u] = \pm1.40$ A), as presented in detail in [22].

VII. EXPERIMENTAL RESULTS

A 1 kW boost converter with the proposed digital feedback loop and feedforward time compensation has been built and tested to illustrate the behavior of the auxiliary circuit that captures the drain-to-source voltage and the performance of the error compensation. The circuit scheme that corresponds to the experimental prototype is shown in Fig. 20. The output voltage reference is 400 V_{dc} with an input voltage ranging from 85 V_{rms} to 250 V_{rms} (universal input voltage range). The switching frequency is 72 kHz. To demonstrate the universality of the proposal, two different inductors have been built, and the results are achieved without modifying any parameter of the digital controller. The first inductor has been built with

an RM12-3C90 core, resulting in inductance L_1 = 1 mH and R_{L1} = 0.25 Ω. The second inductor has been

built with a soft saturation Kool mμ core 77071. In this case, the inductance L_2 =1.5 mH and R_{L2} = 0.35

Ω. The output capacitor C = 220 uF, the MOSFET and diode used to built the prototype were an

IRFP27N60K from International Rectified ™ with R_{on} = 0.18 Ω and an RHRP860 Power Diode from

Fairchild™ with V_D = 1.8 V and R_D = 0.08 Ω. The digital PFC controller and the feedback loop were

described in VHDL and implemented on a XC3S200E field programmable gate array (FPGA) of Xilinx.

A second order *ad-hoc* sigma delta ADC [19] is used for the output voltage and a commercial TLV1572
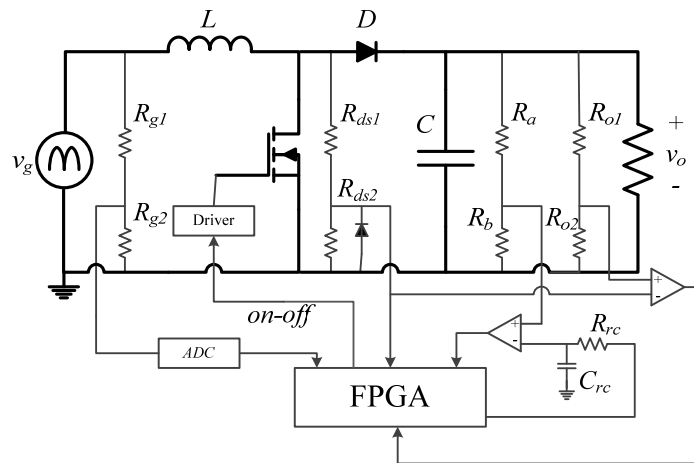
serial 10-bit ADC for the input voltage.

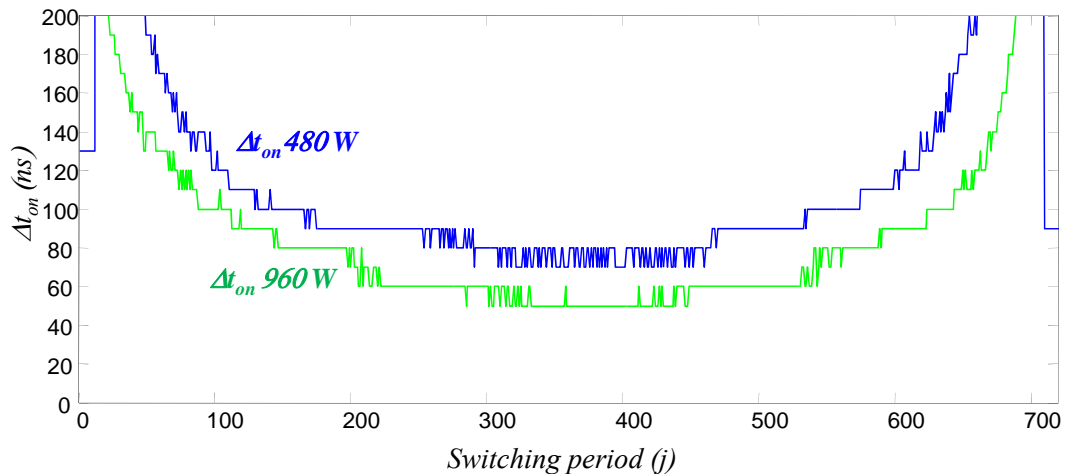Fig. 20. Schematic diagram of the Boost PFC Converter

Fig. 21. Experimental results: Value of the duty cycle modification (Δt_{on}) due to the drive signal delays over the half line cycle.

The ON-time modification (Δt_{on}) due to the drive signal delays over the half line cycle is shown in Fig.

21 for different loads (480 W and 960 W). These delays are a function of the MOSFET gate resistor

value, drain current and the MOSFET parasitic elements. With the auxiliary circuit shown in Fig. 14, the value of Δt_{on} is measured each switching period and the PFC algorithm is compensated instantaneously.
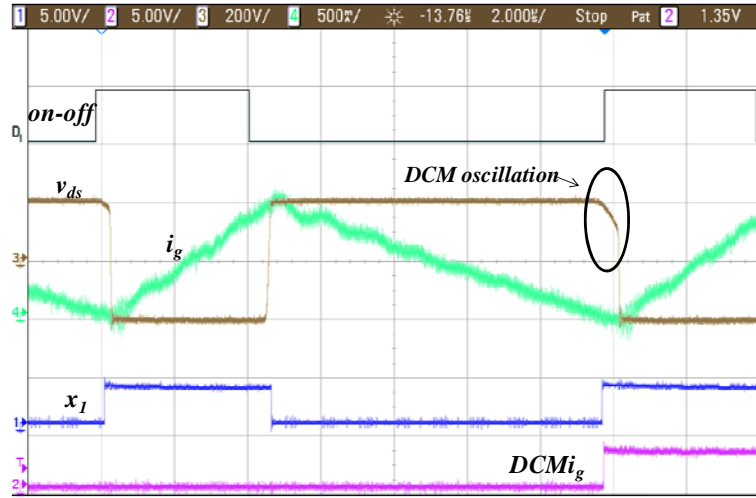

Fig. 22. Experimental results for the DCM condition detection circuit for the real input current.

Figure 22 shows the main waveforms of the DCM condition detection circuit for the real input current with $R_{ds1} = R_a= 1.2$ MΩ and $R_{ds2} = R_b = 9.31$ kΩ. The digital signal, $DCMi_{reb}$ changes to '1' when the first DCM oscillation in the drain-to-source voltage occurs. It can be seen how experimental and simulated waveforms are in good agreement (Fig. 17).

The experimental results in steady-state operation are shown in the oscillograms of Fig. 23 for different input voltages (85 V_{rms} – 60 Hz and 230 V_{rms} – 50 Hz), output power and both inductances (L_1 and L_2). It can be observed that sinusoidal input current is achieved and DCM times are matched. Power factor and Total Harmonic Distortion of the input current ($THDi$) values are listed in Table III for wide input voltage (from 85 V_{rms} – 60 Hz to 250 V_{rms} – 50 Hz) and output power ranges, fulfilling the goal addressed in Fig. 3.

TABLE III. POWER FACTOR AND THDi FOR DIFFERENT CONDITIONS

V_g	L1 = 1 mH			L2 = 1.5 mH		
	P_g	PF	THDi	P_g	PF	THDi
250 V_{rms}	970 W	0.999	5.6 %	970 W	0.995	10.5 %
	800 W	0.998	6.3 %	800 W	0.996	9.5 %
	645 W	0.997	6.8 %	645 W	0.997	8.5 %
	460 W	0.993	8.0 %	460 W	0.994	9.0 %
230 V_{rms}	975 W	0.999	4.6 %	970 W	0.995	10.5 %
	810 W	0.998	6.0 %	800 W	0.995	9.8 %

	650 W	**0.998**	6.0 %	640 W	**0.996**	9.1 %
	480 W	**0.998**	7.0 %	460 W	**0.997**	8.1 %
180 V_{rms}	825 W	**0.999**	4.8 %	820 W	**0.994**	10.5 %
	650 W	**0.999**	3.9 %	650 W	**0.996**	8.6 %
	485 W	**0.998**	5.0 %	485 W	**0.997**	7.1 %
	320 W	**0.997**	6.2 %	323 W	**0.998**	5.4 %
120 V_{rms}	495 W	**0.999**	4.1 %	497 W	**0.995**	9.8 %
	329 W	**0.998**	5.2 %	323 W	**0.995**	9.8 %
	158 W	**0.989**	12.8 %	159 W	**0.990**	10.0 %
85 V_{rms}	330 W	**0.999**	3.9 %	161 W	**0.998**	5.0 %
	161 W	**0.998**	5.3 %	336 W	**0.996**	9.0 %

Measured THD_i values are a little higher with L_1 than with L_2. This is caused by the current dependent inductance of the inductor built with a soft saturation core [27]. The aim of using this inductance in the proposed controller is to show the behavior of the controller under two different conditions. The use of L_2 on one hand introduces a non-linear behavior that produces higher current distortion as the current increases and on the other hand keeps the CCM operation for a higher load range. Despite this aspect, the experimental results present high power factor values for all the tested conditions. It must be remarked that the digital controller has not been retuned to operate under the different conditions, showing the universality of the approach presented in this work, with a switching frequency and inductance value similar to the traditional and commercial analog PFC designs.

The time evolution of the e_{DCM} value under a load step down (970-640 W) is shown in Fig. 24. After the error value peak which occurs when the load step is applied, the fine error feedback loop modifies v_{dig}, compensating the DCM times error reaching a steady state condition with $e_{DCM} = 0$ in around six seconds. During the transient time with $e_{DCM} \neq 0$ not excessive deterioration of the power factor occurs due to the feedforward compensation of the estimation error.
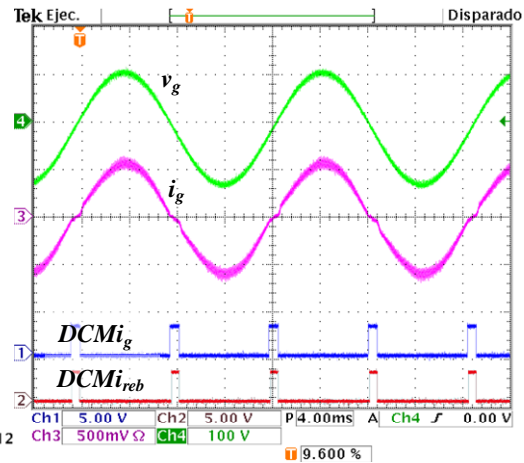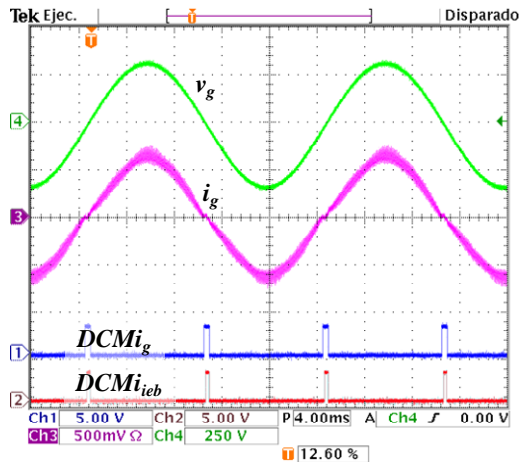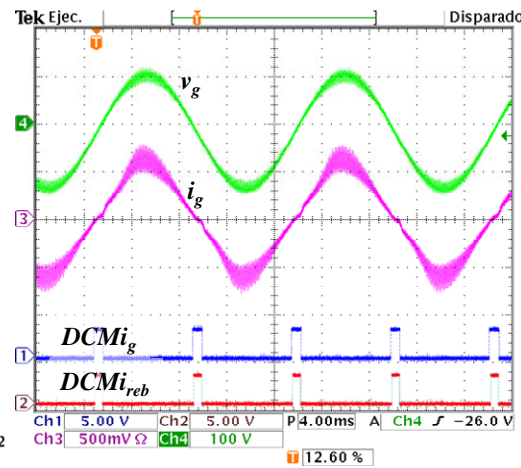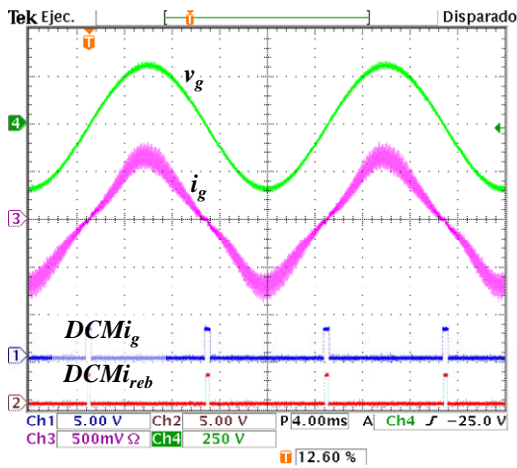
Fig. 23. Experimental results. (a) $V_o = 400\ V_{dc}$, $L_1 = 1\ mH$ and $R_{L1} = 0.25\ \Omega$. Left: $V_g = 230\ V_{rms}$ (50 Hz), $P_g = 970\ W$. Right: $V_g = 85\ V_{rms}$ (60 Hz), $P_g = 320\ W$. (b) $V_o = 400\ V_{dc}$, $L_2 = 1.5\ mH$ and $R_{L2} = 0.35\ \Omega$. Left: $V_g = 230\ V_{rms}$ (50 Hz), $P_g = 970\ W$. Right: $V_g = 85\ V_{rms}$ (60 Hz), $P_g = 320\ W$,
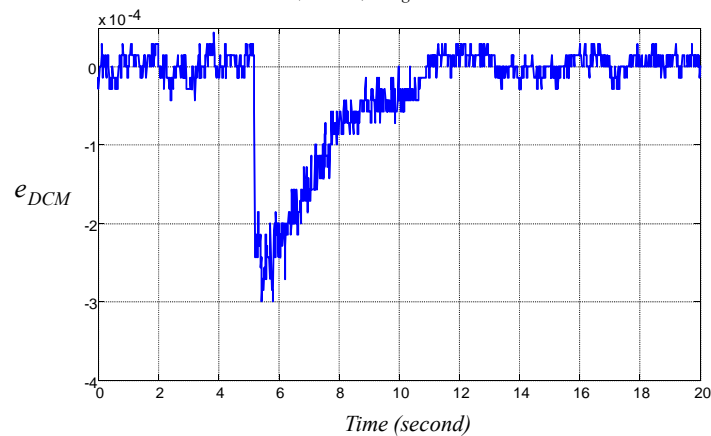

Fig. 24. Experimental results. eDCM time evolution under a 970 to 640 W load step down.

VIII. CONCLUSION

A universal current sensorless controller for Boost PFC stages operating in CCM has been presented. The current is digitally rebuilt in a digital device and this digital signal is used in the PFC current loop. Making the most of the digital control capabilities, the traditional current sensing analog circuit is substituted by a simpler circuit (two resistor dividers and a comparator) that detects DCM condition in the input current by translating the pulsated drain-to-source voltage into a digital signal. With this circuit, an indirect measurement of the current distortion is obtained by comparing the actual and estimated DCM times.

The effect of the parasitic elements in the input current estimation for sensorless PFC Boost digital controllers operating in CCM has been analyzed. In this case, the current estimation is carried out by measuring the input, output and MOSFET drain-to-source voltages.

The error between the estimated and actual DCM periods close to the zero crossing of the input voltage is a key variable to accurately correct the error in the estimation of the input current and the consequent distortion. An auxiliary circuit detects DCM condition in the input current comparing drain-to-source voltage with the output voltage during the MOSFET OFF-time. The single digital signal acquired from the MOSFET drain-to-source voltage drop is used by both the feedforward and feedback compensators. The feedforward one represents a coarse compensation of current estimation errors due to time delays. And the new feedback loop generates a constant digital signal to compensate current estimation errors, modifying the output voltage measurement used to estimate the input current, and minimizes this DCM time error. This feedback loop auto-tunes the value of the digital signal when the converter operates in a wide load or voltage range with a high resolution. An universal Boost PFC digital controller is achieved without current measurement, so in the point of view of the designer the complexity of the PFC controller decreases. With this feedback loop, parasitic element values do not need to be measured, and are compensated for automatically, representing a step forward in comparison with the previous works about PFC sensorless controllers. Experimental results show a boost PFC converter under different load conditions achieving high power factor with reliable performance.

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