Ka-Band Full-Hybrid Cryogenic Low-Noise Amplifier

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Abstract- **This paper describes the design and implementation of a broad-band full-hybrid cryogenic low-noise amplifier (MIC LNA) in the 26 – 36 frequency band, aimed for the front-end module in radio-astronomy receivers. A metamorphic technology process (mHEMT) of 50 nm gate length is used to manufacture the transistor. Design is based on a three stage common source transistor configuration and surface mounted devices (SMD) with high quality factors. Therefore, gain and noise performance are improved compared with monolithic technology (MMIC). At room temperature the mean measured gain is *G* = 22.4 dB and the noise temperature is *Tn* = 175 K. When cooled to *Tp* = 13 K, insertion gain is *Gi* = 23.8 dB and the noise temperature is *Tn* = 26 K. The DC power consumption is extremely low, P_{DC} = 5.7 mW at cryogenic temperatures.**

I. INTRODUCTION

In the field of radio astronomy, the scientist community demands high sensitivity receivers in order to detect very weak signals from the sky. Cryogenic low noise amplifiers (LNA) are placed in the front-end of these receivers to amplify these weak input signals with a very low contribution to the overall noise. Thus the contribution to the noise of the subsequent stages is minimized [1] [2].

Research activity in new materials has led to the development of indium phosphide (InP) semiconductor technology, which allows very high gain and ultra-low noise. However a low stability, fragility and limited access to this technology, whose foundries are mainly located in USA, have pushed the development of hybrid gallium arsenide (GaAs) semiconductor substrates with a high content of InP, producing a high performance semiconductor. Many works based on these transistors, either in metamorphic (mHEMT) or pseudomorphic (pHEMT) structures have been presented with excellent results [3] [4] [5].

Traditionally, monolithic technology (MMIC) has been used for high frequency designs since it presents fewer parasitic effects and a more repeatable performance. However, this technology has the handicap of the costs associated with their production (for low quantities) and sometimes it is not affordable. On the other hand, hybrid technology (MIC), where components are bonded or soldered to the substrate, presents the best noise performance so far and the possibility of post - production adjustments. Moreover, hybrid technology is cheaper than the monolithic technology for low quantities.

This paper describes the design and measurements of a cryogenic MIC LNA in the 26-36 GHz frequency band. In section II, the technology used for the transistor is briefly presented. In section III, the design of the low noise amplifier is described. Models of different devices such as transistor and capacitors are also included. The noise and scattering characterization of the amplifier is shown in section IV. Finally, section V gives the conclusions of this work.

II. TECHNOLOGY

Transistors are built in metamorphic HEMT technology with 50 nm gate length process from the Fraunhofer Institute (IAF) (Freiburg, Germany). Indium content in the channel is 65 % providing a transition extrinsic frequency *fT* = 380 GHz and a maximum oscillation frequency *fmax* = 500 GHz. Transistor size is chosen to have a 4 x 15 µm gate periphery.

III. MIC LNA DESIGN

The MIC LNA is a three stage design with transistors in common source configuration. In order to achieve better noise performance and increase the design stability transistors use source feedback technique.

A. Transistor Small-Signal and Noise models

Small signal model for the transistor is obtained from different scattering measurements. One is at the bias point of minimum noise to extract the intrinsic parameters, *Vds* = 0.7 V and *Ids* = 13 mA, 217 mA/mm. And two more measurements with *Vds* = 0 V (cold-FET technique) for obtaining the extrinsic parameters; one with the gate pinched-off and other with the gate forward biased. Fig.1 shows a picture of the 4x15 µm IAF transistor.

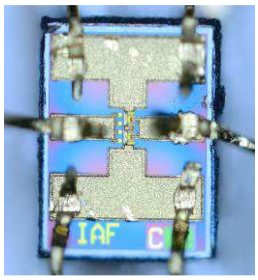

Fig. 1. IAF transistor 4x15 µm.

Fig 2 shows the typical small signal electrical transistor model used for the design of the LNA. Table 1 presents the model parameters.

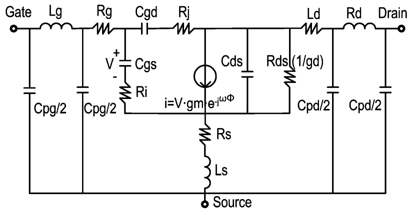

Fig. 2. 4x15 µm transistor model for *Vds* = 0.7 V and *Ids* = 217 mA/mm.

Intrinsic Parameter	Value	Extrinsic Parameter	Value
Cgs	34 fF	*Cpg/2*	7.45 fF
Ri	10 Ω	*Lg*	39.84 pH
Cgd	15 fF	*Rg*	0.5 Ω
Rj	10.5 Ω	*Cpd/2*	7.45 fF
gm	78.3 mS	*Ld*	45.11 pH
Φ	0 ps	*Rd*	2.61 Ω
Cds	17 fF	*Rs*	1.19 Ω
gd	9.6 mS	*Ls*	3.29 pH

Table 1. Small signal parameters for *Vds* = 0.7 V and *Ids* = 217 mA/mm.

A noise model is also required to design the amplifier. Fig 3 shows a noise figure measurement (red line) from 24 to 40 GHz taken with a noise figure analyzer (NFA). Measurement ripple is due to poor matching of the transistor. Simulated noise figure for the model presented in Fig 2 is shown with a green line. Noise figure estimation for the transistor is 2.6 dB in the 26-36 GHz frequency band. The noise performance is included in the transistor model from Pospieszalski [6] setting up the temperature of the drain-source resistor to *Td* = 4200 K and the remaining resistors to ambient temperature *Ta* = 300 K.

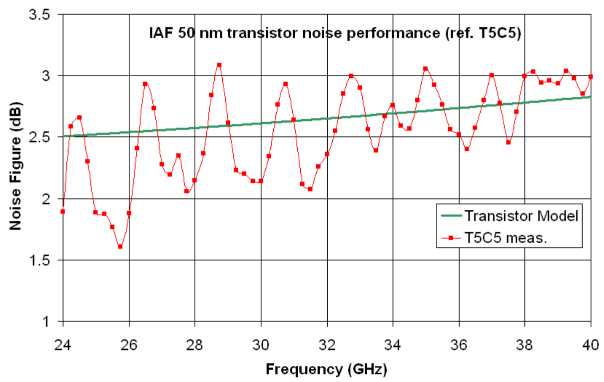

Fig. 3. Noise performance of IAF 50 nm transistor, 4 x 15 µm gate periphery, for *Vds* = 0.7 V and *Ids* = 217 mA/mm.

B. RF Capacitor Model

The SMD capacitors are key components for DC decoupling. Unfortunately the model supplied by the manufacturer often does not work properly at these frequency bands.

Fig 4 shows the set up for scattering measurements of a 0.3 pF capacitor from ATC ceramics manufacturer. The set up includes and 50 Ohm microstrip transmission line where the capacitor is mounted, and JMicro transitions to land the coplanar probes. Proper calibration eliminates the contribution of the transitions in the measurement. Fig 5 shows the electrical model for the capacitor with all the associated parasitic effects. Table 2 provides the values of the capacitor model parameters.

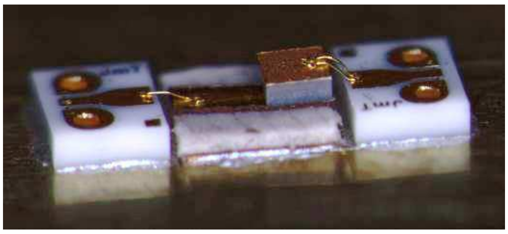

Fig. 4. Measurement setup for a 0.3 pF capacitor with JMicro transitions.

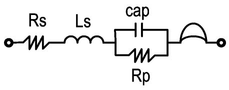

Fig. 5. 0.3 pF ATC capacitor model.

Parameter	Value
cap	0.3 pF
Rs	1 Ω
Ls	20 pH
Rp	100 K Ω

Table 2. Parameters for the capacitor model.

Fig. 6 compares the simulation of the model (red line) with the capacitor measurements (blue line). A quite good agreement between model and measurement can be observed in the 2-50 GHz frequency range.

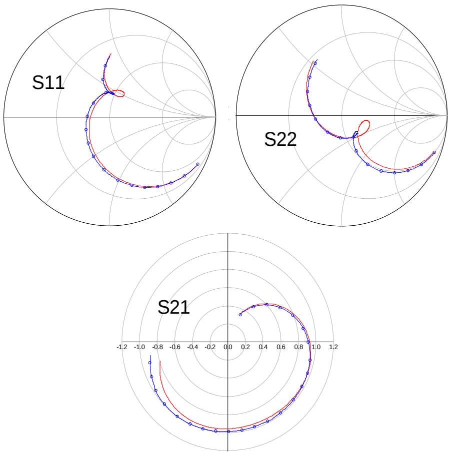

Fig. 6. Scattering performance for the 0.3 pF capacitor in the 2 to 50 GHz band. Measurements in blue line; simulation in red line.

C. LNA Design

The most important part for the noise performance of the LNA is the first stage. Therefore, the design should rely on simple microstrip lines at the input. Design and optimization process is carried out using ADS Momentum simulator from Agilent Technologies. The substrate used for the microstrip lines is CLTE-XT from Arlon (ε_r = 2.79, *h* = 5mils) due to its good performance stability with temperature.

Matching networks between transistors and the output network are designed to achieve flat gain keeping noise as low as possible. Fig. 8 shows the circuit diagram of the LNA. Bias networks are independent and they are formed by a combination of resistors and capacitors providing filtering networks for unwanted signals.

Fig. 7. Photo of MIC LNA manufactured.

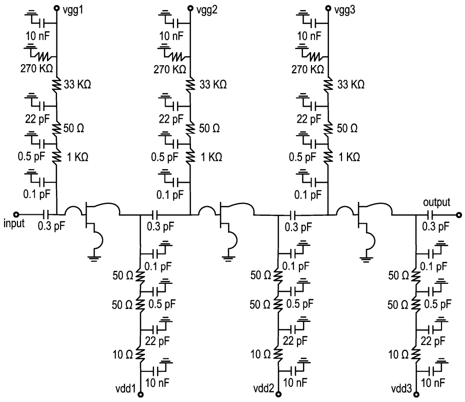

Fig. 8. Scheme of the 3 stage LNA.

A detailed picture of the LNA is shown in Fig. 7. Chassis is equipped with 2.4 mm connector. DC bias accesses are narrow channels perpendiculars to RF channel in order to avoid resonances in the cavity (Fig. 9).

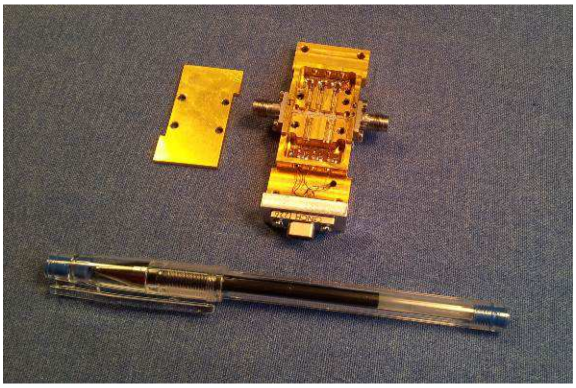

Fig. 9. LNA assembly with 2.4 mm connectors.

IV. LNA PERFORMANCE

Measurements of scattering parameters were taken with a network analyzer E8364A from Agilent Technologies.

The measurement of noise figure in Ka-Band requires a frequency conversion stage in combination with the available N8975A noise figure analyzer and noise source (model 346C_K01 from Agilent Technologies). An attenuator of 6 dB is placed after the noise source for two reasons; first the attenuator reduces the noise source ENR and approximates it to the expected noise of the device under test (DUT) reducing the uncertainty of the measurement [7]. And second: the difference between reflection coefficient of the noise source in the ON and OFF states is smaller, minimizing the ripple in the measurements.

A. Room temperature

Bias point is tuned in order to achieve the best trade-off between gain and noise. Finally the bias point I_{d1} = 15 mA, V_{d1} = 2.3 V and I_{d23} = 16 mA, V_{d23} = 2.5 V was selected. DC power consumption is 114.5 mW.

Fig. 10 shows the small signal gain, S_{21}, and the input and output matching. Mean gain in the 26-36 GHz frequency band is 22.5 dB with a ripple of ± 2.2 dB. Matching mean values are -9.2 dB at the input and -14.7 dB at the output.

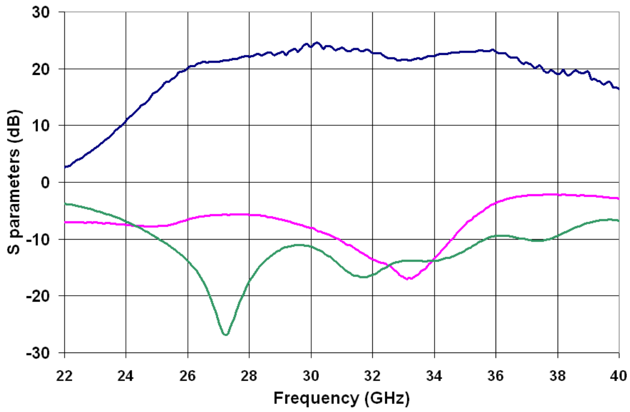

Fig. 10. LNA small signal gain, S_{21} (blue), Input matching, S_{11} (pink), and output matching, S_{22} (green).

Fig. 11 shows noise performance. The mean noise temperature in the 26-36 GHz band is *Tn* = 175 K (2.05 dB noise figure). The minimum noise temperature is 145 K at 35 GHz.

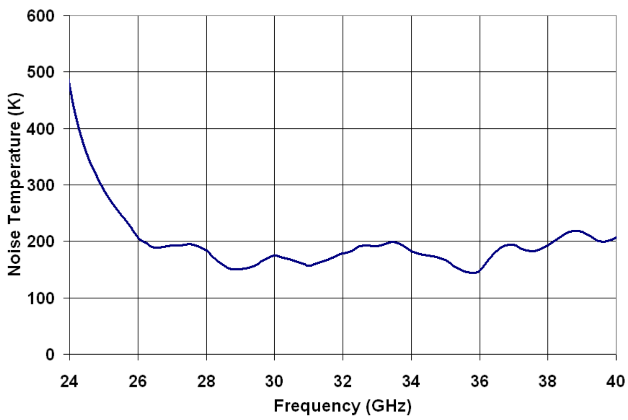

Fig. 11. Noise temperature, *Tn*, at room temperature (300 K).

B. *Cryogenic temperature*

LNA measurements under cryogenic conditions were taken using the cold attenuator technique. It consists in cooling an attenuator placed at the input of the LNA (DUT) to reduce the noise power injected from the noise source outside the cryostat [8] (see Fig. 12).

Calibration is performed following the same procedure as in the room temperature measurement. For the measurement, the noise source is directly connected to the cryostat input, eliminating the 6 dB attenuator used at room temperature, because of the existing 20 dB attenuator inside the cryostat [9].

In Fig.13 the MIC LNA is presented clamped to the cold base inside the cryostat, just before a cooling cycle [10].

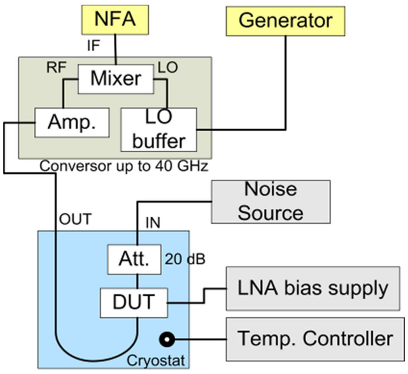

Fig. 12. Noise measurement set up at cryogenic temperature.

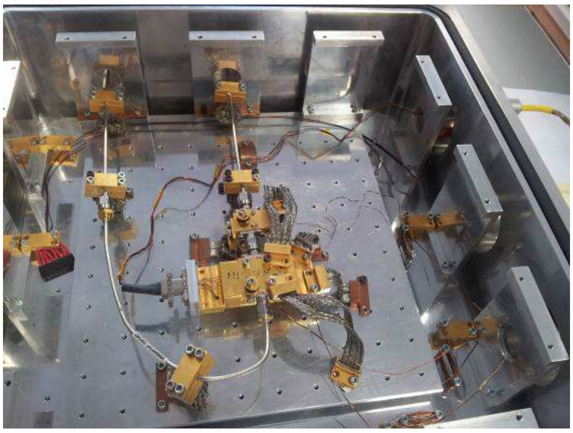

Fig. 13. Picture of the MIC LNA inside the cryostat.

In Fig. 14 the results of the cryogenic measurements are presented. Insertion gain in the 26-36 GHz band is 23.8 ± 2.2 dB, whereas the mean noise temperature is 26 K. Minimum noise temperature is 19.5 K at 29 GHz. The DC power consumption is only 5.7 mW.

V. Conclusions

It has presented the design and characterization of a full-hybrid low-noise cryogenic amplifier developed for radio astronomy applications in the 26-36 GHz frequency band.

The amplifier has three-staged in common source configuration with transistors manufactured on GaAs metamorphic substrate technology.

We have obtained 22.4 dB of gain and 175 K of noise temperature in the 26-36 GHz frequency band for the measurements at room temperature. When the amplifier is cooled down to 13 K, the gain is 23.8 dB and the noise temperature is 26 K. The DC power consumption at cryogenic temperatures is only 5.7 mW.

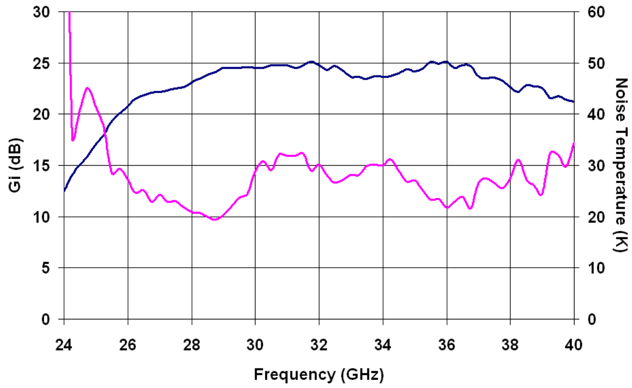

Fig. 14. Insertion gain, Gi (blue), and noise temperature (pink) at physical temperature T_p = 13 K.

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