View metadata, citation and similar papers at core.ac.uk

brought to you by CORE

provided by Kyutacar : Kyushu Institute of Technology Academic Repository

Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test

著者	Miyake Yousuke, Sato Yasuo, Kajihara Seiji, Miura Yukiya
journal or publication title	Asian Test Symposium (ATS), 2014 IEEE 23th
page range	156-161
year	2014-12-11
URL	http://hdl.handle.net/10228/00006259

doi: info:doi/10.1109/ATS.2014.38

Temperature and Voltage Estimation Using Ring-Oscillator-Based Monitor for Field Test

Yousuke Miyake[†], Yasuo Sato[†], Seiji Kajihara[†] and Yukiya Miura[‡]
† Kyushu Institute of Technology, Iizuka, Japan
‡ Tokyo Metropolitan University, Tokyo, Japan
{miyake, sato, kajihara}@aries30.cse.kyutech.ac.jp, miura@tmu.ac.jp

***Abstract*—Field test is performed in diverse environments, in which temperature varies across a wide range. As temperature affects a circuit delay greatly, accurate temperature monitors are required. They should be placed at various locations on a chip including hot spots. This paper proposes a flexible ring-oscillator-based monitor that accurately measures voltage as well as temperature at the same time. The measurement accuracy was confirmed by circuit simulation for 180 *nm*, 90 *nm* and 45 *nm* technologies. An experiment using test chips with 180 *nm* technology shows its feasibility.**

***Keywords*—temperature monitor; voltage monitor; ring oscillator; field test; delay test.**

I. Introduction

Increasing system complexity and geometrically shrinking in semiconductor fabrication process make it harder and harder to achieve high reliability of VLSI systems in field. It is a crucial issue especially for safety-related systems such as automobiles, aircrafts or social infrastructure systems [1-5].

One of promising approaches to achieve high reliability is a field test including delay test, which measures delay margin [6-10]. However, the test will be performed in diverse environment, in which temperature varies in a wide range and the supply voltage may not be stable. Furthermore, there are an issue of hot spots on a chip and an issue of low voltage area caused by IR-drop. While high temperature or low voltage increases delay, low temperature or high voltage will decrease delay. Therefore, both temperature and voltage during testing should be well controlled. When it is difficult to control them, they should be accurately measured with temperature and voltage monitors on a chip. Then, it will be possible to remove environmental factors that affect the measured delay by correction.

There are many works on-chip monitors to measure or estimate temperature/voltage [11-16]. Thermal diodes are the most popular hard sensors with high accuracy. However, they impose various restrictions, which include an analog comparator, an A/D converter, a reference current source, and complex calibration [12-14]. Therefore, they are usually placed at a limited location on the chip and it is difficult to know temperature at every hot spots. An alternative to the hard sensors are ring-oscillator-based soft sensors. Their merits are low power consumption and low area overhead. Therefore, they have less restriction on placement and larger number of sensors can be embedded on a chip. On the other hand, some of them require a reference current for calibration or a clean supply voltage [12, 15-16].

Quenot et al. [16] proposed a temperature and voltage measurement technique based on delay programmable ring oscillators. It requires complex processing for mapping the measured frequencies of ring oscillators into a (T, V) plane, where T is temperature and V is voltage.

In general, the required features for a temperature and voltage monitor for field test are as follows:

a) To measure not only temperature but also voltage in test.
b) To minimize the costs of design and manufacturing to put the monitors on many places on a chip.
c) To measure temperature and voltage in a short time.
d) To measure temperature and voltage with high accuracy, even in a process variation.
e) To avoid aging of the monitor itself.

As a temperature and voltage (*T&V*) monitor for field test, Miura et al. [11] proposed a ring-oscillator (RO)-based circuit to estimate *T&V* using the relationships of temperature, voltage and RO frequency. The proposed monitor is easy to design because it consists of fully digital circuits without any analog circuits. Therefore, it can be placed at various locations such as hot spots of the chip. Also, the monitor has an aging-tolerant structure for electro-migration, BTI (Bias Temperature Instability) and HCI (Hot Carrier Injection). On the other hand, the accuracy of estimation is not so high, (e.g. standard division of errors for T and V are 2.21 ℃ and 7.11 *mV*, respectively. For instance, in order to suppress the error of delay measurement within 6 *ps*, the temperature estimation accuracy is required to be below 1.75 ℃ [10]). If process variation exists, the errors will be larger than the calculated one for the typical process. Also the area overhead due to the monitor and measurement time were not discussed enough. Thus, the work [11] does not satisfy the necessary feature d) stated above and features b) and c) are not sure, although it has features a) and e).

This paper proposes an improved *T&V* estimation method for field test based on the RO-based monitor [11]. The following techniques for estimation are proposed:

- Estimation accuracy is improved by dividing both temperature and voltage ranges into small sub-ranges.

- The proposed method uses a new calibration technique to handle process variation. The error caused by process variation is reduced by comparing measured frequencies and typical frequencies at the initial measurement in field.

Using the proposed method, standard division of errors for *T* and *V* were reduced to 0.99 ℃ and 4.17 *mV*, respectively. Therefore, the proposed method can estimate *T* and *V* more accurately than [11], and it satisfies all the required features for field test. The paper also confirms area overhead and measurement time by a TEG chip implementing the *T&V* monitor. The effect of the proposed calibration technique to avoid the influence of process variation is confirmed by evaluation for ten chips.

This paper is organized as follows. Section 2 describes the concept of the proposed monitor. Section 3 describes the procedure for estimation. Section 4 shows simulation results for the monitors with 180 *nm*, 90 *nm* and 45 *nm* technologies, respectively. Section 5 shows results of TEG chip evaluation. Section 6 concludes the paper.

II. Basic Idea of RO-based TVM

A. RO-based TVM [11]

Miura et al. [11] proposed a *T&V* monitor (*TVM*) using three types of ring-oscillators for the delay measurement in field test. The monitor has the following features:

- The monitor can be implemented with digital circuits; the ROs and the counters consist of logic gates in a standard cell library as shown in Fig. 1.
- Three types of ROs, which have different *T&V* characteristic, are simultaneously operated.
- *T* and *V* are estimated with fully digital processing in a short time. If the ROs do not have to always run, they are highly aging-tolerant for electro-migration, BTI and HCI.

Frequency F_i of RO_i (i=1, 2, 3) is a function of *T&V* as shown in equation (1). Linear equations (2) and (3) are derived from simulation data using the multiple regression analysis.

$$F_1 = g_1(T, V),\ \ F_2 = g_2(T, V),\ \ F_3 = g_3(T, V) \qquad (1)$$
$$T = h(F_1, F_2, F_3) = a_1*F_1 + b_1*F_2 + c_1*F_3 + d_1 \qquad (2)$$
$$V = k(F_1, F_2, F_3) = a_2*F_1 + b_2*F_2 + c_2*F_3 + d_2 \qquad (3)$$

Because the relations of F_i and *T&V* are investigated using *SPICE* simulation, the equations (2) and (3) are created at design phase. When the relations between frequencies F_i ($i=1,2,3$) and *T&V* are not linear, the *T&V* estimated by linear equations such as (2) and (3) generally include some amount of estimation errors. As the linear equation is beneficial for implementing either by software or hardware, the linear estimation *T* range is divided into three *T* sub-ranges. If the focused range is smaller, the error of estimation will be smaller as shown in Fig. 2: that is, temperature estimation accuracy will be improved by dividing the focused range into several small sub-ranges. In a simulation-based evaluation, using this temperature division technique, standard division of errors for *T&V* were reduced from 9.80 ℃ to 2.21℃ and from 18.16 *mV* to 7.11 *mV*, respectively [11].

Even using the division technique, the estimation accuracy was not high enough. Moreover, as process variation is not considered, real errors of estimated values will be larger than the calculated ones.

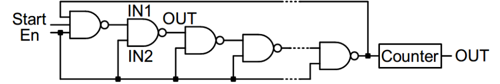


Figure 1. RO Structure of TVM [11]

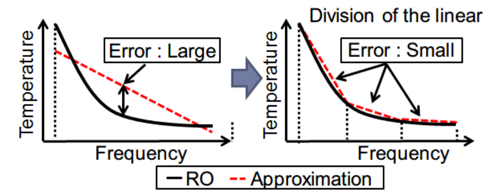


Figure 2. Linear approximation

B. Overview of the proposed method

This paper proposes three improved techniques for *T&V* estimation, which satisfies requirements a)-e) in Section 1.

The first technique is a division of the *T&V* ranges. The proposed method divides the *V* range into three sub-ranges as well as the *T* range. As a result, estimation equations are created for nine small (*T*, *V*) rectangular sub-ranges. The detail of the technique is discussed in Section 3.A.

The second technique is a hierarchical estimation procedure. Because real *T&V* are unknown at the start of the estimation, it is needed to identify the sub-range that includes real *T&V*. In the proposed technique, *T&V* are roughly estimated using full-range's estimation equation to determine the corresponding sub-range where the real *T&V* exist. Then, detailed *T&V* are estimated using the corresponding sub-range's estimation equation. The detail of the hierarchal procedure will be given in Section 3.B.

The third technique is a calibration method that handles process variation. When process variation is not negligible, the errors of estimation would be larger than the calculated ones from the typical process. The evaluation of the proposed technique is confirmed by circuit simulations for 180 *nm*, 90 *nm* and 45 *nm* technologies. How to deal with process variation will be discussed in Section 3.C.

Furthermore, the feasibility of the *TVM* including area overhead and measurement time is confirmed by implementation of a TEG chip. Then, the evaluation using multiple TEG chips confirms that *T* and *V* can be estimated from the RO frequency by the proposed calibration technique when the process variations are not negligible.

Validity of the temperature estimation is confirmed by comparing the values that are estimated from estimation equation, and a measured surface temperature of a TEG chip. And, validity of the voltage estimation is confirmed by comparing the estimated voltage using estimation equation, and a measured current using an ammeter. The detail of the TEG chip evaluation will be discussed in Section 5.A.

III. *T&V* ESTIMATION METHOD

A. Division of T&V Ranges

The division of the *T&V* range is useful for improving estimation accuracy as shown in Fig.2. However, a problem is how to specify the sub-range that includes the real *T&V* before estimation. Moreover, process variation may affect the RO frequencies. It is inconvenient that the divided sub-ranges are varying depending on the process variation. Therefore, the sub-ranges should be determined so as not to be affected by the process variation.

Fig. 3 shows the relation between the estimated and real temperatures. In temperature estimation, an error by process variation (εP_T) and an error by estimation equations (εT) exist in the estimated value. The maximum and minimum of errors by process variation can be computed by simulation corresponding to the highest and lowest V_{th}, respectively. The relations between *T&V* sub-ranges and process variation are given in the equations (4) and (5). Note that εT and εV are the errors by the estimation equation due to the non-linearity, and εP_V and εP_T are the errors by process variation. For example, equation (4) means that the estimated *V* consists of real voltage V_{Real}, which we want to know, and other two errors, εV and εP_V.

$$V = V_{Real} + \varepsilon V + \varepsilon P_V \quad (4)$$

$$T = T_{Real} + \varepsilon T + \varepsilon P_T \quad (5)$$

If the small sub-range does not consider εT, εV, εP_T and εP_V , there is a possibility that the real value does not exist in the selected sub-range; therefore, the corresponding estimation equation is not correct. Fig. 4 shows the relation between the original division sub-ranges and modified sub-ranges for estimation. The original division sub-ranges are decided as simple three sub-ranges. On the other hand, the modified estimation sub-ranges are determined wide enough to include the errors ($\varepsilon T + \varepsilon P_T$), and the estimation equations are created for these sub-ranges. As a consequence, the neighboring sub-ranges are overlapped each other. In the overlapped area, using either estimation equation, the amount of errors is controlled as the larger error of two sub-ranges. Then, Even if there is process variation, the ranges that include real *T&V* don't have to be changed. Either estimation equation of two sub-ranges will be applicable for estimation. The number of the divided ranges is determined in consideration of the errors (εT, εV, εP_T and εP_V) and the modified sub-ranges are wide enough so as not to be overlapped.

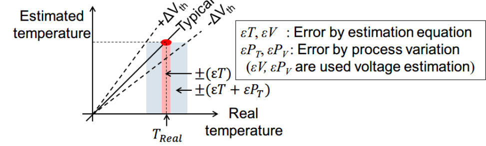


Figure 3. Relation between estimated and real temperature

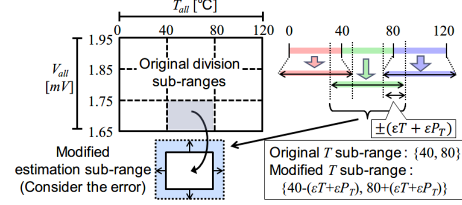


Figure 4. Considerations of Error Ranges

B. Hierarchical procedure of T&V Estimation

Fig. 5 shows a proposed hierarchical estimation method. Each divided sub-range has its estimation equations for *T&V* considering the errors ($\varepsilon V + \varepsilon P_V, \varepsilon T + \varepsilon P_T$). Rough estimation is firstly performed using full-range. Then, a corresponding small sub-range is selected. Finally, *T&V* estimation in the selected small *T&V* sub-range is performed. The details are shown in the following:

Step1. Select a small *V* sub-range using estimation equation in the full-range of *T&V*. The small *V* sub-range is selected considering the effect of the process variation εP_V, which is a part of εV_{small} in equation (6).

$$V_{init} = V_{Real} + \varepsilon V_{small} \quad (6)$$

Step2. Select a small *T* sub-range using estimation equation in the *T* full-range and the selected *V* sub-range at Step1.

$$T_{init} = T_{Real} + \varepsilon T_{small} \quad (7)$$

Step3. Estimate V_{fin} value using the selected *T* sub-range and the selected *V* sub-range.

Step4. Estimate T_{fin} value using the selected *T* sub-range and the selected *V* sub-range.

Finally, *T* and *V* are estimated for the small *T&V* sub-range at Step3 and Step4. It should be noted that three *T* sub-ranges are prepared for each *V* sub-range; therefore, the estimation equations defined for small *T&V* sub-ranges are used. As the influence for the RO frequencies by voltage is higher than that by temperature, selection of *V* sub-range should be performed before selection of *T* sub-range.

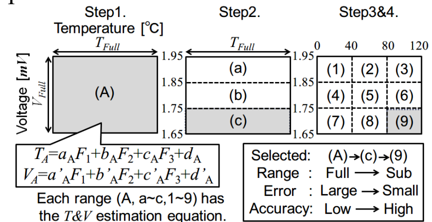


Figure 5. Hierarchical Estimation Method

C. Process Variation Consideration

To tackle with the effect of the process variations, equations (2) and (3) are expanded as a differential approach, which is shown in equations (8) and (9) below.

$$\Delta T = a_1 * \Delta F_1 + b_1 * \Delta F_2 + c_1 * \Delta F_3 + d_1 \quad (8)$$
$$\Delta V = a_2 * \Delta F_1 + b_2 * \Delta F_2 + c_2 * \Delta F_3 + d_2 \quad (9)$$

T and V are estimated as the difference from the initial measurement, in which the initial $T\&V$ are known (i.e. in a very well controlled environment at the final test or at a system debug). By this differential approach, common variation between the initial and current measurement will be compensated as described in the following.

Process variation is classified into two categories: global variation and local variation [17]. Global variation is caused by the non-uniform heat distribution during manufacturing processes, and characteristics of transistor may change smoothly across the entire wafer. Then, the RO frequencies differ depending on the location. Local variation is due to the Gaussian noise, and characteristics of transistor vary independently. Therefore, frequency variation will be reduced to $1/\sqrt{N}$ times according to the law of large numbers, where N is the number of RO stages.

Fig. 6 explains a calibration technique to reduce the error of global variation. At the initial measurement, the ratio of variation to the typical process is obtained by comparing the measured frequency with typical frequencies $\{F_1(T_0)/F_1^{typ}(T_0)\}$ in the environment where T and V are known or controlled as (T_0, V_0). Therefore, the error is able to be reduced by the ratio. Then, the estimation equation is corrected by multiplying the ratio in equations (8) and (9). As each transistor variation differs in a chip or between chips, different correction ratios are assigned for the ROs at each location. As a result, the proposed calibration technique can reduce the influence of global variation such as die-to-die or within-die variation.

$$\Delta T, \Delta V \cong a \frac{F_1^{typ}(T_0)}{F_1(T_0)} \Delta F_1 + b \frac{F_2^{typ}(T_0)}{F_2(T_0)} \Delta F_2 + c \frac{F_3^{typ}(T_0)}{F_3(T_0)} \Delta F_3 + d \quad (10)$$

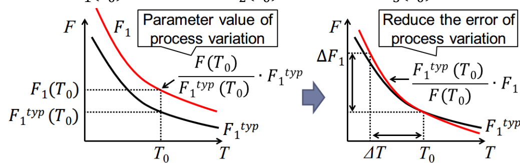


Figure 6. Influence Reduction of Process Variation

IV. EVALUATION BY CIRCUIT SIMULATION

Fig.7 illustrates the circuit architecture of a *TVM* using ROs. The *TVM* consists of three pairs of an RO and a counter. Three counter values are sent to *TVM_controller* in serial after the measurement is over; then, the values are stored in a non-volatile memory, which can be either on-chip or off-chip. More than one *TVM* are placed to various locations on the chip. They are usually placed in each clock domain, or one *TVM* can share plural domains. Thus, the *TVM*s are able to monitor hot spots in the chip.

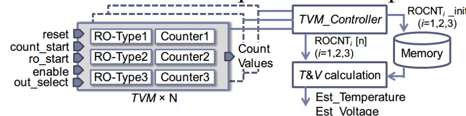


Figure 7. TVM Architecture

In this paper, RO1 is 51-stage 2NAND with 1-fanout. RO2 is 19-stage 4ORNAND with 4-fanouts. RO3 is 21-stage 2NAND with 7-fanouts. There are various RO types (e.g. the types of the circuit, circuit structure, number of the stage and fanout). And, the combination of ROs affects the estimation accuracy. However, the selection method will not be discussed in this paper because of the page number limit.

The characteristics of transistors of the RO are different by technology process. In addition, the RO frequencies are also influenced by wire length between the RO stages. Therefore, to confirm accuracy of the *TVM*, evaluations using *SPICE* simulation was performed for 180 *nm*, 90 *nm* and 45 *nm* technology process, respectively. Tables I, Π and Ш confirm the evaluated estimation accuracy. The accuracy values are expressed with standard deviation of errors. The results show that the division of the $T\&V$ range can improve estimation accuracy better than the non-division. For 180 *nm* technology process, temperature accuracy was improved from 3.21 ℃ to 0.86-0.94 ℃, and voltage accuracy was improved from 11.77 *mV* to 2.98-4.17 *mV* by the division ranges. In the same way, the accuracies were 0.65-1.17℃ and 1.40-3.39 *mV* for 90 *nm*, and 1.42-3.75℃ and 4.17-11.30 *mV* for 45 *nm*, respectively.

TABLE I. ESTIMATION ACCURACY (180 NM)

180*nm*		Estimated temperature [℃]			Estimated voltage [mV]		
V_0 : 1.80v		Temperature division			Temperature division		
T_0 : 60℃		0～40℃	40～80℃	80～120℃	0～40℃	40～80℃	80～120℃
Voltage division	1.85v～1.95v	0.86	0.93	0.99	3.58	3.58	3.55
	1.75v～1.85v	0.86	0.91	0.98	3.97	3.32	3.34
	1.65v～1.75v	0.94	0.91	0.94	4.17	3.52	2.98

TABLE II. ESTIMATION ACCURACY (90 NM) [9]

90*nm*		Estimated temperature [℃]			Estimated voltage [mV]		
V_0 : 1.15v		Temperature division			Temperature division		
T_0 : 50℃		-40～20℃	20～80℃	80～110℃	-40～20℃	20～80℃	80～110℃
Voltage division	1.20v～1.30v	1.17	0.87	0.65	2.58	2.19	1.73
	1.10v～1.20v	1.36	1.28	1.13	3.32	3.39	1.96
	1.00v～1.10v	1.20	1.08	0.76	2.27	2.88	1.40

TABLE III. ESTIMATION ACCURACY (45 NM)

45*nm*		Estimated temperature [℃]			Estimated voltage [mV]		
V_0 : 1.00v		Temperature division			Temperature division		
T_0 : 60℃		0～40℃	40～80℃	80～120℃	0～40℃	40～80℃	80～120℃
Voltage division	1.03v～1.09v	2.09	1.81	1.42	7.72	6.03	4.17
	0.97v～1.03v	2.72	2.22	1.80	9.04	6.57	4.67
	0.91v～0.97v	3.75	2.85	2.29	11.30	7.62	5.33

V. EVALUATION BY TEG CHIP

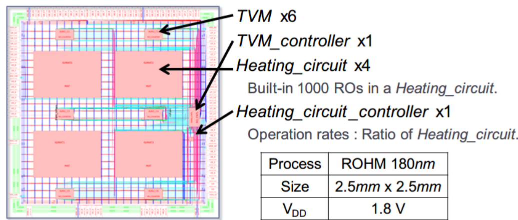
A. TEG Chip Design

Fig. 8 shows the TEG design to evaluate the feasibility of the *TVM*. The structure of the TEG chip is as follows:

- *TVM*: The three types of ROs and counter.
- *TVM_controller*: The controller for the *TVM*.
- *Heating_circuit*: The circuit consists of 1,000 ROs. According to the rate of operating ROs, TEG chip temperature is controlled.
- *Heating_circuit_controller*: The controller for the *Heating_circuits.*

Six *TVM*s are embedded in the TEG chip. Four *TVM*s of them are placed to the boundary of the TEG chip, and the remaining two *TVM*s are placed near the center of the TEG chip. Four *Heating_circuits* are placed between the *TVM*s. TEG chip temperature is controlled roughly by the rate of operating ROs in *Heating_circuits*, (e.g. 10% operating rates means that 100 ROs of *Heating_circuit* are running). If the operating rate goes up, TEG chip temperature becomes high. By changing the operating rate, *TVM*s can be measured at various temperatures.

Table IV confirms the area overhead of the three ROs, the *TVM* and the *TVM_controller*. Here, the *TVM* includes three ROs and counters. As they are so small, the impact on chip design will be small for a large industrial data.



Process	ROHM 180*nm*
Size	2.5*mm* x 2.5*mm*
V_{DD}	1.8 V

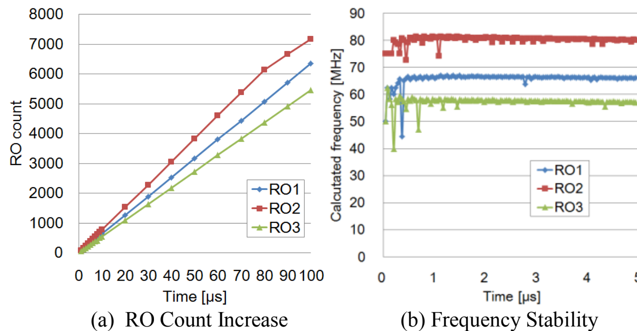
Figure 8. TEG Chip Design

TABLE IV. AREA OVERHEAD (180 *NM*)

	RO1	RO2	RO3	*TVM*	*TVM_Controller*
Number of cells	55	66	44	503	407
Total gates	55	98	68	1138	880

B. Short time measurement

Fig. 9(a) shows the counted values of three ROs in the TVM. The counted value increases at a constant deviation. Fig. 9(b) shows the measured frequencies in a short period (0-5μs). It takes about 1μs for stabilizing the frequencies, which are calculated using counter values of the ROs. This will be because of an insufficient count time. Thus, a stable measurement of the RO frequency after 1us is confirmed. Therefore, it can be confirmed that the measurement time of frequency is short.



(a) RO Count Increase (b) Frequency Stability

Figure 9. Stability of RO Counting

C. Validity of Voltage Estimation

Fig. 10 shows the relation between the estimated voltage by the *TVM* and the measured current increment by ammeter. As the operating rates of *Heating_circuits* increases, estimated voltage becomes lower. This result shows that the change rate of the estimated voltage is the same change rate of current increment. Therefore, this result shows the validity of voltage estimation. Fig. 10 also shows IR-drop effect on the TEG chip. The amount of IR-drop values looks rather large because only two pairs of power pins is available (a QFP package is used for the TEG chip) and *Heating_circuits* dissipated large power.

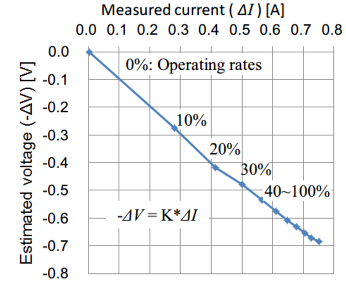


Figure 10. Validity of Voltage Estimation

D. Validity of Temperature Estimation

Fig. 11 shows the experimental setup of the TEG chip. Temperature of the bare chip surface is observed by a thermal image sensor, which is for a comparison between estimated and real temperatures [18]. The temperature of bulk silicon is calculated from the surface temperature using a thermal resistance and the thermal radiation model as shown in Fig. 11. The relation between internal and surface temperatures, which are given in equation (11) below, is extracted with the thermal resistance model using the Laplace transform. Here, R is thermal resistance and C is thermal capacity. X, Y, Z, α and β are results of the calculation from the temperature model. ΔT_a and ΔT_b are differences from the initial temperature of non-operating mode, respectively.

$$\Delta T_b = \frac{\Delta T_a}{R_1 C_1} \cdot \{X + Ye^{-\alpha t} + Ze^{-\beta t}\} \tag{11}$$

Fig.12 shows the comparison between the internal temperature estimated by *TVM* and the internal temperature calculated from surface temperature by equation (11). In the result of 0-20% operating rates, the error between calculated and estimated temperatures is less than about 3℃. This result shows the validity of temperature estimation. However, the error increases over 30% operating rates. This might be the assumption value out of the *V* range by the effect of IR-drop. The estimated voltage of over 30% operating rates is large as shown in Fig.10. This value is beyond corresponding *V* range of the estimation equation. As a result, the error of estimated temperature increased as shown in Fig.12.

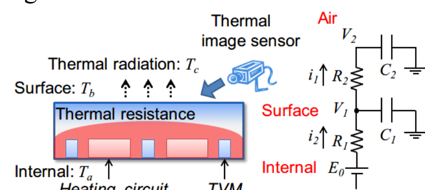


Figure 11. Internal, Surface and Air Temperature Model

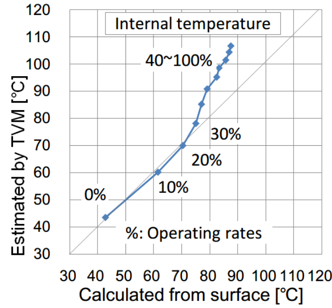
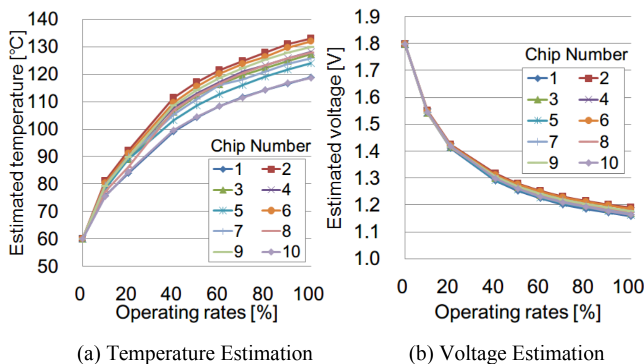


Figure 12. Validity of Temperature Estimation

E. *Evaluation by TEG Chip*

T and *V* at each *TVM* location were estimated from the measured frequencies in 10 chips. The initial measurement was performed at 0% operating rate of *Heating_circuits*. First, the effects of the process variation of chips are reduced using the proposed calibration technique as shown in Section 3.C. The parameter values of process variation are defined from the initial measured frequencies comparing to the values of *SPICE* simulation. Then, *T&V* are estimated from difference between the initial and current frequencies with various operating rates. This experiment was performed for 10 chips.

Fig. 13(a) shows estimated temperature at one *TVM* for the 10 chips. Temperature increases corresponding to the operating rate increase. The difference of increasing rate for each chips are due to process variation of *Heating_circuits*. Fig. 13(b) shows estimated voltage in the same way as Fig. 13(a).



(a) Temperature Estimation (b) Voltage Estimation

Figure 13. Evaluation by TEG chips (10 chips, 1 Monitor)

VI. CONCLUSIONS

This paper proposed a flexible *T&V* monitor and its estimation techniques. This monitor is a soft monitor based on ring-oscillators and can be placed at various locations on a chip because no any analog circuits or reference current are required. A hierarchical estimation and process variation treatment enable measurement with high accuracy. The evaluations using *SPICE* simulation were performed for 180 *nm*, 90 *nm* and 45 *nm* technologies. In the 180 *nm* technology, temperature accuracy was improved from 3.21℃ to 0.86-0.94℃, and voltage accuracy was improved from 11.77 *mV* to 2.98-4.17 *mV* by the division technique. The experiment for TEG chips in 180 *nm* technology confirmed the feasibility of the monitor.

ACKNOWLEDGEMENT

This work is supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc. Cadence Design Systems, Inc., and Mentor Graphics, Inc. The TEG chips in this work have been fabricated in the chip fabrication program of VDEC, the University of Tokyo in collaboration with Rohm Corporation and Toppan Printing Corporation.

REFERENCES

[1] V. Reddy, et al., "Impact of Negative Bias Temperature Instability on Product Parametric Drift," Proc. of Int'l Test Conf., pp. 148-155, 2004.

[2] International Electrotechnical Commission, IEC61508, "Functional safety of electrical / electronic / programmable electronic safety-related systems," Ed.2.0, 2010-4, http://www.iec.ch/functionalsafety/.

[3] ISO26262 "Road vehicles -Functional safety-," First Edition, 2011-11.

[4] N. Kanekawa, et al., Dependability in Electronic Systems, Springer, ISBN 978-1-4419-6714-5, 2010.

[5] K. Shimamura, et al., "A Single-Chip Fail-Safe Microprocessor with Memory Data Comparison Feature," Proc. of Pacific Rim Int'l Symp. on Dependable Computing, pp. 359-368, 2006.

[6] O. Khan and S. Kundu, "A Self-Adaptive System Architecture to Address Transistor Aging," Proc. of Design Automation and Test in Europe, pp. 81-86, 2009.

[7] Y. Li, S. Makar, and S. Mitra, "CASP: Concurrent Autonomous Chip Self-Test Using Stored Test Patterns," Proc. of Design Automation and Test in Europe, pp. 885-89, 2008.

[8] H. Inoue, et al., "VAST: Virtualization-Assisted Concurrent Autonomous Self-Test," Proc. of Int'l Test Conf., paper 12.3, 2008.

[9] Y. Sato, et al., "DART: Dependable VLSI Test Architecture and Its Implementation," Proc. of Int'l Test Conf., paper 15.2, 2012.

[10] Y. Sato, et al., "A Circuit Failure Prediction Mechanism (DART) for High Field Reliability," Proc. of Int'l Conf. on ASIC, pp. 581-584, 2009.

[11] Y. Miura, et al., "On-chip Temperature and Voltage measurement for Field Testing," Digest of European Test Symp., p. 204, 2012.

[12] N. Dutt and J. Henkel, "Temperature- and Process Variation-Aware Dependable Embedded Systems," 18th Asia and South Pacific Design Automation Conference, Tutorial 3, 2013.

[13] S. Remarsu and S. Kundu, "On Process Variation Tolerant Low Cost Thermal Sensor Design in 32nm CMOS Technology," Proc. of Great Lakes Symp. on VLSI, pp. 487-492, 2009.

[14] S, Kaxiras, P. Xekalakis, "4T-Decay Sensors: A New Class of Small, Fast, Robust, and Low-Power, Temperature/Leakage Sensors," Proc. of Int'l Symp. on Low Power Electronics and Design, pp. 108-113, 2004.

[15] Z. Abuhamdeh, V. D'Alassandro, R. Pico, D. Montrone, A. Crouch, A. Tracy, "Separating Temperature Effects from Ring-Oscillator Readings to Measure True IR-Drop on a Chip," Proc. of Int'l Test Conf., paper 11.2, pp. 1-10, 2007.

[16] G. M. QUENOT, N. PARIS, B. ZAVIDOVIQUE, "A Temperature and Voltage Measurement Cell for VLSI Circuits," Proc. of Euro ASIC '91, pp. 334-338, 1991.

[17] I. A.K.M Mahfuzul and H. Onodera, "On-Chip Detection of Process Shift and Process Spread for Silicon Debugging and Model-Hardware Correlation," Proc. of Asian Test Symp., pp. 350-354, 2012.

[18] J. Altet, et al.,"Dynamic Surface Temperature Measurements in ICs," Proc. of the IEEE, Vol. 94, Issue 8, pp.1519-1533, 2006.