A Flexible Power Control Method for Right Power Testing of Scan-Based Logic BIST

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Abstract— **High power dissipation during scan-based logic BIST is a crucial problem that leads to over-testing. Although controlling test power of a circuit under test (CUT) to an appropriate level is strongly required, it is not easy to control test power in BIST. This paper proposes a novel power-controlling method to control the toggle rate of the patterns to an arbitrary level by modifying pseudo random patterns generated by a TPG (Test Pattern Generator) of logic BIST. While many approaches have been proposed to control the toggle rate of the patterns, the proposed approach can provide higher fault coverage. Experimental results show that the proposed approach can control toggle rates to a predetermined target level and modified patterns can achieve high fault coverage without increasing test time.**

Keywords-component; **logic BIST; low power test; scan design; pseudo random pattern; scan shift power control.**

I. INTRODUCTION

It is well-known that scan test may suffer from power-consumption-induced problems during testing [1,2]. The toggle rate of flip-flops in both scan-shift and capture operations is higher than that in normal operation. Higher toggle rates may lead to high power consumption that causes excessive circuit delay or circuit destruction. Especially for logic BIST that uses pseudo random patterns as test patterns, high test power it a serious problem that must be solved.

Many works dealing with the test power of scan-based logic BIST have been done. The blocking technique blocks the propagation of signal value transitions at flip-flops to the combinational portion [3,4]. The segmentation technique divides a scan chain into several segments, and the reduction of test power is achieved by operating only some of segments concurrently in scan-shift operation [5]. Several methods reduce scan-in power by controlling the toggle rate of pseudo random patterns [6,7,13-15], adding to that some others manipulate a part of scan chains into a fixed value [8-10]. While the reduction of the toggle rate can lower power consumption, the randomness of test patterns decreases, resulting in fault coverage loss and/or test escape due to excessive capture power reduction. Some techniques have been developed for improving fault coverage. The vector inhibition technique removes test patterns that detect few faults [11]. The reseeding-based technique generates pseudo random patterns for detecting certain faults [12]. A test power controlling method has been proposed by using a *Pseudo-Low-Pass Filter* (*PLPF*) [13,15]. The *PLPF*, which takes a moving average of scan-in test sequence, reduces scan-in power by suppressing the toggle rate of pseudo random patterns before applying them to scan chains. The Multi-Cycle test technique increases the propagation probability of faults by conducting multiple capture operations between scan-shift operations and making use of partial observation [13,15]. A method has been proposed to reduce the scan-out power by changing flip-flop values before scan-out operation [16].

In order to avoid fault coverage loss or test escape in test power reduction, the toggle rate should be controlled so that test power does not become too high nor too low. As for the capture power, too low toggle rate may lead to test escape for delay faults because there are some toggles even in the normal operation. Methods are available for controlling switching activities of the circuit in capture operation through test generation [16,17]. As for the scan-shift power, an overly low toggle rate in scan-shift operation does not lead to test escape, but it reduces fault coverage. Therefore, scan-shift power should be controlled to an appropriate level, which depends on the circuit under test (CUT).

This paper proposes a method to control the toggle rate of pseudo random patterns to an arbitrary level. The method employs more than one *PLPF* proposed in [13,15] to modify the test patterns. The choice of *PLPF*s determines the toggle rate of the modified patterns. In order to control the toggle rate to a predetermined target scan-in power, the *PLPF* used is switched in scan-shift operation, and the switch timing is determined from the target scan-in power. Because there are multiple switch timings to control the toggle rate to a target scan-in power, the proposed approach chooses one that will lead to high fault coverage. In addition to the approach of modification with the *PLPFs*, this paper proposes an optimized circuit of the *PLPFs* that consists of fewer logic gates than previous methods [13, 15]. Although the *PLPFs* had been configured as a simple majority circuit, the *PLPFs* proposed in this paper are simplified by considering sequential behavior of the *PLPFs*.

Experimental results show that the proposed approach could control the scan-in power (toggle rate) evaluated by *WTM* (*Weight Transition Metrics*) [18] within 0.2% errors from the target level, and fault coverage of the *Basic Control approach* increased 0.81% from the simple use of a *PLPF*. If the proposed approach for fault coverage improvement is applied, fault coverage increased 7.6% from only the *Basic control approach*. Moreover, the area overhead of the optimized *PLPFs* was 66% lower than the original *PLPF* [13,15].

The rest of the paper is organized as follows: Section II introduces a scan-in power control method including *PLPF*s as the previous studies. Section III proposes the optimized *PLPF* structure and a method to control the toggle rate of

pseudo random patterns to the target level. Section IV shows experimental results of the proposed method in terms of toggle rates, fault coverage and area overhead. Finally, Section V summarizes the paper.

II. RELATED WORKS

The *PLPF* (*Pseudo Low-Pass Filter*) has been proposed for scan-in power reduction in logic BIST. Fig. 1 illustrates two types of *PLPF* design, one with 3 feedback inputs and the other with 5 feedback inputs [13]. It is inserted between a scan chain and a *PSF* (*Phase shifter for Filter*) that follows an LFSR. The *PSF*, which is composed of suitable EXOR gates to generate inputs for the *PLPF*, plays the role of a phase shifter. The *PLPF* reduces the toggle probability of an input sequence to the scan chain. Suppose that a *PLPF* has $2n+1$ input bits, S_{j-n}, S_{j-n+1}, … , S_{j-1}, T_j, T_{j+1}, … , T_{j+n-1}, T_{j+n}, where S_{j-k}, S_{j-k+1}, … , S_{j-1} are the past output values of the *PLPF* and obtained from flip-flops of the scan chain, T_j is a current output value of the *PSF*, and T_{j+1}, T_{j+2},…T_{j+n-1}, T_{j+n} are future output values of the *PSF*. When the number of *PLPF* input bits is 3 (i.e., n=1), the *PLPF* inputs are S_{j-1}, T_j, T_{j+1}. Some signal transitions of the original sequence T_j is suppressed by taking the moving average with a majority circuit in the *PLPF*.

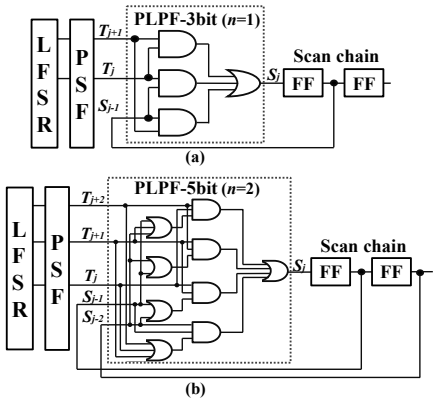
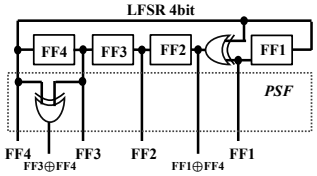


Fig. 1. Structure of *PLPF*-3bit (a) and 5bit (b)

Fig. 2 shows an example of the *PSF* structure for 4-bit LFSR that can provide input sequences for four scan chains. One EXOR gate is added to generate the future bit T_{j+2} for the scan chain 2 (SC2). The *PLPF* gets more and more complex by increasing the number of inputs.



	T_j	T_{j+1}	T_{j+2}
SC1	FF1	FF4	FF3
SC2	FF2	FF1 ⊕ FF4	FF3 ⊕ FF4
SC3	FF3	FF2	FF1 ⊕ FF4
SC4	FF4	FF3	FF2

Fig. 2. Example of *PSF* structure (LFSR-4bit)

III. PROPOSED SCAN-IN POWER CONTROL

As discussed above, the toggle rate of the scan-in patterns has been determined by using the *PLPF* circuit with n-bit inputs independently. In order to realize the flexible scan-in power control, it is a good way to combine the *PLPF* circuits with n-bit inputs into the TPG, and to generate many input sequences with different toggle rates by switching the *PLPF* circuits according to deterministic switch timings. In this section, we introduce a novel approach to control scan-in power flexibly. Section 3.1 shows the scan-in power control circuit which is composed of the optimized *PLPF*s and a multiplexer. It switches *PLPF* or *PSF* to control the average scan-in power during the scan-shift operation. Section 3.2 shows the proposed scan-in control approaches. We show 3 types of timing switch approaches for flexible scan-in power control.

3.1 Scan-in Power Control Circuit

3.1.1 Optimized PLPF

In order to achieve an optimal scan-in power control, this paper proposes a new design of *PLPFs* that consists of fewer logic gates than the original design but have the same power reduction capability as the original one. Fig. 3 shows the new *PLPF*.

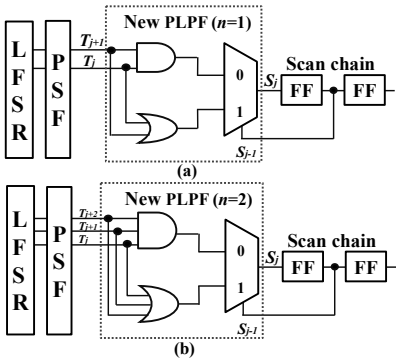


Fig. 3. Optimized *PLPF*s (a) $n=1$ (b) $n=2$

The current bit T_j and the future bit T_{j+n} which are outputs of the *PSF* are connected to the inputs of an OR gate and an AND gate, and the outputs of the OR gate and the AND gate are connected with the data inputs of a multiplexer. The input pattern of a scan chain is selected by the multiplexer controlled by the value of the past bit S_{j-1}.

The output value of the *PLPF* toggles when the value of the past bit S_{j-1} (the value of the first FF of the scan chain) is different from both input values T_j and T_{j+n} Thus, the toggles which occur at the current bit T_j and future bit T_{j+1} of the *PSF* can be ignored. The toggle rate of the output value of the *PLPF* can be calculated by the following formulas:

$$E_n = \sum_{n=1}^{n}(n+E_n)\frac{1}{2}^{n} + n\times\frac{1}{2}^{n} = 2^{n+1}-2 \quad (1)$$

$$T_n[\%] = \frac{1}{E_n} = \frac{1}{2^{n+1}-2} \quad (2)$$

where n denotes the number of inputs of the *PLPF* from the *PSF*, E_n denotes the average number of consecutive bits whose values are toggling except the state of all-zero and all-one, and T_n denotes the toggle rate of the output value of the *PLPF*. Fig. 4 shows the state transition diagram for the *PLPF* of n=1 where two tuples of each state denote the current state value S_j and the future *PSF* value T_{j+1} respectively, and the value attached to each directed edge

denotes the probability of state transition. Note that the original state transition diagram is described using 4 tuples S_{j-1}, S_j, T_j and T_{j+1}, but the diagram is minimized as shown in Fig. 4. The output value of the *PLPF* will toggle when the value of the current bit and the future bit are the same or the value of current bits and the past bits are different. Assume that the occurring probability of value 0 and value 1 are 0.5. Table 1 gives the expect toggle rate of the *PLPF* with different inputs. It can be seen that the toggle rate can be reduced by increasing the number of inputs, and the new *PLPF*s of n=1 and n=2 can achieve the same toggle reduction with the previous 3-bit and 5-bit *PLPFs* in [13], respectively. Compared to the previous *PLPF* structure, the proposed *PLPF* needs fewer gates to achieve the expected toggle rate, and the circuit is simple for DFT design.

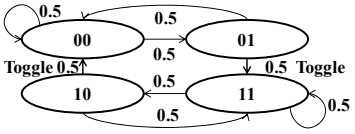


Fig. 4. State transition diagram of *PLPF*(n=1)

Table 1. Expected toggle rate of the *PLPF*

PLPF inputs	***E_n*:Expected Toggle**	***T_n*:Toggle rate[%]**
1 bit (n=0)	2	50
3 bit (n=1)	6	16.67
5 bit (n=2)	14	7.14
7 bit (n=3)	30	3.34

3.1.2 Scan-in Power Control Circuit

If only one *PLPF* is used for scan-in power reduction, the toggle rate is fixed for any circuit. If more than one *PLPF* is implemented, a toggle rate is determined by the choice of the *PLPFs*. Fig. 5 shows the structure of the scan-in power control circuit. While the structure of Fig. 5(a) uses individual *PLPFs*, the structure of Fig. 5(b) is optimized based on the proposed *PLPFs*. *PLPF Control Signals* in Fig. 5(b) are used to select one output value of the *PLPFs*. When both *PLPF Control Signals* are 1, the future bits are inactive and the value of the current bit T_j generated by the *PSF* is scanned into the scan chain. If both *PLPF Control Signals* are 0, the values of the future bits become active and are applied to the *PLPF* that enables the low power pattern generation. In this way, we can obtain test patterns with different toggle rates (*PSF*, *PLPF* of n=1 and *PLPF* of n=2) just by changing the values of the *PLPF Control Signals.*

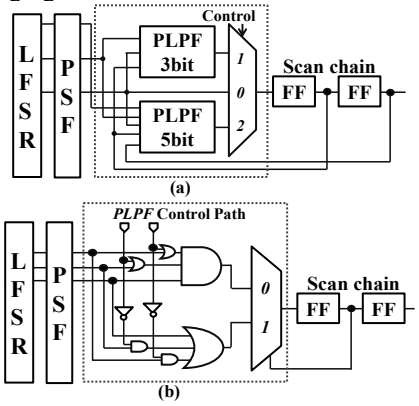


Fig. 5. Flexible scan-in power control circuit

3.2 Scan-in Power Control Approaches

By changing the *PLPF Control Signals* in the scan-shift operation, a flexible toggle rate can be achieved. There are many combinations of changing the *PLPF Control Signals* to achieve target test power. Thus, we should choose the switch timing of *PLPF*s to more controlled scan-shift (in and out) power and high fault coverage. During the scan-shift operation, it is known that more toggles occurring at the head part of a scan-in sequence to a scan chain can cause high scan-in power, and large toggles occurring at the tail part of a captured response can cause high scan-out power. Scan-out power is difficult to directly control but *PLPF*(n=2)'s test patterns expects some scan-out power reducing effect about 50→17.3% [14] as scan-in power reducing effect. Therefore, reducing the toggle rate for the head part and the tail part of the scan-in sequence should be effective to reduce the scan-shift power.

Moreover, it is reported that the fault coverage decreases as reducing the toggle rate of test patterns [6-10,12-15]. The reason is considered to be the low correlation between the values of FFs caused by the low toggle rate of test patterns. Therefore, it should be effective to improve the fault coverage by applying test patterns with high randomness (such as LFSR patterns) to the CUT.

To take a trade-off between power reduction and fault coverage improvement into account, generating a scan-in pattern that consists of the head and tail-part with a low toggle rate (generated by *NewPLPF*), and the middle part with high toggle rate (generated by *LFSR+PSF*) is expected.

This paper utilizes the scan-in power control circuit shown in Fig. 5(b) to generate test patterns in the order of *(PLPF* of n=2 → *PSF* → *PLPF* of n=2*)* to control the scan-in power and to prevent fault coverage loss. It is necessary to calculate timing to switch the pattern generation. There are two constraints for switch timing calculation: (1) for n-inputs *PLPF*, test vector including at least 2^{n+1}-2 bits (as shown in Table 1) is needed in order to achieve the expected power reduction. (2) Test vectors with low toggle rate (generated by the *PLPF*) need to be applied to the head and tail parts of a test pattern, respectively.

The timing parameters used to switch the pattern generation mode are defined as α, β and γ, where α denotes the length of the tail part, β denotes the length of the middle part and γ denotes the length of the head part for a complete scan-in sequence. The length of the scan chain is denoted by L, and $\alpha+\beta+\gamma$ equals to L. For a specified scan-in power, the switching timing α, β and γ can be calculated by formula (3).

$$WTM_{in}(t)=\frac{\sum_{i=1}^{\alpha} i\times 0.0714}{\sum_{j=1}^{L} j}+\frac{\sum_{i=\alpha+1}^{\alpha+\beta} i\times 0.5}{\sum_{j=1}^{L} j}+\frac{\sum_{i=\alpha+\beta+1}^{\alpha+\beta+\gamma} i\times 0.0714}{\sum_{j=1}^{L} j} \quad (3)$$

Note that *WTM* [18] is used to estimate the scan-in power. For a given WTM_{in}, a combination of (α, β, γ) which can achieve the closest scan-in power to WTM_{in} is used for power control. This paper proposes three approaches to control the *PLPF* for scan-in power control for different purposes.

1) Basic Control

In the *Basic Control approach*, the head part and the tail part, which take sequences generated by the *PLPF* of n=2, have the same length (α=γ) for all scan chains. Therefore, it is just needed to calculate the length (β) of the middle part (*PSF*) of the scan-in patterns. Fig. 6 shows an example. This approach is easy to apply, but high fault coverage cannot be guaranteed.

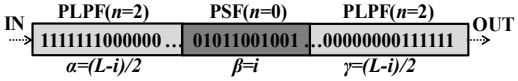


Fig. 6. *Basic Control approach*

2) Swap Control

In the *Swap Control approach*, the length of the head part α and the tail part γ are set to α=(L/2)-β and γ= L/2, respectively. And the values of α and γ will be swapped [(α, β, γ)→(γ, β, α)] between the scan chains with the odd and even numbers when generating a new scan-in pattern. Fig.7 shows an example. In this approach, random patterns from the *PSF* can be applied to more FFs (the range for applying *PSF* patterns is extended from β to 2β) on the scan chains that contribute to fault coverage increase. In addition, the peak power can be reduced due to the swapping of the head part α and the tail part γ which have a low toggle rate. However, this approach requires more additional circuitry to realize the swapping operation compared with the *Basic Control approach*.

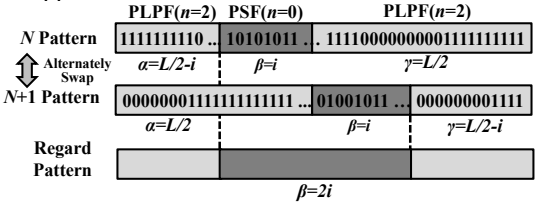


Fig. 7. *Swap Control approach*

3) Moving Control

The *Moving Control approach* focuses on achieving the most fault coverage improvement in scan-in power control. In the approach, the middle part with a high toggle rate will be moved bit by bit on the scan chain when generating new scan-in patterns. Fig. 8 shows an example. For a scan-in pattern N, the length of the tail part γ is set to j, and the length of the middle part β is set to i, then the length of the head part α will be (L/2)-i-j. When generating a new pattern N+1, the length of the tail part γ increases by 1 bit (γ = j +1), and the length of the head part α decreases by 1 bit (α=(L/2)-i-j-1). Thus, the middle part β can move from the tail to the head on the scan chain, and random patterns can be applied to all FFs (the range for applying *PSF* patterns is extended from β to L-2E_n(e.g. n=2:L-28)) on the scan chains that contributes to fault coverage improvement. However, this approach requires large additional circuits to perform the *Moving Control approach* compared to the *Basic* and *Swap Control approaches*.

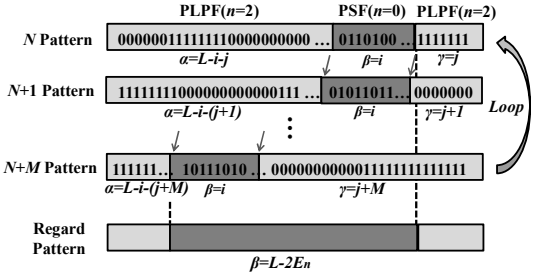


Fig. 8. *Moving Control approach*

IV. Experimental Results

4.1 Experimental Setup

We evaluated the proposed method using the *ISCAS89* and *ITC99* benchmark circuits. 30k test patterns (a test includes a scan-shift and a capture mode) were generated by a 16-bit internal type of LFSR (characteristic polynomial: $X^{16}+X^{15}+X^{13}+X^4+1$) from one seed (1010 ... 1010). A parallel scan structure, with scan-chain lengths of 100 to 200 FFs, was adopted. The primary inputs were fed by the patterns generated by another LFSR. Here, the primary outputs were not observed during BIST because the internal test speed is faster than that of an outside tester. A home-made fault simulator was used to calculate the single stuck-at fault coverage. *PSF* generated the future bits, however, it can be easily combined with an ordinal phase shifter. The scan-shift power was evaluated with the metric *WTM* (*Weight Transition Metric*) [18]. Here, WTM_{in} is the average scan-in power, WTM_{out} is the average scan-out power and *WTM* is the average scan-shift power of the test pattern, which is calculated as (WTM_{in} + WTM_{out}) / 2

4.2 PLPF Simulation Result

Table 2 shows the simulated WTM_{in} of the original *PLPF* and the *NewPLPF*, respectively. The proposed *NewPLPF* (n=1) and *PLPF*-3bit of previous studies [13, 15] show the same values. This confirms that the proposed *NewPLPF* has the equivalent function with the previous ones. On the other hand, *NewPLPF* (n=2) shows 0.11% lower WTM_{in} than the *PLPF*-5bit because the feedback value from the scan chain is reduced from two to one. And toggle rates of *NewPLPF* (n=2) are close to the theoretical values of Table 1 because previous *PLPF*'s patterns are rarely unstable by capture feedback values at first scan-shift operation and *NewPLPF* solve it.

Table 2. Toggle rate of individual *PLPFs* (WTM_{in})

Circuits	*WTMin[%]*				
	LFSR	*PLPF3bit (n=1)[13,15]*	*NewPLPF (n=1)*	*PLPF 5bit (n=2)[13,15]*	*NewPLPF (n=2)*
s9234	50.00	16.72	16.72	7.41	7.18
s13207	50.00	16.96	16.96	7.56	7.49
s15850	50.00	17.01	17.01	7.61	7.51
s38417	50.00	16.78	16.78	7.38	7.26
s38584	50.00	16.84	16.84	7.65	7.32
b14	50.01	16.97	16.97	7.60	7.51
b15	49.99	16.82	16.82	7.35	7.34
b20	50.00	16.68	16.68	7.19	7.15
b21	50.00	16.68	16.68	7.19	7.15
b22	49.99	16.78	16.78	7.33	7.28
Average	**50.00**	**16.82**	**16.82**	**7.43**	**7.32**

Table 3. Scan-in power result (*WTM*)

Circuits	CAP Ave.	Tagert WTM_{in}	Basic Control			Swap Control			Moving Control		
			ΔWTM_{in}	ΔWTM	$\Delta PEAK\ WTM$	ΔWTM_{in}	ΔWTM	$\Delta PEAK\ WTM$	ΔWTM_{in}	ΔWTM	$\Delta PEAK\ WTM$
s9234	27.81	17.81	-0.08	3.09	18.13	0.05	2.04	14.46	0.03	2.43	19.27
s13207	36.32	26.32	0.19	4.85	12.79	0.40	5.42	13.35	0.40	5.16	14.14
s15850	29.03	19.03	0.52	2.11	11.08	0.53	1.79	9.04	0.53	1.88	11.31
s38417	27.63	17.63	0.02	4.03	9.57	0.02	3.91	9.52	0.03	3.97	10.46
s38584	37.53	27.53	0.04	2.65	10.89	0.24	2.65	9.63	0.26	2.66	10.71
b14	13.14	13.14	-0.01	3.33	17.28	0.06	3.46	16.03	0.07	3.42	16.47
b15	5.95	5.95	0.09	0.58	6.42	0.13	-0.15	6.68	0.11	0.66	7.29
b20	13.08	13.08	0.09	2.13	11.52	0.09	2.23	10.98	0.10	1.99	12.32
b21	13.08	13.08	0.09	2.16	11.52	0.09	2.25	10.98	0.10	2.01	12.32
b22	13.12	13.12	0.04	1.93	9.61	0.12	1.97	8.93	0.13	2.04	10.15
Average	**21.67**	-	**0.10**	**2.69**	**11.88**	**0.18**	**2.56**	**10.96**	**0.18**	**2.63**	**12.45**

4.3 Simulation Result of proposed method

The column 3 of Table 3 shows the target scan-in power WTM_{in} of each benchmark. Although power analysis of CUT should be performed to assign the best target value, we defined it as the average capture power when random patterns are consecutively applied from the primary inputs as if in the user mode. However, as such power in ISCAS'89 was so high, target WTM_{in} was set 10% lower. As the control structure, *NewPLPF* (n=2) was used for each circuit except b15 whose target rate was so low of 7.14%. Then, *NewPLPF* (n=3) was used for b15. Table 4 shows the *PLPF* switching time combination of (α, β, γ) for scan-in power control, where SC denotes the length of scan chain, and the switching time (α, β, γ) of *Basic Control*, *Swap Control* and *Moving Control* are defined in the section III.

Table 4. Switch timing (α,β,γ)

Circuits	# FF of SC	Basic Control			Swap Control			Moving Control		
		α	*β*	*γ*	*α*	*β*	*γ*	*α*	*β*	*γ*
s9234	76	28	19	29	38	19	19	38	19	19
s13207	96	26	43	27	14	43	39	14	43	39
s15850	100	36	28	36	50	28	22	50	28	22
s38417	182	69	44	69	91	44	47	91	44	47
s38584	97	25	46	26	14	46	37	14	46	37
b14	82	35	11	36	41	11	30	41	11	30
b15	90	42	5	43	45	5	40	45	5	40
b20	98	42	14	42	49	14	35	49	14	35
b21	98	42	14	42	49	14	35	49	14	35
b22	92	39	13	40	46	13	33	46	13	33

Table 3 shows the simulation results of scan-in power WTM_{in} control where the switching times were set as shown in Table 4. All of the proposed approaches were able to achieve the target WTM_{in} within average 0.2% error. Furthermore, the *Swap Control approach* reduced the peak scan-shift power 0.92% lower than *Basic Control approach*'s because the power was differently controlled for each chain as shown in the previous section. On the other hand, the average peak scan-shift power of *Moving Control approach* worsened 0.57% than *Basic Control* because it doesn't consider peak scan-shift power. In each approach, the controlled *WTM* was nearly 2.6% higher than Target WTM_{in}. This shows the difficulty of controlling scan-out power. The figures in the table suggests that 2~3% lower Target WTM_{in} be used as a real application because we know WTM_{out} is 6% higher than WTM_{in} reported in [14, 15]. The authors have proposed a reduction method of scan-out power WTM_{out} in [14, 15], which was not used in this experiment.

Table 5 shows the simulation result of fault coverage by the proposed approaches. *Basic Control approach* improved 0.81% of average coverage compared with the *NewPLPF* (n=2) because the test patterns with higher toggle rate were input into scan chains. *Swap Control approach* achieved 1.77% higher fault coverage than *Basic Control approach*. *Moving Control approach* increased 7.6% compared with *Basic Control approach*. Especially, *Moving Control approach* achieved only 0.5% lower fault coverage than the original LFSR's because it has the most randomness among the three approaches.

Table 5. Fault coverage

Circuits	LFSR	New PLPF (n=2)	Basic Control	Swap Control	Moving Control
s9234	85.71	77.77	81.94	85.58	86.72
s13207	88.39	69.75	79.43	80.47	80.61
s15850	87.38	79.69	79.29	82	85.83
s38417	93.69	90.13	90.23	91.2	92.97
s38584	90.96	83.62	86.24	88.99	88.83
b14	84.61	79.42	79.22	79.49	89.4
b15	68.1	39.28	37.36	37.39	58.71
b20	83.95	81.35	79.61	80.55	88.92
b21	85.73	83.04	80.45	81.88	90.23
b22	85.22	80.53	78.95	82.88	86.45
Average	**85.37**	**76.46**	**77.27**	**79.04**	**84.87**

4.4 Area Overhead

Fig. 9 shows the area overhead of the proposed approaches and the other published approaches [6,10] for b22 benchmark circuit of ITC'99. In the experiment, the number of b22's scan chains was 9, and we evaluated the additional circuit's area after logical synthesis by Synopsys Design Compiler using ROHM 0.18μm CMOS technology. In *PLPF* [13,15], the area overhead was 0.88% for b22. On the other hand, that of *Basic Control*, the *Swap Control* and that of *Moving Control* approach was 0.3%, 0.38% and 0.67%, respectively. This means the 66% reduction from *PLPF's* by the *Basic Control approach*. The area is almost the same as *LT-RTPG's* [6], which has fixed controllability. It corresponds to maximum 70% reduction from *PRESTO's* [10].

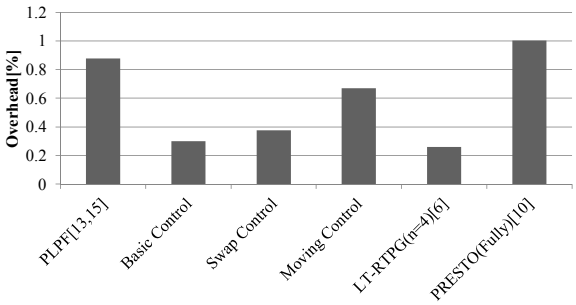


Fig. 9. Area overhead for b22 benchmark circuit

V. CONCLUSIONS

This paper proposes a novel scan-in power control circuit and flexible controlling approaches of the scan-in power. A new *PLPF* (*NewPLPF*) structure is introduced to reduce its hardware overhead and to achieve easy controlling. Three types of the approaches, *Basic*, *Swap* and *Moving* are proposed. All of the approaches control scan-in power of WTM_{in} within 0.2% error, and scan-shift power of *WTM* within 2.7% error. The *Basic Control approach* achieves the 66% circuit's area reduction from the original *PLPF's*. The average fault coverage of benchmark circuits show that *Basic, Swap and Moving approaches* achieve 0.81%, 2.58% and 8.41% increase respectively, from that of the conventional approach using the *NewPLPF*. The evaluation of area overhead shows *Moving Control approach* achieves the best coverage when the area overhead is not a big concern. The other two approaches can be available for the case when the area overhead is much concerned.

The authors' former researches indicate that the fault coverage can be further improved by combining the multi-cycle technique. More integrated evaluation is planned including capture power reduction and scan-out power reduction in the future work.

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REFERENCES

[1] M. Bushnell, V. Agrawal, *Essential of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits*, New York: Kluwer Academic Publisher, Nov.2000.

[2] P.Girard, N.Bicolici, and X.Wen, *Power-Aware Testing and Test Strategies for Low Power Devices*, Springer, ISBN 978-1-4419-0927-5, New York, 2010.

[3] S. Gerstendorfer and H.-J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST," *Proc. ITC.*, pp. 77-84, 1999.

[4] A. Hertwig and H.-J. Wunderlich, "Low Power Serial Built-In Self-Test," *Proc. European Test Workshop*, pp. 49-53, 1998.

[5] L. Whetsel, "Adapting Scan Architecture for Low Power Operation," *Proc. ITC*, pp. 863-872, 2000.

[6] S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BISTTPG for Low Heat Dissipation," *Proc. ITC*, pp. 85-94, Oct. 1999.

[7] X.Lin and J. Rajski, "Adaptive Low Shift Power Test Pattern Generator for Logic BIST," *Proc. ATS*, pp. 355-360, Dec.2010

[8] M. Filipek, Y. Fukui, H. Iwata, G. Mrugalski, J. Rajiski, M. Takakura and J. Tyszer, "Low Power Decompressor and PRPG with Constant Value Broadcast," *Proc. ATS*, pp. 84-89, 2011.

[9] J. Rajski, J. Tyszer, G. Mrugalski and B. N.-Dostie, "Test Generator with Preselected Toggling for Low Power Built-In Self-Test," *Proc. VLSI Test Symp.*, pp.1-6, April. 2012

[10] M. Filipek, G. Mrugalski, N. Mukherjee, B.-Dostie, J. Rajski, J. Solecki and J. Tyszer, "Low-Power Programmable PRPG With Test Compression Capabilities," *IEEE Trans. on VLSI systems*, Vol. 23, Issue 6, pp. 1063-1076, 2015.

[11] P. Girard, L. Guiller, C. Landrault and S. Pravossoudovitch, "A Test Vector Inhibiting Technique for Low Energy BIST Design," *Proc. VLSI Test Symp.*, pp. 407-412, 1999.

[12] C. V. Krishna and N. A. Touba, "Reducing test data volume using LFSR reseeding with seed compression," *Proc. ITC*, pp. 321-330, 2002.

[13] Y. Sato, S. Wang, T. Kato, K. Miyase, S. Kajihara, "Low Power BIST for Scan-Shift and Capture Power," *Proc. ATS*, pp.173-178, 2012.

[14] S. Wang, Y. Sato, K. Miyase and S. Kajihara, "A Scan-Out Power Reduction Method for Multi-cycle BIST," *Proc. ATS*, pp.272-277, Nov. 2012.

[15] S. Wang, Y. Sato, S. Kajihara and H. Takahashi, "Physical Power Evaluation of Low Power Logic-BIST Scheme Using Test Element Group Chip," *Journal of Low Power Electronics*, pp.528-540, 2015.

[16] X. Wen, Y. Nishida, K. Miyase, S. Kajihara, P. Girard, M. Tehranipoor, and L.-T. Wang, "On Pinpoint Capture Power Management in At-Speed Scan Test Generation," *Proc. ITC*, pp.1-10, Nov. 2012.

[17] X. Wen, "Power-Aware Testing: The Next Stage," *Proc. European Test Symposium*, May 29, 2012.

[18] R. Sankaralingam, R. R. Oruganti and N. A. Touba, "Static Compaction Techniques to Control Scan Vector Power Dissipation," *Proc. IEEE VLSI Test Symp.*, pp. 35-40 ,2000.