Low Power BIST for Scan-Shift and Capture Power

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Low Power BIST for Scan-Shift and Capture Power

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Abstract

Low-power test technology has been investigated deeply to achieve an accurate and efficient testing. Although many sophisticated methods are proposed for scan-test, there are not so many for logic BIST because of its uncontrollable randomness. However, logic BIST currently becomes vital for system debug or field test. This paper proposes a novel low power BIST technology that eliminates the specified high-frequency parts of vectors in scan-shift and also reduces capture power. The authors show that the proposed technology not only reduces test power but also keeps test coverage with little loss.

1. Introduction

The power density of latest LSIs rapidly increases because the circuit density increases steadily whereas the supply voltage cannot be reduced so much because of the difficulty in keeping its noise margin, especially, for memory cells [1]. Therefore, the power problem becomes a vital issue. Moreover, it is known that the power in testing is far higher than that in normal operation [2] and, therefore, the power problem is more serious.

The power problem has various aspects. For example, excessive current during scan-shifting causes an IR-drop issue, and in consequently, causes hold-time violations, which prevents correct scan-shift during flip-flops (FF). At-speed capture at FFs requires high speed current more than on-chip capacitance's supply and causes a voltage droop due to inductance. High temperature causes delay variations in the circuit under test .

Many approaches have been investigated deeply to tackle the problem. Software approaches [2], most of which are for scan-test, utilize don't-care (X) bits to reduce the number of toggles during scan-shift (low-shift-power X-filling) or in capture. Hardware approaches include a variety of methods, such as the inserting blocking circuitry [3-4] or the scan segmentation technique [5].

Logic BIST currently becomes vital for system debug or field test. To improve test quality for these purposes, at-speed testing is required and its test power should be carefully controlled. Although variety of methods is proposed for scan-test, there are not so many for logic BIST because its uncontrollable randomness makes software approaches difficult. Hardware approaches for scan-test still are available for logic BIST. However, the inserting blocking circuitry technique requires delay penalty for user paths and the power consumed at FFs, which might be 30-50% of the total area, is not reduced. The scan segmentation technique requires a complex clock control and capture power might not be reduced.

The combination approaches of software and hardware [6-8] propose the vector inhibition and selection techniques that focus on the ratio of care bits on a scan chain or on a block and ineffective ones are enabled with a mask logic or turning-off the clock. These techniques require huge simulation efforts and a sophisticated clock controlling.

Another approach [9-11] insert some logics between random pattern generators (e.g. LFSR: linear feedback signature register) and scan chain inputs so that their toggle rate will be very low. The paper [11] proposes a method that provides constant values into the specified ratio of scan-chains at a time. These methods reduce scan-shift power, but capture power reduction is not sure. Moreover, they cause test coverage decrease. Although our proposed approach is categorized in this approach, it also reduces capture power with little loss of test coverage. The approach inserts newly proposed pseudo low-pass filters that eliminate the specified high-frequency parts of vectors in scan-shift and also reduces capture power using the multi-cycle BIST scheme with partial observation [12].

This paper is organized as follows. Section 2 introduces the related works and discusses the pros and cons. Section 3 describes our proposed method. Section 4 shows the experimental data. Section 5 concludes the paper.

2. Related Works

Test power is divided into the following three in this paper.

- **Scan-in power**: The power consumed by scan-in vectors during scan-in and scan-out.
- **Scan-out power**: The power consumed by captured vectors during scan-in and scan-out.
- **Capture power**: The instantaneous power consumed by captured vectors at capture time.

As scan-in and scan-out are done concurrently, **scan-shift power** is defined as the sum of scan-in power and scan-out power. In case of the launch-off-capture (broad-side) delay test, the first capture is more important than the second capture because it affects propagation delays [2]. The following two methods are referenced for comparison.

Fig. 1 shows the concept of LT-RTPG [9]. The output *N* bits from LFSR go through an AND gate and toggle FF (T-FF). Then, the scan-in bit toggles when all of the N-bit values are 1, which should be small probability. In the

paper, N= 2 or 3 is recommended. It is proved that the fault coverage is guaranteed for large number of vectors. We refer this method as LT (N).

Fig. 2 shows the concept of ALP-RTPG [10], which is based-on LT-RTPG. There is a feedback from the last two scan-FFs (S-FF) on a scan-chain. The feedback may control scan-out power, which is not directly analyzed in the paper. N= 1 or 2 is recommended. We refer this method as ALP (N).

Fig. 3 shows the comparison of LT (2), LT (3) and the original LFSR. The shadowed cells show value 1 and white cells show value 0. Using an 8-bit LFSR, their output bits are plotted. Although LT (2) and LT (3) reduce toggles, it is seen that frequent toggles remain in some part. Furthermore, as almost half of the original bits are changed in LT (2 or 3), there is little correlation between LT's vectors and the original ones. The motivation of our work is generating low power vectors that have strong correlation to the original vectors, controlling both scan-in power and capture power.

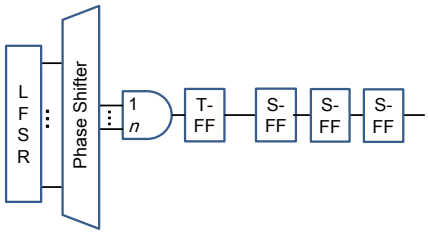


Fig. 1 LT-RTPG [9]

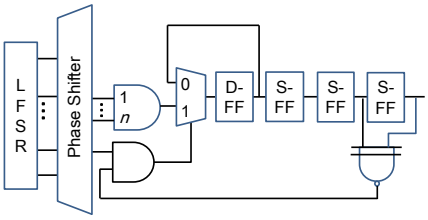


Fig. 2 ALP-RTPG [10]

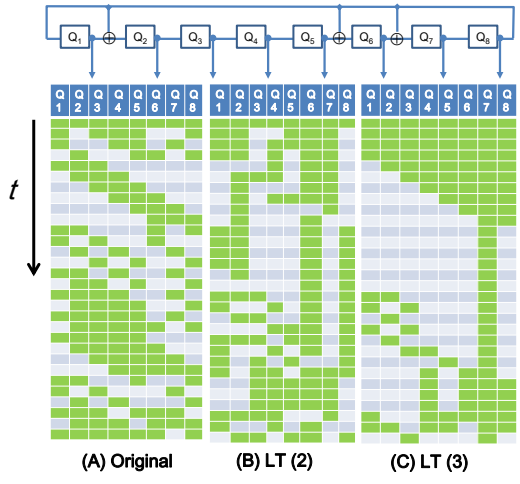


Fig. 3 Vector Comparison

3. Proposed Low Power BIST Method

3.1 Ideas and BIST Scheme

(a) Scan-in Power

Scan-in power reduction requires reducing a number of toggles in scan-chain. Let define f_1 as a pattern of repeated bits "01010101…," which has the most toggles. In the same way, f_2 be "001100110011…," which has the secondary many toggles in vectors of repeated bits. Seeing the vector in Fig. 4, some parts of f_1 patterns or f_2 patterns are found. It is apparent if these high frequency parts are removed from the vector, the number of toggles will be reduced in a convincing way. It suggests a kind of low-pass filter will be effective.

(b) Capture Power

The approach for scan-in power does not directly reduce the capture power. Therefore, another method should be combined together. It is reported that many capture cycles reduce its capture power [13]. As an excessive capture power causes timing issues during at-speed test, many captures with a slow timing might reduce the capture power without causing timing issues. Fig. 5 shows an improved capture timing scheme. The first M captures are applied with a slow timing and the last capture is applied with at-speed timing. However, a significant decrease of fault coverage is a concern. To tackle this problem, we utilize the multi-cycle BIST scheme [12] in Fig. 6. In the scheme, a part of FFs are directly observed using a compactor during many captures, which prevent the decrease of fault coverage. In the paper, the observation of 20% FFs are recommended with 2% area penalty. Fig. 7 is the proposed capture timing. The first M capture clocks are applied with a slow speed and the following N captures are applied with at-speed timing. A part of FFs are directly observed during M+N captures (in this case, the stuck-at faults can be detected in the first M captures while the delay faults are detected in the following N captures) or during the last N captures (in this case, only the delay faults are focused).

3.2 Metrics

We set the following metrics for our evaluation.

- **Scan-in power**: The part of the average weighted transition metric (WTM) [2] that is related to the scan-in vector is used. The formulation for a test vector t_i is shown in the following.

$$WTM_{in}(t_i) = \frac{2\sum_{j=1}^{L-1}(t_{i,j} \otimes t_{i,j+1}) \times j}{\sum_{j=1}^{L-1} j} \quad (1)$$

where L is the scan chain length and $t_{i,j}$ is the j th bit of t_i. WTM_{in} is defined as the average of (1) for all the test vectors.

- **Scan-out power**: The formulation for a test response r_i is shown in the following.

$$WTM_{out}(r_i) = \frac{2\sum_{j=1}^{L-1}(r_{i,j} \otimes r_{i,j+1}) \times j}{\sum_{j=1}^{L-1} j} \quad (2)$$

where L is the scan chain length and $r_{i,j}$ is the j th bit of t_i. WTM_{out} is defined as the average of (2) for all the test response vectors.

- **Scan-shift power**: The average of WTM_{in} and WTM_{out} is used as the metric of scan-shift power. This is the same as the average weighted transition metric. The metric for test vector t_i and test response r_i will be as follows.

$$WTM(t_i, r_i) = \frac{1}{2}\left[WTM_{in}(t_i) + WTM_{out}(r_i)\right] \quad (3)$$

WTM is defined as the average of (3) for all the test vectors and the test responses.

- **Capture power**: A simple metric that measures the toggle rate at FFs is used for our evaluation. The metric for a test vector t_i and test response r_i will be as follows.

$$CTM(r_i) = \frac{1}{L}\sum_{j=1}^{L}(t_{i,j} \otimes r_{i,j}) \quad (4)$$

where L is the scan chain length and $t_{i,j}$ ($r_{i,j}$) is the j-th bit of t_i (r_j). *CTM* is defined as the average of (3) for all the test vectors and the test responses.

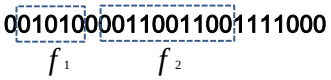


Fig. 4 High Frequency in a Vector

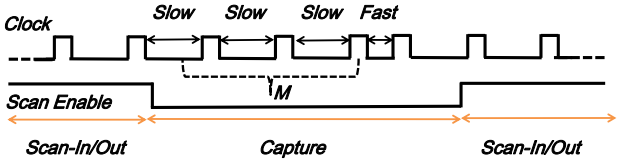


Fig. 5 Improved Capture Timing

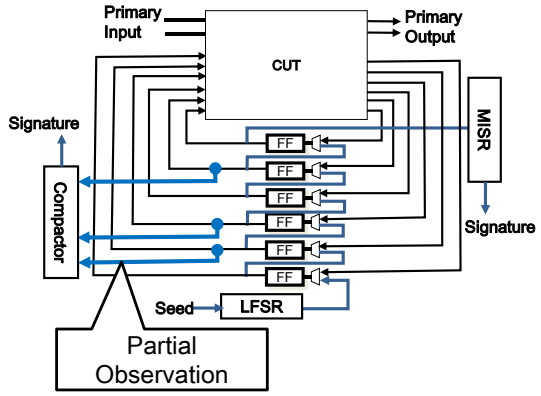


Fig. 6 Multi-Cycle BIST [12]

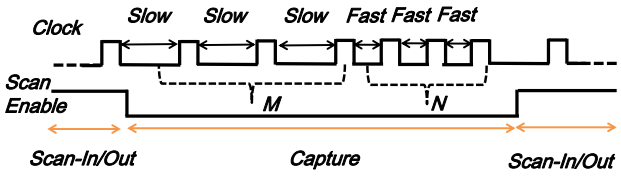


Fig. 7 Proposed Capture Timing

3.3 Structure of Pseudo Low-Pass Filter

Fig. 8 shows the overall proposed structure. We use a conventional linear feedback shift register (LFSR), which can be an internal type or an external type. The pseudo low-pass filter (PLPF) is proposed, which is a combinational circuit and generates a modified bit of S_i (i=1, L) from the 2k+1 bits inputs $S_{i,j-k}$, $S_{i,j-k+1}$, , , $S_{i,j-1}$, $T_{i,j}$, $T_{i,j+1}$, , , $T_{i,j+k-1}$, $T_{i,j+k}$. The past bits $S_{i,j-k}$, $S_{i,j-k+1}$, , , $S_{i,j-1}$ come from the scan chain connected to the PLPF through feedback loops and the current and future bits $T_{i,j}$, $T_{i,j+1}$, , , $T_{i,j+k-1}$, $T_{i,j+k}$ come from a kind of phase shifter (PSF: the phase shifter for filter). It is well-known that the future bits can be extracted using the current bits with a combinational logic. However, in case of 2k+1=3 or 5, PSF is very simple as shown later.

We define PLPF (2k+1) as a PLPF with 2k+1 bits. Fig. 9 shows the detailed structure of PLPF (3). The output bit $S_{i,j}$ is defined as the moving average (a low-pass filter) of the three input bits $S_{i,j-1}$, $T_{i,j}$, $T_{i,j+1}$. The moving average is the average of the past, current and future, which makes the sequence smoother and remove high frequency factors. Using this filter, f_1 (i.e. 010 or 101) components are completely eliminated. This function can be implemented based on the following equation.

$$S_{i,j} = (S_{i,j-1} \,\&\, T_{i,j}) \,|\, (T_{i,j} \,\&\, T_{i,j+1}) \,|\, (S_{i,j-1} \,\&\, T_{i,j+1}) \quad (5)$$

In the same way, f_2 (i.e. 001100 or 110011) components can be eliminated by PLPF (5), and f_k components can be eliminated by PLPF (2k+1) as proved in the following.

Definition 1 The output bit S_j of PLPF (2k+1) with inputs S_{j-k}, S_{j-k+1}, ... , S_{j-1}, T_j, T_{j+1}, … , T_{j+k-1}, T_{j+k} is defined as follows.

If sum of all input bits > k, then S_j =1; else S_j =0;

Theorem 1 The output vectors constructed of S_j of PLPF (2k+1) contain no f_l (l < k+1) components once it satisfies the following initial condition at some *j0*.

(A) *The sequence of {S_{j0-l} (l=1 to k+1)} has one or no toggle.*

Proof: In case of $T_j = S_{j-1}$: When all of S_{j-l} (l=1 to k+1) are the same, there are more than k+1 same values around (i.e. $l = j-k, j-k+1, \ldots, j-1, j, j+1, \ldots, j+k$) T_j, therefore, $S_j = S_{j-l}$ (l=1 to k+1). When $S_{j-m} \neq S_{j-m-1}$ (m < k+1), $S_{j-1} = S_{j-2} = \ldots = S_{j-m}$ and $S_{j-m-1} = S_{j-m-2} = \ldots = S_{j-k-1}$ from (A). As there are more than k+1 same values around S_{j-1}, they also exist around T_j. Therefore, $S_j = S_{j-l}$ (l=1 to m). In both case, (A) is kept.

In case of $T_j \neq S_{j-1}$: When all of S_{j-l} (l=1 to k+1) are the same, it is apparent that only the case of T_j=T_{j+l} (l=1 to k), $S_j = T_j$ (l=1 to k) and $S_{j+l} = S_j$ (l=1 to k). For S_{j+l} (l=1 to k), (A) is kept. When $S_{j-m} \neq S_{j-m-1}$ ($m < k$), $S_{j-1} = S_{j-2} = \ldots = S_{j-m}$ and $S_{j-m-1} = S_{j-m-2} = \ldots = S_{j-k-1}$ from (A). As there are more than k+1 same values around S_{j-1}, they also exist around T_j. Therefore, $S_j = S_{j-l}$ (l=1 to m). In both cases, (A) is kept. From the above discussion, it is shown that S_j toggles in only the case of k consecutive bits. *Q. E. D.*

Regarding the initial condition (A), as it is a loose restriction, it is satisfied soon in our experience. Fig. 10 and Fig. 11 show examples of PSF circuits for PLPF (3) and for FPLPF (5), respectively. In PLPF (3), the PSF constructs of only wire connections. Even in PLPF (5), the PSF constructs of small number of gates.

Fig. 12 shows the comparison with the original vector and the vector modified by PLPF (3). It is seen that the new vector is quite similar to the original one and only 17% bits are changed whereas nearly 50% bits are changed by LT (2) and LT (3). The ratio of 0 and 1 value are kept almost the same. These features are preferable because the experimental knowhow with the original vectors regarding such as fault coverage, power or reseeding information might be kept even in the new vectors.

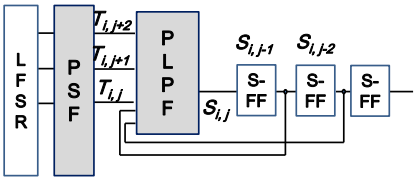
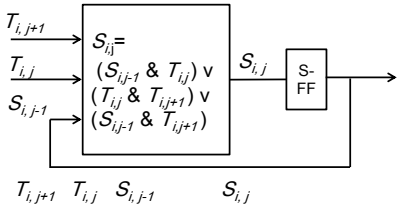


Fig. 8 Proposed Overall Structure



$T_{i,j+1}$	$T_{i,j}$	$S_{i,j-1}$	$S_{i,j}$
0,	0,	0	(0+0+0) /3 = 0/3 --> 0
0,	0,	1	(0+0+1) /3 = 1/3 --> 0
0,	1,	0	(0+1+0) /3 = 1/3 --> 0
0,	1,	1	(0+1+1) /3 = 2/3 --> 1
1,	0,	0	(1+0+0) /3 = 1/3 --> 0
1,	0,	1	(1+0+1) /3 = 2/3 --> 1
1,	1,	0	(1+1+0) /3 = 2/3 --> 1
1,	1,	1	(1+1+1) /3 = 3/3 --> 1

Fig. 9 Detail Structure of PLPF (3)

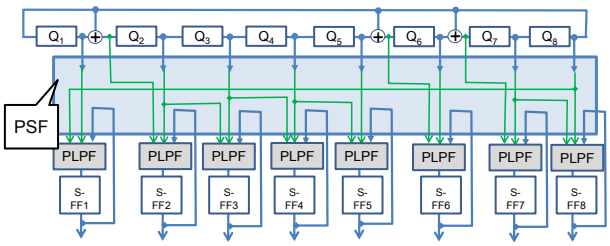


Fig. 10 PSF for PLPF (3)

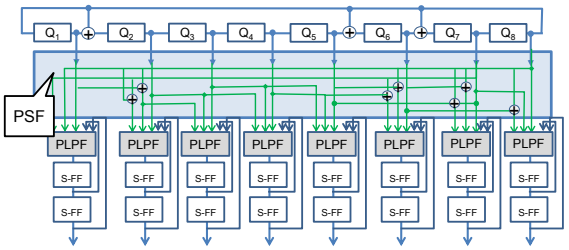


Fig. 11 PSF for PLPF (5)

Fig. 12 Vector Comparison

4. Experimental Results

4.1 Experimental Setup

The proposed technology was evaluated using the ISCAS89 and ITC99 benchmark. A 16-bit internal type LFSR (characteristic polynomial: $X^{16}+X^{15}+X^{13}+X^4+1$) and generated 30k vectors were used. A parallel scan structure with 100 FFs scan-chain is adopted. Primary inputs are also fed by a LFSR. Primary outputs are not observed during BIST. Multi-cycle BIST with M slow capture and N fast capture is used (we refer this scheme as Mul (M, N)). In the scheme, 20% of FFs are observed using the SCOPE-based selection [12]. An in-house fault simulator is used to calculate the single stuck-at fault coverage. For comparison purpose, consecutive bits of LFSR outputs are input to LT (N) (N=3, 4) or ALP (N) (N=2, 3) for the evaluation. Although inputs bits are not restricted to those in the original papers, this is done for convenience.

4.2 Scan-in Power Reduction

Table 1 shows the comparison of scan-in power reduction using Mul (0, 1) scheme. Here, "IN", 'OUT" and "Ave." show WTM_{in}, WTM_{out} and WTM respectively. "Peak" means the maximum of WTM (t_i, r_i). LT (3), ALP (2) and PLPF (3) achieve from 13 to 17% rate of WTM_{in}. LT (4), ALP (3) and PLPF (5) achieve from 7 to 8% rate of WTM_{in}. This shows that these two groups of methods should be selected according to the required grade of reduction rate. It is seen that WTM_{in} is well-controlled with LT and PLPF in variation of less than 0.7%. However, it is up to 4.6% variation with ALP. WTM_{out} is also reduced. However, its

amount differs greatly depending the circuit and usually is larger than WTM_{in} except s35932. The peak rate of WTM (t_i, r_i) is an important metric because the problem of IR-drop are caused vector by vector. PLPF (5) looks to have a good controllability of the peak power than others. However, it is still greater than twofold of WTM_{in}.

4.3 Capture Power Reduction

Table 2 shows the comparison of capture power reduction using Mul (N, 1) scheme, where N is set to 1, 15, 20 or 30. "Ave." shows CTM and "Peak" shows the maximum of CTM (r_i). The peak rate of CTM (r_i) is an important metric because voltage droop are caused vector by vector. It is easily seen that LT has a little effect of capture power reduction. ALP reduces CTM up to nearly 10%; however, it has also little effect of peak capture power reduction. Mult (N, 1) not only reduces CTM drastically (to 7.3% by PLPF (3) and 6.9% by PLPF (5)), but also reduces the peak capture power up to nearly 15%.

Fig. 13 shows the reduction curve of Mult (N, 1) for each data. Although, the effect of the proposed method is large, there are some data whose peak power doesn't reduce so much such as s35932 or b14s. Therefore, more improved technique is required for future.

4.4 Test Coverage Estimation

Table 3 shows the comparison of test coverage. Here, "Scan", "Cap." and "TC" show WTM, CTM and test coverage respectively. As referred in section 4.2, LT (3), ALP (2) and PLPF (3) achieve the similar WTM rate each other and LT (4), ALP (3) and PLPF (5) achieve the similar WTM rate each other too. PLPF (3) with Mult (10, 10) scheme and PLPF (5) with Mult (10, 10) scheme achieve nearly 10% better test coverage (in average) than LT or ALP. It should be noted that it is better than the original LFSR's (in average) even at low shift-power. For applying Mult (10, 10) scheme, it is reported that 2% area penalty/investment is needed [12]. The proposed power BIST technology achieves low scan-sift power and low capture power with high test coverage.

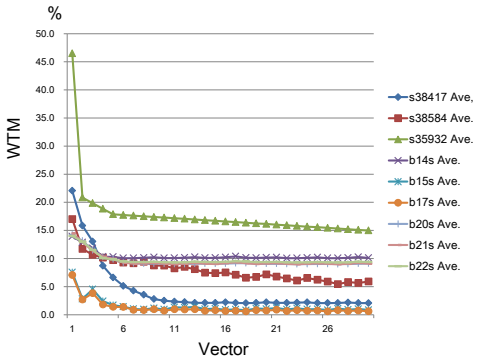


Fig. 13 Capture-Power Reduction with Mul (N, 1)

5. Conclusions

A novel low-power BIST technology, which controls scan-in power and capture power while keeping test coverage at high level, was introduced. The experimental data using ISCAS89 and ITC99 benchmark data showed both significant scan-in power reduction rate (the original rate of 50% is reduced to 7~8%) and capture power reduction rate (the original rate of 20% is reduced to 6~7%). The test coverage had little loss, or on the contrary some were improved using the multi-capture scheme. The possibility of controlling scan-shift power was also discussed and the experiments showed good controllability of scan-in power. However, the controllability of scan-out power remained in the future work. The peak power of scan-shift and capture, and the scan-out power are investigated in detail, which shows more improvement in future.

As logic BIST currently becomes vital for system debug or field test, the research on low-power BIST technology will contribute to the at-speed test in a system environment with safe power.

Table 1 Scan-In Power Reduction_ Mul (0, 1)

Circuit	LFSR				LT (3)				LT (4)				ALP (2)				ALP (3)				PLPF (3)				PLPF (5)			
	IN	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak	*IN*	OUT	Ave.	Peak
s38417	***50.2***	44.7	47.5	55.7	***12.9***	25.8	19.3	28.1	***6.6***	22.0	14.3	23.3	***14.0***	22.7	18.3	26.9	***7.4***	16.7	12.1	19.1	***17.0***	28.7	22.8	29.8	***7.5***	23.0	15.3	21.2
s38584	***50.4***	47.5	49.0	60.5	***12.9***	22.5	17.7	30.9	***6.6***	18.4	12.5	25.4	***14.2***	21.0	17.6	29.5	***8.0***	16.3	12.1	21.9	***17.2***	25.4	21.3	29.6	***7.6***	19.0	13.3	22.0
s35932	***50.3***	25.2	37.7	59.0	***13.0***	9.4	11.2	27.0	***6.7***	5.9	6.3	19.4	***14.1***	9.5	11.8	26.9	***7.7***	5.6	6.7	18.1	***17.1***	11.6	14.3	26.6	***7.6***	6.4	7.0	16.2
b14s	***50.4***	48.1	49.3	65.5	***13.4***	16.7	15.1	27.0	***7.2***	11.0	9.1	25.8	***18.6***	20.5	19.5	37.2	***10.0***	12.9	11.4	24.3	***17.5***	20.3	18.9	32.6	***8.1***	11.7	9.9	23.1
b15s	***50.5***	47.7	49.1	62.6	***12.9***	13.6	13.2	26.6	***6.7***	8.1	7.4	18.6	***15.8***	15.6	15.7	29.9	***8.6***	9.5	9.1	18.2	***17.1***	17.3	17.2	27.1	***7.6***	8.9	8.2	15.6
b17s	***50.2***	47.8	49.0	58.6	***13.1***	13.4	13.3	23.2	***7.0***	7.9	7.4	16.2	***14.1***	14.5	14.3	22.0	***8.0***	9.4	8.7	15.7	***17.2***	17.1	17.2	22.7	***7.8***	8.6	8.2	13.3
b20s	***50.5***	48.6	49.5	63.9	***12.8***	16.9	14.9	28.1	***6.6***	10.7	8.6	21.0	***15.6***	18.0	16.8	33.0	***8.3***	10.8	9.6	21.9	***17.0***	20.9	18.9	29.1	***7.4***	12.1	9.8	19.0
b21s	***50.5***	48.6	49.5	63.2	***12.8***	17.1	15.0	28.1	***6.6***	11.1	8.8	21.0	***15.6***	18.0	16.8	33.0	***8.3***	10.7	9.5	21.9	***17.0***	20.9	18.9	29.1	***7.4***	12.2	9.8	18.9
b22s	***50.5***	48.5	49.5	62.1	***13.0***	17.4	15.2	29.6	***6.8***	11.5	9.2	22.1	***14.3***	18.2	16.2	29.7	***7.6***	12.7	10.1	19.9	***17.1***	21.4	19.3	28.6	***7.6***	12.9	10.2	17.6
Ave.	***50.4***	45.2	47.8	61.2	***13.0***	17.0	15.0	27.6	***6.8***	11.8	9.3	21.4	***15.1***	17.5	16.3	29.8	***8.2***	11.6	9.9	20.1	***17.1***	20.4	18.8	28.4	***7.6***	12.8	10.2	18.5

Table 2 Capture Power Reduction_Mul (1/15/20/30, 1)

Circuit	LFSR		LT (3)		LT (4)		ALP (2)		ALP (3)		PLPF (3)								PLPF (5)							
											Mul (1,1)		Mul (15,1)		Mul (20,1)		Mul (30,1)		Mul (1,1)		Mul (15,1)		Mul (20,1)		Mul (30,1)	
	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak	Ave.	Peak
s38417	27.6	35.3	22.7	36.6	21.9	36.2	15.1	27.0	11.8	25.7	23.1	34.2	2.5	10.5	2.6	10.8	2.4	10.1	22.1	35.6	2.1	9.1	2.2	9.8	2.1	9.8
s38584	37.5	59.7	19.6	32.6	16.8	31.6	16.0	28.8	11.7	26.4	21.3	31.2	8.7	14.8	7.6	15.3	5.9	14.7	17.0	32.2	7.4	13.8	7.2	15.2	5.9	14.6
s35932	50.0	59.8	46.8	72.2	44.6	74.7	25.6	64.9	18.0	58.9	47.2	65.6	18.3	55.3	17.7	55.7	16.5	55.7	46.5	74.3	16.7	58.8	16.1	58.8	15.0	58.1
b14s	13.1	41.2	12.9	44.1	14.7	48.6	10.5	44.1	9.0	43.7	12.8	41.6	10.2	28.2	10.1	27.3	10.1	28.6	13.9	51.0	10.1	28.2	10.2	28.6	10.1	27.8
b15s	5.9	19.6	7.1	22.9	7.7	25.4	6.6	24.7	6.7	16.9	6.9	21.8	1.2	13.4	1.0	12.7	0.9	11.4	7.5	21.6	1.1	13.4	1.0	18.0	0.9	11.6
b17s	5.8	13.9	6.8	15.5	7.3	17.0	7.2	17.0	7.2	16.2	6.6	16.5	0.9	7.3	0.7	7.1	0.6	7.6	7.1	17.0	0.8	6.9	0.7	5.7	0.6	6.9
b20s	13.1	37.3	13.1	36.9	14.5	45.5	9.3	41.0	6.7	43.5	12.9	36.5	9.6	26.3	9.6	26.5	9.6	24.7	14.2	43.5	9.1	27.6	9.1	26.5	9.1	25.3
b21s	13.1	37.6	13.5	39.2	15.5	43.9	9.6	42.2	6.9	42.7	13.0	35.9	9.6	26.3	9.6	26.7	9.6	26.5	14.5	40.8	9.0	28.0	9.1	28.0	9.1	29.6
b22s	13.1	30.9	13.9	36.3	16.0	42.0	9.5	35.4	7.5	28.6	12.9	32.0	9.8	21.1	9.8	22.3	9.8	24.1	14.0	37.4	9.4	26.0	9.4	23.4	9.4	22.9
Ave.	19.9	37.3	17.4	37.4	17.7	40.5	12.2	36.1	9.5	33.6	17.4	35.0	7.9	22.6	7.6	22.7	7.3	22.6	17.4	39.3	7.3	23.5	7.2	23.8	6.9	23.0

Table 3 Test Coverage Evaluation

Circuit	LFSR			.LT (3)			ALP (2)			.PLPF (3) Mult (0,1)			.PLPF (3) Mult (10,10)			.LT (4)			ALP (3)			.PLPF (5) Mult (0,1)			.PLPF (5) Mult (10,10)		
	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*	Scan	Cap.	*TC*
s38417	47.5	27.6	***93.7***	19.3	22.7	***90.9***	18.3	16.1	***88.2***	22.8	23.1	***91.9***	19.7	2.6	***93.9***	14.3	21.9	***90.2***	12.1	11.8	***83.9***	15.3	22.1	***90.1***	13.3	2.2	***92.1***
s38584	49.0	37.5	***91.2***	17.7	19.6	***86.8***	17.6	16.0	***86.9***	21.3	21.3	***87.1***	18.7	7.6	***88.0***	12.5	16.8	***86.0***	12.1	11.7	***81.9***	13.3	17.0	***83.7***	13.3	7.2	***86.0***
s35932	37.7	50.0	***86.7***	11.2	46.8	***86.7***	11.8	25.6	***86.7***	14.3	47.2	***86.7***	17.2	17.7	***83.8***	6.3	44.6	***86.7***	6.7	18.0	***86.7***	7.0	46.5	***86.7***	11.4	16.1	***83.8***
b14s	49.3	13.1	***85.0***	15.1	12.9	***80.5***	19.5	10.5	***86.3***	18.9	12.8	***82.0***	20.7	10.1	***90.1***	9.1	14.7	***79.0***	11.4	9.0	***81.2***	9.9	13.9	***77.3***	12.8	10.2	***89.3***
b15s	49.1	5.9	***75.2***	13.2	7.1	***43.6***	15.7	6.6	***58.0***	17.2	6.9	***42.9***	19.2	1.0	***92.9***	7.4	7.7	***40.8***	9.1	6.7	***52.2***	8.2	7.5	***39.8***	11.0	1.0	***92.9***
b17s	49.5	5.8	***84.3***	14.8	6.8	***83.8***	16.8	7.2	***85.4***	18.9	6.6	***81.8***	20.9	0.7	***90.8***	8.6	7.3	***83.9***	9.6	7.2	***81.1***	9.7	7.1	***81.5***	12.7	0.7	***91.7***
b20s	49.0	13.1	***80.5***	13.3	13.1	***59.7***	14.3	9.3	***54.8***	17.2	12.9	***42.1***	18.0	9.6	***73.4***	7.4	14.5	***56.4***	8.7	6.7	***49.6***	8.2	14.2	***39.0***	9.4	9.1	***67.6***
b21s	49.5	13.1	***86.0***	15.0	13.5	***85.2***	16.8	9.6	***87.4***	18.9	13.0	***83.2***	20.8	9.6	***91.7***	8.8	15.5	***84.9***	9.5	6.9	***82.8***	.9.8	14.5	***82.7***	12.7	9.1	***92.4***
b22s	49.5	13.1	***85.3***	15.2	13.9	***84.3***	16.2	9.5	***85.9***	19.3	12.9	***82.1***	21.3	9.8	***90.6***	9.1	16.0	***83.2***	10.1	7.5	***81.4***	10.2	14.0	***80.4***	13.3	9.4	***91.4***
Ave.	47.8	19.9	***85.3***	15.0	17.4	***77.9***	16.3	12.3	***80.0***	18.8	17.4	***75.7***	19.6	7.6	***88.4***	9.3	17.7	***76.8***	9.9	9.5	***75.6***	9.1	17.4	***73.5***	12.2	7.2	***87.5***

References

[1] Int'l Technology Roadmap for Semiconductors, 2011 Edition, 2011.

[2] P. Girard, N. Nicolici and X. Wen, "Power-Aware Testing and Test Strategies for Low Power Devices," Springer, ISBN 978-1-4419-0927-5, 2010.

[3] S. Gerstendorfer and H.-J. Wunderlich, "Minimized Power Consumption for Scan-Based BIST," *Proc. Int'l Test Conf.*, pp. 77-84, 1999.

[4] A. Hertwig and H.-J. Wunderlich, "Low Power Serial Built-In Self-Test," *Proc. European Test Workshop*, pp. 49-53, 1998.

[5] L. Whetsel, "Adapting Scan Architecture for Low Power Operation," *Proc. Int'l Test Conf.*, pp. 863-872, 2000.

[6] F. Corno, M. Rebaudengo, M. S. Reorda and M. Violante, "A new BIST architecture for low power circuits," *Proc. European Test Workshop*, pp. 160-164, 1999.

[7] P. Girard, L. Guiller, C. Landrault and S. Pravossoudovitch, "A Test Vector Inhibiting Technique for Low Energy BIST Design," *Proc. VLSI Test Symp.,* pp. 407-412, 1999.

[8] C. Zoellin, H.-J. Wunderlich, N. Maeding and J. Leenstra, "BIST Power Reduction Using Scan-Chain Disable in the Cell Processor," *Proc. Int'l Test Conf.*, paper 32.3, 2006.

[9] S. Wang and S. K. Gupta, "LT-RTPG: A New Test-Per-Scan BISTTPG for Low Heat Dissipation," *Int. Test Conf.*, pp. 85-94, 1999.

[10] X. Lin and J. Rajski, "Adaptive Low Shift Power Test Pattern Generator for Logic BIST," *Asian. Test Symp.*, pp. 355-360, 2010.

[11] M. Filipek, Y. Fukui, H. Iwata, G. Mrugalski, J. Rajiski, M. Takakura and J. Tyszer, "Low Power Decompressor and PRPG with Constant Value Broadcast," *Asian. Test Symp.*, pp. 84-89, 2011.

[12] Y. Sato, H. Yamaguchi, M. Matsuzono and S. Kajihara, "Multi-Cycle Test with Partial Observation on Scan-Based BIST Structure," *Asian Test Symp.*, pp. 54-59, 2011.

[13] E. K. Moghaddam, J. Rajski, S. M. Reddy and M. Kassab, "At-Speed Scan Test with Low Switching Activity," *Proc. VLSI Test Symp.*, pp.177-182, 2010.