A Scan-Out Power Reduction Method for Multi-Cycle BIST

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Abstract- **High test power in logic BIST is a serious problem not only for production test, but also for board test, system debug or field test. Many low power BIST approaches that focus on scan-shift power or capture power have been proposed. However, it is known that a half of scan-shift power is compensated by test responses, which is difficult to control in those approaches. This paper proposes a novel approach that directly reduces scan-out power by modifying some flip-flops' values in scan chains at the last capture. Experimental results show that the proposed method reduces scan-out power up to 30% with little loss of test coverage.**

Keywords- low power; BIST; multi-cycle test; shift power.

I. INTRODUCTION

Power dissipation during test has become a vital issue in the latest process technologies. The increased power during test can cause several problems such as IR-drop which results in hold-time violation, or overheating which causes delay variation in the CUT or even damages the circuit [1].

Logic BIST is widely used for system debug or field test. For these purposes, at-speed testing is crucial to improve test quality. Therefore its test power should be carefully controlled. Although many power reduction approaches have been proposed for scan-test, there are not so many for logic BIST because of its uncontrollable randomness.

As the most of the software-based methods for scan test [1] such as utilizing don't-care (X) bits are not applicable to logic BIST, some hardware-based methods seem to be candidates, which include blocking circuitry inserting [2-3], scan segmentation technique [4], vector inhibition and selection techniques [5-7], and methods inserting some logics that control scan-in patterns [8-11].

Above all, [8-11] reduces both scan-shift power and capture power of logic BIST. Although they focus on controlling the scan-in patterns to achieve low switching activity in scan-in operation, it is known that a half of scan-shift power is compensated by test responses, which is difficult to control in their approaches. Sato, et al. [12] evaluated three methods [8-9, 12] and found that scan-out power was reduced indirectly, but the reduction amount was not enough compared to that of scan-in power. Therefore, an effective method of scan-out power reduction is strongly required.

In this paper, we propose a novel method that directly reduces scan-out power. The approach selects some flip-flops (FFs) that have less impact on test coverage from the scan chains, and fill them with proper values at the last capture so that the scan-out power will be reduced.

The remainder of this paper is organized as follows. In section 2, we introduce the related works and our previous work [12]. In section 3, we present our idea of scan-out power reduction and discuss the proposed approach. Section 4 shows the experimental data. Section 5 concludes the paper.

II. RELATED WORKS

Power consumed in test mainly consists of three parts: scan-in power, scan-out power and capture power. It should be noted that scan-in and scan-out operate concurrently. Therefore, scan-shift power is defined the sum of scan-in power and scan-out power. Many low power BIST approaches reduce scan-shift power by reducing the number of toggles in scan-in test patterns so that the switching activity during scan-in will be very low. In LT-RTPG [8], an AND gate and a toggle FF (T-FF) are inserted between LFSR and the input of a scan chain so that the scan-in bit will toggle only when all of the input values of the AND gate are one, which should be in small probability. This method reduces scan-in power directly and scan-out/capture power indirectly with the effect of scan-in power reduction. In [9], ALP-RTPG is proposed which is based-on LT-RTPG. There is a feedback from the last two scan FFs (S-FF) on a scan-chain. This feedback mechanism may control scan-out power. However, the effect of scan-out power reduction is not analyzed in the paper.

In [12], the authors proposed a low power multi-cycle BIST scheme, which is shown in Fig.1. A pseudo low-pass filter (PLPF) is inserted between LFSRs and the scan chain inputs, where PLPF is a combination circuit that works as a filter, which eliminates high frequency toggles in scan-in operations. In consequence, the scan-in vector will be smoother with low switching activity. PLPF generates a modified low power scan-in vector, which is the moving average of the past vectors (feedback from scan chain), current and future vectors (extracted by a phase shifter: PSF). In order to reduce the capture power, the multi-cycle test scheme [13] is combined, in which decrease of fault coverage is prevented by a partial observation of FFs during multiple capture cycles [14].

Fig.2 shows the comparison of scan-in power and scan-out power reductions in LT-RTPG, ALP-RTPG and PLPF for 6

ITC99 benchmark data. It shows that three methods achieve significant scan-in power reduction. Although the scan-out power is reduced, it is almost 2-times higher than the scan-in power. For further reduction of the scan-shift power (the sum of scan-in and scan-out power), the reduction of scan-out power is indispensable.

The motivation of our work is directly reducing scan-out power to achieve lower scan-shift power using our previous work of the low power multi-cycle BIST [12].

III. PROPOSED SCAN-OUT POWER REDUCTION METHODS

A. Idea of scan-out power reduction

Fig.3 shows the idea of scan-out power reduction. Some "controllable" FFs (denoted as "C") are selected and their values are modified at the last capture using an additional circuit to make the scan-out vector smoother. Here, a "controllable" FF means a FF in which modifying its value will affect very little test coverage. It should be noted that the power of the first capture affects delay propagation in the next time frame (i.e. the capture power is defined as that of the first capture). Therefore, the modification at the last capture will not affect capture power.

In the proposed scheme in Fig.1, a part of FFs are directly observed using a compactor during multiple captures. Such FFs are named as "observation-FFs" in this paper. The responses of CUT captured into observation-FFs are compressed into a compactor during multiple captures so that faults will be detected at each capture. Therefore, even if the values of the observation-FFs at the last capture are modified, the loss of test coverage will be little. It means that "observation-FFs" can be "controllable".

Moreover, it reported that the toggle rate of FFs at the last capture is reduced significantly, and many FFs do not switch at the last capture in most of patterns [13]. If a FF has very low switching frequency at the last capture, the transition delay faults (TDFs) may be difficult to be detected there. It suggests that such FFs may be "controllable".

Table1 shows the number of FFs with low switching frequency (#LSWF-FFs) and their TDF coverage contribution on ITC99 benchmarks. When a FF switches in less than 1% of 30k patterns at the last capture, it is defined as a low switching frequency FF (LSWF-FF). We performed a low power BIST [12] with 20 capture clocks using 30k test patterns and examined the ratio of LSWF-FF at the last capture and their TDF coverage contribution except observation-FFs. The results show that almost 60% of FFs are LSWF-FFs and the TDF coverage of LSWF-FFs is at a very low level. Therefore, LSWF-FFs are confirmed to be "controllable".

B. Flip-Flops selection

For reducing scan-out power and preventing test coverage loss, 20% of FFs are firstly selected as observation-FFs using the SCOAP-based selection method [14]. Then, LSWF-FFs are selected considering the following issues.

a. When the value of a LSWF-FF is always equal to its adjacent FF's at the last capture, the reduction will be in vain.

b. To prevent an increase of area overhead (area investment), a specified ratio of LSWF-FFs that are most effective for power reduction should be selected.

The proposed selection method of LSWF-FFs is as follows.

Step1. Perform logic simulation with 20 captures using 30k patterns in the scheme in Fig. 1. Compute the switching activity of each FF and compare the value with its adjacent FF's at the last capture. When they are different, the FF is registered in a list of candidates.

Step2. Select LSWF-FFs (i.e. switched in less than 1% of 30k patterns) from the list and multiply their toggle rate by a location number in a scan chain. The location number is counted from the first scan-out FF (i.e. =1) to the first scan-in FF (i.e. =the scan chain length).

Step3. For each scan chain, select the FF that has the largest number calculated in Step2, and repeat it until the ratio of selected FFs reaches the specified value.

In step2, a location number shows the contribution to the scan-out power of the scan chain in which the FF belongs, because the number of scan-out clocks of the FF is proportional to its location number.

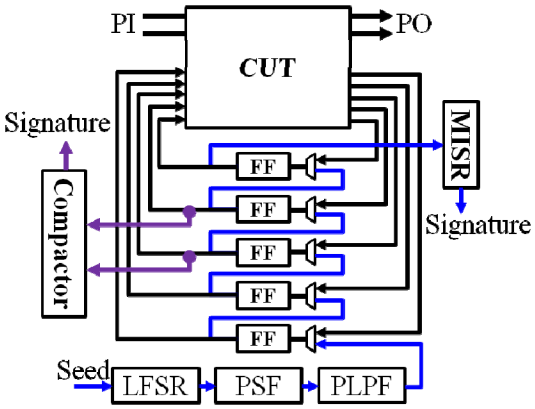

Fig. 1 Overall Structure of low power approach in [12]

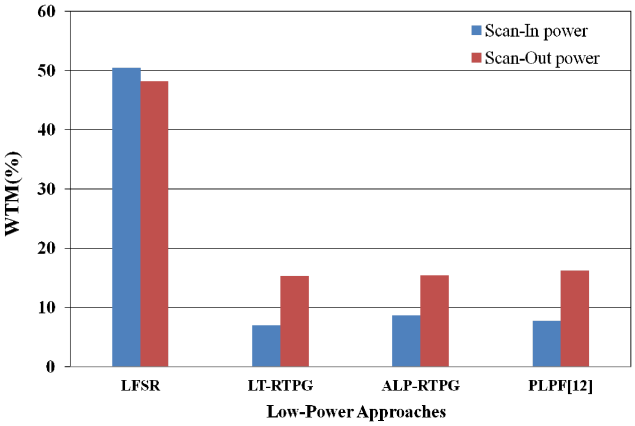

Fig.2: Comparison of scan-in/out power reduction

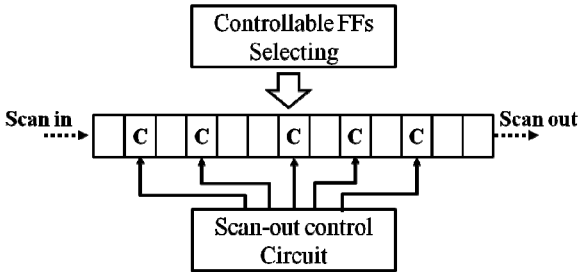

Fig.3: Idea of scan-out power reduction

Table 1: Low switching frequency FFs and TDFs detection contribution

circuit	#FFs	#LSWF-FFs	Ratio (%)	Average TDF Coverage (%)
b14s	245	140	57	0.12
b15s	449	284	63	0.14
b20s	490	273	56	0.10
b21s	490	286	58	0.11
b22s	735	464	63	0.05
AVE	482	289	60	0.09

C. Value filling for scan-out power reduction

a). Fixed-value filling

The selected FFs are filled with a fixed value (0 or 1) at the last capture. As 0 appears more often than 1 in scan-out empirically, 0-value is used as the fixed value. In order to control the FF values, two types of FF structures are proposed as shown in Fig.4 and 5. Fig.4 shows a control structure of observation-FF. The capture clock (CLK) and the last capture signal (LCAP) go through a NAND gate and generate a reset signal at the last capture. Fig.5 shows a control structure of LSWF-FF. An exclusive-NOR gate is added for observing the switching activity of FF, where the reset signal is set to 0 in case that no switching activity occurs (i.e. DI and DO are the same) at the last capture. A buffer is inserted between DO and exclusive-NOR gate to meet delay constraints.

The control structure for fixed-value filling is very simple and has small impact on area overhead. However, the method is not so effective for scan-out power reduction in some cases. Fig.6 shows an example. Suppose that the state of a scan chain at the last capture is "0011111011", where is a high frequency part of pattern f_1 "101". If two controllable FFs (denoted as "C") are selected for 0-filling, the scan-out vector becomes "0010111011". In this case, 0-filling does not eliminate f_1, instead produces a new high frequency pattern f_2 in the scan-out vector. To solve this problem, the following adjacent-value filling is proposed.

b). Adjacent-value Filling

Fig.7 shows the concept of the adjacent-value filling. A selected controllable FF (denoted as "C") is filled with the value of its adjacent FF that locates in the scan-in direction. This method dynamically fills the selected FFs with the values observed from the adjacent FFs so that high frequency patterns such as "010" will always be eliminated and the original low frequency part of patterns will be unaffected. Fig.8 shows an example, in which the same original vector in Fig. 6 is used. The selected controllable FFs (denoted as "C") are filled with the adjacent FFs' values at the last capture. It shows that the high frequency part of patterns in the original scan-out vector is eliminated, and also the low frequency patterns are not affected.

Fig.9 shows the control structure for observation-FFs. The capture clock (CLK) and the last capture signal (LCAP) generate a control signal through an AND gate to drive two NAND gates. The input DI of the adjacent FF is directly applied to one NAND gate and the other NAND gate though a NOT gate. The output of two NAND gates set the observation-FF to the same value as its adjacent FF's. Fig.10 shows the control structure for LSWF-FFs. An exclusive-NOR gate observes the switching activity in FF, and two NAND gates of the capture clock (CLK) and the last capture signal (LCAP) generates a control signal through two AND gates to activate the set or reset. When there is no switching activity in FF at the last capture, it is set to the same value as its adjacent FF's.

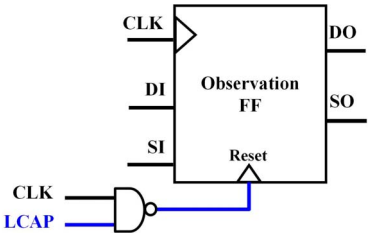

Fig.4 Control structure of observation-FFs for 0-filling

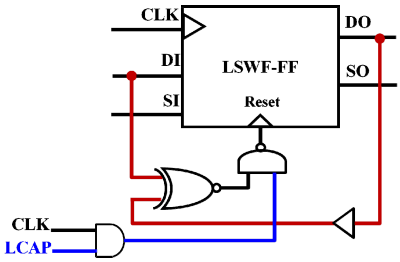

Fig.5 Control structure of LSWF-FFs for 0-filling

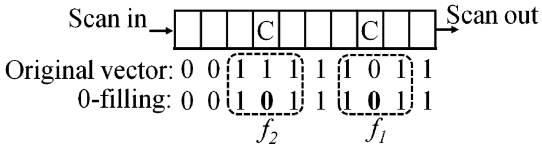

Fig.6 Scan-out power increased by 0-filling

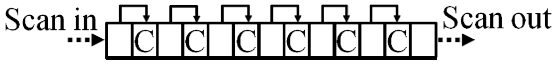

Fig.7 Concept of adjacent-value filling

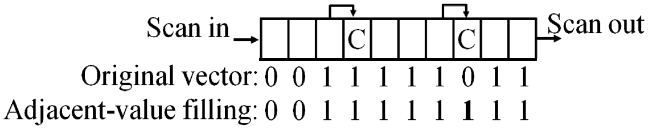

Fig.8 Example of adjacent-value filling

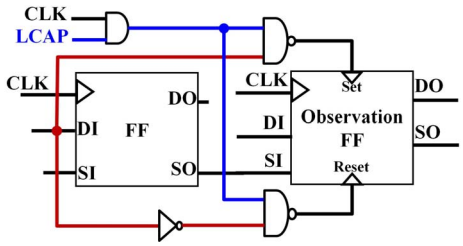

Fig.9 Structure of observation-FF for Adjacent-value filling

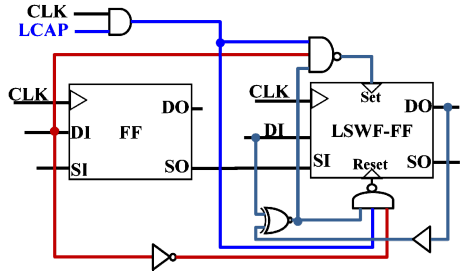

Fig.10 Structure of low switching frequency FF for Adjacent-value filling

Fig.11 shows a part of the distribution of selected observation-FFs (denoted as "O") and LSWF-FFs (denoted as "L") in scan chains of b14s circuit. It shows that many selected FFs are adjacent to each other. If we would feed adjacent observation-FFs or LSWF-FFs with the same FF's value, it should be more effective for scan-out power reduction. However, it would make difficult to control path delay between the FFs. To avoid such problem, the following modified selection method is proposed.

a. In case of an observation-FF, at most two FFs are fed by one adjacent FF's value synchronously.

b. In case of a LSWF-FF, one FF is fed by one adjacent FF.

The reason is explained in Fig.12. In case of an observation-FF (denoted as "O"), filling two adjacent FFs with the same value will not only eliminate high frequency part of patterns "010" but also eliminate "0110". However, in case of LSWF-FF, its value will be changed only when no switching occurs at the last capture. Then, feeding two LSWF-FFs by the same FF might produce a new high frequency pattern as shown in Fig.13. Suppose there are five LSWF-FFs (denoted as "L") in a scan chain and every two adjacent FFs are fed by one FF respectively. The vector is "1110101100" at capture N-1 and "1100011000" at the last capture N. Note that the 3rd and 6th bits are switched at the last capture so that their value will not be modified. Since the 4th and 7th bits are not switched at the last capture, they are filled with 1 and 0 respectively. After the filling, the scan-out vector will be "1101010000" where a high frequency pattern "010" is newly produced. To avoid this problem, in case of a LSWF-FF, one FF is fed by one adjacent FF.

D. Fault detection for scan-out control

Modifying the value of observation-FFs at the last capture will affect test coverage little because the responses of CUT captured into observation-FFs are directly observed by the additional compactor during many captures. However, for the selected LSWF-FFs, the value changes might affect the test coverage due to the modified scan-out responses. For accurate fault detecting, the recalculation of the expected responses and faulty responses is needed. Fig.14 shows the flow of computing the expected responses and faulty responses in the scan-out control. If the selected LSWF-FFs switch at the last capture in the fault-free circuit but do not switch in a faulty circuit, the fault might be missed in case that the modified value in the faulty circuit is equal to the non-faulty responses. If the selected LSWF-FFs do not switch at the last capture in the fault-free circuit but switch in a faulty circuit, the fault might be undetected in case that the faulty values are equal to the expected responses. Both cases are considered in the flow.

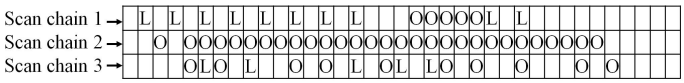

Fig.11 Distribution of selected FFs in scan chains

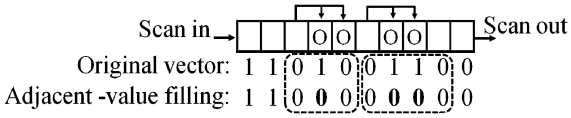

Fig.12 Feeding two observation-FFs by one FF

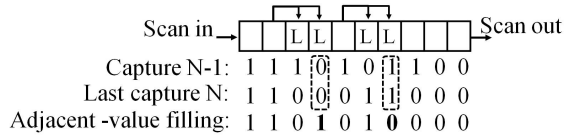

Fig.13 Feeding two LSWF-FFs by one FF

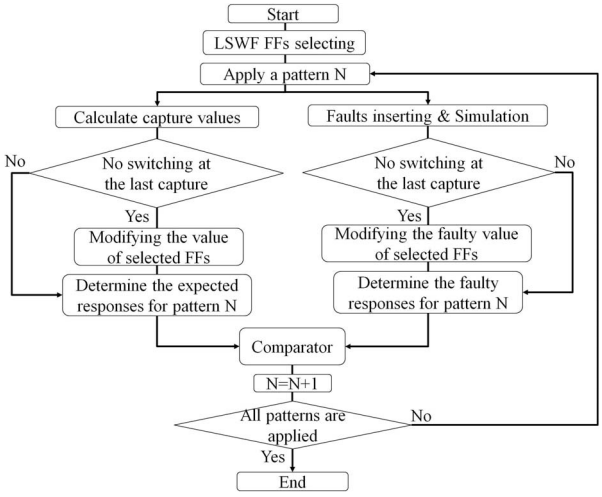

Fig.14 Expected responses and faulty responses computing

IV. EXPERIMENTS

A. Experimental step

We evaluated our proposed methods using ITC99 benchmark data. A 16-bit internal type LFSR (characteristic polynomial:

$X^{16}+X^{15}+X^{13}+X^4+1$) and pseudo low-pass filter (PLPF) in [12] are used to generate 30k vectors. A parallel scan structure with 100 FF-length of scan-chains is adopted (when # of FFs > 1600, 200 FF-length). A multi-cycle BIST with 10 slow-captures (focused on stuck-at faults) and 10 fast-captures (focused on delay faults) [12] is used. For scan-out power reduction, we select 20% of FFs as observation-FFs [14] and also selected 10% to 20% of FFs as LSWF-FFs for each scan-chain using the method in section 3. The weighted transition metric [12] is used for scan-shift power evaluation. A home-made fault simulator is used to estimate the single stuck-at fault coverage and transition fault coverage. The expected responses and faulty responses are calculated with the flow shown in Fig.14.

B. Scan-out power reduction

Table 2 shows the comparison of the 0-filling and the adjacent-value filling. Here, "In" and "Out" shows scan-in power and scan-out power respectively (For definition, see [12]). "20%" denotes the 20% of FFs in a chip are controlled, but in this case, only the observation-FFs are selected. "30%" and "40%" denotes that in addition of 20% observation-FFs, 10% and 20% LSWF-FFs are also selected for scan-out control. The original results of the low-power method without scan-out control [12] are shown in the second and third columns for comparison. Peak power reduction is very crucial because IR-drop or crosstalk is caused by high peak current. Therefore, we also evaluated the peak scan-out power and shift-power in Table 3, which are denoted by "P.Out" and "P.Shift", respectively.

Table 2 shows that the 0-filling reduces scan-out power of all circuit from the original 17.3% to 15.6% (i.e. 10% reduction) on average in case that 40% FFs are controlled. However, scan-out power is increased in b14s and b20s. The reason can be explained by Fig.6, some low frequency patterns in the original vector are broken and new high frequency patterns are produced by filling the selected FFs with 0. The adjacent-value filling shows better results. The scan-out power of all circuits is reduced from the original 17.3% to 15.2% (i.e. 12% reduction) on average by controlling 20% FFs, and is reduced to 14.4% (i.e. 17% reduction) as the ratio of selected FFs to 40% increases. Table 3 shows that both of the proposed methods reduced peak scan-out power and peak shift power. The peak scan-out power is reduced from the original 22.3% to 19.7% (i.e. 12% reduction) by the 0-filling method, and is reduced to 17.9% (i.e. 20% reduction) by the adjacent-value filling. Especially for b15s and b22s, almost 30% scan-out peak power is reduced by adjacent-value filling. As the scan-shift power is already at a very low level, nearly 30% reduction of peak power is a big advantage, which is not achieved by the conventional methods.

C. Test Coverage Estimation

Table 4 shows the comparison of test coverage for stuck-at faults (SA) and transition delay faults (TD) using the proposed two filling methods. It shows that no test coverage is lost in controlling the observation FFs. Even if select 10% and 20% LSWF-FFs for scan-out control, they have little loss of test coverage (2.5% transition fault coverage lost by 0-filling, 1% is lost by adjacent-value filling).

D. Area overhead (investment) Estimation

We evaluated the area overhead imposed by 0-filling and adjacent-value filling methods on a large data model that is based on the SoC model in the Test and Test Equipment chapter of ITRS2009 [15]. We consider that FFs in the SoC model are set-reset flip-flops for area overhead computing. As our scan-out power reduction approach is based on the multi-cycle BIST scheme, the additional compactor causes 1.95% area overhead with 20% FFs observation [14], which is included in our evaluation. Fig.15 shows the estimation. It shows that the 0-filling increases very little area overhead controlling 20% observation-FFs (one gate is needed for each FF), and also has less increase of area overhead when controlling more LSWF-FFs (4 gates are required for each FF). It should be noted that LSWF-FFs are not observed during multiple capture cycles so that there is no area overhead increase in the additional compactor. The adjacent-value filling causes 1.4% increase of area overhead controlling 20% observation-FFs (4 gates are required for each FF) and 6.0% for controlling the additional 20% LSWF-FFs (6 gates are required for each FF). Although the adjacent-value filling cost more area overhead, it achieves more power reduction and has less test coverage loss than 0-filling.

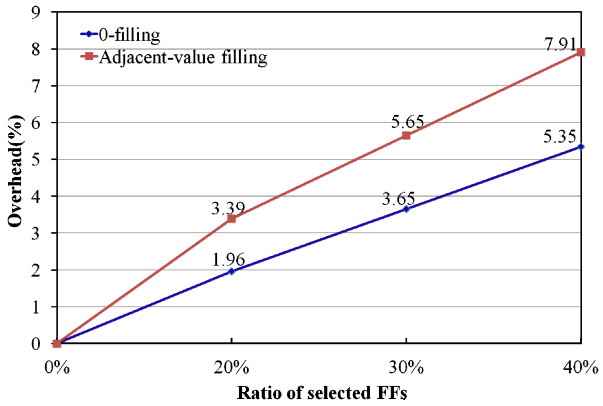

Fig.15 Area overhead (investment) estimation

V. CONCLUSIONS

In this paper, a novel approach that directly reduces scan-out power based on the multi-cycle BIST is proposed. Some FFs that have less impact on test coverage are selected and are filled with proper values so that the scan-out vector will be smoother. Two methods of the 0-filling and the adjacent value filling are proposed and are compared. The former has less area overhead and the latter has more power reduction and less coverage loss.

The experiment shows the effectiveness of the methods. The scan-out power is reduced to 14.4% (i.e. 17% reduction) with 40% FFs selection. The peak scan-out power is reduced to 17.9% (i.e. 20% reduction) and 30% reduction for some circuits. Test coverage loss is 1% for transition faults.

As the scan-out power is already at a very low level, nearly 30% reduction is a big advantage, which is not achieved by the conventional methods. Peak shift-power is very sensitive to the

timing issues such as a hold time error during scan-shifting, a very severe reduction is needed in the very deep submicron technologies. Then, the proposed approach will contribute to this problem. Since this paper is the first trial, the proposed selection methods and the modification methods have much room of improvement. This is remained for future work.

Table 2: Scan-out power reduction

Circuit	No SO Control [12]		0-Filling						Adjacent-value Filling					
			20%		30%		40%		20%		30%		40%	
	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT	IN	OUT
b14s	8.24	17.37	8.24	18.43	8.24	17.96	8.24	17.11	8.24	15.27	8.24	14.61	8.24	14.42
b15s	7.74	14.29	7.75	11.76	7.75	11.87	7.75	11.48	7.74	13.24	7.74	12.61	7.74	12.25
b20s	7.54	17.86	7.69	19.41	7.69	18.61	7.69	17.94	7.54	16.47	7.54	15.90	7.54	15.73
b21s	7.54	17.82	7.69	16.71	7.69	16.01	7.69	15.51	7.56	14.98	7.56	14.69	7.56	14.58
b22s	7.69	18.98	7.69	17.51	7.69	16.82	7.69	15.98	7.69	15.85	7.69	15.28	7.69	15.16
AVE	7.75	17.27	7.81	16.76	7.81	16.25	7.81	15.60	7.75	15.16	7.75	14.62	7.75	14.43

Table 3: Peak power evaluation

Circuit	No SO Control [12]		0-Filling						Adjacent-value Filling					
			20%		30%		40%		20%		30%		40%	
	P.Out	P.Shift	P.Out	P.Shift	P.Out	P.Shift	P.Out	P.Shift	P.Out	P.Shift	P.Out	P.Shift	P.Out	P.Shift
b14s	25.21	16.08	26.37	16.17	24.89	15.70	23.41	14.84	20.76	13.80	20.79	13.57	20.81	13.46
b15s	19.36	12.55	15.75	10.75	15.40	10.57	14.20	10.07	17.76	11.75	15.00	10.46	13.61	10.00
b20s	20.76	15.13	21.67	15.01	21.29	14.85	21.36	14.78	19.37	14.37	18.72	14.04	18.52	14.04
b21s	19.80	14.79	18.89	13.83	18.53	13.56	18.49	14.02	17.71	13.75	17.71	13.75	17.71	13.75
b22s	26.56	16.49	23.10	14.81	22.93	14.68	20.91	14.17	20.64	13.53	19.70	13.25	18.82	13.13
AVE	22.34	15.01	21.16	14.11	20.61	13.87	19.67	13.57	19.25	13.44	18.38	13.01	17.89	12.88

Table 4: Test coverage evaluation

Circuit	No SO Control [12]		0-Filling						Adjacent-value Filling					
			20%		30%		40%		20%		30%		40%	
	SA	TD	SA	TD	SA	TD	SA	TD	SA	TD	SA	TD	SA	TD
b14s	88.93	45.62	88.93	45.62	88.65	45.40	88.20	44.72	88.93	45.62	88.91	45.53	88.87	45.44
b15s	92.81	70.40	92.81	70.40	91.88	68.63	91.19	66.86	92.81	70.40	92.74	70.08	92.63	69.80
b20s	91.35	78.75	91.35	78.75	86.11	75.99	86.08	75.72	91.35	78.75	88.20	76.95	88.20	76.92
b21s	91.96	81.26	91.96	81.26	87.68	78.56	87.67	78.39	91.96	81.26	89.03	79.49	89.02	79.47
b22s	90.98	77.76	90.98	77.76	87.59	75.65	87.42	75.32	90.98	77.76	89.67	77.03	89.67	76.95
AVE	91.21	70.76	91.21	70.76	88.38	68.85	88.11	68.20	91.21	70.76	89.71	69.81	89.68	69.72

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