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High-throughput and full automatic DBC-module screening tester for high power IGBT

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Abstract

We developed a high-throughput screening tester for DBC-module of IGBT. The tester realizes a new screening test with current distribution in addition to a conventional switching test. It consists of a power circuit, a replaceable test head, sensor array module and digitizer with LabVIEW program. Therefore, all kinds of DBC-modules can be screened by switching the test head. The tester acquires magnetic field signals and displays GO/NOGO judgment automatically after digital calibration and signal processing in 10 seconds. It is expected to be applied for screening in a production line and analysis in order to prevent the failure of power modules.

1. Introduction: Proposal of new screening test

High performance Insulated Gate Bipolar Transistor (IGBT) modules are widely applied to various fields, such as hybrid electric vehicles (HEVs), railway traffic and wind power generation, and are becoming a key component of social infrastructure. Therefore, reliable IGBT modules are required. It is particularly important to prevent the imbalanced current in a chip or among chips triggering destruction due to partial high temperature or partial avalanche breakdown. Current distribution has already been reported, and research results suggest the high possibility of an imbalanced current [1-4]. However, the conventional screening tester does not employ a current distribution test.

We propose a new screening tester with current distribution in addition to the conventional screening test with a switching test. For the realization of the new screening by automatic GO/NOGO judgment, the high-throughput screening tester employs film sensor technology [5-8].

2. Screening tester configuration

The developed high-throughput screening tester consists of the following four components.

2.1. Power circuit for single/double pulse switching

The screening tester can test all kinds of Direct bonded copper module (DBC-modules) by replacing a test head. The maximum Direct-Current (DC) voltage is 1000 V, and the maximum current is 1200 A. There are five steps – from 50 μH to 500 μH – of load inductance for double pulse switching test. It also has a security mechanism comprised of overcurrent protection, an electric discharge switch, and an emergency stop button.

2.2. Replaceable test head

The test head is placed in the central part of the tester. Sensor array modules are mounted by arms and DBC-modules are placed on the stage (see Fig. 1). The stray inductance of the electric circuit is reduced to 29 nH by the special structure of the emitter/collector contact pins, parallel plate wiring and the close layout of the high side/Low side DBC-

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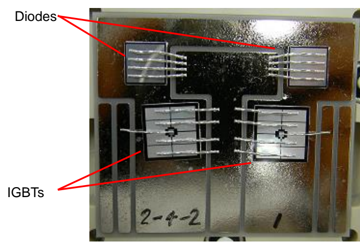
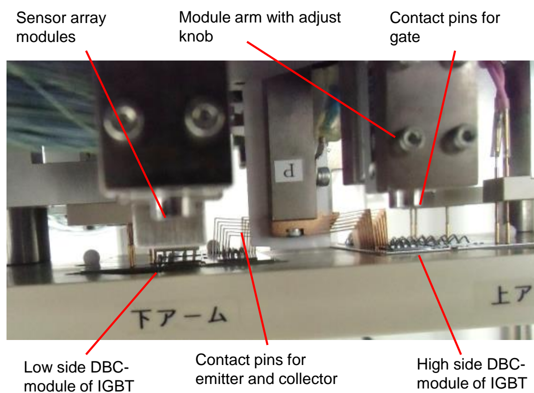


(a) DBC-module of 2 parallel IGBT



(b) DBC-modules of IGBT under the sensor modules

Fig. 1. DBC-module and test head in the tester.

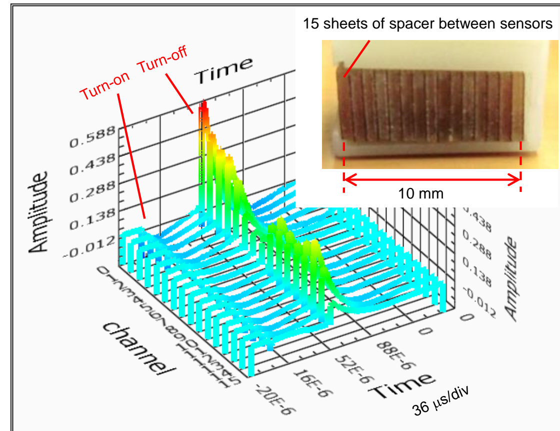
module of IGBT.

2.3. Flat sensitivity sensor array modules

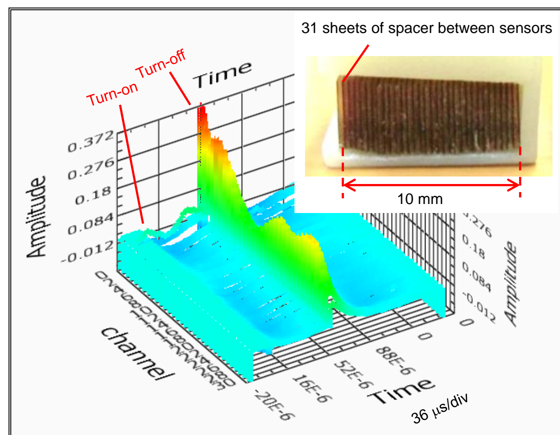
The sensor array module consists of 16 CH sensors with amplifiers by printed circuit board (PCB) technology, and is placed over the bonding wires of each chip. The special resolution of the imbalanced current is about 0.7 mm because the resolution is determined by the distance between sensors. The sensitivity of each sensor with an amplifier is about 100 mV/A. The sensitivity of the module is extremely flat because the original signals are digitally calibrated by LabVIEW program. Although analog amplifiers increase the signal to noise (S/N) ratio, the amplifier boards are directly affected by switching noise from near wiring and contact pins. So, the amplifier boards are surrounded by a shield case. Furthermore, to enhance spatial resolution, a 32 CH module has been developed on a trial basis (see Fig. 2).

2.4. Digitizer with LabVIEW program

The role of the digitizer with the LabVIEW program [9] is “digital calibration for sensor array



(a) 16CH sensor array module



(b) 32CH sensor array module on a trial basis

Fig. 2. Structure of sensor head and signal

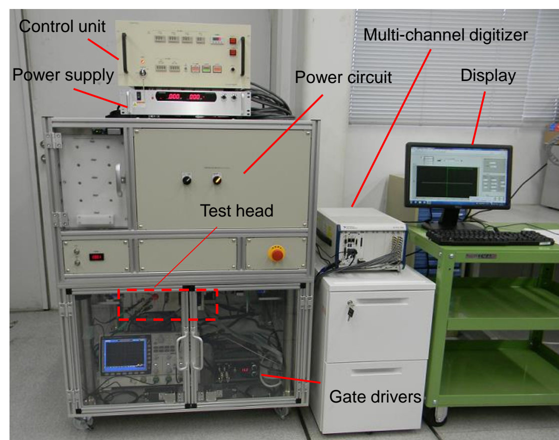
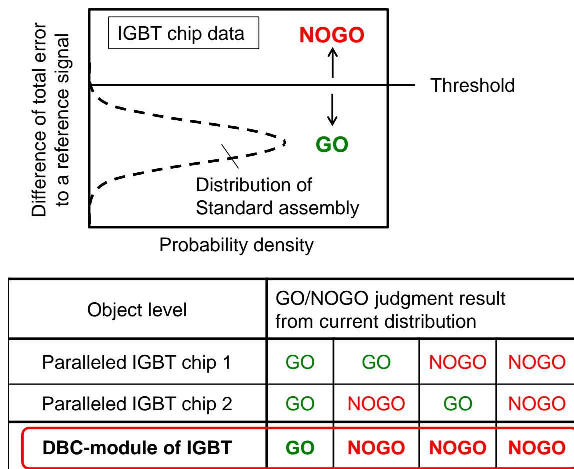


Fig. 3. DBC-module screening tester for IGBT.

module," "signal processing" and "display of GO/NOGO judgment" (see Fig. 3). Generally, a sensor array module has non-uniform sensitivity between sensors by electric parts (resister and capacitor and so forth) variations and/or module fabrication variations. So, the digital calibration is sufficiently effective to save hardware cost. Signal processing is also needed because of the cancellation of the noise effect and GO/NOGO judgment.



Object level	GO/NOGO judgment result from current distribution			
Paralleled IGBT chip 1	GO	GO	NOGO	NOGO
Paralleled IGBT chip 2	GO	NOGO	GO	NOGO
DBC-module of IGBT	**GO**	**NOGO**	**NOGO**	**NOGO**

Fig. 4. Proposed DBC-module screening test with current distribution (2 parallel IGBT case).

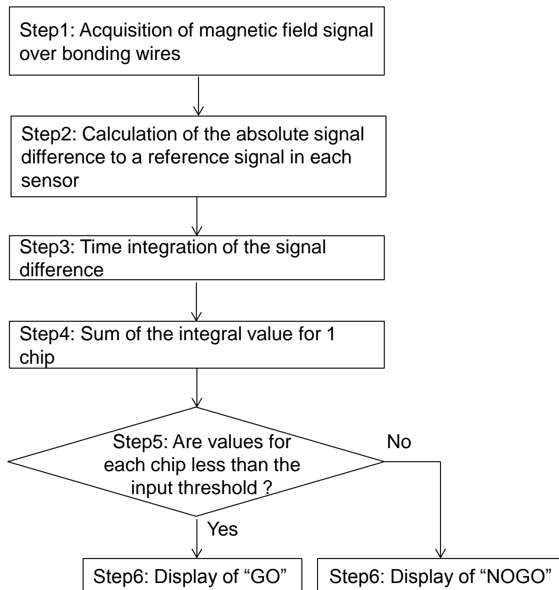


Fig. 5. GO/NOGO judgment procedure.

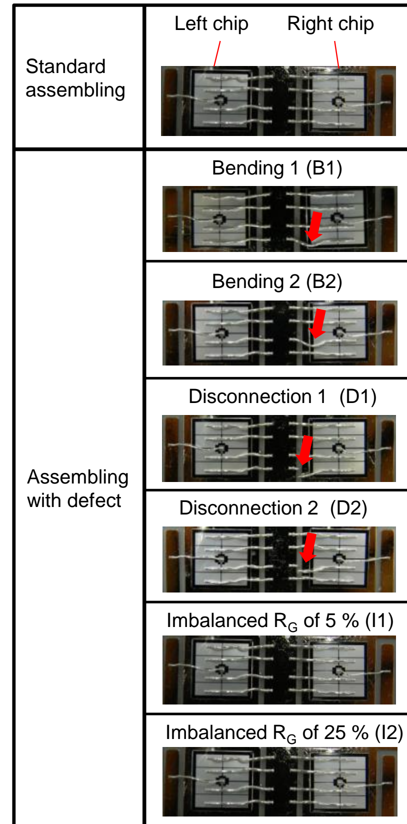


Fig. 6. DBC-module of IGBTs for experiment.

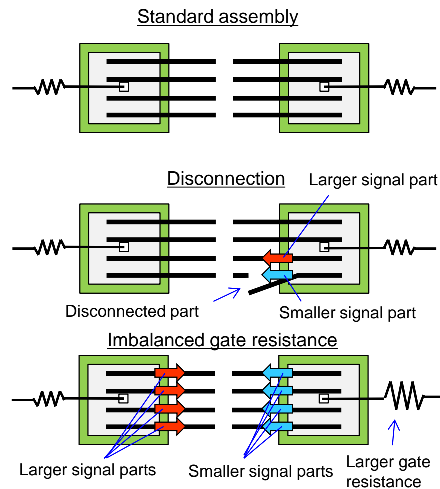
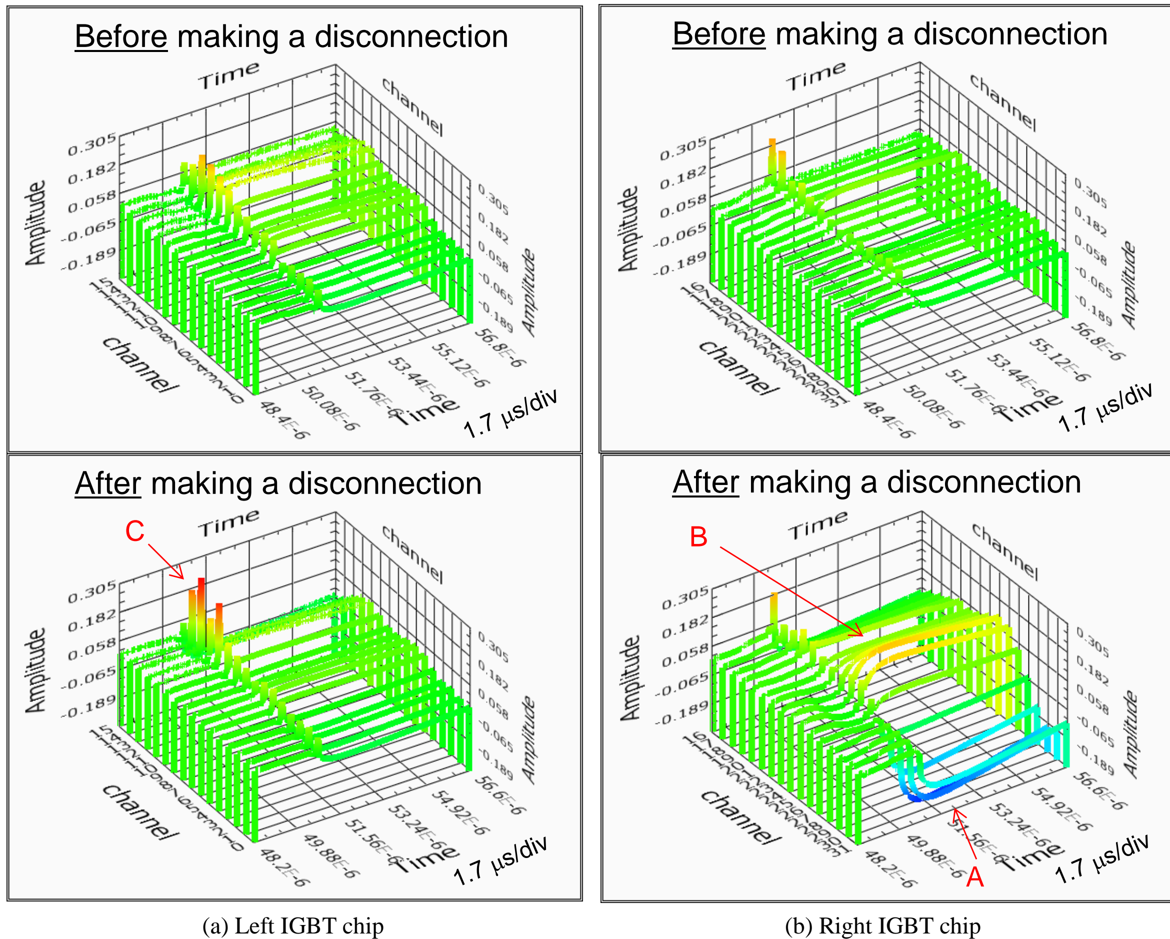


Fig. 7. Schematic view of differential signals of parallel IGBTs at turn-off.

3. Automatic GO/NOGO judgment



(a) Left IGBT chip

(b) Right IGBT chip

Fig. 8. Signal differences to reference signal (average signal) corresponding to disconnection 1 as shown in Fig. 6.

Automatic GO/NOGO judgment for the DBC-module of parallel IGBT is processed in 6 steps (see Fig. 4, Fig. 5). First, magnetic field signals over bonding wires are acquired (Step 1), and the absolute value of the signal difference to the reference signal is calculated to cancel the noise (Step 2). Then, the difference is integrated during the specified turn-off period (Step 3) and the integrated values for 1 chip are summed (Step 4). Finally, if the summed values for each chip are less than the input threshold, "GO" judgment is displayed. If the summed values are equal to a threshold or more, "NOGO" judgment is displayed (Step 5 and Step 6).

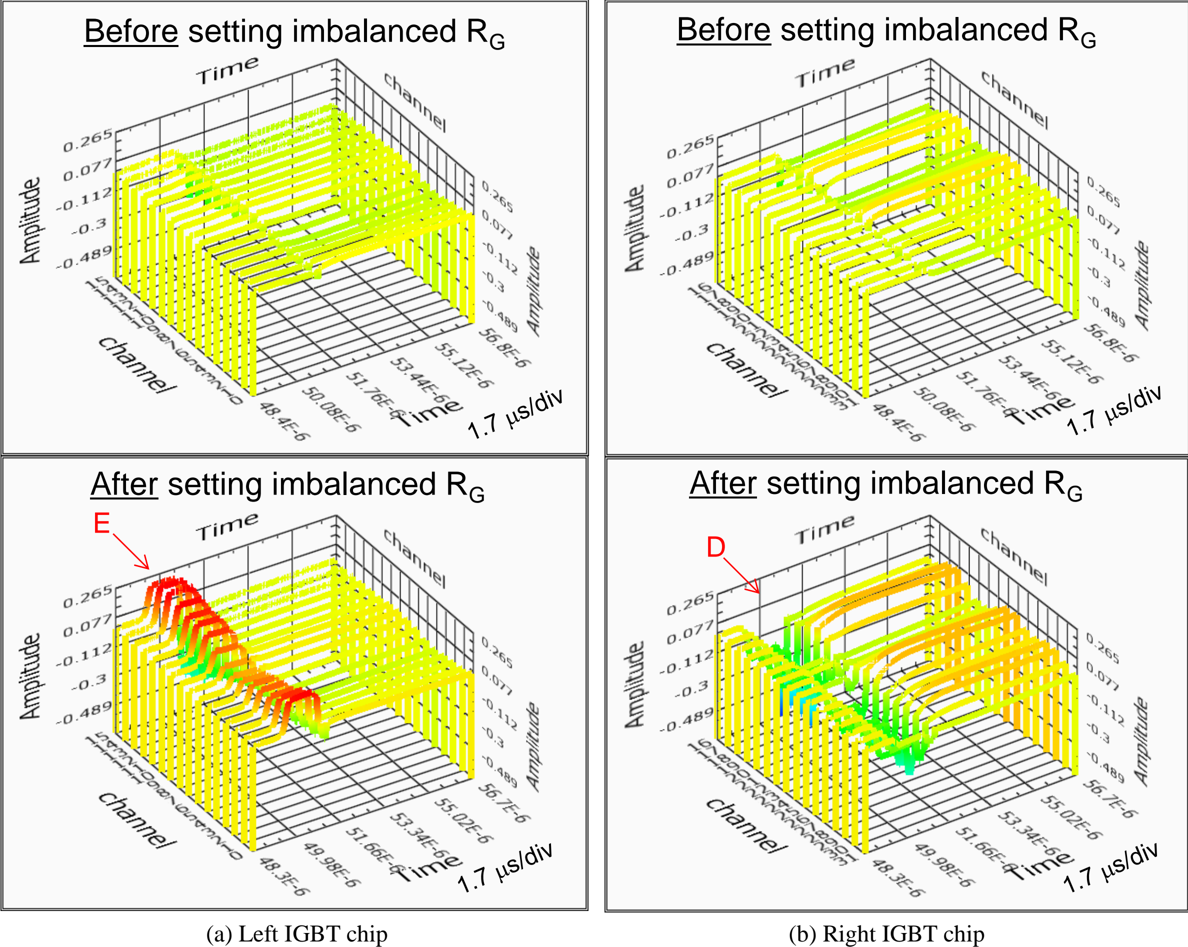
The GO/NOGO judgment was demonstrated by the DBC-module of 2 parallel IGBT chips with an original assembly (see Fig. 6). The switching test method was inductive load and single pulse. DC voltage and turn-off current were 100 V and 25 A respectively. After the signal acquisition with standard assembly, we prepared several defective IGBTs and acquired signals once again. The bending and the disconnection simulate defects in the assembly process. The imbalanced gate resistance simulates gate characteristics variations in chips such as a threshold voltage difference. For example, current does not flow in disconnected bonding wire and the diverted current through nearby bonding wire therefore the signals of the disconnected part are decreased and the signals of the nearby part are increased to standard assembly (see Fig. 7). In still other cases, the turn-off with larger gate resistance is derailed to the other turn-off therefore most signals are decreased with larger gate resistance and most signals of the other side are increased especially in the Miller period.

Before making any defects (under standard assembly), there is a little signal difference (see Fig. 8 (a) and Fig. 9 (a)). After making a disconnection (Fig. 8 (b)), the signal difference over the disconnection part is decreased (A), and the signal difference over another part in the same chip and another chip is increased by diverted current (B and C). And after setting imbalanced gate resistance (Fig. 9 (b)), the signal difference becomes extremely large during the Miller period for both IGBT chips (D and E)). The standard score in statistics is calculated from the sum of the difference as shown in Fig. 10 and Fig. 11. IGBT chip makers present different graphs. The results reveal that the standard score is sufficiently applicable to GO/NOGO judgment regardless of the chip maker. The result of GO/NOGO judgment is displayed with a standard score and a color image in the display in 10 seconds (see Fig. 12).

4. Conclusion

We developed a high-throughput screening tester to realize a new IGBT screening test. The tester acquires magnetic field signals and displays GO/NOGO judgment automatically after digital calibration and signal processing in 10 seconds. It is expected to be applied for screening in a production line and analysis in order to prevent the failure of power modules. We established statistics based GO/NOGO judgment this time. Next, we will take more data and investigate the relationship between the distribution and device reliability

Acknowledgements



(a) Left IGBT chip

(b) Right IGBT chip

Fig. 9. Signal differences to reference signal corresponding to imbalanced gate resistance of 25 %.

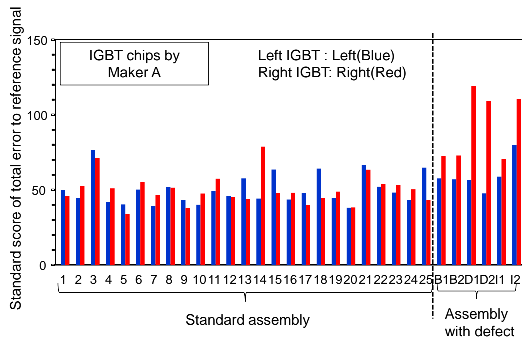


Fig. 10. Standard score in statistics for IGBT chip of maker A corresponding to IGBTs as shown in Fig. 6.

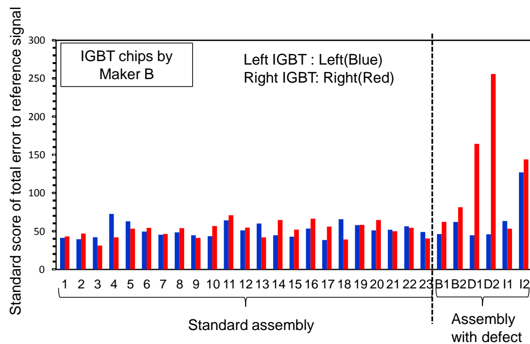
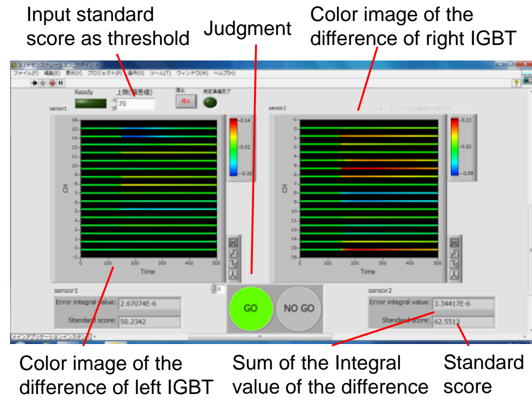
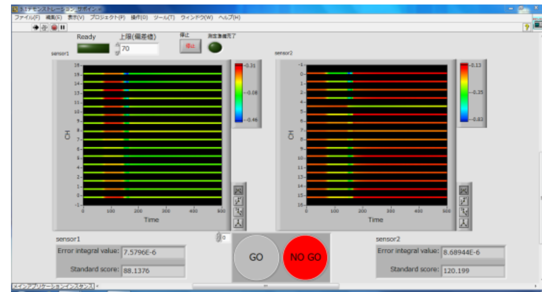


Fig. 11. Standard score in statistics for IGBT chip of maker B corresponding to IGBTs as shown in Fig. 6.



(a) Display for “GO” judgment



(b) Display for “NOGO” judgment

Fig. 12. Judgment display for imbalanced R_G of 25 %.

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References

[1] T. Domon, I. Omura, K. Kodani and T. Ogura, “Chip current measurement in IGBT modules,” IEEJ, pp. 7-8, 2004.(in Japanese).

[2] M. Babler, M. Munzer and S. Burkert, “Research of Current Distribution in IGBT Modules with Multiple Chips in Parallel,” PCIM Power Electronics Conference, pp. 548-551, 2005.

[3] R. Azar, F. Udrea, W. T. Ng, F. Dawson, W. Findlay and P. Waind, “The Current Sharing Optimization of Paralleld IGBTs in a Power Module Tile Using a PSpice Frequency Dependent Impedance Model,” IEEE Trans. on power electronics, Vol. 23, No. 1, January, pp. 206-216, 2008.

[4] A. Musing, G. Oritz and J. W. Kolar, “Optimization of the Current Distribution in Press-Pack High Power IGBT Modules,” The 2010 International Power Electronics Conference, pp. 1139-1146, 2010.

[5] Y. Kasho, H. Hirai, M. Tsukuda and I. Omura, “Tiny-scale “stealth” current sensor to probe power semiconductor device failure,” Microelectronics Reliability, Vol. 51, Iss.9-11, pp. 1689-1692, 2011.

[6] H. Hirai, Y. Kasho, M. Tsukuda and I. Omura, “Bonding wire current measurement with tiny film current sensors,” Proc. of ISPSD, pp. 287-290, 2012.

[7] H. Shiratsuchi, K. Matsushita and I. Omura, “IGBT chip current imaging system by scanning local magnetic field,” Microelectronics Reliability, Vol. 53, Iss.9-11, pp. 1409-1412, 2013.

[8] M. Tsukuda, S. Okoda, R. Noda, K. Tashiro and I. Omura, “High-throughput DBC-assembled IGBT screening for power module,” Proc. of CIPS, pp. 1-6, 2014.

[9] http://www.ni.com/labview/