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Real time degradation monitoring system for high power IGBT module under power cycling test

A. Watanabe[a,*], M. Tsukuda[a,b] and I. Omura[a]

[a] *Department of Electrical Engineering/Electronics, Kyushu Institute of Technology, 1-1 Sensui, Tobata, Kitakyushu, 804-8550, Japan*
[b] *The International Centre for the Study of East Asian Development, 1-8 Hibikino, Wakamatsu-ku, Kitakyushu 808-0138, Japan*

Abstract

A "real time" monitoring system which enables to observe internal degradation process to failure of power semiconductors under power cycling test is proposed. The system was realized by combining a scanning acoustic tomography (SAT/SAM), power stress controlling, device cooling, water jet system and chip temperature monitoring. Two contradictory problems, namely, electrically wiring for power cycling and waterproof of device for SAT imaging were compatible with each other by experimental setup with an original water tank. Self-heating of power devices was supressed by controlling temperature of water which is couplant of ultrasonic wave for the SAT. A demonstration of this system was performed by using an IGBT module which maximum rating of collector current was 400 A (DC).

Corresponding author.
nave@elcs.kyutech.ac.jp
Tel & Fax: +81 (93) 884 3298

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A. Watanabe[a, *], M. Tsukuda[a, b] and I. Omura[a]

1. Introduction

Wide area of power semiconductor applications promises huge volume manufacturing of them in the not-too-distant future. Downsizing of power semiconductors increases their productivity and enable such huge volume manufacturing. On the other hand, the downsizing increases power density of the devices and maximizes reliability risk of them. In this situation, failure mechanism based reliability assessment would be important to minimize reliability risk of power semiconductors. A "real time" monitoring of internal process to failure in power semiconductors under operating is a helpful tool for the failure mechanism based reliability assessment. It has significant advantages over the

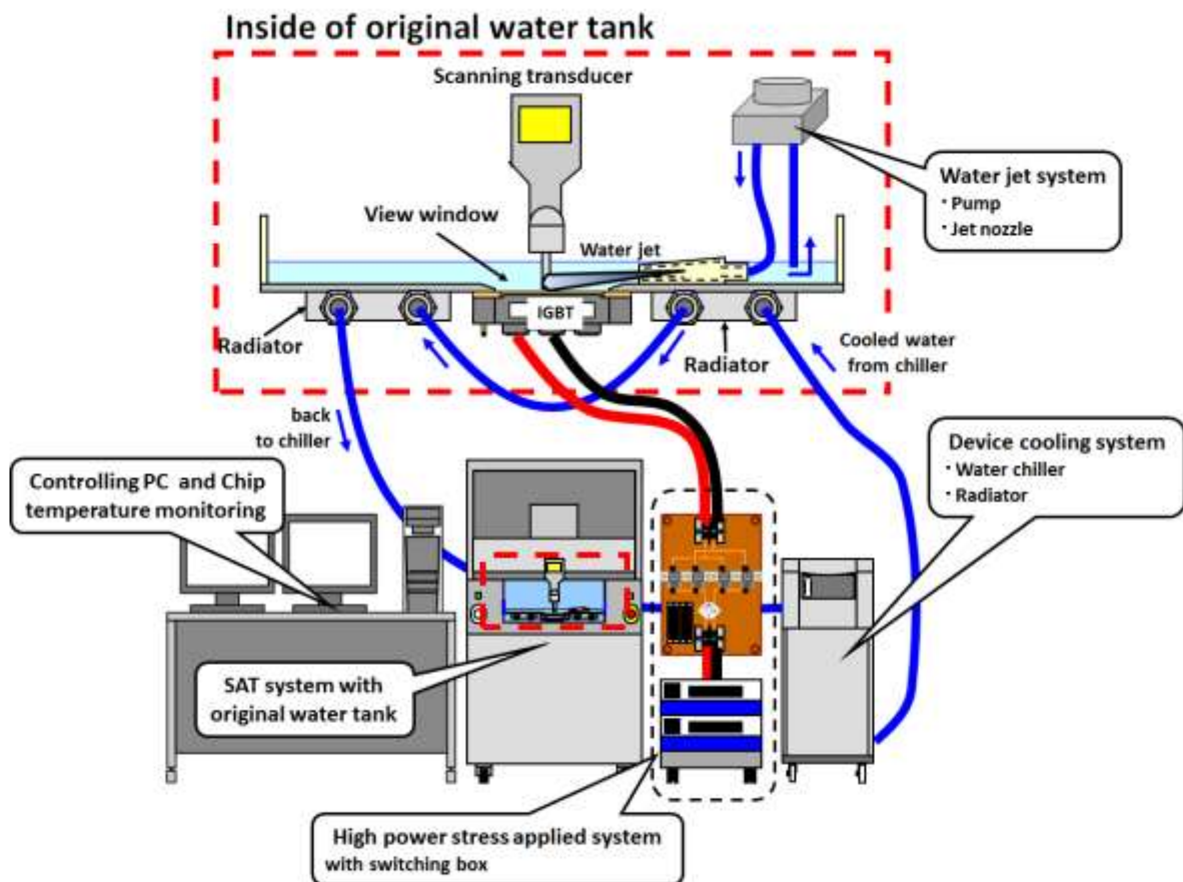

Fig. 1. Real time degradation monitoring system for high power IGBT module.

Table 1
Components of the real time degradation monitoring system

Function	Apparatus	Product Model
Inside imaging of DUT	Scanning Acoustic Tomography	FineSAT FS100 III (Hitachi Power Solutions Co., LTD.)
High power stress	DC power supply	PAT30-532TM (KIKUSUI ELECTRONICS CORP.)
	Stress control	LabView (National Instruments)
Device cooling	Water chiller	RKE1500B1-V-G2 (ORION MACHINERY Co., LTD.)
	Radiator	HS-C100 (KAWASO TEXCEL)
Water jet	Water pump	LMB15107315 (Laing Thermotech)
	Water jet nozzle	Own made
Temperature monitoring	Fiber optic temperature sensor	FOT-L-SD (FISO Technologies)
(Water and base plate)	Controller	UMI8 (FISO Technologies)
Chip temperature monitoring	Switching box	Own made with GX16CEB & BD9521 (GIGAVAC)
	Voltage monitor	TDS2022 (Tektronix, Inc.)
	Control program	LabView (National Instruments)

conventional “post stress” failure analysis technique in capturing the real trigger point of the failure before the defects are propagated substantially large areas.

In this paper, a “real time” monitoring system which enables to observe internal degradation process to failure of power semiconductors under power cycling test. This system was designed for widely used high power IGBT modules which base plate substrate area is ~50 cm^2 and realized by combining a scanning acoustic tomography (SAT/SAM), power stress controlling, device cooling, water jet system and chip temperature monitoring.

2. Real time monitoring system Set-Up

The main components for the proposed system were a) inside imaging of DUT, 2) high power stress control, 3) device cooling and 4) chip temperature monitoring as shown Fig. 1, Fig. 2 and Table 1.

2.1. Scanning acoustic tomography (SAT)

The SAT was employed as an imaging tool for monitoring internal process to failure of device under test (DUT) as a movie. The SAT is widely used for the failure inspection of the power devices by means of non-destructive imaging [1-8]. Two contradictory problems, namely electrically wiring for power cycling test and waterproof of the module for SAT imaging, were compatible with each other by experimental setup with an original water tank shown in Fig. 3. The DUT was attached to the view window at the bottom of the water tank with a sealing sheet made of silicone rubber. Inside images of an IGBT module could be observed by the SAT with 50 MHz and 20 mm focal distance transducer through from the base plate substrate.

2.2. Power stress circuit

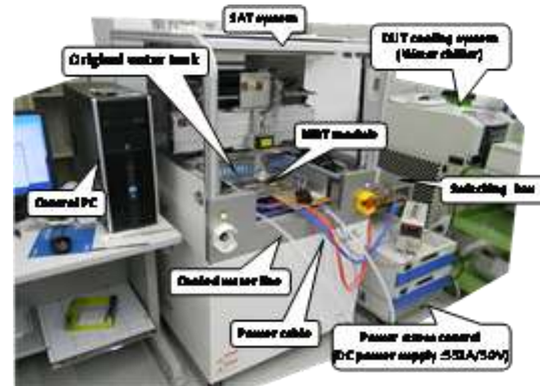

Fig. 2. Photograph of the system.

High power stress was applied to the DUT by a 16 kW DC power supply which controlled by a PC. A switching box shown in Fig. 4 was inserted between the output of power supply and DUT to separate them completely when the power stress was turn off. This switching box was also used for the chip temperature measurement.

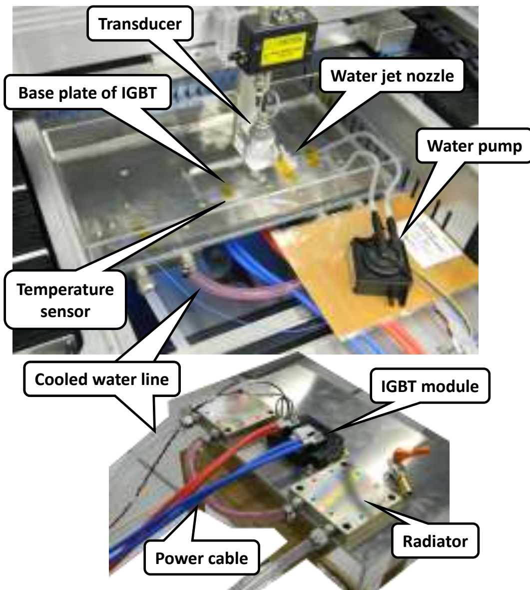

Fig. 3. DUT preparation and its setup in the SAT stage.

2.3. Device cooling

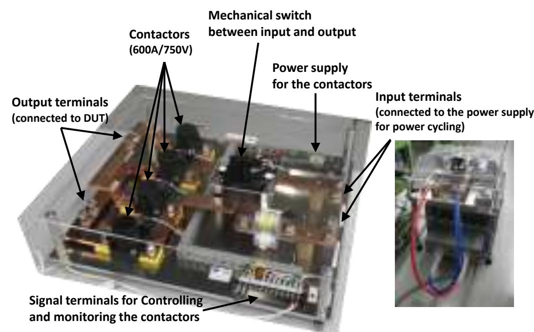

Fig. 4. 500 A switching box. This switching box constructed by four DC contactors (600 A / 750 V) forming a bridge circuit.

An appropriate cooling system was necessary for the real time observation of DUT especially for the SAT observation, because an abnormal temperature rise of couplant water results in degradation of SAT images [8]. The device temperature was controlled by the couplant water temperature for this system. The water cooled by a chiller was lead to a radiator attached to the bottom of the water tank made of aluminium. The radiator cooled down the couplant water surrounding the DUT and maintained the temperature of its surface.

2.4. Water jet system

A local convection and formation of tiny bubbles on the observation surface caused by self-heating of DUT also degrade the SAT images [8]. These problems were solved by introducing water jet system which generates a high speed water flow along the scanning interface. The water flow suppresses the convection just beneath the transducer and pushes out the bubbles on the surface.

2.5. Chip temperature monitoring

The device cooling manner of this system using surrounded water is much different from that of actual power devices under operating. One typical parameter enabling to compare these power stress condition is the temperature swing ΔT_j, is given by the temperature difference between maximal junction temperature T_{high} at the end of the heating phase and the minimal junction temperature T_{low} at the end of the cooling interval:

$\Delta T_j = T_{high} - T_{low}$ [9,10]

Temperature sensitive parameters of device, such as on-state voltage drop at low current and threshold voltage in IGBT's or the on-state voltage drop at low current in freewheeling diodes, are often utilized for measuring the ΔT_j. The switching circuit between the power supply and DUT enables these different current polarity measurements.

2.6. GUI for the system control

These systems are controlled via GUI which consists of SAT Image Acquisition window and power stress control window (Fig. 5). SAT acquisition parameters such as gate of reflected echo from DUT are set in the SAT controller window and

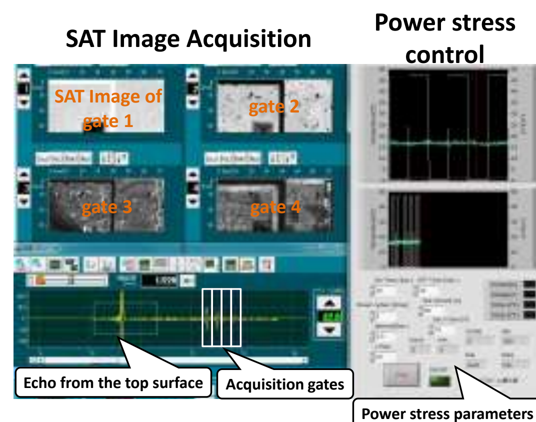

Fig. 5. Control window on PC.

continuous scan image is displayed in the same window. The power stress parameters such as a load current, a power cycle time and a duration of the cycle, are set in the power stress controller window. Temperatures of the water and DUT surface, electric current and voltage are also monitored in this window. The power stress controller window is programmed with LabView.

3. Real time monitoring results

The demonstration was performed with an IGBT module which maximum rating of collector current was 400 A (DC). A constant gate-emitter voltage (V_{GE}) of 15 V was applied to only the high-side IGBT and the high-side emitter was connected to the earth. The load current to the collector was switched by DC power supply with a programmed sequence.

Figure 6 shows SAT images of the DUT obtained under the different load current. Four acquisition gates were configured from the base plate substrate to obtain SAT images of different interface region. It took 16 second to obtain one frame of the SAT image of 75 mm × 35 mm region with 500 μm resolution, therefore the load current sequence was configured 30 second turn-on and -off cycle. Comparing with the images under the load current was turn-on and turn-off, any remarkable image degradation has not been recognized even under the 200 A load current flow. This result is also confirmed by the fact that the quality of image is not differ between the biased high-side region and the low-side region under the 200 A load current flow. Some dark spots (pointed by black arrow in Fig. 6) of tiny bubble appeared on the image, but it is able to solve by optimizing the water jet system.

Temperatures of the water and DUT surface monitored under the load current of 50 A and 200 A is shown in Fig. 7. The temperature of surrounded water under the load current of 200 A was gradually elevated and finally settled at around 25 ºC. The base plate temperature indicated the same behaviour with a vibration in 5 ºC followed by the load sequence and finally saturated between 24 ~ 30 ºC. Although this temperature behaviour did not affect the SAT image in this demonstration, its influence could become obvious when the high power stress is applied. Furthermore, temperature variation in the DUT is complicated because heat condition of assemblies is not equal depending on its material or interface

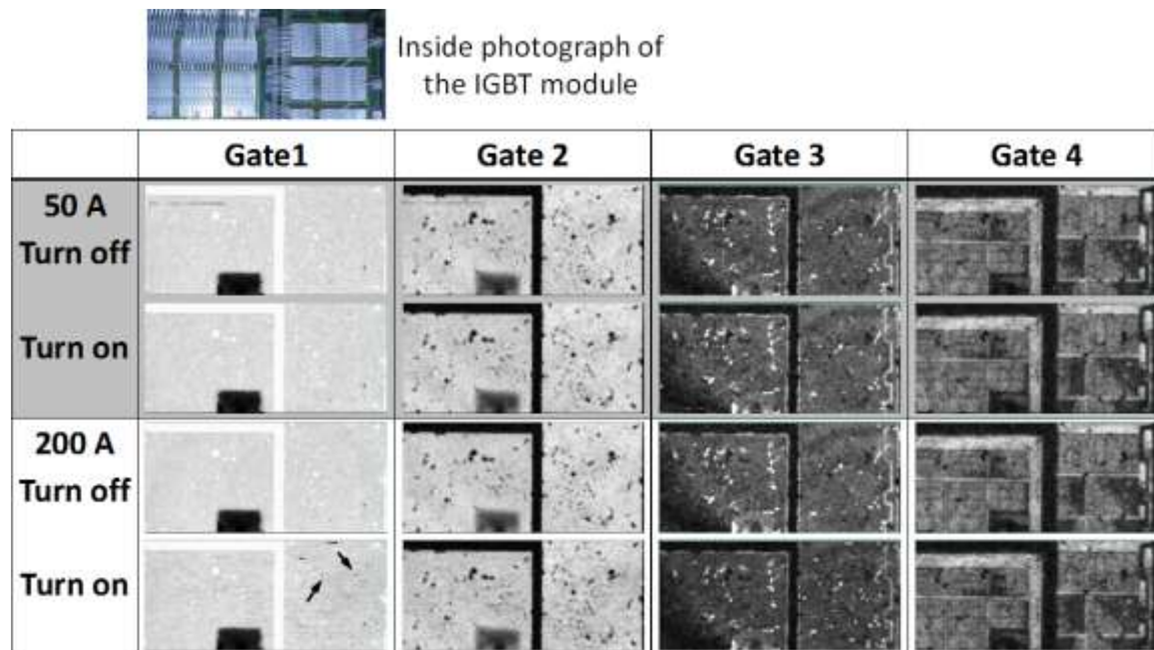

Fig. 6. SAT images of the DUT obtained under the different load current. The biased high-side chip is observed in the right side region of each image. The inside photograph is upset the top and bottom to adjust to these SAT images observed from the base plate substrate. A rectangular shadow in the bottom center is a shadow of adhesive tape to settle the temperature sensor.

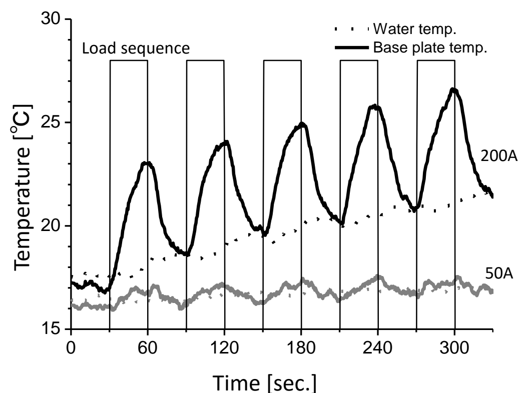

Fig. 7. Temperature change of the base plate surface and surrounded water under the power cycling test. The setting temperature of the water chiller was 15 ^{o}C.

structure. The propagation of ultrasonic wave would be affected by such temperature variation, therefore, detailed analysis of the reflected echo under the power cycling is necessary for the real time observation under power cycling test.

In contrast to previously reported papers for scanning acoustic method [2,3,6,7], the proposed system features monitoring function of degradation progress under acceleration stress test. This function provides a new approach to identify the fundamental mechanism to failure with the time-domain captured image of mechanical structure change inside the package under the stress. Moreover, this system successfully monitored larger area over 26 cm^2 than our previous demonstration [8] with sufficient resolution and frame rate of 500 μm and 4 frames / minutes, respectively thanks to the high electric current supply and the water cooling system. We have also confirmed the frame rate is improved more than four times with an arrayed transducer [11].

4. Conclusion

A real time monitoring system of internal process for 500 W class power semiconductor devices are proposed. The system enables to observe mechanical modification, e.g. propagation of defects and void, in power devices in real time and establishes that real time monitoring of DUT is possible even under high power stress. To analyze the information of internal process to failure obtained in real time realises failure mechanism based reliability assessment.

Acknowledgements

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References

[1] De Liso G, Muschitiello M and Stucchi M. Failure analysis of encapsulated electronic devices by means of scanning ultra microscopy technique. SCANNING 15 (1993) 236-242.

[2] Angrisania L, Bechoub L, Dalletb D, Dapontec P and Oustenb Y. Detection and location of defects in electronic devices by means of scanning ultrasonic microscopy and the wavelet transform. Measurement 31 (2002) 77–91.

[3] Feller L, Hartmann S and Schneider D. Lifetime analysis of solder joints in high power IGBT modules for increasing the reliability for operation at 150 oC. Microelectronics Reliability 48 (2008) 1161–1166.

[4] Brand S, Czurratis P, Hoffrogge P, Temple D, Malta D, Reed J and Petzold M. Extending acoustic microscopy for comprehensive failure analysis applications. J. Mater. Sci. Mater. Electron. 22 (2011) 1580–1593.

[5] Chung T, Jhang J, Chen J, Lo Y, Ho G, Wu M, Sun C. A study of large area die bonding materials and their corresponding mechanical and thermal properties. Microelectronics Reliability 52 (2012) 872-877.

[6] Mario P, Josef M, Michael I. Inverted high frequency Scanning Acoustic Microscopy inspection of power semiconductor devices. Microelectronics Reliability 52 (2012) 2115-2119.

[7] Schilling O, Schäfer M, Mainka K, Thoben M, Sauerland F. Power cycling testing and FE modelling focussed on Al wire bond fatigue in high power IGBT modules. Microelectronics Reliability 52 (2012) 2347-2352.

[8] Watanabe A, Omura I. Real-time failure imaging system under power stress for power semiconductors using Scanning Acoustic Tomography (SAT). Microelectronics Reliability 52 (2012) 2081-2086.

[9] Cova P, Fantini F. On the effect of power cycling stress on IGBT modules. Microelectronics Reliability 38 (1998) 1347-1352.

[10] Amro R. Packaging and interconnection technologies of power devices, challenges and future trends. World Academy of Science, Engineering and Technologies 49 (2009) 691-694.

[11] Web site of Hitachi Power Solutions Co., Ltd.; http://www.hitachi-power-solutions.com/en/products/product14/p030_01.html