Internal Degradation Monitoring of Power Devices During Power Cycling Test

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Akihiko Watanabe[a], Masahiro Tsukuda[b] and Ichiro Omura[a],
[a] Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu, Japan
[b] ICSEAD, 1-8 Hibikino, Wakamatsu-ku, Kitakyushu, Japan

Summary

A technique to monitor internal degradation to failure of power devices in real time was proposed. Required components for this technique are (1) non-destructive inside imaging, (2) power stress control and (3) device cooling. We constructed the system with scanning acoustic tomography (SAT), DC power supply controlled by own made program and water cooling system, respectively. In the case of a TO-3P packaged MOSFET, propagation of internal degradations to failure was successfully recorded as time series data by using this system. At the present time, the system is modified for high power and large size IGBT modules.

1 Failure analysis based on real time monitoring

Downsizing of power semiconductors improves their performance and increases their productivity. On the other hand, it increases power density of the devices and leads to high reliability risk of them as a consequence. Failure analysis is becoming more important to reduce the reliability risk of power devices. In many cases, post-defect or interim samples picking out under testing have been used for the failure analysis. With this way, it is often difficult to identify the real cause of failure because of incidental damages especially for high power density modules. A real time monitoring of internal phenomena of devices under test (DUT) is one solution for this difficulty of the failure analysis. By monitoring the internal degradation process of DUT in real time, a real trigger point of the failure is able to be identified before incidental damages propagate to substantially large areas.

In this paper, a technique to monitor internal degradation to failure of power devices in real time was proposed. The system was constructed by combining a scanning acoustic tomography (SAT), DC power supply controlled by own made program and water cooling system. In the case of a TO-3P packaged MOSFET under the power stress of 20 A, propagation of internal degradations to failure was successfully recorded as time series data. The system is modified for a high power and large size IGBT modules at the present time and some fundamentally tests have been done.

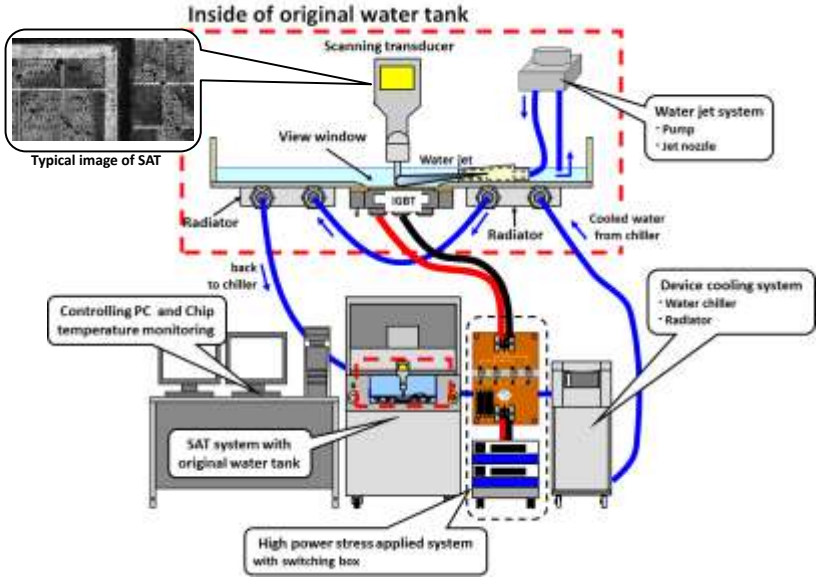

Figure 1 Components of the real time degradation monitoring system

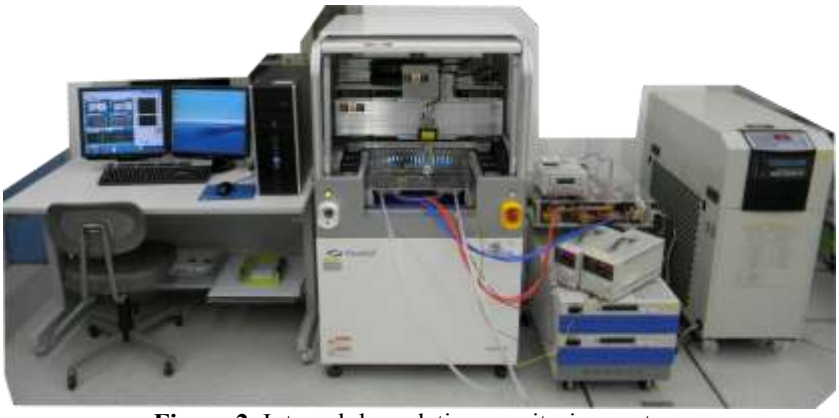

Figure 2 Internal degradation monitoring system

2 Real time degradation monitoring system for power devices

Required components to the real time monitoring of internal phenomena of DUT are (1) non-destructive inside imaging, (2) power stress control and (3) device cooling as shown in Figure 1 and 2.

Scanning acoustic tomography (FineSAT FS100 III, Hitachi Power Solutions Co., Ltd.) was employed as an imaging tool for internal process of DUT. The SAT is widely used for the failure inspection of the power devices by means of non-destructive imaging with ultrasonic wave [1-8]. Inside images of MOSFET or IGBT was observed by 50 MHz and 20 mm focal distance transducer through from the base plate substrate. The DUT was attached to the view window at the bottom of an original water tank because couplant water for ultrasonic wave propagation is necessary for SAT imaging (Figure 3).

Power stress was applied to the DUT by a 16 kW DC power supply (PAT30-532TM, KIKUSUI ELECTRONICS Corp.). The power stress sequence was programed through an original GUI written by LabView (National Instruments). Figure 4 shows a switching system was inserted between the output of the power supply and DUT. This switching system has four contactors (GX16, GIGAVAC) with bridge connection. The contactors are controlled by TTL signal form PC and enable to isolate DUT from the power supply mechanically and also enable to change a polarity of the bias applied to the DUT.

The temperature of DUT was controlled by using the couplant water. Cooled water from a chiller was lead to a radiator attached at the bottom of the water tank and the radiator cooled down the couplant water in the tank. The cooled water in the tank was flowed to the DUT surfaces with water jet generated by a pump and a jet nozzle to keep the DUT surface temperature. The water jet also suppressed a local convection at the surface by self-heating of DUT which degrade the SAT image. The temperature of the base plate of DUT and that of water in the tank were monitored by fiber optic temperature sensors during the measurement.

The device cooling manner of this system using surrounded water is much different from that of actual power devices under operating. One typical parameter enabling to compare these power stress condition is the temperature swing ΔT_j, is given by the temperature difference between maximal junction temperature T_{high} at the end of the heating phase and the minimal junction temperature T_{low} at the end of the cooling interval [9,10]. To estimate the junction temperature, temperature sensitive parameters (TSP) of devices was measured by the system. The TSP, such as on-state voltage drop of IGBT at low current

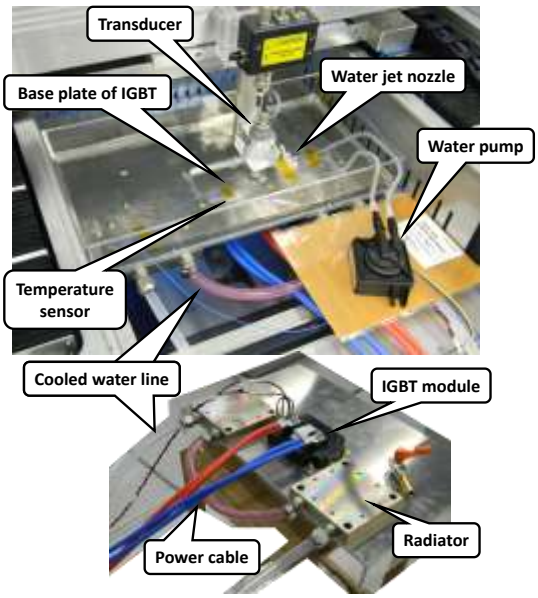

Figure 3 DUT preparation and its setup in the SAT stage

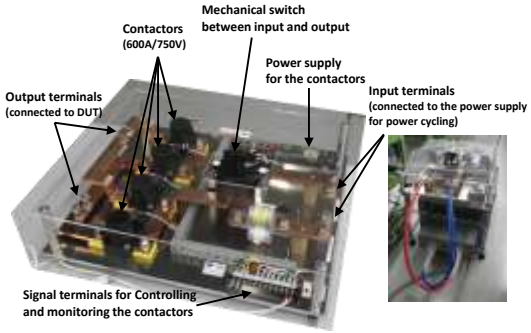

Figure 4 Switching system construvcted by TTL controll contactors

or freewheeling diodes, are often utilized for measuring the ΔT_j. The switching system between the power supply and DUT enables these different current polarity measurements.

3 Results of real time internal degradation monitoring

Internal degradation process to failure of a TO-3P packaged MOSFET during power cycling test was successively recorded by the real time monitoring system. Figure 5 is a series of snapshot captured in a time series when mean power stress of 134 W (24A) was applied to the DUT [8]. In this case, an internal change was observed at the edge of the chip after 20 cycle power stress (see the snapshot 1 in Figure 5) and it propagated to wide area. After about 100 times power cycling, other damage suddenly occurred at the bonding site (see the snapshot 6), and then this device was broken after more 20 times power cycling. If a post-defect device is used as a sample for failure analysis, we can do only imagine a cause of the failure from the snapshot 8. On the other hand, using the real time monitoring technique, we can obtain evidence for real cause of the failure with tracing the internal degradation process in a time series.

The system is modified for high power and large size

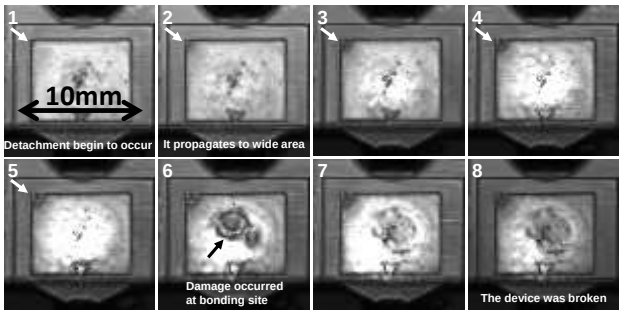

Figure 5 Internal degradation process to failure of MOSFET captures by the real time monitoring system

Function	Low power system (TO-3P)	Modified to High power system (IGBT module)
Power stress applied system	30A (～400W)	500A (～16kW)
Device cooling	1.2kW chiller with aluminium pipe radiator	5kW chiller with two flat radiators
Temperature monitoring	Base plate & water (Fiber optic temperature sensor)	& Junction temperature (TSP)
Water proof of devices	Capsuled in a water-proof holder	Attached directly to the bottom of original made water tank

Table 1 Main points of modification to high power and large size IGBT modules

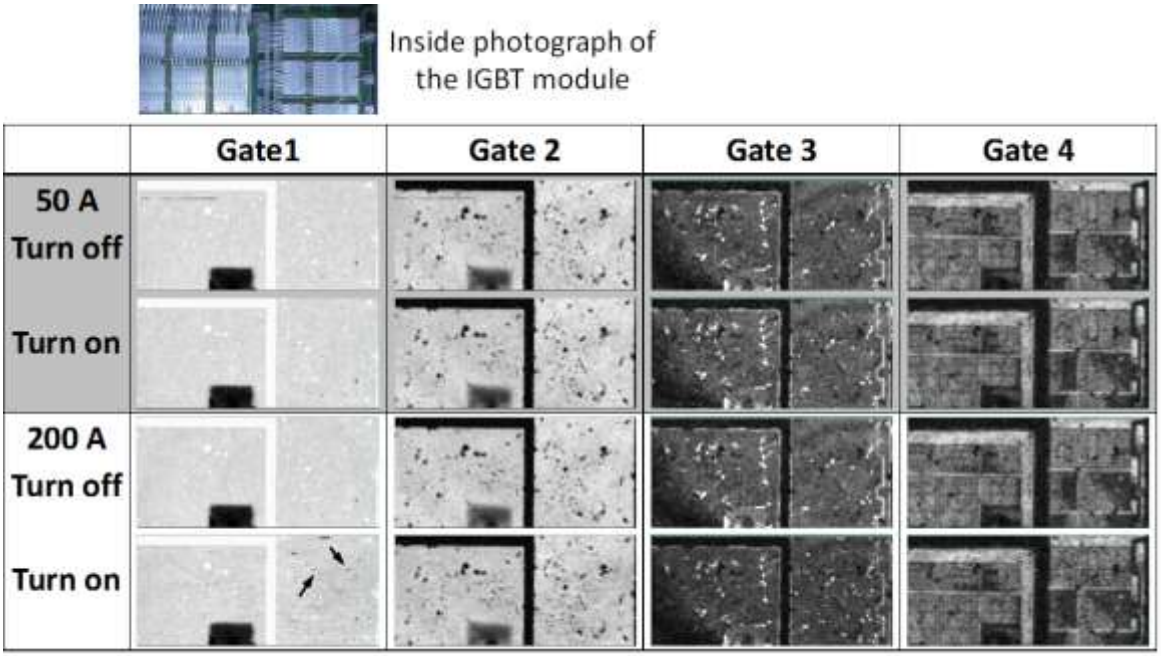

Figure 6 Internal SAT images of the DUT obtained under the different load current. The biased high-side chip is observed in the right side region of each image. The inside photograph is upset the top and bottom to adjust to these SAT images observed from the base plate substrate. A rectangular shadow in the bottom center is a shadow of adhesive tape to settle the temperature sensor.

IGBT modules at the present time. The main points of modification are listed in Table 1. Some fundamentally tests have been done with an IGBT module which maximum rating of collector current was 400 A (DC). A constant gate-emitter voltage (V_{GE}) of 15 V was applied to only the high-side IGBT and the high-side emitter was grounded. The load current to the collector was switched by DC power supply with a programmed sequence. Figure 6 shows SAT images of the DUT obtained under the power stress of 50 A and 200A. Four acquisition gates of reflected echo were configured from the base plate substrate to obtain SAT images of different interface region. It took 16 s to obtain one frame of the SAT image of 75 mm × 35 mm region with 500 μm resolution, therefore the load current sequence was configured 30 s turn-on and turn-off cycle. Comparing with the images under the load current was turn-on and turn-off, any remarkable image degradation has not been recognized even under the 200 A load current. This result is also confirmed by the fact that the quality of image is not differ between the biased high-side region and the low-side region under the 200 A load current flow. Some dark spots (pointed by black arrow in Figure. 6) of tiny bubble appeared on the image, but it is able to solve by optimizing the water jet system.
The temperature of surrounded water under the load current of 200 A was gradually elevated and finally settled at around 25 °C. The base plate temperature indicated the same behaviour with a vibration in 5 °C followed by the load sequence and finally saturated between 24 and 30 °C. Although this temperature behaviour did not affect the SAT image in this demonstration, its influence could become obvious when the high power stress is applied.
This system successfully monitored larger area over 26 cm^2 than our previous demonstration [8] with sufficient resolution and frame rate of 500 μm and 4 frames / min, respectively. We have also confirmed the frame rate is improved more than four times with an arrayed transducer [11].

4 Conclusion

Real time monitoring of internal degradation to failure of power semiconductor devices was demonstrated and successfully identified a real trigger point of the failure of a TO-3P packaged MOSFET. The system was modified for high power and large size IGBT modules and it confirmed that the system able to apply high power modules.

5 Acknowledgement

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6 References

[1] G. De Liso, M. Muschitiello and M. Stucchi, SCANNING 15 (1993) 236-242.

[2] L. Angrisania, L. Bechoub, D. Dalletb, P. Dapontec and Y. Oustenb, Measurement 31 (2002) 77–91.

[3] L. Feller, S. Hartmann and D. Schneider, Microelectronics Reliability 48 (2008) 1161–1166.

[4] S. Brand, P. Czurratis, P. Hoffrogge, D. Temple, D. Malta, J. Reed and M. Petzold, J. Mater. Sci. Mater. Electron. 22 (2011) 1580–1593.

[5] T. Chung, J. Jhang, J. Chen, Y. Lo, G. Ho, M. Wu and C. Sun, Microelectronics Reliability 52 (2012) 872-877.

[6] P. Mario, M. Josef and I. Michael, Microelectronics Reliability 52 (2012) 2115-2119.

[7] O. Schilling, M. Schäfer, K. Mainka, M. Thoben and F. Sau-erland, Microelectronics Reliability 52 (2012) 2347-2352.

[8] A. Watanabe, I. Omura, Microelectronics Reliability 52 (2012) 2081-2086.

[9] P. Cova, F. Fantini, On the effect of power cycling stress on IGBT modules, Microelectronics Reliability 38 (1998) 1347-1352.

[10] R. Amro, Packaging and interconnection technologies of power devices, challenges and future trends, World Academy of Science, Engineering and Technologies 49 (2009) 691-694.

[11] Web site of Hitachi Power Solutions Co., Ltd. <http://www.hitachi-power-solutions.com/en/products/product14/p030_01.html>.