DESIGN OF A PRECISION LOW VOLTAGE RESISTOR MULTIPLYING DIGITAL-TO-ANALOG CONVERTER

A Thesis

by

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ABSTRACT

This work aims to model the effect of the input offset voltage of an operational amplifier on the performance of a high-precision, voltage-mode, resistor-based multiplying digital-to-analog converter (M-DAC). Based on the model, a high precision current buffer is proposed to isolate the resistor ladder from the operational amplifier. A 14-bit M-DAC operating with a $\pm$1V reference is designed using the IBM-130nm PDK to illustrate the offset tolerance of the proposed architecture. Post-layout simulations show that the proposed architecture reduces the offset voltage to an offset error in the DAC transfer function. The maximum DNL is maintained at -0.385 LSB for an input offset voltage of up to 60mV (1024 LSB). The current buffer also introduces an inversion of the output voltage, yielding a non-inverted output. This alleviates the need for an additional high precision op-amp to invert the output voltage.

DEDICATION

To my loving grand-parents,

Late Dr. B.V. Rama Raju

B. Rama Bai

Late T.V. Subba Rao

T. Sesha Kumari

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NOMENCLATURE

ADC	Analog-to-Digital Converter
M-DAC	Multiplying Digital-to-Analog Converter
MSB	Most Significant Bit
LSB	Least Significant Bit
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
OP-AMP	Operational Amplifier
VOUT	Output Voltage
IOUT	Output Current (Positive Terminal)
IOUTB	Output Current (Negative Terminal)
REF	Reference Voltage
DVDD	Digital VDD Supply
DVSS	Digital VSS Supply
FS	Full-scale
THD	Total Harmonic Distortion
CMOS	Complementary Metal Oxide Semiconductor
FET	Field Effect Transistor
PVT	Process Voltage and Temperature

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1. INTRODUCTION

High-precision test equipment and medical instruments demand the use of a digitally-controllable AC signal processing component [5]. With the equipment becoming more portable each day, the need for low voltage designs is ever increasing. Voltage-mode Multiplying-DACs (M-DACs) are ideally suited for such applications. This is because M-DACs, unlike other DACs, use a variable reference along with a digitally switched resistor ladder to produce variable output current, which is converted to voltage by a current to voltage (I-V) converter.

As with any resistor-based DACs, the M-DAC performance also depends on the matching of the resistors [6]. In addition to this, at low voltages the M-DAC performance, particularly linearity, becomes heavily dependent on the design of the current-to-voltage (I-V) converter. This thesis studies the performance dependency of the I-V converter design on the M-DAC's performance and also proposes a new block in the M-DAC architecture to minimize this dependency.

The following chapter describes the various DAC architectures and parameters before narrowing down the discussion to the voltage-mode M-DAC. Following this, the limitations of using an op-amp based I-V converter for low voltage high precision applications are discussed. Chapter 3 proposes the introduction of a new block in the M-DAC architecture to tolerate the static limitations of the op-amp followed by the design of a 14-bit M-DAC using the proposed architecture. Chapter 4 illustrates the post layout results of the proposed design. Chapter 5 discusses the possible solutions to the issues associated with the proposed architecture before concluding in Chapter 6.

2. BACKGROUND

A Digital-to-Analog Converter (DAC) converts a multi-bit digital input signal to an analog output voltage or current. In most cases, this is achieved by using an array of passive elements, such as resistors or capacitors, to attenuate or amplify a reference voltage and use the digital input code to select a particular branch. Active elements such as op-amps or transconductance amplifiers (OTA) may also be used to convert the output voltage or current and also achieve high load driving capability. DACs also employ CMOS switches for the conversion. The switches may be used to either select an output voltage or steer an output current [7].

Instead of an array of passive devices, transistors acting as a current sources can also be used for the digital-to-analog conversion [8]. They offer higher speeds of operation compared to the passive devices at the expense of matching and linearity. In addition to speed, matching and linearity, various DAC architectures can be compared based on their settling time and glitch energy.

2.1 DAC Performance Metrics

A DAC performance for a particular reference voltage, resolution and speed is characterized by static and dynamic metrics [9]. Typically a DAC is optimized for a specific set of metrics depending on the application.

2.1.1 Resolution (n)

It determines how finely the output may change between discrete binary steps. For an n-input DAC, the number of unique digital codes and output signal values are $2^n - 1$.

2.1.2 Full-scale Code (FS)

The maximum digital input code to the DAC is defined as the full-scale (FS) of the DAC. This typically corresponds to all the input bits being set to "1".

2.1.3 Zero Code (ZC)

The minimum digital input code to the DAC is defined as the zero of the DAC. This corresponds to all input bits being set to "0". In unipolar DACs the output for zero code is zero while for bipolar DACs it is the negative of the signal obtained at full-scale.

2.1.4 Least Significant Bit

The Least Significant Bit (LSB) or Δ is the smallest change in the DAC output. For an ideal DAC this can be computed as,

$$LSB(\Delta) = \frac{Output(FS) - Output(ZC)}{2^n} \tag{2.1}$$

2.1.5 Static Metrics

A DAC transfer function can be obtained by plotting the output analog signal versus input digital code as shown in Figure 2.1. Each of the static performance metrics - offset, gain, differential nonlinearity and integral nonlinearity errors can be obtained from this plot as explained in the following sub-section.

2.1.5.1 End-Point Errors

Based on the end-points of a DAC transfer curve the offset and gain error are specified. The *offset error* is the deviation from ideal at Zero code. On the other hand, the difference between the slope of the ideal transfer curve and the obtained transfer curve is measured as the *gain error*. The effect of both the errors on the transfer curve is shown in Figure 2.2.

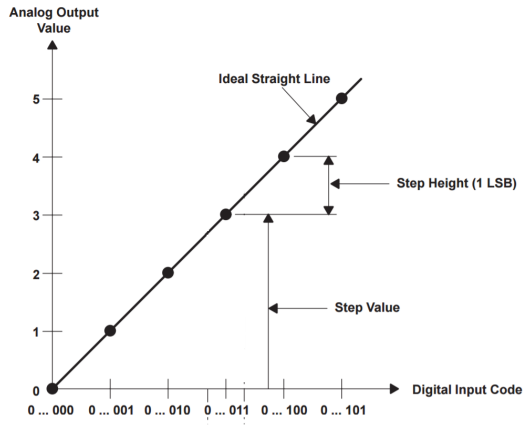
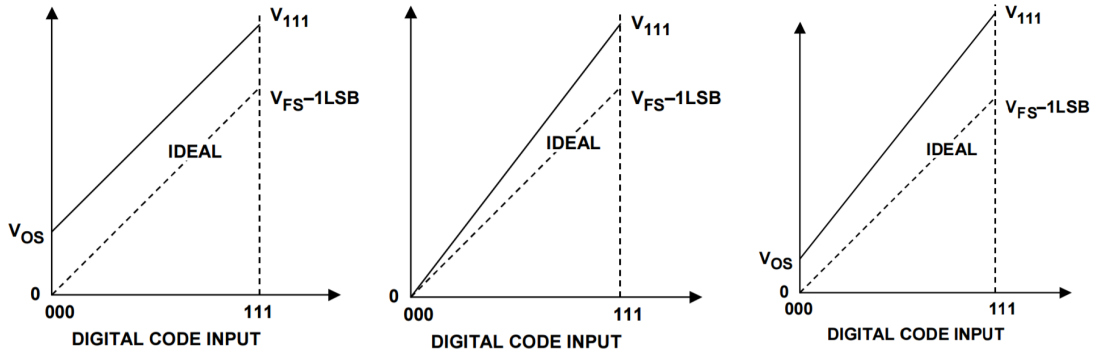


Figure 2.1: Ideal DAC transfer curve [1]



(a) Offset error (b) Gain error (c) Offset and gain error

Figure 2.2: End-point errors [2]

2.1.5.2 Linearity Errors

Since DACs are typically made of an array of resistors, capacitors or current sources, matching between the elements determines its linearity, i.e., the larger the mismatch, the larger the nonlinearity. To quantify the linearity of a DAC, the *integral nonlinearity (INL)* and *differential nonlinearity (DNL)* are measured. The INL is the deviation of the actual transfer curve from a reference line, which can be a best-fit line, the end-point line or the

ideal DAC line [7]. If the output analog signal for each code is expressed as $Y(i), i = 0...(2^n - 1)$ and each code ideally contributes to Δ change in the output analog signal, then the INL can be expressed as,

$$INL(i) = \frac{Y(i) - Y_{ref}(i)}{\Delta} \tag{2.2}$$

On the other hand, DNL is the maximum deviation of an actual analog output step, between adjacent input codes, from the ideal step value of Δ. This can be expressed as,

$$DNL(i) = \frac{Y(i+1) - Y(i) - \Delta}{\Delta} \tag{2.3}$$

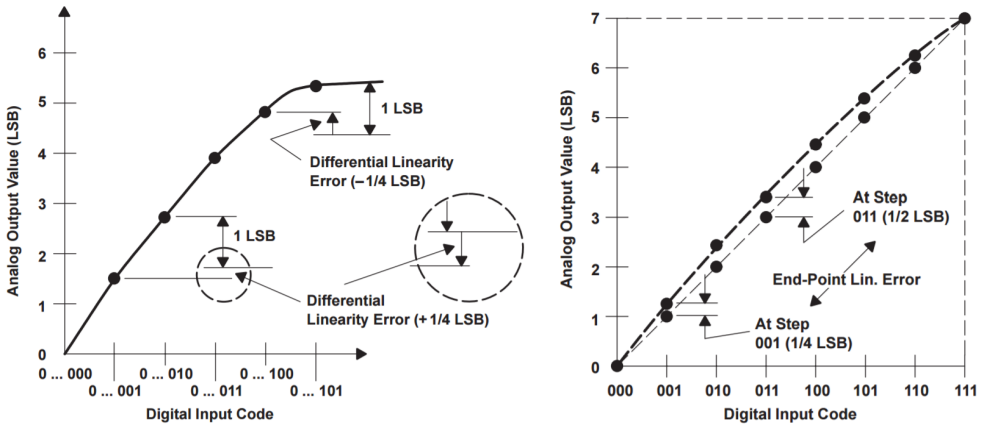
From (2.3) it is apparent that for DNL $<$ -1 the DAC is non-monotonic. Another thing to note is that, if the INL is estimated using the end-point line then the INL becomes a running sum of DNL at each code.

$$INL(k) = \sum_{i=1}^{k} DNL(i) \tag{2.4}$$

Figure 2.3 shows the transfer curve of a nonideal DAC depicting DNL and INL errors.

2.1.6 Dynamic Metrics

In some applications such as audio or communications, the AC or transient performance of the DAC is more crucial than the static performance. Such applications demand that the DAC have fast settling time, low glitch impulse area and low distortion while having a fast conversion rate and a wide operating frequency range. These performance metrics are tested using either sine or step functions applied to the digital input or analog reference input.



(a) DNL error (b) INL error

Figure 2.3: Linearity errors [1]

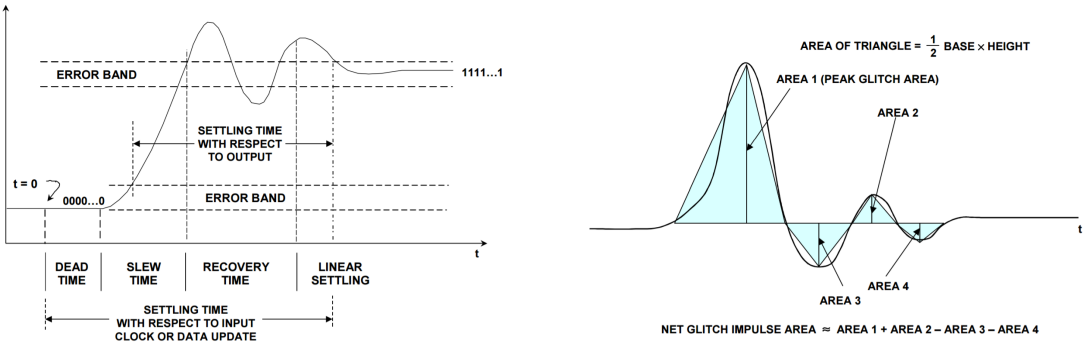
2.1.6.1 Step Response

A step change in the digital code or analog reference signal is used to measure the DACs settling and glitch impulse area.

Settling time can be defined as the amount of time required for the output to settle within the specified error band measured with respect to the output when the input data to the switches changes as shown in Figure 2.4a [2]. The specified error band is defined in terms of Δ or LSB of the DAC and is typically defined to be 1 LSB.

During code transitions, the output voltage of the DAC shows initial overshoot and undershoot behavior before settling to the final value as shown in Figure 2.4b. These *glitches* in the output voltage are typically a consequence of the DAC internal switches being out-of-sync or the switch parasitic capacitance being charged or discharged. The worst-case glitch is observed when all the switches toggle, which typically occurs during the mid-scale transition for M-DACs. This code transition is also referred to as a major carry transition.

In certain applications, these glitches can disrupt system behavior and lead to dynamic



(a) Settling time

(b) Glitch impulse area

Figure 2.4: Step response [2]

non-linearity [10]. The magnitude of the glitch is quantified as an area under the impulse as shown in Figure 2.4b, which represents the amount of energy during the glitching.

2.1.6.2 AC Response

A stream of digital codes representing a single or multi-tone sine wave is applied at the input to the DAC to measure its total harmonic distortion (THD), signal-to-noise ratio (SNR), signal to noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) [2]. However, for M-DACs, which are capable of having a time-varying analog reference signal, these metrics are also measured with respect to the reference.

Relevant specifications for the M-DAC include the reference multiplying bandwidth, Analog/Digital total harmonic distortion (THD) and the multiplying feedthrough error.

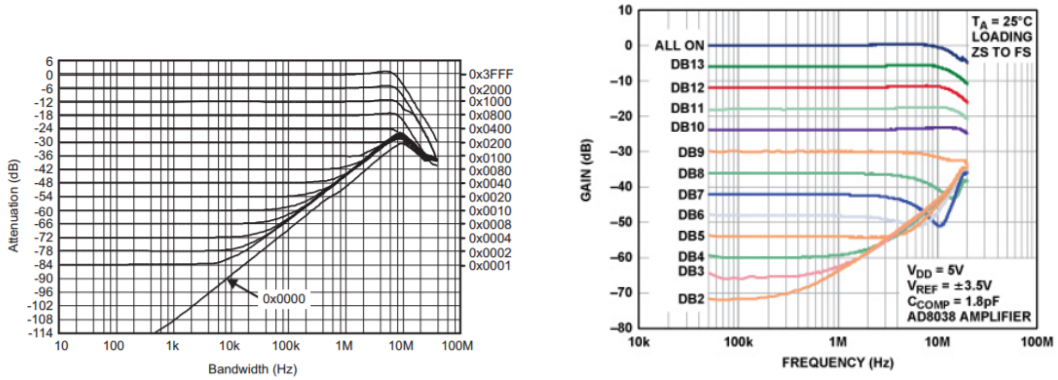
The *reference multiplying bandwidth* is defined as the reference input frequency at which the gain of the DAC is -3dB when the DAC code is set to full-scale [11]. It is strongly dependent on the parasitic capacitance of the switches and the GBW of the I-V converter used in the M-DAC. Figure 2.5a shows the AC response of an M-DAC from Texas Instruments DAC8802 for different input codes. The response at full-scale is used to define the multiplying bandwidth, which is about 10MHz from the plot.

The *analog THD* is the mathematical representation of the harmonic content in the output multiplied waveform signal [11] when a sinusoidal reference is applied. If V_i represents the i^{th} harmonic then the THD is,

$$THD(dB) = 20\log_{10}\left(\frac{\sqrt{\sum_{i=2}^{\infty} V_i^2}}{V_1}\right) \tag{2.5}$$

The *digital THD* is the mathematical representation of the harmonic content in the output multiplied waveform signal [11] when a stream of digital code representing a sinusoidal wave is applied.

The *multiplying feedthrough error* is the error due to the parasitic capacitive feedthrough from the reference input to the DAC output, when the digital input to the DAC is zero code [11]. At high frequencies, when the capacitance impedance falls, the feedthrough increases as shown in Figure 2.5b.



(a) Reference multiplying bandwidth [12] (b) Multiplying feedthrough [11]

Figure 2.5: AC response

Based on the discussed metrics various DAC topologies can be compared.

2.2 Resistor-based DAC Architectures

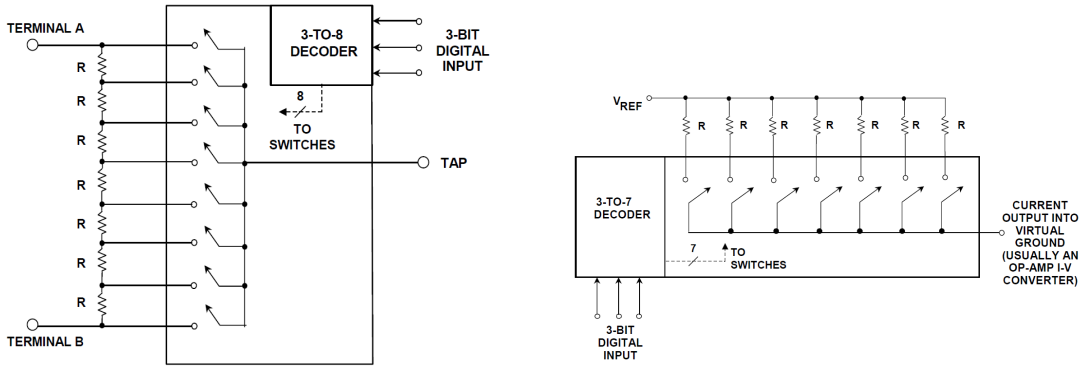
Among the various elements that can be used to create a DAC, the current source based implementation offers the highest conversion speed with the least untrimmed accuracy. Capacitors offer the best matching, but leakage causes a loss in accuracy within a few milliseconds [2]. Resistors offer moderate matching and their precision is not lost due to leakage. When coupled with CMOS switches, which can conduct bi-directional current, the resistor-based architecture can also be employed with a bipolar time-varying reference. Since the design of a precision DAC having a time-varying reference is the focus of this thesis, the scope of this discussion is limited to different resistor-based architectures.

An array of switched resistors that create the DAC is sometimes referred to as a resistor ladder. Based on the design of the ladder, the resistor architectures can be further classified into - unary, binary and segmented architectures.

2.2.1 Unary Resistor Ladder

If all the resistors in the ladder are equally weighted, then the ladder is called a *unary DAC* ladder. A series connection of multiple unit resistors forms a String DAC [7], and each tap of the string generates a different voltage as shown in Figure 2.6a. If "Terminal B" is connected to ground, then the architecture is termed as a Kelvin Divider, otherwise it is called a digital potentiometer. Connecting multiple unit resistors in parallel yields a current output DAC as shown in Figure 2.6b.

The resistor ladder is simple, inherently monotonic and has a low glitch impulse area when switching. However, to generate an n-bit DAC, 2^n-1 unit resistors are required yielding an exponentially growing area requirement as the resolution increases.



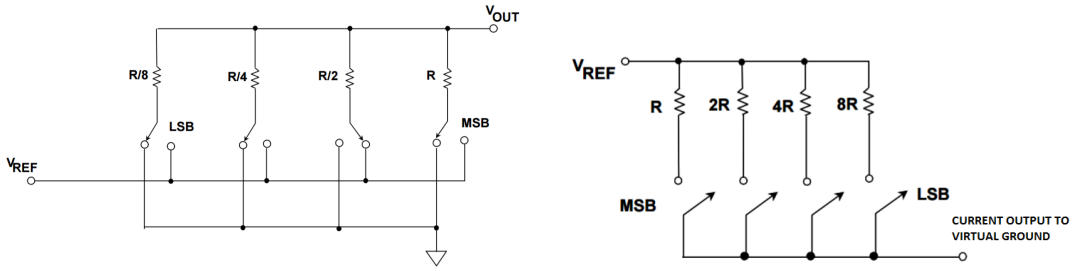
(a) Voltage output unary DAC (b) Current output unary DAC

Figure 2.6: Unary DAC [2]

2.2.2 Binary Resistor Ladder

If the resistors along the ladder are scaled by a factor of two then the ladder is called a *binary DAC*. Figure 2.7 shows the voltage mode and current mode variations of the DAC.

Since only one resistor is associated with each bit, these DACs are more efficient than the unary DACs at higher resolutions. However, these DACs are not inherently monotonic and maintaining good matching across the different values of resistors is difficult.



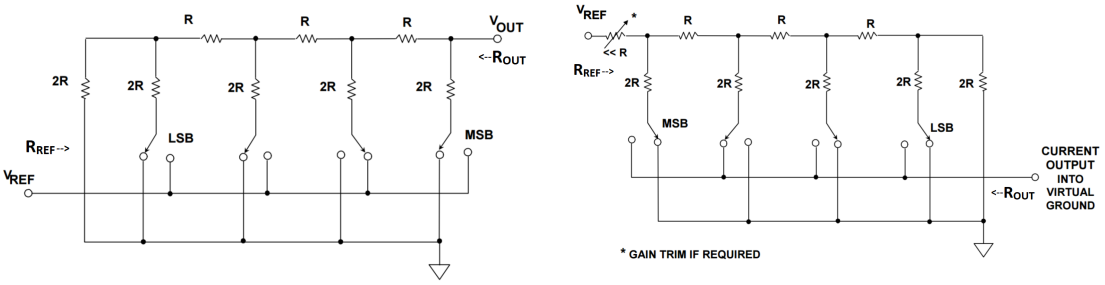
(a) Voltage output binary DAC (b) Current output binary DAC

Figure 2.7: Binary DAC [2]

The matching in the binary ladder can be improved by using an R-2R ladder as shown

in Figure 2.8. This requires matching between only two values of resistors and offers similar area advantages as the original binary DAC. However, this ladder also does not guarantee monotonicity.

Another issue with the voltage mode R-2R DAC is that the impedance looking into the reference terminal (R_{REF}) is code-dependent. As a consequence, for all the applications using R-2R voltage mode DAC the reference is buffered. For high precision application, the buffer specification must be commensurate with the required precision. On the other hand, the current-mode DAC offers a code-independent impedance R and hence, alleviates the need for a buffer. In addition to this, if the switches of a current-mode DAC are capable of carrying current in either direction (such as CMOS devices), the reference voltage may have either polarity. A DAC using such a structure is referred to as a *multiplying DAC*. A major drawback in the current mode DAC is that the switches are typically large to minimize their R_{on} and hence can introduce large glitches when switching.



(a) Voltage output R-2R DAC (b) Current output R-2R DAC

Figure 2.8: R-2R DAC [2]

An active current to voltage (I-V) conversion stage can be employed to create a voltage from the current output. Figure 2.9 shows an operational amplifier used as an I-V converter to create a *voltage-mode M-DAC*.

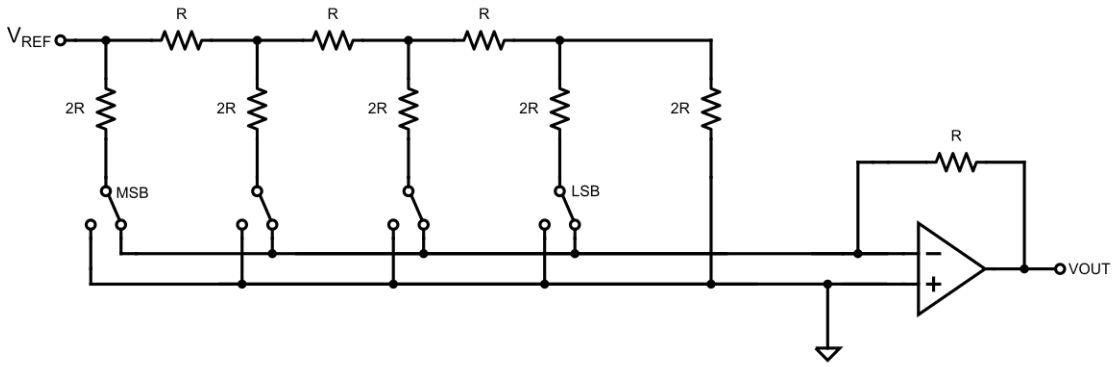


Figure 2.9: Voltage output M-DAC

2.2.2.1 Segmented Ladder

To achieve higher resolutions, multiple DAC ladders can be combined to create a *segmented ladder*. One ladder handles the MSBs while the other handles the LSBs. Figure 2.10 shows an example of a current mode segmented DAC where the first 3 bits are unary or thermometer DAC while the last four bits are R-2R.

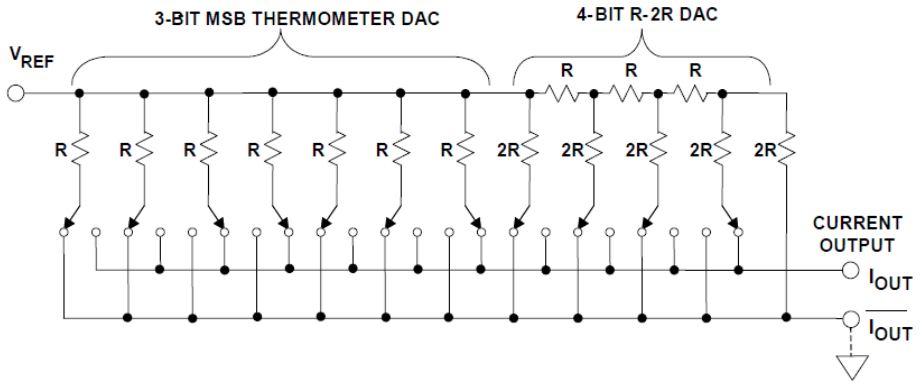


Figure 2.10: Segmented ladder

Consider an n-bit DAC having m-bits as unary elements and n-m bits as binary. If the

spread of the resistor mismatch across the PVT range of the technology is represented by σ_ϵ then to achieve n-bits of resolution, the above ladders can be compared as shown in Table 2.1. It can be concluded that the all the resistor ladders have the same INL however, the segmented ladder is able to achieve a higher DNL compared to a binary DAC, for lesser area compared to a unary DAC.

Table 2.1: Resistor ladder comparison [4]

	Area	σ_{INL} **(LSB)**	σ_{DNL} **(LSB)**	**Glitch Impulse Area**
Unary	$2^n - 1$	$2^{(n/2-1)}\sigma_\epsilon$	σ_ϵ	Low
Binary	n	$2^{(n/2-1)}\sigma_\epsilon$	$2^{n/2}\sigma_\epsilon$	High
Segmented	$2^m - 1 + (n - m)$	$2^{(n/2-1)}\sigma_\epsilon$	$2^{(n-m+1)/2}\sigma_\epsilon$	Medium

To process AC signals with high precision, a voltage mode multiplying DAC with a segmented ladder would, therefore, be an optimum choice. However, the performance of the M-DAC also depends on the I-V converter. In most precision applications, a high gain operational amplifier is connected in an inverting configuration to act as an I-V converter as shown in Figure 2.9. The amplifier topology is also commonly referred as trans-impedance amplifier or TIA. Certain parameters of the TIA design and performance can have a significant impact on the M-DAC performance as explained in the next section.

2.3 Op-amp Specifications

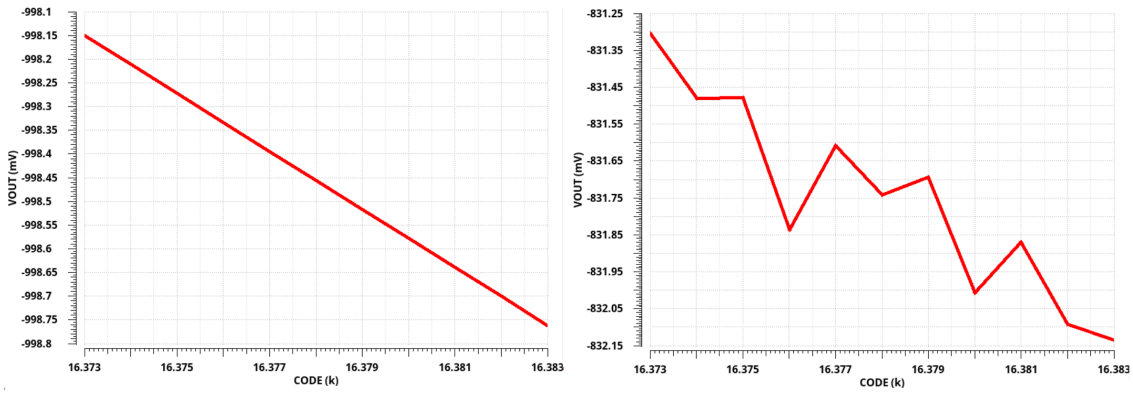
The selection or design of the op-amp to be connected as a TIA at the output of a current-mode DAC is of paramount importance when designing a voltage-mode M-DAC. Both the static and dynamic limitations of a non-ideal op-amp can be detrimental to the overall DAC performance. This heavily constraints the design of the TIA. A key point to note here is that since the TIA is an inverting amplifier, it is going to invert the DAC output

transfer function. To obtain a non-inverting output, another equally constrained inverting amplifier must be designed.

2.3.1 Dynamic Limitations

The effect of the *open-loop response* of the amplifier can limit the overall DAC precision. The open-loop gain (A_{ol}), in particular, can cause nonlinearity, gain and offset errors. This effect is more prominent for codes near full scale, as shown in Figure 2.11, due to the higher output current. Therefore, A_{ol} must be in commensurate with the resolution (n) of the ladder. The relation is established as [7],

$$A_{ol} \geq 20 \log_{10}(2^n) = 6.02n \tag{2.6}$$



(a) V_{OUT} vs CODE with high gain (b) V_{OUT} vs CODE with low gain

Figure 2.11: Effect of open-loop gain on V_{OUT}

Since the M-DAC would use the amplifier in a closed loop configuration, the *stability* and *unity-gain bandwidth* (f_t) of the system will impact the overall settling time and multiplying bandwidth. Sometimes when a stable TIA is connected to the resistor ladder, instability may ensue. This is because of the switch parasitic capacitance at the current

output terminal which can degrade the phase margin of the system. To achieve a phase margin of 45°, a compensation capacitor is usually placed across the feedback resistor, as modeled in Figure 2.12 [11], calculated as

$$C_f = \frac{1 + \sqrt{1 + 8\pi R_{FB} C_{par} f_t}}{4\pi R_{FB} f_t} \approx \sqrt{\frac{2C_{par}}{\pi R_{FB} f_t}} \tag{2.7}$$

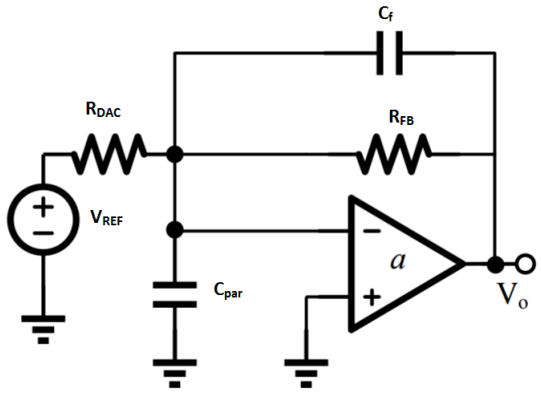


Figure 2.12: Compensation for parasitic capacitance

The M-DAC uses the virtual ground of the amplifier to precisely steer current into the feedback resistor. The accuracy of the virtual ground is given by the *closed-loop input impedance* of the op-amp which in turn is a function of the loop gain of the amplifier [13].

The *slew rate* (SR) of the amplifier can limit the maximum input voltage reference swing of the M-DAC at full-scale, given by

$$V_{REF} < \frac{SR}{\pi f_t} \tag{2.8}$$

A higher voltage reference swing will be severely distorted.

2.3.2 Static Limitations

The *input bias current* of an amplifier can reduce the amount of current flowing through the feedback resistor leading to gain errors. CMOS and FET amplifiers are therefore preferred as TIAs for the M-DAC because they have very low input bias currents ($\leq$1pA).

The *input offset voltage* is defined in [14] as the voltage that must be applied between the two input terminals of the op-amp to obtain zero volts at the output. This difference is caused because of the inherent mismatch of the input transistors and components during fabrication. In CMOS amplifiers the input offset voltage is primarily due to the differences in the threshold voltages of the input transistors of the differential pair which is caused due to the variation of the width, length, thickness and doping levels of the channels in the transistors [15].

The effect of the offset on the DAC's performance can be modeled as shown in Figure 2.13, where R_{IOUT} represents the impedance measured when looking into the I_{OUT} terminal. Using this model, and considering the amplifier to be ideal, V_{OUT} can be given as

$$V_{OUT} = V_{REF}\Big(\frac{-R_{FB}}{R_{DAC}}\Big) + V_{OS}\Big(1 + \frac{R_{FB}}{R_{IOUT}}\Big) \tag{2.9}$$

where, the R_{DAC} is the code-dependent resistor that controls the output current. For an n-bit DAC it is given by

$$R_{DAC} = R\left(\frac{2^n}{CODE}\right) \tag{2.10}$$

For R-2R resistor ladders the code dependence of R_{IOUT} is highly non-linear [3], as shown in Figure 2.14. This leads to non-linearity in V_{OUT}, depicted in Figure 2.15. On the other hand, for unary ladders the R_{IOUT} is equal to R_{DAC} and hence, is more tolerant to offset.

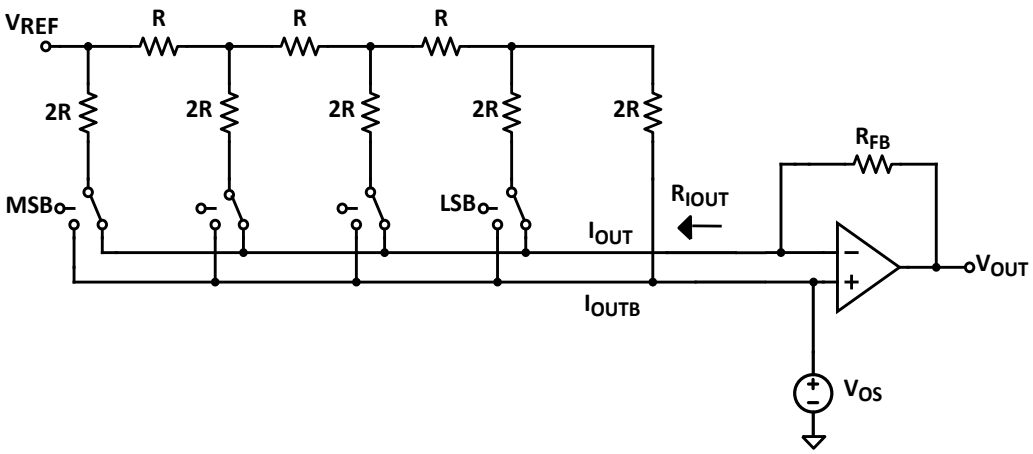


Figure 2.13: Modeling the effect of the offset on V_{OUT}

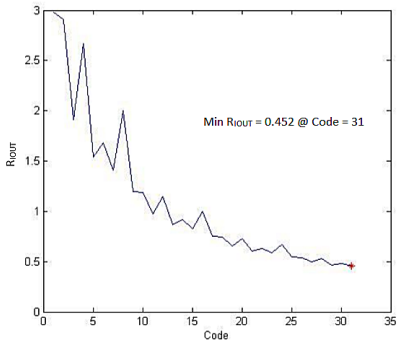
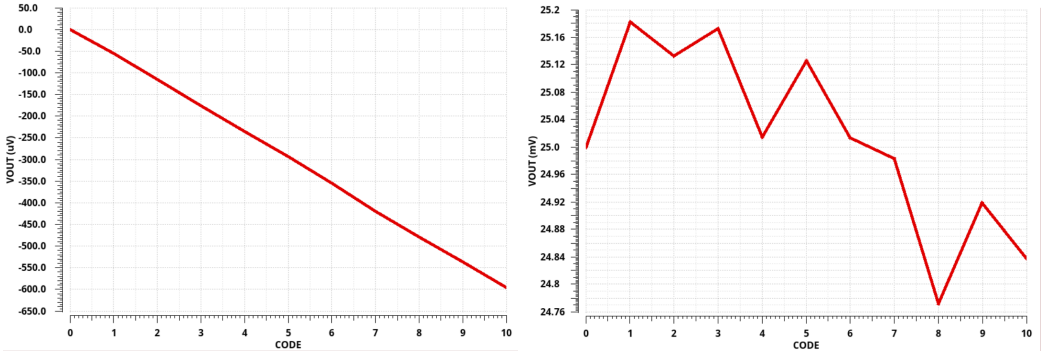


Figure 2.14: R_{IOUT} vs CODE for a 5-bit R-2R DAC [3]



(a) V_{OUT} vs CODE without offset (b) V_{OUT} vs CODE with 25mV offset

Figure 2.15: Effect of offset on V_{OUT}

Another way of modeling the effect of the offset is shown in Figure 2.16. Here, the offset is modeled at the inverting terminal. During the code transition, the current switching from the This causes different currents through the I_{OUT} and I_{OUTB} terminals given by

$$I_{IOUTB} = \frac{V_{REF}}{R_{DAC\_IOUTB}} \tag{2.11}$$

$$I_{IOUT} = \frac{V_{REF} - V_{OS}}{R_{DAC\_IOUT}} \tag{2.12}$$

where the R_{DAC_IOUTB} and R_{DAC_IOUT} represent the code-dependent resistance between the reference (REF) and the output current terminals (IOUT and IOUTB). For an n-bit DAC, they can be given as

$$R_{DAC\_IOUT} = \frac{1}{R_{DAC\_IOUTB}} = R\left(\frac{2^n}{CODE}\right) \tag{2.13}$$

The difference between the current causes non-linearity errors as shown in Figure 2.17

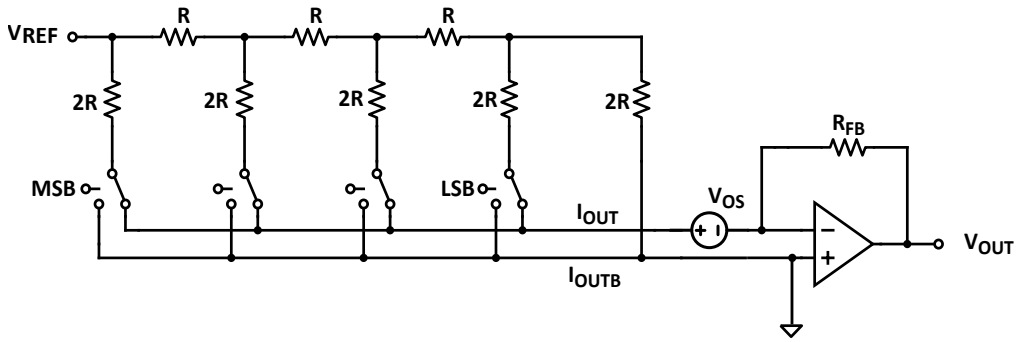
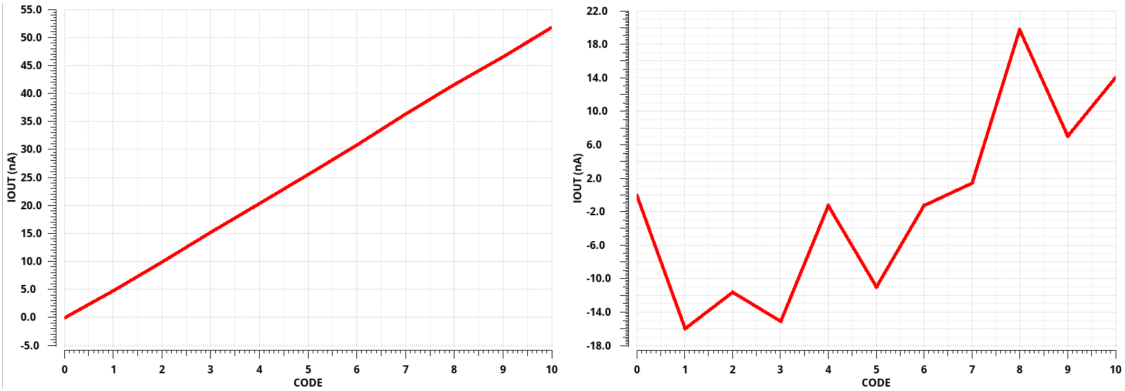


Figure 2.16: Modeling the effect of the offset on I_{OUT}



(a) I_{OUT} vs CODE without offset (b) I_{OUT} vs CODE with 25mV offset

Figure 2.17: Effect of offset on I_{OUT}

Linearity can be preserved only if the offset voltage is less than 1 LSB. For low voltage high precision DACs, this value can be in the order of 10μV. Unfortunately, the offset voltage of an untrimmed CMOS amplifier can be in the range of $\pm$5mV to $\pm$50mV [16] which can only be reduced and not eliminated. Cancellation techniques [17] such as trimming (<1mV), auto-zeroing (<500μV) or chopping (<1μV) may be used to reduce the offset. In addition to these popular techniques, negative impedances [18] and feedback loops [19] have also been proposed to cancel offset. These techniques are often expensive or complex for high-performance applications. So, instead of canceling or reducing the offset, this work attempts to tolerate the offset voltage. This eases the design or choice of the op-amp especially at low supply voltages.

3. PROPOSED ARCHITECTURE AND DESIGN

This work proposes the use of a current buffer between the resistive ladder and trans-impedance amplifier (TIA) as shown in Figure 3.1. The current buffer will be able to isolate the code-dependent output impedance (R_{IOUT}) from the TIA making the DAC insensitive to the amplifier's input offset voltage. Furthermore, if the current buffer offers an output impedance much larger than the feedback resistor (R_{FB}) then the offset voltage would experience no gain and appear at the output as a fixed offset error.

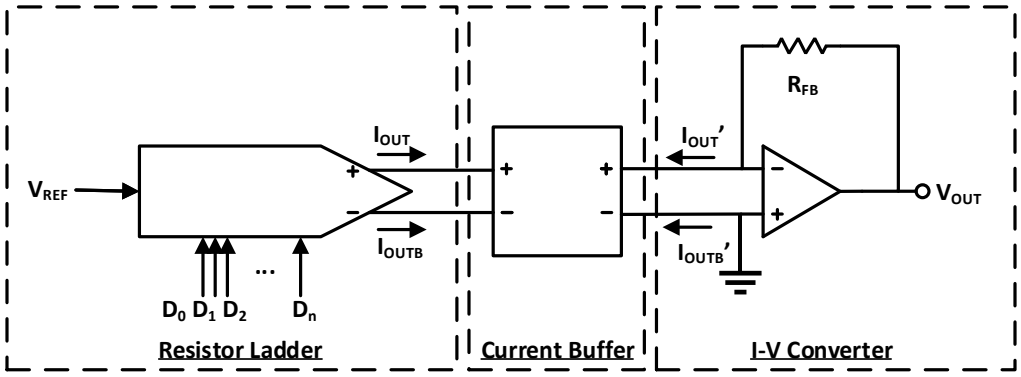


Figure 3.1: Proposed architecture

To illustrate the proposed architecture, a 14-bit M-DAC is designed to meet the following specifications:

Table 3.1: Design specifications for the proposed M-DAC

Parameter	**Value**
Resolution	14-bits
Reference Voltage	$\pm$1V
DNL	$<$0.5 LSB
Multiplying Bandwidth	10MHz
Resistor Ladder Noise	20nV/$\sqrt{Hz}$
Major carry glitch energy	$<$1nVs
Process Node	IBM-130nm

3.1 Resistor Ladder

3.1.1 Topology

Considering the area, precision and linearity the segmented ladder is chosen. To optimize the area, the ladder employs multiple levels of segmentation similar to the ladder shown in Figure 3.2. Each segment is budgeted based on the maximum offset expected from the differential input of the current buffer. As explained next, the current buffer is designed to have a maximum untrimmed offset of 3mV considering mismatches. Since the R-2R would be most affected by this offset (V_{OS}), its resolution (n) is determined to be 8-bits by

$$n = floor\Big(\log_2\Big(\frac{V_{REF}}{V_{OS}}\Big)\Big) \tag{3.1}$$

A trade-off between the accuracy and area leads the choice of the resolution for the MSB and MID segments of the ladder. In this design, 2 bits are budgeted for the MID segment while the remaining 4-bits are implemented in the MSB segment.

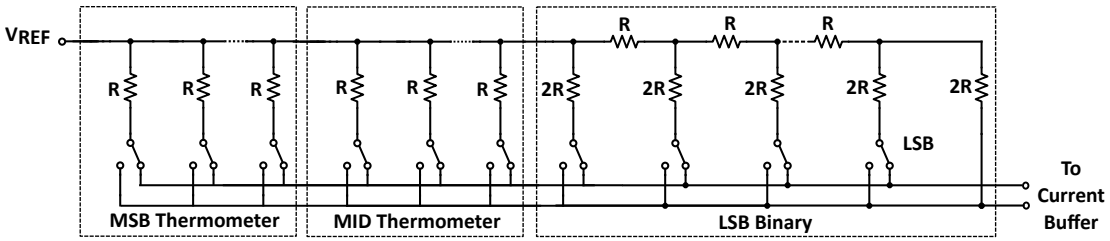


Figure 3.2: Multiple segmented ladder

3.1.2 Resistor Type

The IBM-130nm PDK allows the fabrication of poly, n-well, diffusion and thin-film resistors. Table 3.2 shows the comparison of the different implementations of a 1kΩ resistor in IBM-130. From the comparison, it is clear that the thin-film resistors offer very good matching and low parasitic capacitance, both of which are essential for high performance. In fact, as explained in [2] thin-film resistors such as Si-Cr are heavily used in the industry to design high-performance resistor ladders. Their sheet resistance can be as high as 1kΩ/square [20] however, the sheet resistance of the thin-films resistors offered in IBM-130 is less than 100Ω/square. This would entail a massive chip area making them unsuitable for this design. Moreover, the fabrication of thin-film resistors would require an additional mask layer which is not available for academic use. Diffusion and n-well resistors offer higher sheet resistances but are accompanied by large parasitics that can degrade the bandwidth of the circuit. So, this design uses poly resistors despite their poor matching. The area and technology trade-offs therefore constraint the choice of the resistor.

3.1.3 Resistor Value

Considering the resistor ladder noise specification, the value of the resistance ladder at full-scale is chosen to be 10kΩ. To achieve good matching via a common centroid layout, each resistance in the ladder is implemented by a series/parallel combination of

Table 3.2: Resistor comparison

	Matching σ	Area	Parasitic Capacitance
Poly	0.7%	$56\mu m^2$	$\approx$20fF
N-well	0.3%	$160\mu m^2$	$\approx$200fF
Diffusion	0.1%	$160\mu m^2$	$\approx$1300fF
Thin-film	0.04%	$1600\mu m^2$	$<$20fF

a unit resistance bar of 160kΩ. The area of the unit resistance bar is chosen based on the matching requirements of the ladder. To achieve the matching requirement for the DNL accuracy from the poly resistors the size of the unit resistance bar was chosen to be 220μm$\times$0.5μm after running multiple mismatch/monte-carlo simulations.

3.2 Switches

The ladder employs two switches forming a single-pole double-throw (SPDT) connection between the ladder and the IOUT/IOUTB output. The choice and design of the switch is crucial for reliability and linearity.

3.2.1 Choice of Switch

The SPDT switch can be implemented by using an NMOS or PMOS, or even a complementary switch. In the resistor ladder, the switch must have a very low R_{on} and should connect the resistors to a low impedance node or virtual ground so, an NMOS switch is typically used. To achieve very low R_{on}, low V_t or zero V_t transistors can be used, however it must be noted that these transistors suffer from large process variations. Instead, low-voltage or digital switches can be used, because the drop across the switch is expected to be in the order of millivolts. However, the maximum tolerable voltage of the V_{bd} must be taken into account before opting for low-voltage switches. For an SOI process, this is not a problem, since the bulk can be shorted to the source to ensure reliable operation. However, for IBM-130, which is a bulk-CMOS process, the low voltage (1.2V) transistors

can tolerate upto 1.5V of V_{bd} and since this design employs a -1.6V VSS reliability issues may occur. To avoid this high voltage (3.3V) NMOS switches are used.

3.2.2 Switch Sizing

If all the CMOS switches are sized equally, then their R_{on} must be very small compared to the resistors to keep the non-linearity errors low. This would entail large size switches which are accompanied with parasitic capacitances. To alleviate this problem, the switches can be binary weighted similar to the resistors. This would mean that the switches near the MSB would be large and can lead to large-glitch impulses during transitions. This design employs a good compromise between these two choices by employing a fixed switch size for each resistor segment but scaling the switches between the segments. The switch size for the LSB section was fixed to be at 1μm/0.4μm, which yields an R_{on} of 3kΩ which is less than 1% of the unit resistor used in the LSB section. The switches in the MID section were scaled by $2\times$ while the switches in the MSB were scaled by $8\times$. Each of the switches were fingered in the layout to reduce the parasitic capacitance and hence any associated glitch impulse energy.

The final resistor ladder schematic is shown in Figure 3.3.

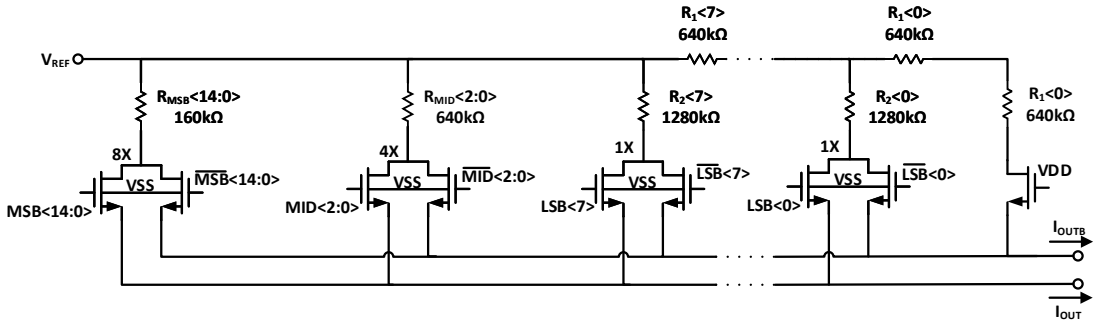


Figure 3.3: Resistor ladder schematic

3.3 Current Buffer

An ideal current buffer must offer zero input impedance and infinite output impedance. For this design to maintain linearity, the input impedance must be less than 0.1Ω and the output impedance must be greater than the unit resistance (10kΩ).

The proposed current buffer topology is shown in Figure 3.4. Transistors M_1 to M_3 form a common gate amplifier whose input impedance is given by $1/g_{m1}$. Amplifier A_1 is used to boost the g_m of the transistor and reduce the input impedance. In order to achieve a low input impedance using g_m boosting, the gain of the A_1 must be very high ($\approx$ 80dB). So, this topology employs a second shunt-shunt feedback in M_4-M_5-M_2. Transistor M_4 along with M_5 act as level shifters while providing a small signal gain of 1. The current flowing into IN+ produces a voltage at IN+ propotional to the impedance at that node. When the current increases, the corresponding voltage also increases, which causes an increase of the voltage at the drain of M_1. This increase is reflected at the gate of M_2 via M_4 making M_2 sink more current and hence reduce the voltage swing at IN+. The use of this dual feedback allows achieving input impedance in the order of 0.1Ω as given by [21],

$$R_{in} \approx \frac{1/g_{m1}}{A_{v1}.g_{m2}.r_{ds3}} \tag{3.2}$$

To improve the output impedance, auxiliary amplifiers A_2 and A_3 are used to maintain equal voltages at the drains of M_6 and M_3. This increases the output impedance of the mirror and allows for precise mirroring of the current to the output. The transistor-level implementation of the amplifiers A_1 and A_2/A_3 is shown in Figure 3.5. In amplifier A_1, the output pole is designed to be the dominant pole. In amplifier A_2/A_3 however, the dominant pole is set to be at the output of the first stage. The second stage amplifier would offer a low impedance at output, pushing that pole to a high frequency.

Since the current buffer is connected to the resistor ladder, it is important that the offset

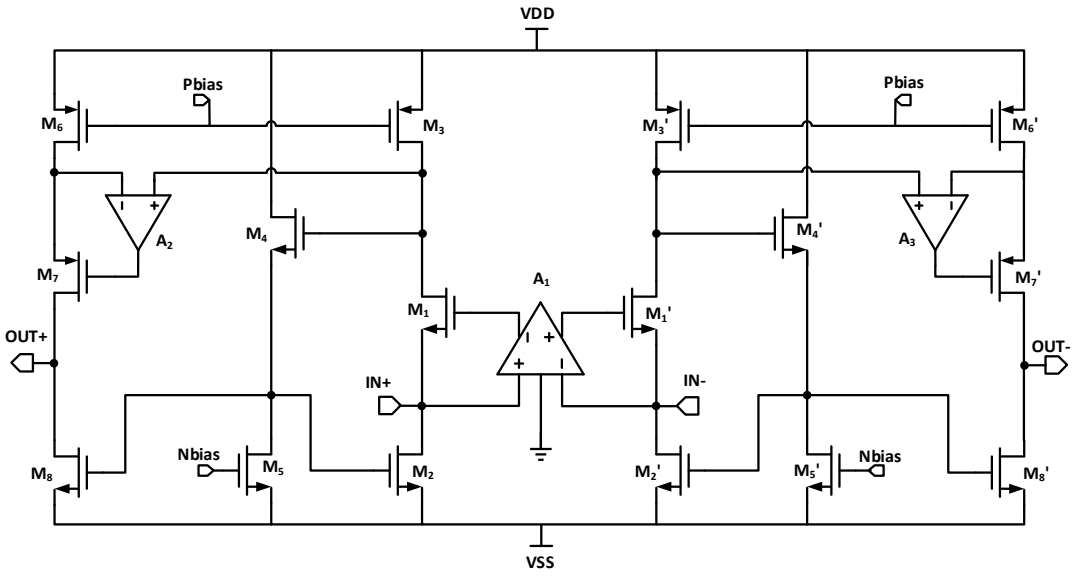
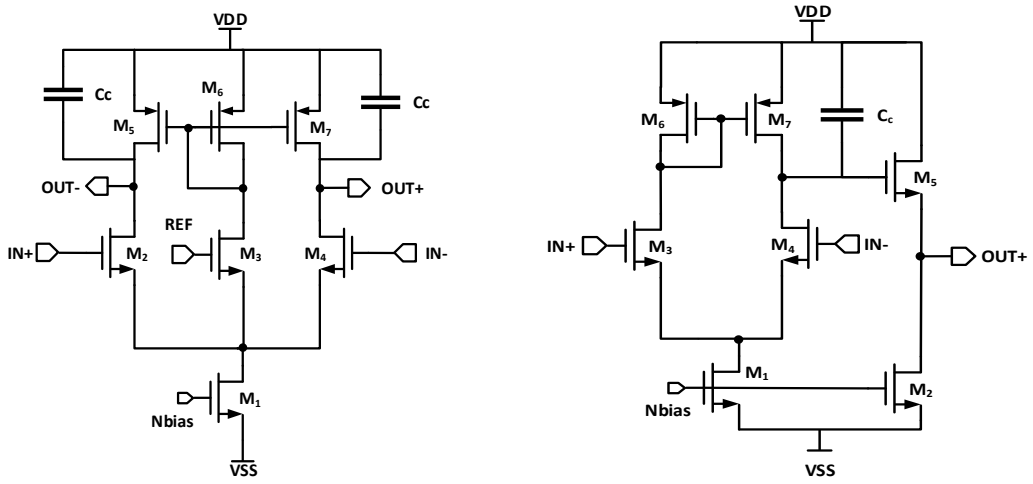


Figure 3.4: Current buffer schematic

between the differential input terminals of the current buffer must be minimum. To ensure this, the input transistors of the current buffer were sized to offer no more than 3mV of offset considering mismatches. This offset margin dictates the design of the resistor ladder's LSB segment. In addition to this, the current buffer should be able to sink 100uA of current from the ladder. So to maintain a linear operation, the current sources in the buffer are designed to source about 200uA of current. The final design sizes are listed in Table 3.3.



(a) Amplifier A_1 schematic (b) Amplifier A_2/A_3 schematic

Figure 3.5: Auxiliary amplifiers

Table 3.3: Current buffer design sizes

Amplifier A_1

Transistor	**W/L (μm)**
M_1	160/0.8
M_2	12/0.8
M_3	12/0.8
M_4	12/0.8
M_5	40/0.8
M_6	40/0.8
M_7	40/0.8

Amplifier A_2/A_3

Transistor	**W/L (μm)**
M_1	20/0.8
M_2	5/0.8
M_3	12/0.8
M_4	12/0.8
M_5	12/0.8
M_6	10/0.8
M_7	10/0.8

Current buffer

Transistor	**W/L (μm)**
M_1	10/0.8
M_2	5/0.8
M_3	300/0.8
M_4	1/0.8
M_5	2/0.8
M_6	300/0.8
M_7	100/0.8
M_8	5/0.8

The symmetric layout of the current buffer is crucial in minimizing offset. A fully symmetric place-and-route is performed and care is taken to implement common centroid techniques. Since the buffer should be capable of sinking and sourcing relatively large currents, the metals in the layout are larger than minimum width to reduce parasitic resis-

tances. Care is also taken to keep the metal between the resistor ladder and the current buffer as thick as possible to minimize resistance while keeping the parasitic capacitance low.

3.4 Transimpedance Amplifier Design

Based on the resolution, multiplying bandwidth and voltage reference swing, the op-amp used in the TIA is expected to have a DC Gain of 84dB with a gain-bandwidth product of 20MHz and a slew rate of at least 32V/us. The TIA is expected to have an output voltage swing of $\pm$1V as well. As shown in Figure 3.6, a folded cascode topology with a class AB output stage [22][23] with indirect compensation is designed to satisfy the specs while using minimum power. The op-amp design is optimized for a closed loop gain of -1. When connected to the resistor ladder, the op-amp observes a parasitic capacitance (C_{par}) of nearly 2pF. This parasitic capacitance can degrade the phase margin of the circuit. So, a compensation capacitor (C_f), as shown in Figure 2.12, is connected to maintain atleast 45° of phase margin. The value of the capacitor is computed to be 3pF using Equation (2.7).

Choosing a 300fF miller capacitance (C_M), the final transistor designs are listed in Table 3.4

Table 3.4: Op-amp design sizes

Transistor	**W/L (μm)**
M_1	20/0.8
M_2	20/0.8
M_3	190/0.8
M_4	76/0.8
M_5	19/0.8
M_6	2.5/0.8
M_7	5/0.8
M_8	5/0.8
M_9	304/0.8
M_10	20/0.8

Typical M-DAC architectures demand a fully symmetric amplifier layout to minimize the offset. However, in this design since the M-DAC is tolerant to offset, the layout of the op-amp is not very stringent. In order to prove this point, the op-amp was placed and routed as shown in the schematic with no consideration for offset. This yielded an offset of about 2.5mV.

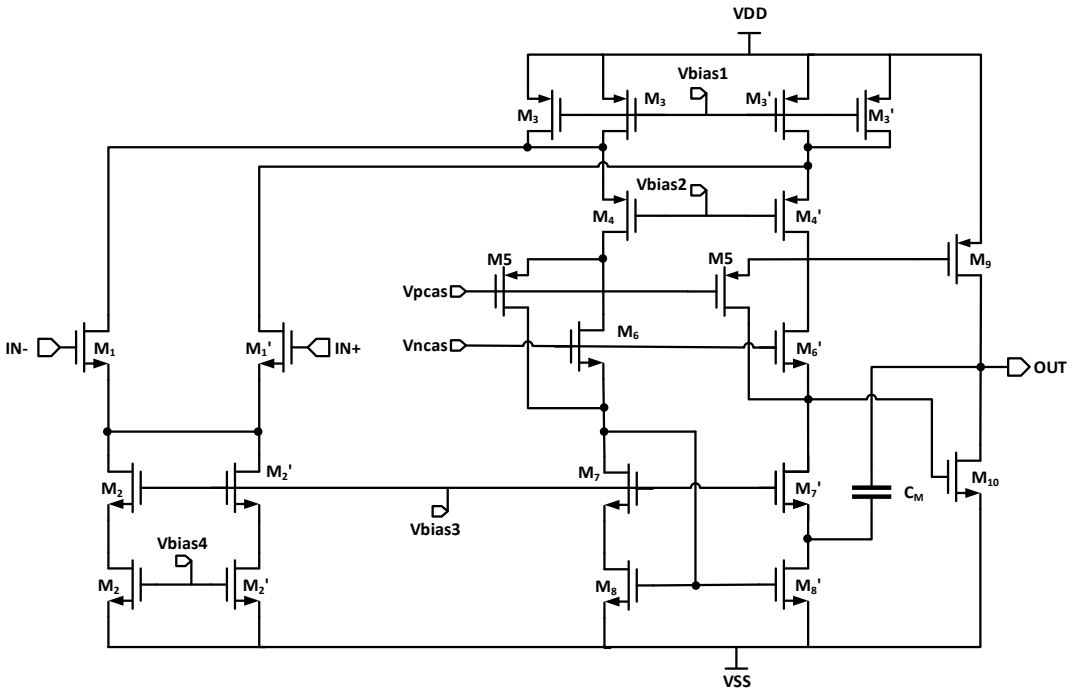
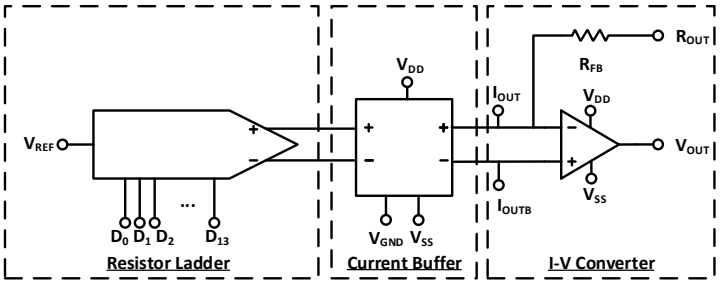
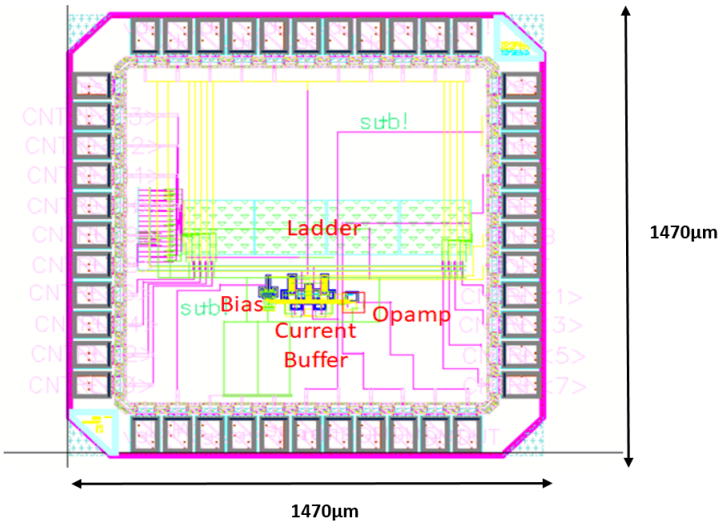


Figure 3.6: Folded cascode amplifier with indirect compensation

At the top-level schematic, the feedback resistor is not connected to the op-amp as shown in Figure 3.7a. This allows connecting external op-amps for testing the offset tolerance. Figure 3.7b shows the layout with the total area being $1470\mu\text{m}\times1470\mu\text{m}$, where the resistor ladder occupies $1036\mu\text{m}\times182\mu\text{m}$, while the active circuit occupy $324\mu\text{m}\times140\mu\text{m}$.



(a) Schematic



(b) Layout

Figure 3.7: Chip top

4. RESULTS AND DISCUSSION

This section presents the results of the M-DAC design. All the results are post-layout simulations post-layout, unless specified.

The M-DAC is designed to achieve a resolution of 14-bits and with a DC voltage reference of 1V, it has an LSB of 61μV.

4.1 Static Performance

Figure 4.1 shows the DC transfer function of the M-DAC. Notice that the transfer function increases with code, unlike a typical M-DAC that shows inverting output. This is due to the additional inversion of the current mirror in the current buffer. The offset error is measured to be 42 LSB or 2.5mV, and the gain error is 0.001 LSB. The offset error is due to the intentional input offset voltage created in the layout of the folded cascode op-amp.

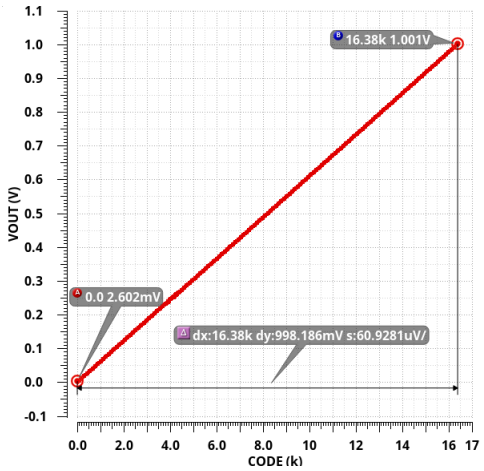
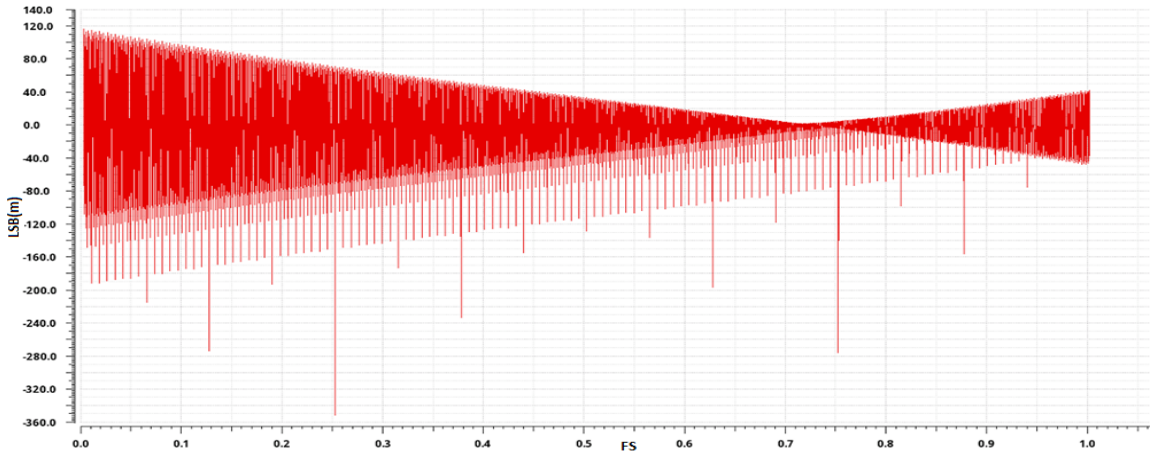


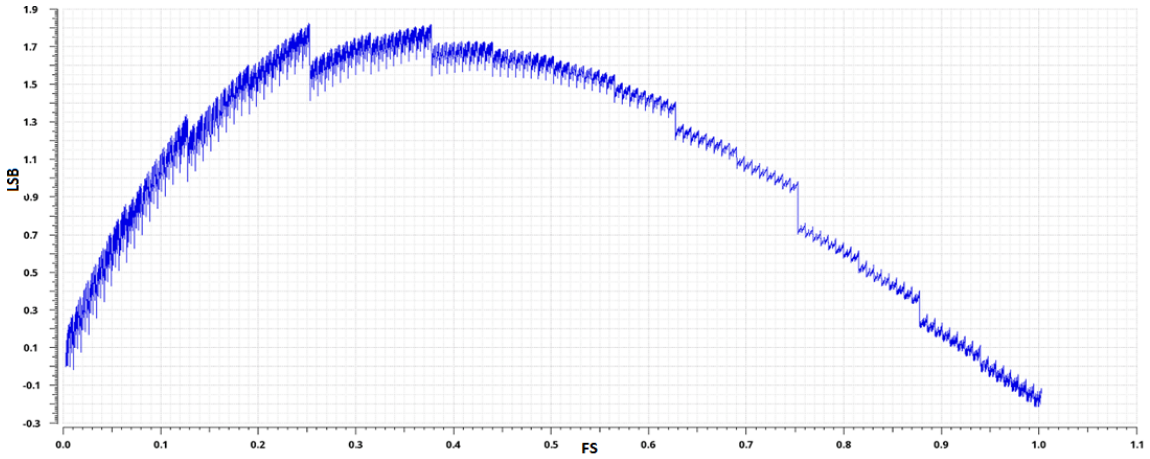
Figure 4.1: DAC transfer function

Figure 4.2 shows the DNL and INL curve across all the DAC codes for the typical

corner. The worst corner DNL is found to be -0.385 LSB while the INL is 1.8 LSB. The conical shape of the DNL curve in Figure 4.2a is because at around mid-scale the current flowing into the two terminals of the current buffer are nearly equal and hence experience equal voltages at the input of the current buffer. At zero code (or full-scale), the IOUTB(IOUT) is much smaller than IOUT(IOUTB) causing the two terminals to experience slightly different voltages leading to non-linearity. The layout parasitic resistances shift the minimum DNL point from mid-scale.



(a) DNL curve



(b) INL curve

Figure 4.2: Non-linearity curves

To demonstrate the effect of offset on linearity, an ideal op-amp with variable input offset voltage was used in simulation. Figure 4.3 show the effect of 25mV offset on the linearity of the DAC at mid-scale without the current buffer. Figure 4.4 shows the improved linearity in the presence of the buffer, and Figure 4.5 shows that the offset voltage of the op-amp is reduced to an offset error of the overall DAC with minimal impact on the gain error or linearity.

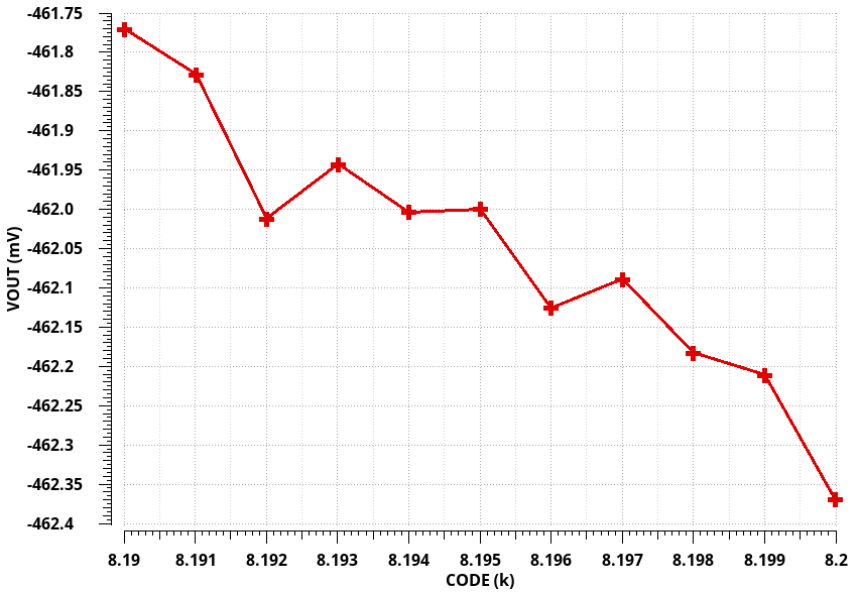


Figure 4.3: V_{OUT} vs CODE without the current buffer

Schematic-level monte-carlo mismatch simulations are also performed on the design to find the yield. Here, the yield is defined as the number of mismatch conditions for which the DNL would be under the targeted $\pm$0.5 LSB. The simulations reveal that the yield is about 30$\%$ meaning that for every 100 designs chosen at random 30 designs would achieve a DNL $<$0.5 LSB. This can be improved by using better matching thin-film resistors instead of the poly.

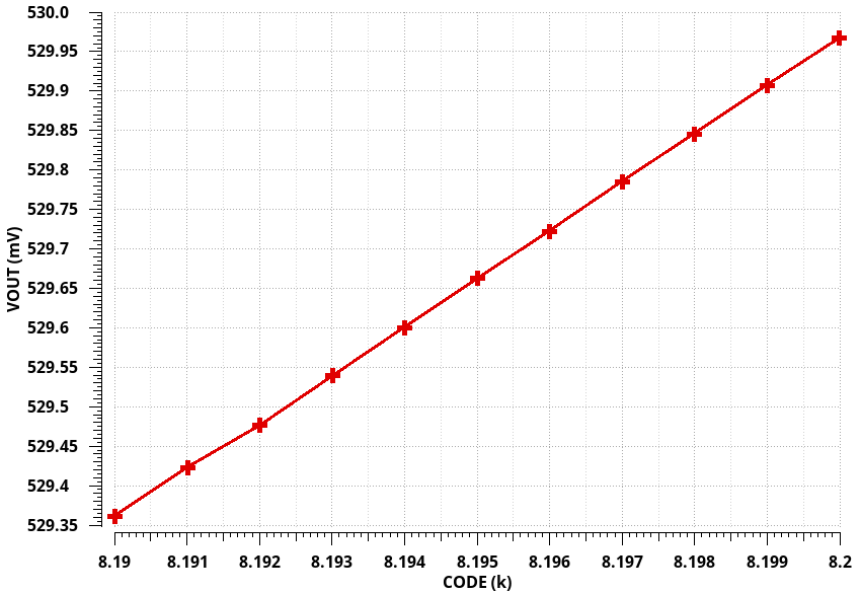


Figure 4.4: V_{OUT} vs CODE with the current buffer

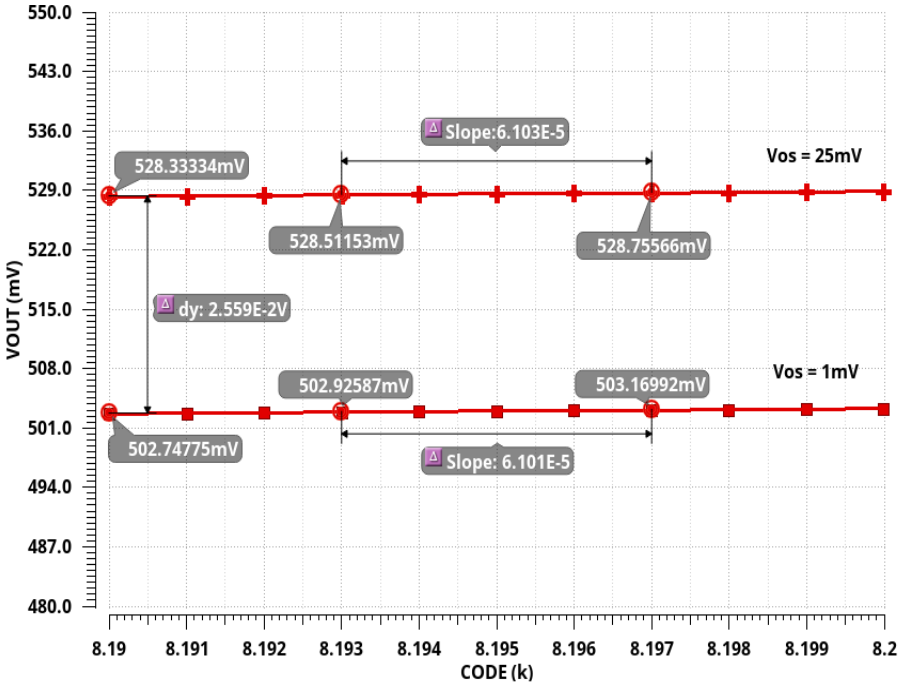


Figure 4.5: Input offset voltage reduced to offset error

4.2 Dynamic Performance

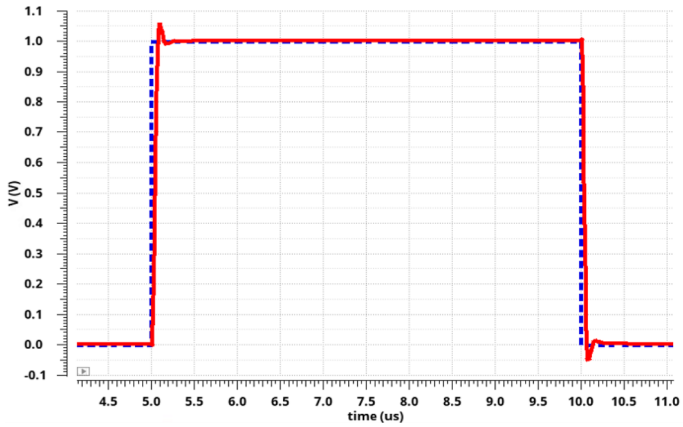
Figure 4.6 shows the response of the M-DAC to a step of the reference voltage and Code. The output voltage settles to within 1 LSB of the final value in 1μs for a step in reference, and 589ns when the code changes from 0 to FS. For an LSB change at the mid-scale, the glitch impulse energy is computed to be 0.6nVs as shown in Figure 4.6c.

Figure 4.7 shows the AC response of the M-DAC with respect to the reference signal. Figure 4.7a shows the multiplying bandwidth to be 8.6MHz while Figure 4.7b shows the multiplying feedthrough to be -130dB at 100kHz.

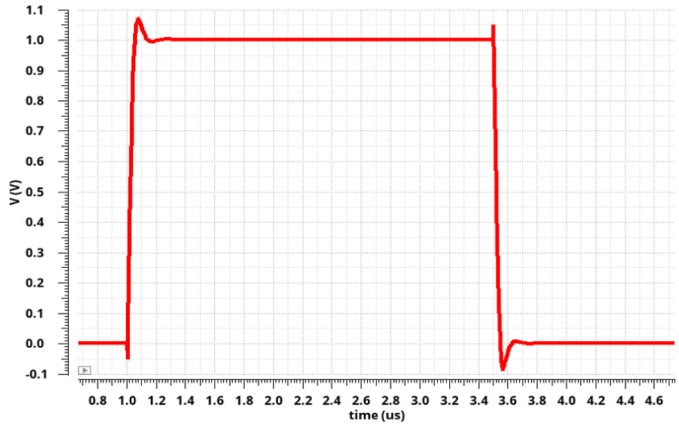
Figure 4.8 shows the response of the M-DAC to a sinusoidal reference at full-scale. The reference has an amplitude of 100mV with a frequency of 10kHz.

The analog THD is measured to be 80dB with the DAC being driven by a 10kHz 1V_{pp} sine wave reference at mid-scale.

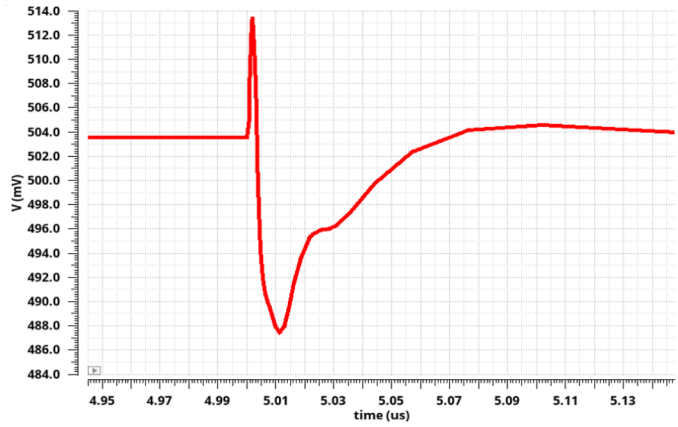
The digital THD of the DAC was measured by converting a 10kHz sine wave into 14-bit code using a 1-MHz ADC. Figure 4.9 shows the transient waveform at the input of the ADC and the output of the DAC. The digital THD was measured to be 90dB.



(a) V_{out} settling for a 1V step in reference voltage

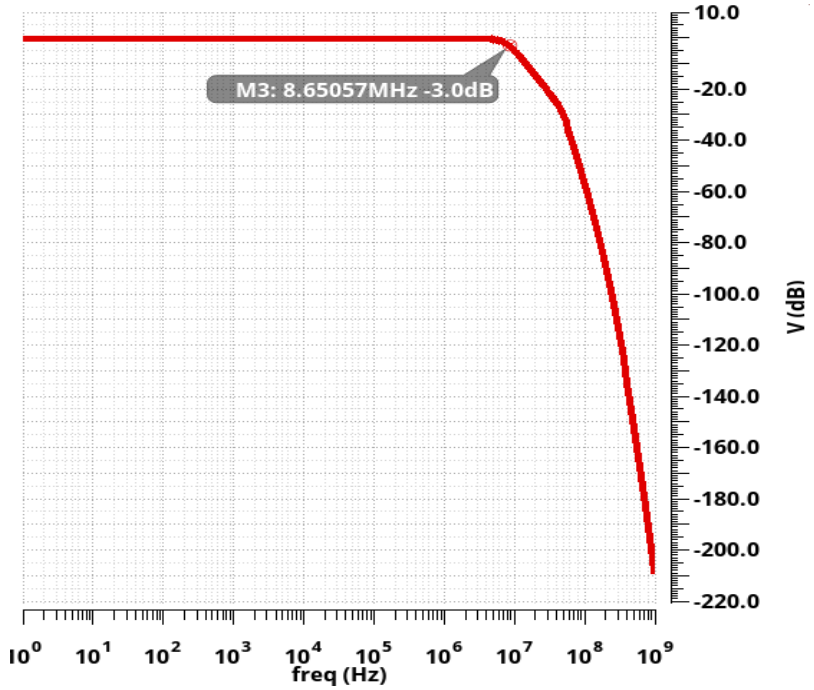


(b) V_{out} settling for a code step from 0 to FS

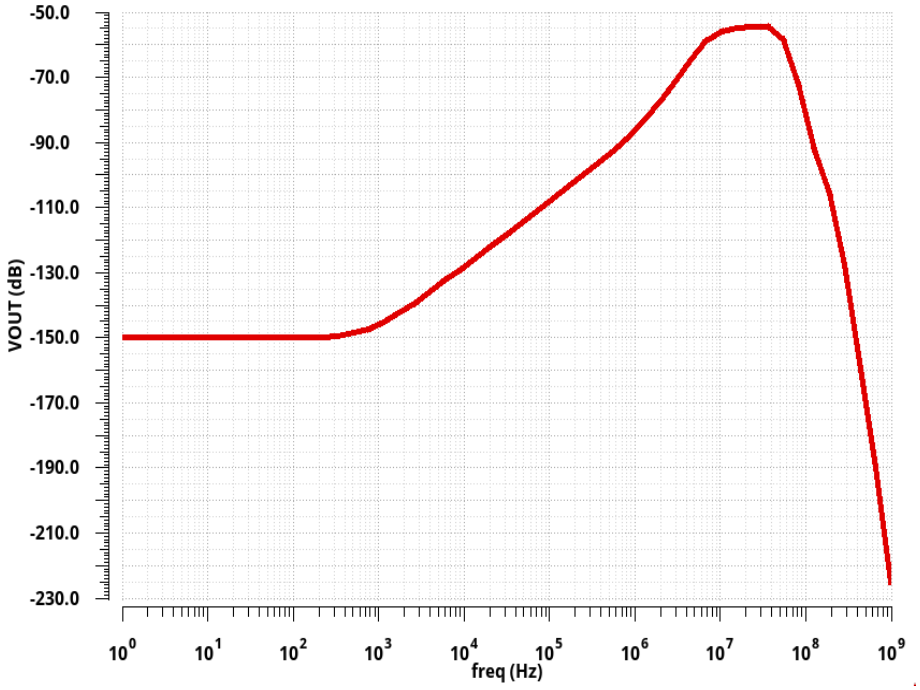


(c) Major-carry glitch

Figure 4.6: Step response



(a) Multiplying bandwidth



(b) Multiplying feedthrough

Figure 4.7: Reference AC response

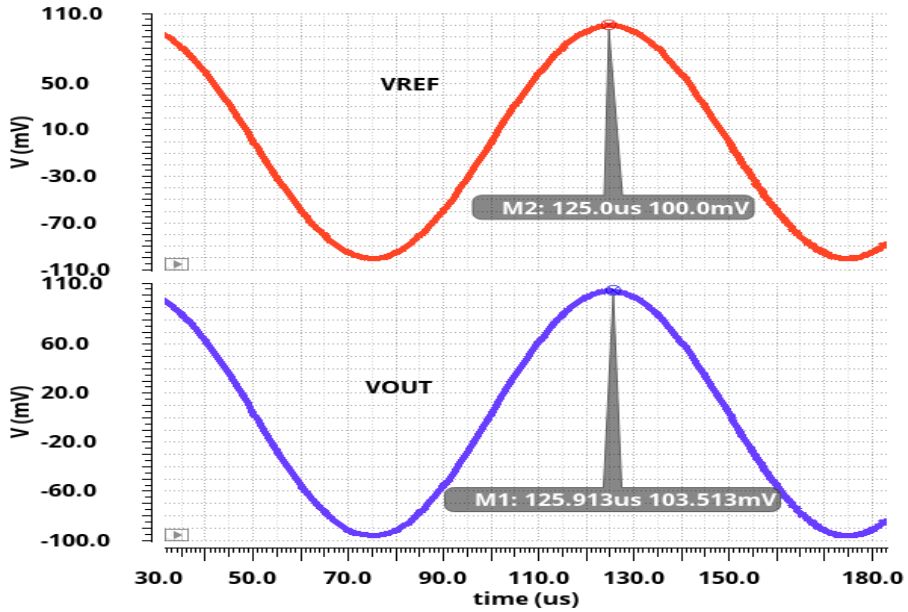


Figure 4.8: Reference sine response

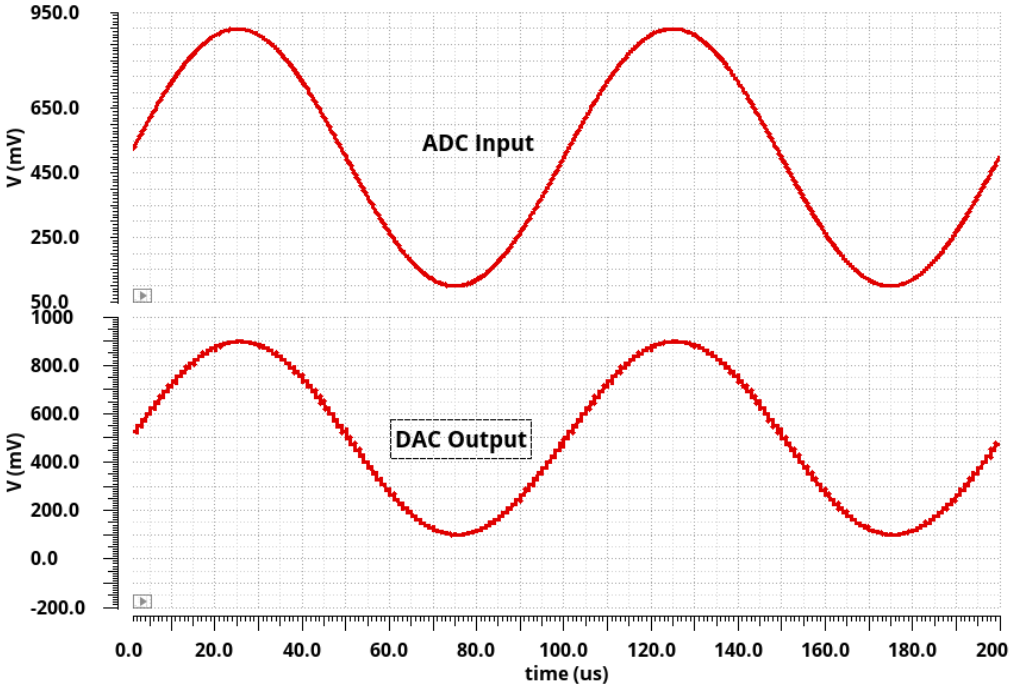


Figure 4.9: Digital sine response

4.3 Noise Performance

The noise performance of the M-DAC is measured at the output of a commercially available operational amplifier OP177. Figure 4.10 shows the equivalent output noise spectral density with and without the current buffer. The additional active components in the current buffer contribute to the difference in the output noise with the output NMOS transistors M2 and M8 being the dominant sources. The flicker noise near DC can be as high as $140\mu V/\sqrt{Hz}$ which can degrade the ENOB of the converter by at-least 1 LSB.

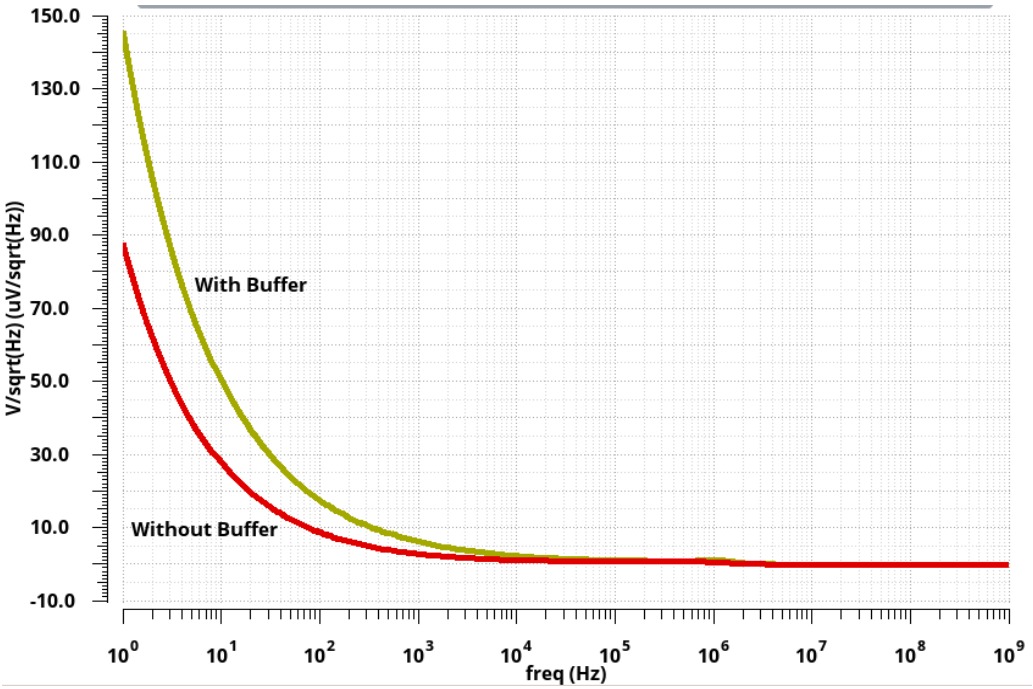


Figure 4.10: Equivalent output noise performance

4.4 Performance Comparison

Table 4.1 shows the comparison of the proposed DAC design against commercial M-DACs [12][24][25]. Since most M-DAC research in the academia is concentrated in capacitor-based DAC designs, commercial M-DACs are used as a comparison metric.

Table 4.1: Comparison with commercial M-DACs

	This Work	**[12]**	**[24]**	**[25]**
Resolution	14-bits	14-bits	14-bits	14-bits
Reference Voltage	$\pm$**1V**	$\pm$10V	$\pm$10V	$\pm$10V
DNL	-0.385 LSB	$\pm$1 LSB	$\pm$0.5 LSB	$\pm$1 LSB
INL	*1.8 LSB*	$\pm$1 LSB	$\pm$1 LSB	$\pm$1 LSB
Offset Tolerance	**1024 LSB**	<64 LSB	<64 LSB	<25 LSB
Multiplying Bandwidth	*8.65MHz*	10MHz	12MHz	-
Multiplying Feedthrough	**-130dB**	-70dB	-72dB	-86dB
Resistor Ladder Spot Noise	13nV/$\sqrt{Hz}$	12nV/$\sqrt{Hz}$	25nV/$\sqrt{Hz}$	11nV/$\sqrt{Hz}$
Output Spot Noise at 1kHz	*6μV/$\sqrt{Hz}$*	*3μV/$\sqrt{Hz}$*	*3μV/$\sqrt{Hz}$*	*3μV/$\sqrt{Hz}$*
Glitch Impulse Area	**0.6nVs**	5nVs	2nVs	2nVs
V_{out} Settling	1μs	0.5μs	100ns	2μs
Analog THD	-81dB	-105dB	-83dB	-108dB
DVDD/DVSS	1.6V/-1.6V	5V/0V	5V/0V	5V/0V

It can be seen that the proposed design operates at a reference voltage much lower than that of the commercial M-DACs. The technology used for the current design will not be able to support such high voltages. On the other hand, the commercial M-DACs are typically restricted to a minimum of 2.5V DC reference owing to the linearity problems that may arise with lower references. Despite the different reference voltages, the proposed design is capable of showing minimal linearity degradation with high offset voltages due to the current buffer.

The commercial M-DACs are known to use large technology sizes in the order of

0.6μm or higher, while the proposed design uses a 0.13μm technology. The reduced size and segmented ladder design offer lower parasitics and hence the proposed M-DAC shows smaller multiplying feedthrough and glitch impulse area.

Owing to the different definition used for the V_{out} settling time, the values in Table 4.1 are widely different. [12] measures 14-bit settling time for a code change from 0 to mid-scale while [24] measures settling time to within $\pm$1mV of FS for a code change from 0 to FS. On the other hand, [25] measures 16-bit settling for a 0 to 5V step in the response. The settling time for this design is measured for both the reference step and code change from 0 to FS. The larger of the two is reported in the table. The test setup for the Analog THD also varies from one DAC to the other. This design employs a 100mVpp sine input at 10kHz with the DAC set to mid-scale.

5. FUTURE WORK

The introduction of the current buffer in the M-DAC architecture adds considerable noise to the output current. As shown in the previous section, for low frequency or DC applications the flicker noise of the MOS devices in the current buffer is capable of reducing the effective resolution of the DAC. A future design should be capable of minimizing this noise. Possible solutions include the use of larger devices, fully symmetric differential circuits or even switched biasing [26]. Besides noise, the current buffer consumes power in the order of 2.5mW. The large power consumption is because of the bias current required for maintaining the linearity of the current buffer. A future design should be able to reduce the power consumed and yet maintain the required linearity. A possible solution includes the use of a precision class-AB current mirrors [27] or even current conveyors [28].

In addition to tolerating the offset of the TIA, the proposed architecture also relaxes the requirement for a high open-loop gain op-amp in the TIA. In the traditional architecture, the open-loop gain of the op-amp ensured a low closed loop input impedance for maintaining linearity. In the proposed architecture however, the current buffer is tasked with maintaining a low input impedance. So, future designs of the voltage mode DAC can use low power moderate gain op-amps for the TIA. However, it must also be noted that while using a low gain amplifier may not impact the linearity, it does lead to a gain error.

Calibration schemes as in [29] can also be used in future design to correct the offset and gain errors.

6. CONCLUSION

This work presents the effect of the input offset voltage of a transimpedance amplifier (TIA) on the linearity (DNL) of a voltage-mode M-DAC. It then proposes an introduction of a current buffer between the M-DAC resistor ladder and the TIA to minimize the non-linearity. A 14-bit M-DAC was designed with the proposed architecture. Post-layout simulation results show that the effect of the offset voltage is reduced to an offset error in the DAC's transfer function while maintaining a maximum DNL of -0.385 LSB. The current buffer is also able to provide an inversion to the signal alleviating the need for an additional high precision inverting amplifier. The THD of the DAC was found to be commensurate with the resolution, while the use of the 130nm process node and segmented ladder structure yielded a multiplying feedthrough error of -130dB and glitch impulse area of 0.6nVs, which is superior than the commercial DACs. The flicker noise of the MOS devices in the current buffer dominated the noise performance of the proposed architecture; reducing the effective resolution of the DAC to 13-bits at DC or low frequency. Possible solutions to reduce the flicker noise and power consumption were also briefly discussed.

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