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MULTI-HARMONIC MODELING OF LOW-POWER PWM DC-DC CONVERTER

A Thesis

by

DI GAO

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MASTER OF SCIENCE

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ABSTRACT

Modeling and simulation of switched-mode Pulse Width Modulated (PWM) DC-DC converters form an essential ingredient in the analysis and design process of integrated circuits. In this research work, we present a novel large-signal modeling technique for low-power PWM DC-DC converters. The proposed model captures not only the time-averaged response within each moving switching cycle but also high-order harmonics of an arbitrary degree, hence modeling both the average component and ripple very accurately. The proposed model retains the inductor current as a state variable and accurately captures the circuit dynamics even in the transient state. By continuously monitoring state variables, our model seamlessly transitions between the continuous conduction mode (CCM) and discontinuous conduction mode (DCM), which often occurs in low-power applications. The nonlinearities of devices are also considered and efficiently evaluated resulting in a significant improvement in model accuracy. With a system decoupling technique, the DC response of the model is decoupled from higher-order harmonics, providing additional simulation speedups. For a number of converter designs, the proposed model obtains up to 10× runtime speedups over transistor-level transient simulation with a maximum output voltage error less than 4%.

ACKNOWLEDGEMENTS

My sincere gratitude goes to my advisor, Prof. Peng Li. Without his guidance and support, most of the work presented in this dissertation would not have been accomplished. He has enlightened me through his wide knowledge in Electronic Design Automation area and his deep intuitions about where my research should go and what is necessary to get there. I learn so much from Prof. Li in every one-on-one meeting, informal discussion and group meeting. I would also like to thank my committee members Prof. Gwan Choi and Prof. Rabi Mahapatra for their support.

Thanks to my friends and colleagues in our group. Ya Wang worked with me and gave me a lot of instructions on this topic. His great idea on device nonlinearities evaluation is essential to this work. Dr. Dani Tannir initialized the averaged modeling of DC-DC converters. He participated in many meaningful discussions and helped a lot on writing the companion paper for this work. Qian Wang has been a big brother to me and introduced me to VLSI computer aided design.

Last but not the least, I would like to thank my parents and grandparents for all their bring-up, encouragements and supports all these years.

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INTRODUCTION

I.A. Motivations

DC-DC power electronic systems are widely used in industry to provide power management for applications ranging from computing communications to medical and automobile electronics. In [1], Pulse Width Modulated (PWM) DC-DC converters usually involve a switching cell composed of semiconductor switches like MOS transistors and diodes, as well as passive elements such as inductors and capacitors. PWM DC-DC converters are one of most fundamental types of DC-DC converters, and are the subject of the presented modeling work.

The transient simulation of DC-DC power electronic system is generally very time-consuming due to the co-existence of fast switching activities and slow load variations. With an efficient and accurate modeling and simulation, designers can better choose topology, determine component parameters and predict circuit performance. However, difficulties still exit, including generality and usability of the model, long simulation time and consideration of important non-ideal device characteristics.

I.B. Survey of Previous Work

One fundamental modeling methodology of DC-DC converters is switched time-varying large-signal non-linear state-space models. These models can produce detailed behaviors

within one switching cycle but generally remain slow and intricate for designer to use. Circuit averaging techniques, which average the switching behaviors and present the cycle-to-cycle dynamics, are well suited for the efficient simulation of DC-DC converters [3]. In particular, state-space averaging has been a very popular simulation technique of PWM DC-DC converters. In [4], both large-signal and small signal state-space average models for DC-DC converters operating in continuous conduction mode (CCM) are presented. However, in many applications, average models for circuits operating in discontinuous conduction mode (DCM) are also desired. This is especially the case for low-power designs in which the load current is at a low level and discontinuous in time. In [5], a numerically constructed average model that extends the state-space averaging technique and allows for the simulation of DC-DC converters in both CCM and DCM is presented, whereas [6] investigates the relations governing all the different average currents under DCM operation and presents an enhanced state-space average model that accurately predicts the average value of the discontinuous inductor current. However, without considering nonlinear device characteristics, [6] and [5] are inaccurate in simulating low-power DC-DC converters. Also the modeling approach of [6] and [5] is circuit-specific, thereby limiting the ability to automate the modeling and simulation process on arbitrary DC-DC converter topologies.

Alternatively, the PWM switch circuit model that was first introduced in [7][8], which is a linearization of the three-terminal switch cell, can be readily applied to a wide range of DC-DC converters. However, neither of [7][8] presents a general model that supports the transitions between CCM and DCM operation. In [2], the basic PWM

switch model is enhanced by continuously tracking the circuit operating mode in order to allow for the simulation of DC-DC converters operating in both CCM and DCM. While the PWM switch model is simple to apply and very CPU efficient during simulation, the major limitation of the PWM switch model is that it neglects the dynamic behavior of DC-DC converters within one cycle and provides no information about the waveform ripples. As suggested in [12], the PWM switch model has an underlying assumption of a small ripple condition, which prevents it from being applied to converters with large ripples. It has been shown that neglecting the ripples of state variables can lead to large discrepancies in the simulation results of converters operating at low frequencies [11].

To address this problem, a lot of work has been done on the generalized averaging techniques [2]. In [11], a multi-frequency averaged model is introduced which conducts frequency selective averaging on the switched state-space models of DC-DC converters. However, this method is based on boost converters and cannot be easily applied to other converter configurations. In [12], a flexible method of in-place averaging that replaces elements in DC-DC converters with the k^{th} index averaged elements is presented, thereby allowing for the tracking of responses with harmonics up to k^{th} degree. However, the method in [12] assumes a continuous inductor current with ideal switches that have no nonlinear characteristics. As a result, such a model becomes neither suitable nor accurate enough for low-power DC-DC converter simulations.

I.C. Proposed Solutions

In this research work, we present a complete solution to low-power PWM DC-DC

converter modeling and simulation. The proposed solution combines the accuracy of enhanced state-space averaging with the flexibility of PWM switch models and the multi-harmonic nature of the generalized models.

The proposed model has four main features. First, the model approximates the actual converter responses by multiple harmonics of ripples up to an arbitrary degree. Second, the model accounts for the effects of device nonlinearities, such as the forward voltage drop of diodes and the on resistance of transistors. An efficient method is provided to evaluate these nonlinearities during the simulation. The third feature lies in its generality. Similarly to the PWM switch model, our proposed model is based on the switch cell and can be applied to many DC-DC converters including buck, boost and buck-boost converters without any modifications. It is also general in the sense that both CCM and DCM operations are supported. Finally, a system decoupling technique is introduced to simulate converters with improved efficiency. As a result, when applied to several open-loop and closed-loop DC-DC converters, the proposed model generates almost identical responses as the transistor-level simulations with a runtime speedup of one order of magnitude.

CHAPTER II

BACKGROUND

In this chapter we shall describe the concepts and background work that made this thesis possible. An example of buck converters is built to analyze the operation of DC-DC converters. Firstly, we present the nonlinear and periodic features of the PWM switch cell, which is fundamental for many key analysis and methodologies in this work. Usually, DC-DC converters have two operation modes: CCM and DCM, whose circuit configurations and equivalent models are interpreted in detail. Switched state space modeling is a basic and straightforward modeling technique for DC-DC converters. However, due to the applicable limitations of its switching feature, more efficient state space averaged modeling has been developed. The different models of CCM and DCM are presented in this chapter as the foundation for our proposed modeling methodology.

II.A. Pulse Width Modulation (PWM)

DC-DC converters change output voltage level by adjusting the conduction time of power switches. In other words, the pulse length of the controlling the gate of the power switch determines the input-output voltage relationship. In PWM, a rectangular pulse signal is generated for the gate. PWM mechanism is widely used in voltage regulation, motor control and information technology.

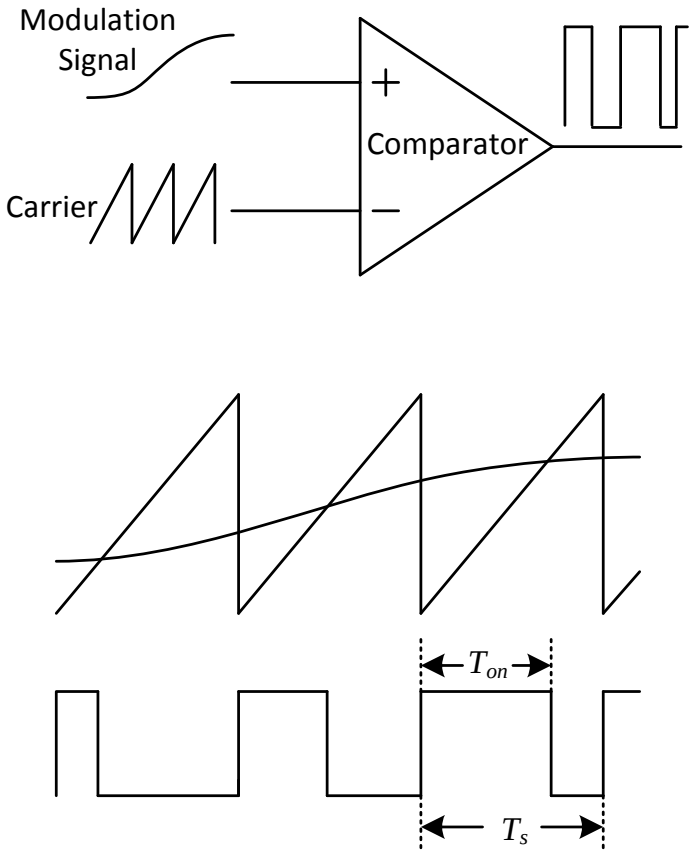


Fig. 1. Mechanism of PWM

Simplest way to generate a PWM signal is the intersective method, which requires only a saw tooth or a triangle waveform (easily generated using a simple oscillator) at certain frequency f_s and a comparator [13]. When the value of the modulation signal waveform is more than the carrier waveform, the PWM signal is in the high state, otherwise it is in the low state, as shown in Fig. 1.

The pulse width is modulated resulting in the variation of the average value of output voltage. The term duty ratio is the percentage of one period in which a signal is in high state, given by

$$d = \frac{T_{on}}{T_s}, \tag{2.1}$$

where d is the duty ratio, T_{on} is the time pulse stays high and T_s is the total period of the pulse. In this manner, PWM can be used to control the amount of power delivered to the load without incurring the losses that would result from linear power delivery by resistive transmission. Modern semiconductor switches such as MOSFETs and IGBTs are well suited components for high-efficiency PWM DC-DC power conversion.

In [13], duty ratio d has a discrete spectrum in the frequency domain due to its periodicity. Based on Fourier expansion, the resulting spectrum contains a dc component and an infinite order of harmonics at nf_s, where n represents the n^{th} order, f_s is the switching frequency. The spectrum is shown in Fig. 2. The infinite bandwidth is caused by the nonlinear operation of the pulse-width comparator. The concepts of Fourier series and multi-harmonics are the key feature in our proposed model. More details will be given in Chapter IV.

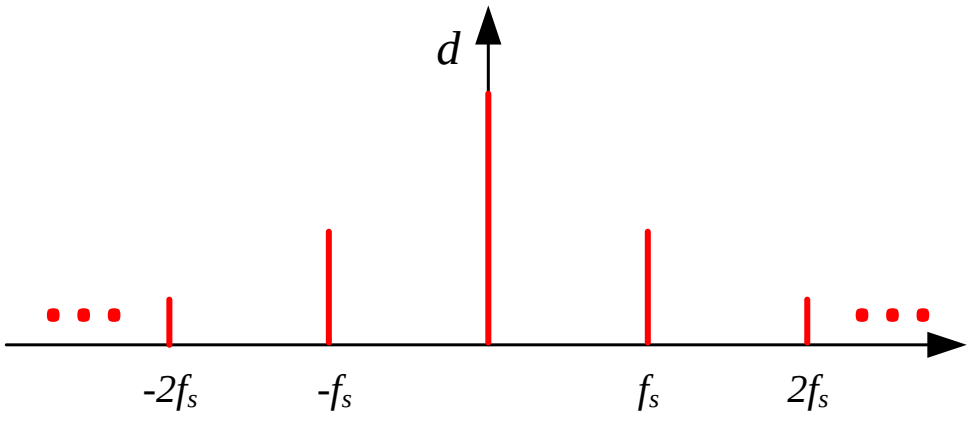
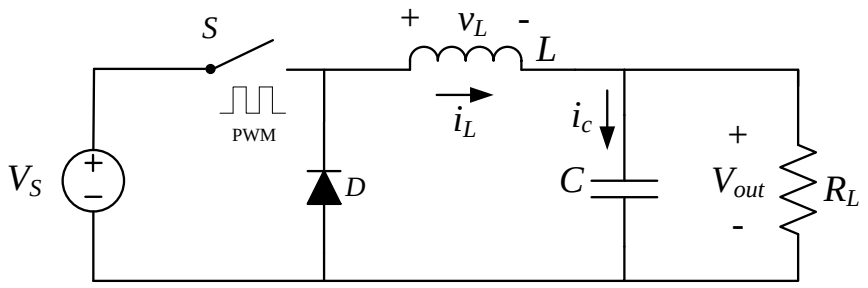


Fig. 2. Spectra of duty ratio d

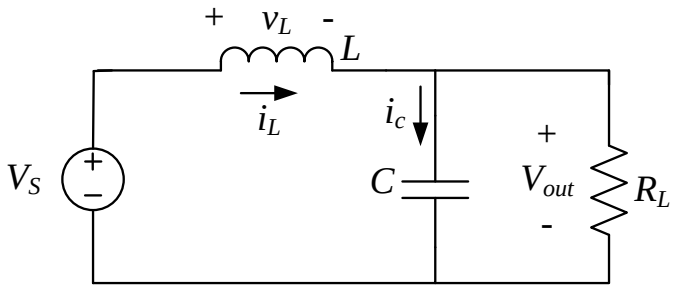
II.B. Buck Converter Operating in Continuous Conduction Mode

Buck converters are widely-used as step-down DC-DC converters. To gain a dc output voltage, a PWM switch cell and an LC low-pass filter are connected between the input voltage source and the load. The fundamental configuration of a buck converter is shown in Fig. 3 (a). The diode is reverse-biased when the switch is closed but conducts and provides a path for the inductor current when the switch is open. All the components are idealized in Fig. 3 for easy analysis, while the non-ideal characterization of devices will be discussed in Chapter III.

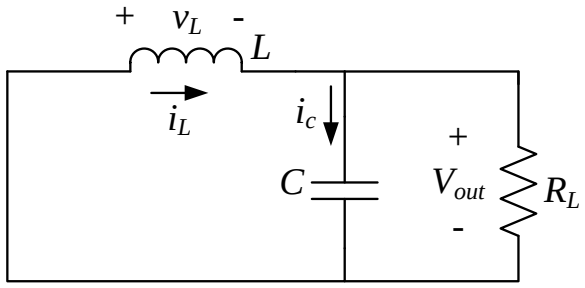
A good way for presenting the operation of a buck converter is to analyze the relationship of inductor current and voltage throughout one switching period. When the switch is closed, the inductor begins to charge, as shown in Fig. 4 (b). The inductor current increases linearly and therefore produces an induced voltage across it. When the switch is open, the inductor current starts to decrease with the voltage across it reversed. The energy stored in the inductor is transferred to the capacitor and loads through the diode conduction loop, as shown in Fig. 4 (c) and (d). A buck converter is operating in the continuous conduction mode (CCM) if the inductor current always remains positive and never drops to zero. On the other side, discontinuous conduction mode (DCM) happens if the inductor gets fully discharged in part of the switching period and the inductor current falls to zero. For compliance with DCM, duty ratio of the transistor switch is denoted as d_1 in the following chapters.



(a)



(b)



(c)

Fig. 3. Basics of buck converter: (a) fundamental configuration, (b) equivalent circuit when the switch is closed, (c) equivalent circuit when the switch is open

II.B.1. Analysis of the Inductor in CCM

The examination of PWM DC-DC converters operating in CCM starts with the following assumptions:

- The converter is operating in steady state.
- The inductor current is periodic and continuous (never drops to zero).
- According to PWM, the switch is closed for time $d_1 T_s$ and open for time $(1 - d_1)T_s$.
- The components are ideal (no parasitics are considered here).

Based on the above assumptions, the following results are obtained naturally: the inductor current is periodic and the average inductor voltage is zero,

$$i_L(t + T_s) = i_L(t) \tag{2.2}$$

$$V_L = \frac{1}{T}\int_t^{t+T_s} v_L(\tau)d\tau = 0, \tag{2.3}$$

where i_L is the inductor current, T_s is the switching period, v_L is the inductor voltage and V_L is the average value of the inductor voltage.

When the switch is closed (the PWM signal stays high), the diode is reversely biased and the equivalent circuit of a buck converter is shown in Fig. 3 (b). The voltage across the inductor is

$$v_L = V_S - V_O = L\frac{di_L}{dt}, \tag{2.4}$$

where V_S is the input voltage, V_O is the output voltage.

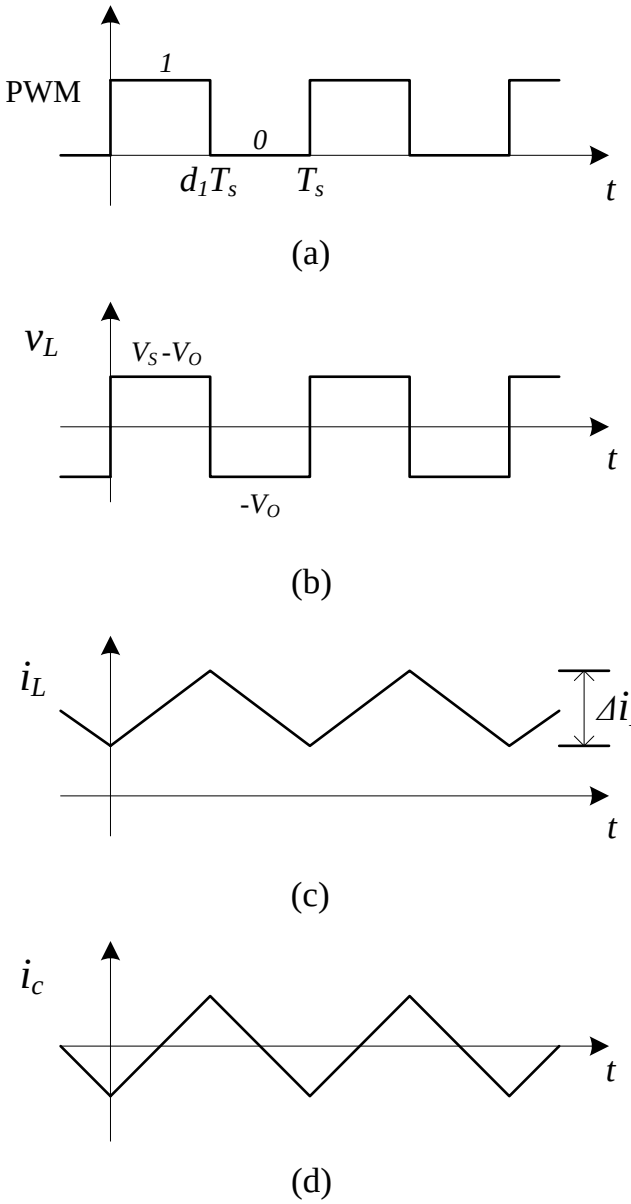


Fig. 4. Buck converter CCM waveforms

Under the assumption that the output voltage has small ripples, the inductor current and capacitor current increase linearly, as shown in Fig. 4 (c) and (d). The change of the inductor during this interval can be given by

$$\frac{di_L}{dt} = \frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{d_1 T_s} = \frac{V_S - V_O}{L} \tag{2.5}$$

$$(\Delta i_L)_{closed} = \left(\frac{V_S - V_O}{L}\right) d_1 T_s. \tag{2.6}$$

When the switch is open, the diode is in the conduction mode and provides a path for the inductor current to get discharged. The equivalent circuit is shown in Fig. 3 (c). In this situation, the voltage across the inductor is calculated as

$$v_L = -V_O = L\frac{di_L}{dt}. \tag{2.7}$$

The inductor current will decrease linearly due to the negative derivative, as shown in Fig. 4 (c). The change of the inductor during this interval can be given by

$$\frac{\Delta i_L}{\Delta t} = \frac{\Delta i_L}{(1 - d_1)T_s} = -\frac{V_O}{L} \tag{2.8}$$

$$(\Delta i_L)_{open} = -\left(\frac{V_O}{L}\right)(1 - d_1)T_s. \tag{2.9}$$

As shown in (2.2), the value of inductor current at the end of one cycle should be equal to that at the beginning. Thus the current change of the entire switching cycle including switch closed and switch open intervals is zero:

$$\left(\frac{V_S - V_O}{L}\right) d_1 T_s - \left(\frac{V_O}{L}\right)(1 - d_1)T_s = 0. \tag{2.10}$$

We can obtain the output input voltage relationship by solving the above equation:

$$V_O = d_1 V_S. \tag{2.11}$$

From the above formula, the output of the buck converter is only determined by the input voltage and duty ratio. If the input has disturbances, a feedback control adjusting the PWM duty ratio is always added to stabilize the output.

II.B.2. Analysis for the Output Ripple

In the above analysis, we assume that the output ripple is small enough to be negligible. However, for practical DC-DC converters, it is impossible that the capacitor keeps the output voltage stay constant even with a very large capacitance. Most DC-DC converters can experience significant large-signal output ripples in light load or DCM operation. Previously, the inductor current and voltage play the key role in analyzing the average value of the output voltage. To examine the variations or ripple of output voltage, another important component, capacitor must be considered.

Due to the specific topology of buck converter, the inductor current is divided into capacitor current and load current throughout the entire switching cycle. Thus the capacitor current is given by

$$i_C = i_L - i_{R.} \tag{2.12}$$

The capacitor experiences charge and discharge alternatively in every cycle. When the capacitor current is above zero, the capacitor is being charged. From the definition of capacitance $C = \frac{Q}{V}$, we have

$$\Delta V_O = \frac{\Delta Q}{C}, \tag{2.13}$$

where ΔQ is the change in charge. As shown in Fig. 5, ΔQ also equals to the area of the triangular capacitor current i_c above the axis

$$\Delta Q = \frac{1}{2}\left(\frac{T_s}{2}\right)\left(\frac{\Delta i_L}{2}\right) = \frac{T_s \Delta i_L}{8}. \tag{2.14}$$

Combining (2.13) and (2.14) results in

$$\Delta V_O = \frac{T_s \Delta i_L}{8C}. \tag{2.15}$$

Substituting Δi_L from (2.9) into (2.15), we can write

$$\Delta V_O = \frac{T_s V_O}{8CL}(1 - d_1)T = \frac{V_O(1 - d_1)}{8LC{f_s}^2}. \tag{2.16}$$

From the above formula, the output ripple is related to the switching frequency, duty ratio, inductance and capacitance. In modern DC-DC converters, designers usually use a high switching frequency to reduce or eliminate the output variations. However, under some circumstances, DC-DC converters are designed to operate in DCM or with a low frequency to drive light loads and improve efficiency. In this situation, large output ripples may occur. The analysis and modeling of such ripples is of significant value to designers.

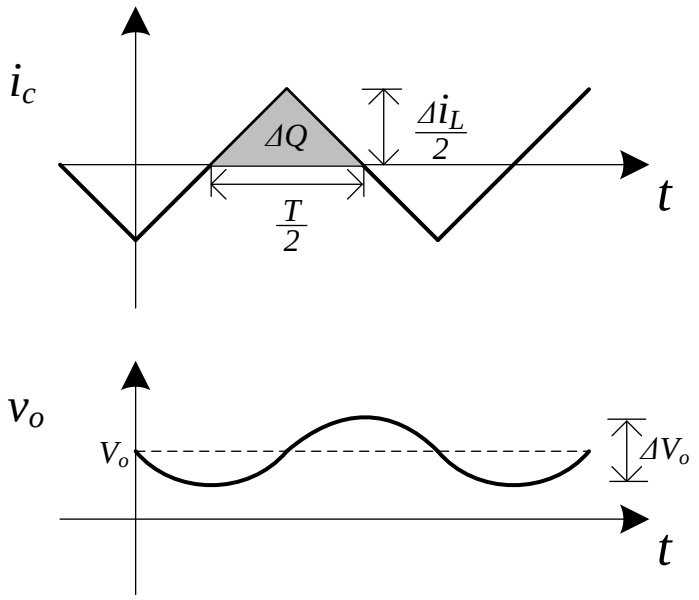


Fig. 5. Buck converter capacitor waveforms

II.C. Buck Converter Operating in Discontinuous Conduction Mode

Previous discussion on DC-DC converters is focused on continuous conduction mode; however, it is possible for the converter to enter DCM. DCM usually happens when the load is light and the switches are unidirectional. A different analysis is required for the DCM operation.

The most significant difference between CCM and DCM is that the inductor gets completely discharged at the end of each cycle. In DCM, the inductor current falls to zero at some point when the switch is open, as shown in Fig. 6. From here on, we define d_1 and d_2 as the duty ratio of the two intervals d_1T and d_2T, respectively.

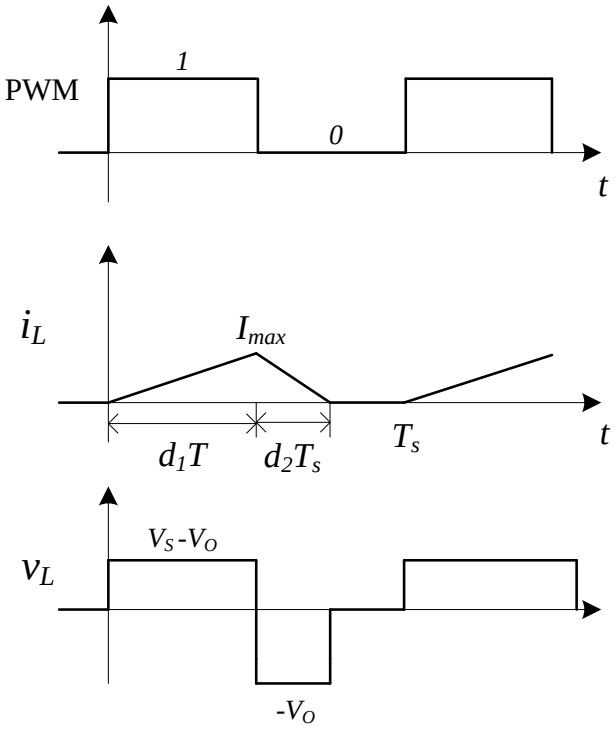


Fig. 6. Inductor waveforms in DCM

The assumption that the buck converter operates in the steady state still exists. The relationship between the output and input voltages is also determined by the fact that the average voltage across the inductor is zero throughout one switching period. From the inductor voltage waveforms shown in Fig. 6, we have

$$(V_S - V_O)d_1T_s - V_O d_2 T_s = 0 \tag{2.17}$$

$$\frac{V_O}{V_S} = \frac{d_1}{d_1 + d_2}. \tag{2.18}$$

From the above formula, d_2 becomes the key to solve the output voltage. To calculate d_2, we start with the analysis of the average value of the inductor current. Based on the characteristics of the capacitor, the average current flowing through the

capacitor within one cycle is zero. That means the average inductor current equals to the average load current:

$$I_L = I_R = \frac{V_O}{R}. \tag{2.19}$$

The average value of the inductor current can also be computed by the shape of its waveform:

$$I_L = \frac{1}{T}\left(\frac{1}{2} I_{max} d_1 T_s + \frac{1}{2} I_{max} d_2 T_s\right) = \frac{1}{2} I_{max}(d_1 + d_2). \tag{2.20}$$

Since the inductor current rises from zero at the beginning of one cycle, the maxim value I_{max} is the same as the change of current Δi_L, given by

$$I_{max} = \Delta i_L = \frac{V_O d_2 T_s}{L}. \tag{2.21}$$

Substituting I_{max} in (2.20), d_2 can be represented by

$$d_2 = \frac{-d_1 + \sqrt{d_1^2 + \frac{8L}{RT_s}}}{2}. \tag{2.22}$$

Substituting d_2 in (2.18), we have

$$V_O = V_S \left[\frac{2d_1}{d_1 + \sqrt{d_1^2 + \frac{8L}{RT_s}}}\right]. \tag{2.23}$$

Note that the output voltage $V_O$is not only related to duty ratio and V_S, but also the circuit parameters and switching frequency. That makes the analysis and design of DCM more

complicated. State space averaged model of DC-DC converters in DCM [6] serves as a basic approach for modeling and will be discussed later in this chapter.

II.D. Switched State Space Model of Buck Converters

Switched state space is the most fundamental and natural modeling technology of DC-DC converters, which is nonlinear, time-varying and time-continuous. Simulation of such models is probably straightforward and accurate, but hard switching activities lead to long runtimes in transistor-level transient (e.g. SPICE) simulations. On the other hand, fairly detailed behaviors and effects are captured in the state space model, which are sometimes unnecessary. This makes such models not always appropriate for designers to analyze and deal with. Averaging techniques have been proposed to address the above problems [2]. We present a switched model of buck converters as a general methodology which basically further leads to the state space averaged model.

To model the switching signal produced by the comparator inside the PWM cell, the concept of switching function $q(t)$ is used. When the switch is closed, $q(t) = 1$; when the switch is open,$q(t) = 0$.

$$q(t) = \begin{cases} 1, & switch\ is\ on \\ 0, & swich\ is\ off. \end{cases} \tag{2.24}$$

In other words, the switching function $q(t)$ represents the control signal to the gate of the transistor.

The inductor current $i_L(t)$ and capacitor voltage $v_C(t)$ are the natural state variables in a buck converter. The output voltage $v_o(t)$ is the voltage across the load resistor and happens to be the same as $v_C(t)$ if neglecting ESR, as shown in Fig. 3 (a). Based on the

branch constitutive relations (BCRs) of inductors and capacitors, when the switch is closed, we have the following state equations:

$$\begin{aligned} L\frac{di_L(t)}{dt} &= v_S(t) - v_C(t) \\ C\frac{dv_C(t)}{dt} &= i_L(t) - \frac{v_C(t)}{R}. \end{aligned} \tag{2.25}$$

When the switch is open, the equations change to

$$\begin{aligned} L\frac{di_L(t)}{dt} &= -v_C(t) \\ C\frac{dv_C(t)}{dt} &= i_L - \frac{v_C(t)}{R}. \end{aligned} \tag{2.26}$$

Combining the above equations with $q(t)$, we obtain the switched model description of a buck converter:

$$\begin{aligned} \frac{di_L(t)}{dt} &= \frac{1}{L}[q(t)v_S(t) - v_C(t)] \\ \frac{dv_C(t)}{dt} &= \frac{1}{C}\left[i_L(t) - \frac{v_C(t)}{R}\right] \\ v_o(t) &= v_C(t). \end{aligned} \tag{2.27}$$

Following the generated representation of state space $\dot{x} = \boldsymbol{A}x + \boldsymbol{b}u$, we have $x = [i_L(t) \quad v_C(t)]'$. The state equations are transformed into the following state space form

$$\begin{aligned} \frac{dx(t)}{dt} &= \boldsymbol{A}x + q(t)\boldsymbol{b}v_S(t) \\ v_o(t) &= \boldsymbol{c}x. \end{aligned} \tag{2.28}$$

The state matrices and input vectors of the buck converter are

$$\boldsymbol{A} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$$

$$\boldsymbol{b} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{2.29}$$

$$\boldsymbol{c} = [0 \quad 1].$$

The existence of switching function $q(t)$ distinguishes the above state space formula from the state space averaged model. Thus, we usually regard it as the switched or instantaneous model. This model is nonlinear with hard switching characteristics, and hence hard to be dealt with, which leads us to the development of averaged models.

II.E. State Space Averaged Model in CCM

As illustrated previously, state space averaged (SSA) modeling [2] is developed to overcome the difficulties in switched models. Assuming the detailed ripples of the output voltage and the inductor current are not of interest, the ripples are neglected by performing the local averaging within one switching cycle.

$$\bar{v}_o(t) = \frac{1}{T}\int_{t-T_s}^{t} v_o(\tau)d\tau \tag{2.30}$$

Our goal is to represent the state space combining the switching activities and state variables. To do this, the switching function $q(t)$ is modeled as the duty ratio d, which calculates the averaged value of $q(t)$ within one cycle.

$$d = \frac{1}{T}\int_{t-T_s}^{t} q(\tau)d\tau \tag{2.31}$$

Note that if $q(t)$ is periodic at the frequency f_s, the value of duty ratio d is fixed and also called steady state duty ratio. In the analysis of PWM DC-DC converter, the fixed switching frequency of the carrier waveform inside the comparator determines the periodic feature of $q(t)$.

By defining the local average of variables, the next step is to take the local average of the entire state equations of the switched state space in (2.27). The averaging of the derivative is the same as the derivative of the local averaged value, due to the linear time-invariant feature of averaged modeling. The local average of the product of functions and variables are kept in the initial averaged state equations. By performing the local average of the switched state equation of the buck converter, we have

$$\begin{aligned}
\frac{d\bar{\imath}_L(t)}{dt} &= \frac{1}{L}[\overline{q v_S}(t) - \bar{v}_C(t)] \\
\frac{d\bar{v}_C(t)}{dt} &= \frac{1}{C}\left[\bar{\imath}_L(t) - \frac{\bar{v}_C(t)}{R}\right] \\
\bar{v}_o(t) &= \bar{v}_C(t).
\end{aligned} \tag{2.32}$$

Since the product terms exit in the above model, the model is not an SSA model yet. For simplicity, we assume that the average of a product equal to the product of the averages.

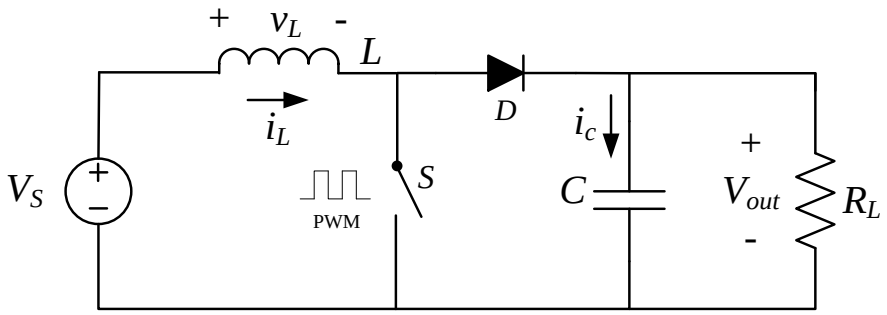


Fig. 7. Basic configuration of boost converter

Since the SSA model of the buck converter has only one product of q and v_s, we present the state space model of boost converter for better demonstration, as shown in Fig. 7. The state space equations are as followed:

$$\begin{aligned} \frac{d\bar{\imath}_L(t)}{dt} &= \frac{1}{L}[\overline{qv_C}(t) - \bar{v}_C(t) + \bar{v}_S(t)] \\ \frac{d\bar{v}_C(t)}{dt} &= \frac{1}{C}\left[\bar{\imath}_L(t) - \overline{q\imath_L}(t) - \frac{\bar{v}_C(t)}{R}\right] \\ \bar{v}_o(t) &= \bar{v}_C(t). \end{aligned} \tag{2.33}$$

To remove the average of the products, we assume

$$\begin{aligned} \overline{qv_C}(t) &\approx \bar{q}(t)\bar{v}_C(t) = d\bar{v}_C(t) \\ \overline{q\imath_L}(t) &\approx \bar{q}(t)\bar{\imath}_L(t) = d\bar{\imath}_L(t). \end{aligned} \tag{2.34}$$

Note that high frequency operation in CCM allows us to remove all the harmonic terms in the above formula, due to the small variation of capacitor voltage and inductor current in one cycle. Under these approximations, we can generate the SSA model of boost converter:

$$\frac{d\bar{\imath}_L(t)}{dt} = \frac{1}{L}[(d-1)\bar{v}_C(t) + \bar{v}_S(t)]$$
$$\frac{d\bar{v}_C(t)}{dt} = \frac{1}{C}\left[(1-d)\bar{\imath}_L(t) - \frac{\bar{v}_C(t)}{R}\right] \tag{2.35}$$
$$\bar{v}_o(t) = \bar{v}_C(t).$$

In terms of the matrix form, the SSA model can be written in the following notation:

$$\frac{d\bar{x}(t)}{dt} = [(1-d)\boldsymbol{A_0} + d\boldsymbol{A_1}]\bar{x} + \boldsymbol{b}\bar{v}_S(t)$$
$$\bar{v}_o(t) = \boldsymbol{c}\bar{x}. \tag{2.36}$$

Besides averaging the state equation, circuit averaging techniques are also an important physical modeling method. Unlike the mathematical modeling which is specified to one topology, circuit averaging has better generality [14]. The techniques require that the voltage or current sources are replaced by their local averages, the switches including transistors and diodes by controlled voltage or current sources. In the equivalent circuit of ideal boost converters, the transistor is modeled by a controlled voltage source $(1-d)\bar{v}_C(t)$ and diode by a controlled current source $(1-d)\bar{\imath}_L(t)$. The averaged equivalent circuit model of boost converter is shown in Fig. 8. Note that this is a large-signal non-linear time-invariant model and actually determined by (2.35), respecting the Kirchhoff's laws.

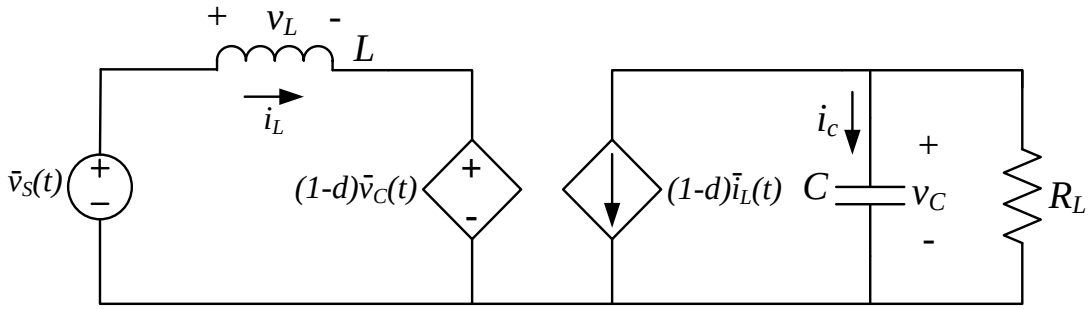


Fig. 8. State space averaged model of boost converter

Similarly, we go back to the SSA model of the buck converter given by

$$\frac{d\bar{\imath}_L(t)}{dt} = \frac{1}{L}[d\bar{v}_S(t) - \bar{v}_C(t)]$$

$$\frac{d\bar{v}_C(t)}{dt} = \frac{1}{C}\left[\bar{\imath}_L(t) - \frac{\bar{v}_C(t)}{R}\right] \tag{2.37}$$

$$\bar{v}_o(t) = \bar{v}_C(t).$$

Correspondingly, the equivalent circuit model of the buck converter is shown in Fig. 9.

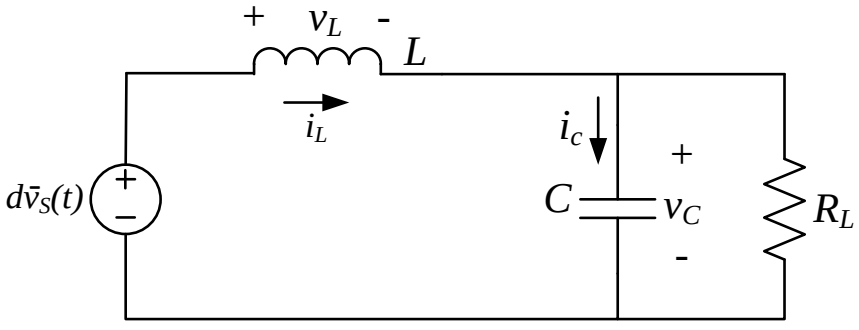


Fig. 9. State space averaged model of buck converter

In state equation (2.37), all the instantaneous variables are presented by the local average values. Identically, the SSA model can also be transformed into the state space matrix form, given by

$$\begin{aligned} \frac{d\bar{x}(t)}{dt} &= \boldsymbol{A}\bar{x} + d\boldsymbol{b}\bar{v}_S(t) \\ \bar{v}_o(t) &= \boldsymbol{c}\bar{x}. \end{aligned} \tag{2.38}$$

A natural application of the state space averaged model is to simulate the steady state response and operating point with the restriction of constant input voltage source and invariant duty ratio. In behavioral simulation, the switching function cell is replaced by a constant duty ratio, leading to more efficient simulation. Moreover, using the averaging techniques, designers no longer care about the dynamic behaviors within one cycle. Spice simulation can be performed with larger time steps when the switching transitions are not included in the model. Small-signal model can be obtained by performing the linearization based on the averaged model.

II.F. State Space Averaged Model in DCM

In the above paragraphs, we have discussed the basics about discontinuous conduction mode. The most obvious difference of DCM operation from CCM is that an extra time interval is added in the inductor current waveform. If we call the transistor the first switch and regard the diode as the second, then $q_1(t)$ and $q_2(t)$ are defined as the switching functions of the transistor and the diode, respectively. Correspondingly, d_1T and d_2T are the lengths of the first and second time intervals, respectively. The inductor current waveform in DCM is shown in Fig. 10.

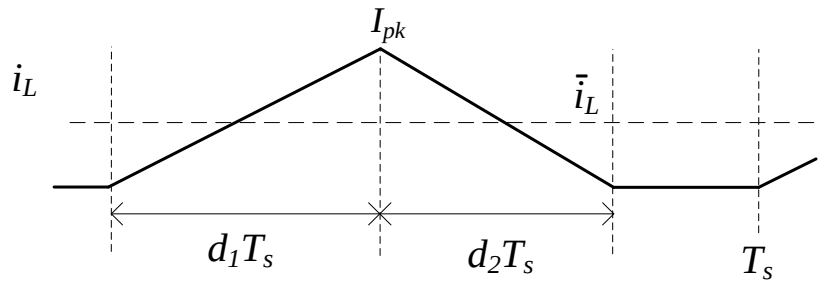


Fig. 10. DCM inductor current waveform

From the previous analysis on DCM operation, we can generate the switched state equations of buck converters easily:

$$\begin{aligned} \frac{di_L(t)}{dt} &= \frac{1}{L}[q_1(t)(v_S(t) - v_C(t)) - q_2(t)v_C(t)] \\ \frac{dv_C(t)}{dt} &= \frac{1}{C}\left[i_L(t) - \frac{v_C(t)}{R}\right] \\ v_o(t) &= v_C(t). \end{aligned} \tag{2.39}$$

The duty ratio of the second interval d_2 is determined by the state variables and control parameters. The average value of the inductor current can be calculated by the current area above zero:

$$\bar{\imath}_L(t) = \frac{\frac{1}{2}I_{peak}(d_1T_s + d_2T_s)}{T} = \frac{I_{peak}}{2}(d_1 + d_2). \tag{2.40}$$

In the first interval, we have

$$I_{peak} = \frac{di_L}{dt} \cdot d_1T_s = \frac{v_S(t) - v_C(t)}{L} \cdot d_1T_s. \tag{2.41}$$

Combining (2.40) and (2.41), the formula of d_2 is obtained:

$$d_2 = \frac{2L\bar{\imath}_L(t)}{(v_S(t) - v_C(t))d_1 T_s} - d_1. \tag{2.42}$$

Upon substitution of d_2 and averaging over one switching cycle, the switched model (2.39) becomes

$$\begin{aligned} \frac{d\bar{\imath}_L(t)}{dt} &= \frac{d_1 v_S(t)}{L} - \frac{2\bar{\imath}_L(t)\bar{v}_C(t)}{d_1 T\left(v_S(t) - \bar{v}_C(t)\right)} \\ \frac{d\bar{v}_C(t)}{dt} &= \frac{\bar{\imath}_L}{C} - \frac{\bar{v}_C(t)}{RC} \\ \bar{v}_o(t) &= \bar{v}_C(t). \end{aligned} \tag{2.43}$$

The DCM averaged model can be used to develop small-signal model and closed-loop control. However, the large ripple of DCM currents cannot be captured in this model. The solution for this is to involve harmonics to capture the dynamic ripples in the generalized model. In the following chapters, we will focus on the multi-harmonic generalized model.

CHAPTER III

NONIDEAL SWITCH MODEL

From the previous introduction of typical DC-DC converters, we notice that the inductor and the switch cell including both transistor and diode constitute the kernel part of a converter. A general modeling method specific on this unit draws our attention and has been fully developed. From this chapter and on, we present a generalized model of a three-terminal switch cell based on a standard buck converter shown in Fig. 11. A lot of work has been done on modeling of a buck converter. However, device nonlinearities such as forward voltage drop and leakage current, which were always ignored, actually contribute significantly to low power DC-DC converters. To accurately capture the real circuit behaviors, the device-level nonlinearities are considered and modeled properly in the switch cell in this proposed work. Some of existing work handles the modeling of CCM and DCM separately, which makes the model lack generality. To solve this problem, our proposed model can seamlessly transition between CCM and DCM by continuously monitoring the circuit variables. The generalized switch model can also be applied to other DC-DC converters with the three-terminal switch cell, e.g. buck-boost converters and boost converters with no additional changes.

III.A. Generalized Switch Model Based on Switching Functions

To propose a generalized switch model suitable for both CCM and DCM, we assume that CCM is a special situation in DCM, which will be discussed later in this chapter. Thus all the following analysis is based on the assumption that the buck converter shown

in Fig. 11 is operating in DCM with a discontinuous inductor current i_c shown in Fig. 12. Every switching cycle T_s is divided into three intervals by three binary switching functions $q_1(t)$, $q_2(t)$ and $q_3(t)$, defined in (2.24). As illustrated above, $q(t)$ switches between 1 and 0 when the gate signal stays high or low. When $q_1(t) = 1$, the transistor is conducting and the diode is reversely biased. Starting from zero, the inductor current i_c linearly increases. When $q_2(t) = 1$, the transistor goes off and the diode conducts; meanwhile, the inductor current starts to drop to zero. When $q_3(t) = 1$, the inductor is fully discharged and its current stays at zero. Fig. 13 (a) shows the extracted switch cell from Fig. 11, while Fig. 13 (b), (c) and (d) show the three equivalent sub circuits corresponding to the three operation intervals.

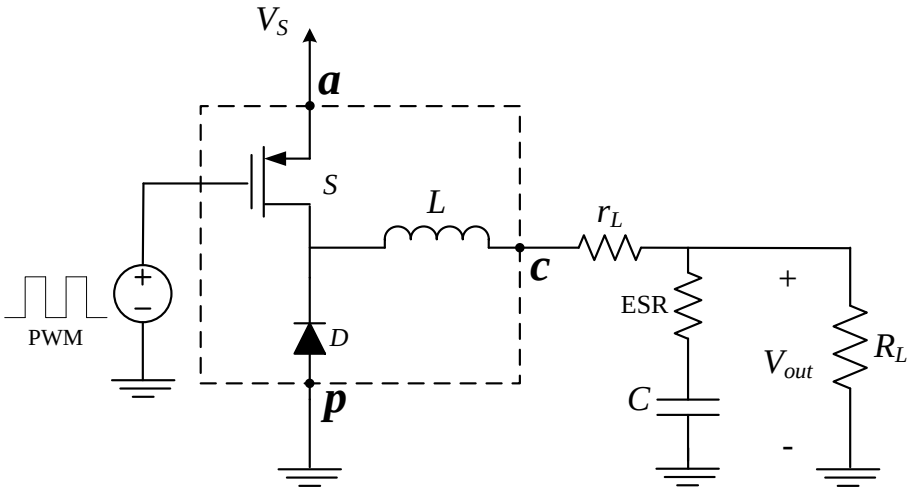


Fig. 11. Buck converter circuit

Previously in Chapter II, the inductor current and capacitor voltage are chosen as the natural state variables in state space modeling. Similarly, we choose one terminal

voltage and one branch current as the state variables, like v_{ag} and i_p in the switch model. The relationship of the terminal voltages and branch currents within the switch cell can construct a complete nonlinear DCM switch model. In the first interval, the MOS transistor operates in the triode region producing a nonlinear resistance of $R_{ds(on)}$. That results in a voltage drop of $V_{ds(on)}$. Meantime, the diode is reversely biased, no current going through. The corresponding equivalent circuit model is shown in Fig. 13 (b). Thus, in the first interval, we have $v_{ag} = V_{ds(on)}$ and $i_p = 0$.

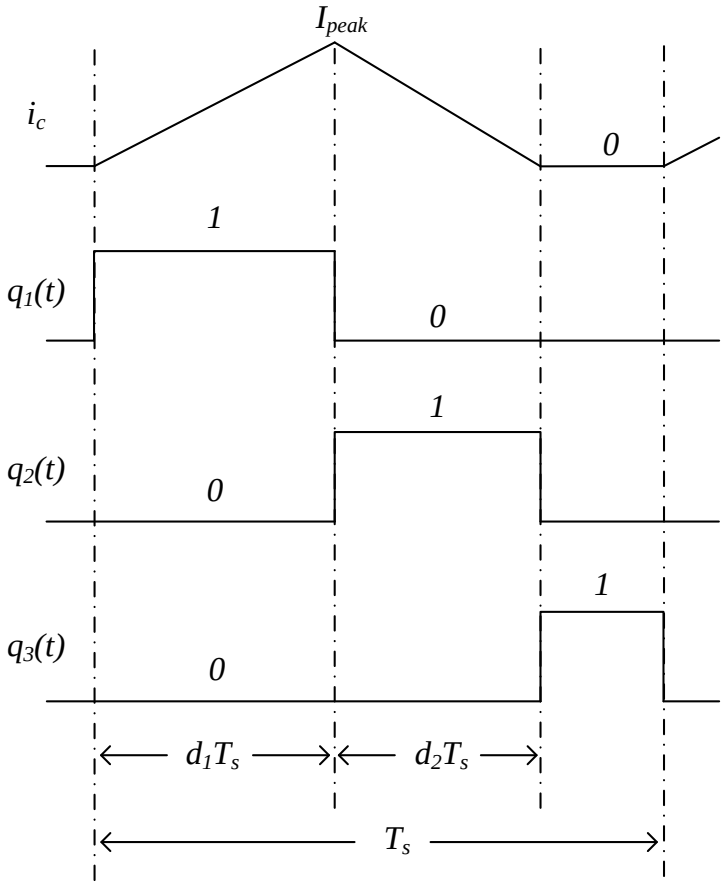


Fig. 12. The inductor current i_c in DCM and the three switching functions q_1, q_2 and q_3

In the second interval, the diode is forwardly biased and holds a forward voltage drop V_d. At the same time, the MOS transistor is operating in sub-threshold conduction, where a leakage current I_{leak} is present, which is an exponential function of V_{ds}. To consider the sub-threshold conduction of the MOS switch, we model the transistor using an equivalent resistor $R_{ds(off)}$ between nodes a and g. As shown in Fig. 13 (c), in the second interval we have $v_{ag} = v_{ap} + V_d$ and $i_p = i_c - I_{leak}$.

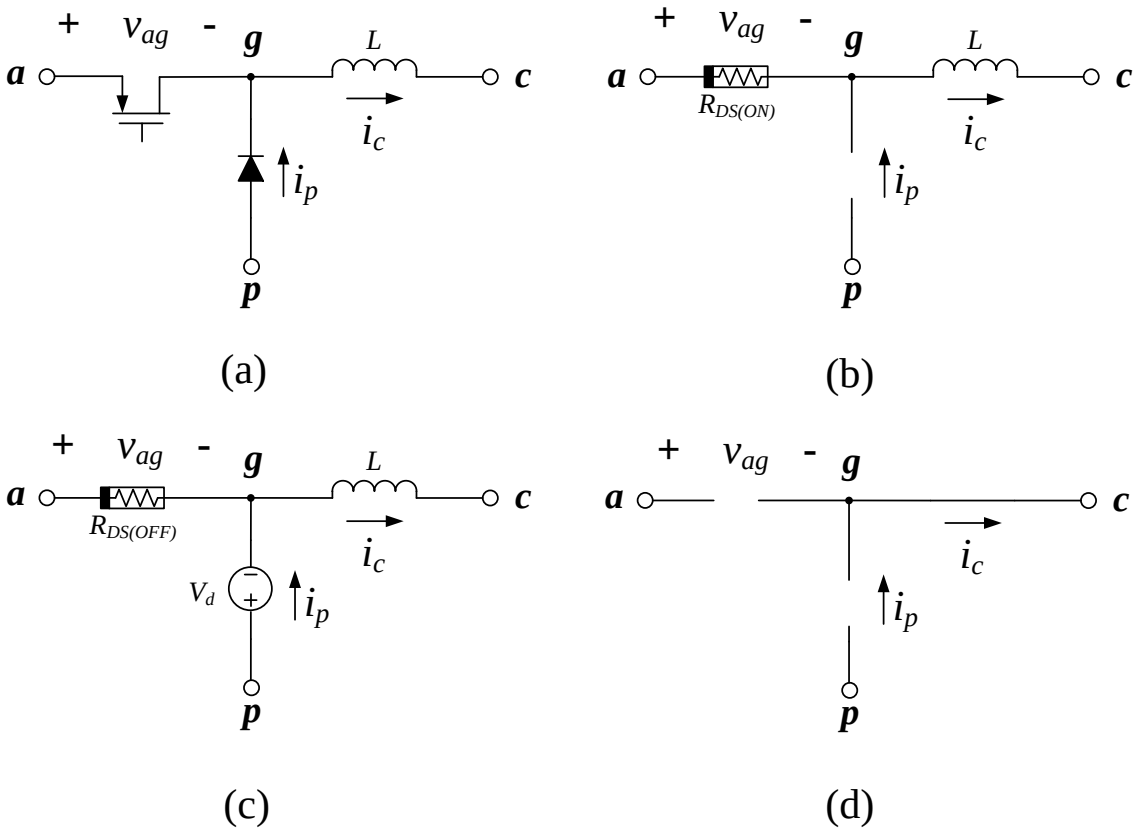


Fig. 13. (a) The three-terminal switch cell and its equivalent circuits in three operation intervals (b) (c) (d)

In the third interval, the inductor current remains at zero while both the transistor and the diode are open circuits. According to the constitutive equation of inductors $v_L(t) = L\frac{di_L(t)}{dt}$, the inductor is shortened such that $v_{gc} = 0$. In the third interval, we have $v_{ag} = v_{ac}$ and $i_p = 0$.

To present the expressions of v_{ag} and i_p, which are actually periodic piecewise functions, we use the product of piecewise expression and the corresponding switching function of that interval. Adding up the three products results in the general formulas:

$$v_{ag} = q_1(t)V_{ds(on)} + q_2(t)\big(v_{ap} + V_d\big) + q_3(t)v_{ac} \tag{3.1}$$

$$i_p = q_2(t)(i_c - I_{leak}). \tag{3.2}$$

In the above equations, $q_1(t)$ is an external input, while $q_2(t)$ and $q_3(t)$ are restricted by constraint equations which will be shown soon. We can easily find that the circuit variables v_{ag} and $i_p$are dependent on other terminal voltages and branch currents throughout the entire switching cycle. A natural approach is to replace the transistor and the diode in the original circuit by voltage controlled voltage sources (VCVS) obeying the regulation in (3.1), and by current controlled current sources (CCCS) using the relation in (3.2). This leads to the circuit model shown in Fig. 14, which is essentially the equivalent switch model accounting for the characteristics of nonlinear devices. Substituting the switch cell shown in Fig. 11 by the above model will result in a switched model that accurately captures the dynamic behaviors of the converter.

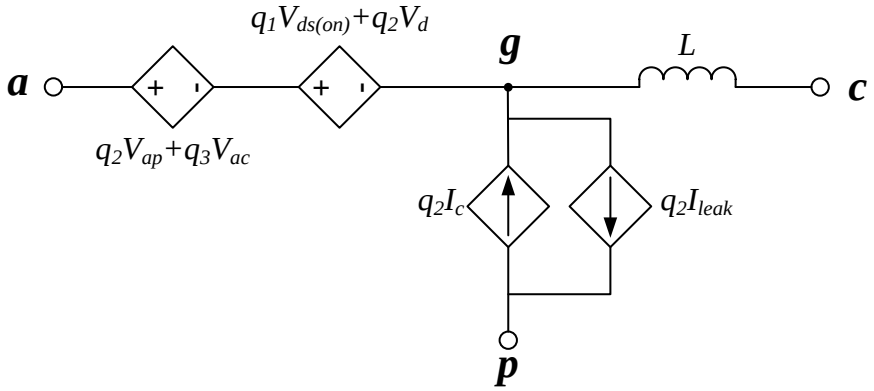


Fig. 14. The equivalent model of the switch cell with nonlinear device characteristics

The above switch model can easily be applied to a converter operating in CCM with one additional constraint $d_1 + d_2 = 1$. The process of determining the operation mode is automated by calculating d_2 concurrently as the model is being simulated using

$$d_2 = \frac{2L}{T_s}\frac{\bar{\imath}_c}{d_1\bar{v}_{ac}}, \tag{3.3}$$

where $\bar{\imath}_c$ is the inductor current and $\bar{v}_{ac}$ is the average voltage across node a and c, both of which are immediately available in the multi-harmonic model later in the following chapter. If $d_1 + d_2 < 1$ exists, the converter operates in DCM. Otherwise, CCM occurs with $d_2 = 1 - d_1$ [5].

III.B. Nonideal Device Modeling

In Fig. 14, the accuracy of the model depends on the evaluation of newly introduced variables $V_{ds(on)}$, V_d and I_{leak}, which are nonlinear functions of the circuit state and vary dynamically during the circuit simulation. These three values can be evaluated without

simulating the actual buck converter in Fig. 11, but by exploiting the information immediately available in the equivalent model in Fig. 14. The process is demonstrated through the example of computing the leak current I_{leak} as shown in Fig. 15. A buck converter operating in the second interval is shown in Fig. 15 (a), where the transistor Q_1 is turned off. Due to sub-threshold conduction, a leakage current I_{leak1} is flowing from the drain to source.

In the equivalent model, the evaluation of leakage current I_{leak2} is achieved by adding an additional sub circuit in Fig. 15 (b), which is constructed such that the transistor Q_2 has the same bias (i.e. gate-to-source voltage and drain-to-source voltage) as the transistor Q_1. To do this, we observe that in the second interval the drain-to-source voltage of Q_1 corresponds to v_{ag} of the equivalent model and the gate-to-source voltage of Q_1 is zero. We force the drain-to-source voltage of $Q_2$to be v_{ag} by adding a VCVS with the value of v_{ag}. Likely, the gate of Q_2 is connected to ground. Thus, we make sure that leakage current produced by Q_2 in the sub circuit is the same as that of Q_1 in the buck converter. Putting a CCCS with the same value of the leakage current of Q_2 back to the equivalent model allows the model to account for this type of nonideality. A similar procedure can be used to obtain $V_{ds(on)}$ and V_d. With three additional sub circuits and controlled sources running along, the complete equivalent model can automatically take into account all nonideal device characteristics.

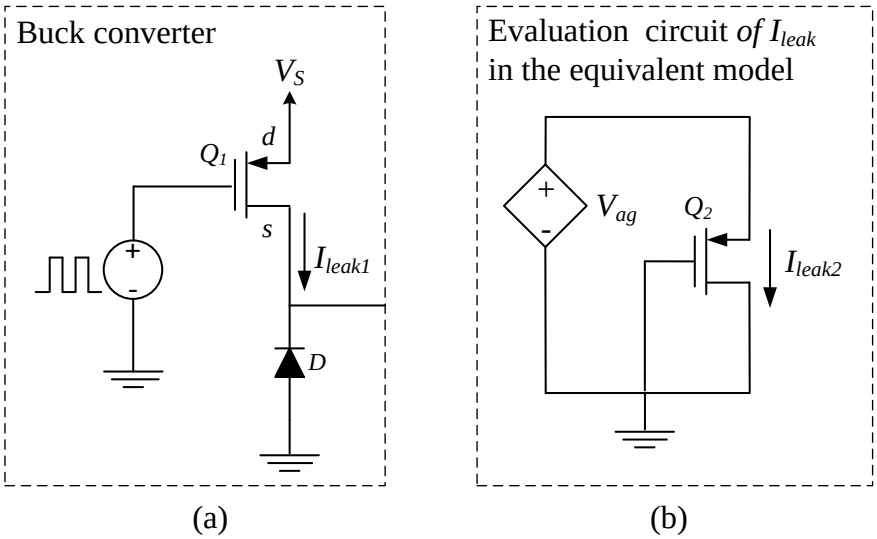


Fig. 15. The evaluation of leakage current: (a) real transistor in buck converter (b) equivalent sub circuit of evaluating leakage current

The key benefits of the proposed DC-DC converter model structure shown in Fig. 15 (b) are as follows. First, the use of the equivalent switch model, which will be further detailed in the following sections, allows us to efficiently characterize the switching activities of the converter and speed up the simulation dramatically. At the same time, by including simple additional transistor circuits as shown in Fig. 15 (b), we are able to construct a complete DC-DC converter model in which essential device non-idealities from the MOS switch and the diode can be accurately evaluated as part of the overall converter model. These two characteristics lead to the efficiency and accuracy of the proposed converter model.

CHAPTER IV

MULTI-HARMONIC MODEL

Fig. 14 presents a switched model considering all nonlinear device characteristics; however, it is essentially a switching circuit due to the presence of switching functions and is computationally expensive for performing transient simulations. As illustrated in Chapter II, the switched model is awkward to deal with in practice and usually developed using averaging techniques. In this chapter, we propose a multi-harmonic averaged model that is even more accurate and efficient. The proposed model approximates the actual transient response of a DC-DC converter using a Fourier series of arbitrary order of choice. Since the switching functions are decomposed into several Fourier series and are no longer present in the model, the proposed model is highly efficient.

IV.A. Multi-harmonic Model of Switch Cell

Multi-harmonic model decomposes each state variable into an averaged value and multiple harmonics. Recall that any time-domain periodic signal $x(\tau)$ can be expanded using the Fourier series as

$$x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega_s \tau}, \tag{4.1}$$

where $\omega_s = 2\pi f_s$ and f_s is the switching frequency. $\langle x \rangle_k(t)$ is the k^{th} complex Fourier coefficient [7], which is given by

$$\langle x\rangle_k(t) = \frac{1}{T_s}\int_{t-T_s}^{t} x(\tau)e^{-jk\omega_s\tau}d\tau. \tag{4.2}$$

As shown in (4.2), $\langle x\rangle_k(t)$ is defined by taking the average of $x(\tau)$ at the frequency kf_s. For instance, $\langle x\rangle_0(t)$ represents the dc component and $\langle x\rangle_1(t)$ represents the harmonic component at the fundamental frequency. Thus, we denote $\langle x\rangle_k(t)$ as the index-k average.

From (4.1) and (4.2), three properties can be immediately identified that allow us to calculate the index-k averages of the switch model. The first property is the average of differentiation based upon the following equation

$$\langle\frac{dx}{dt}\rangle_k(t) = \frac{d\langle x\rangle_k(t)}{dt} + jk\omega_s\langle x\rangle_k(t). \tag{4.3}$$

This can be easily verified by differentiating both sides of (4.2) with respect to time. Applying (4.3) to the constitutive equation of inductors $v_L = L\frac{di_L}{dt}$ leads to the index-k average

$$\langle L\frac{di_L}{dt}\rangle_k = L\frac{d\langle i_L\rangle_k}{dt} + jk\omega_s L\langle i_L\rangle_k. \tag{4.4}$$

The first term on the right hand side of (4.4) is the voltage drop of the inductor with a current of $\langle i_L\rangle_k$. The second term on the right hand side represents additional impedance. A close examination of (4.4) reveals that an index-k average of an inductor can be modeled by an inductor model with the same inductance in series with an impedance of $jk\omega_s L$.

The second property is the linearity property given by

$$\langle ax + by\rangle_k = a\langle x\rangle_k + b\langle y\rangle_k, \tag{4.5}$$

where a and b are constant and $x$and y are functions of time. Since $V_{ds(on)}$, $V_d$and I_{leak} do not vary significantly over time in each operational interval, they can be treated as fixed values. Hence, the index-k averages of (3.1) and (3.2) can be rewritten as

$$\langle v_{ag}\rangle_k = \langle q_1\rangle_k V_{ds(on)} + \langle q_2 v_{ap}\rangle_k + \langle q_2\rangle_k V_d + \langle q_3 v_{ac}\rangle_k \tag{4.6}$$

$$\langle i_p\rangle_k = \langle q_2 i_c\rangle_k + \langle q_2\rangle_k I_{leak.} \tag{4.7}$$

The last property that we exploit is the one that is based upon discrete convolution. Using this property, each product term in (4.6) and in (4.7) can be written as

$$\langle qx\rangle_k = \sum_{i=-\infty}^{\infty} \langle q\rangle_{k-i}\langle x\rangle_i. \tag{4.8}$$

Since every complex Fourier coefficient includes a real and an imaginary part, $\langle q\rangle_k$ and $\langle x\rangle_k$ can be rewritten as

$$\langle x\rangle_k = \langle x\rangle_k^R + j\langle x\rangle_k^I \tag{4.9}$$

$$\langle q\rangle_k = \langle q\rangle_k^R + j\langle q\rangle_k^I, \tag{4.10}$$

where R represents the real part and I the imaginary part. Substituting (4.9) and (4.10) into (4.8) gives

$$\langle qx\rangle_k = \sum_{i=-\infty}^{\infty} [\langle q\rangle_{k-i}^R\langle x\rangle_i^R - \langle q\rangle_{k-i}^I\langle x\rangle_i^I] + j\sum_{i=-\infty}^{\infty} [\langle q\rangle_{k-i}^R\langle x\rangle_i^I + \langle q\rangle_{k-i}^I\langle x\rangle_i^R]. \tag{4.11}$$

According to (4.2), we also know that $\langle x\rangle_k$ and $\langle x\rangle_{-k}$ are conjugates of each other, which means $\langle x\rangle_k^R = \langle x\rangle_{-k}^R$ and$\langle x\rangle_k^I = -\langle x\rangle_{-k}^I$. Now we have a general equation (4.11)

for calculating the index-k averages of a product. We simplify the calculation by considering only the index-0 and index-1 averages and neglecting all higher order terms [11]. Exploiting the conjugation property provides the following expression for the index-0 average of a product

$$\langle qx\rangle_0 = \langle q\rangle_0\langle x\rangle_0 + 2(\langle q\rangle_1^R\langle x\rangle_1^R + \langle q\rangle_1^I\langle x\rangle_1^I). \tag{4.12}$$

Substituting (4.12) into (4.6) and (4.7) gives the index-0 average model of the switch cell.

$$\begin{aligned}\langle v_{ag}\rangle_0 = {} & \langle q_1\rangle_0 V_{ds(on)} + \langle q_2\rangle_0 V_d + \langle q_2\rangle_0\langle v_{ap}\rangle_0 \\ & + 2\big(\langle q_2\rangle_1^R\langle v_{ap}\rangle_1^R + \langle q_2\rangle_1^I\langle v_{ap}\rangle_1^I\big) + \langle q_3\rangle_0\langle v_{ac}\rangle_0 \\ & + 2(\langle q_3\rangle_1^R\langle v_{ac}\rangle_1^R + \langle q_3\rangle_1^I\langle v_{ac}\rangle_1^I) \\ \langle i_p\rangle_0 = {} & \langle q_2\rangle_0 I_{leak} + \langle q_2\rangle_0\langle i_c\rangle_0 + 2(\langle q_2\rangle_1^R\langle i_c\rangle_1^R + \langle q_2\rangle_1^I\langle i_c\rangle_1^I)\end{aligned} \tag{4.13}$$

Similarly, the index-1 average of a product is given by

$$\langle qx\rangle_1^R = \langle q\rangle_0\langle x\rangle_1^R + \langle q\rangle_1^R\langle x\rangle_0 \tag{4.14}$$

$$\langle qx\rangle_1^I = \langle q\rangle_0\langle x\rangle_1^I + \langle q\rangle_1^I\langle x\rangle_0. \tag{4.15}$$

Substituting (4.14) and (4.15) into (4.6) and (4.7) gives the real part of the index-1 average model of the switch cell as

$$\begin{aligned}\langle v_{ag}\rangle_1^R = {} & \langle q_1\rangle_1^R V_{ds(on)} + \langle q_2\rangle_0\langle v_{ap}\rangle_1^R + \langle q_2\rangle_1^R\langle v_{ap}\rangle_0 \\ & + \langle q_2\rangle_1^R V_d + \langle q_3\rangle_0\langle v_{ac}\rangle_1^R + \langle q_3\rangle_1^R\langle v_{ac}\rangle_0 \\ \langle i_p\rangle_1^R = {} & \langle q_2\rangle_0 I_{leak} + \langle q_2\rangle_0\langle i_c\rangle_1^R + \langle q_2\rangle_1^R\langle i_c\rangle_0\end{aligned} \tag{4.16}$$

and the imaginary part of the index-1 average model as

$$\langle v_{ag}\rangle_1^I = \langle q_1\rangle_1^I V_{ds(on)} + \langle q_2\rangle_0\langle v_{ap}\rangle_1^I + \langle q_2\rangle_1^I\langle v_{ap}\rangle_0 + \langle q_3\rangle_1^I\langle v_{ac}\rangle_0 + \langle q_2\rangle_1^I V_d + \langle q_3\rangle_0\langle v_{ac}\rangle_1^I \tag{4.17}$$

$$\langle i_p\rangle_1^I = \langle q_2\rangle_0 I_{leak} + \langle q_2\rangle_0\langle i_c\rangle_1^I + \langle q_2\rangle_1^I\langle i_c\rangle_0$$

Combining (4.4), (4.11), (4.12), (4.14) and (4.15) produces the final circuit model of the switch including index-0 and index-1 averages, as shown in Fig. 16. The same derivation process can be taken to derive multi-harmonic models of an arbitrary order. To our sense, the model might be more accurate when including more indexes of high orders. However, in the tests, the utilization of more indexes of equivalent circuits significantly slows down the simulation but hardly improves the accuracy. The tradeoff between speedup and accuracy encourages us to include index-1 only. It should also be noted that a multi-harmonic model is generally highly coupled due to the interactions between averages of different orders.

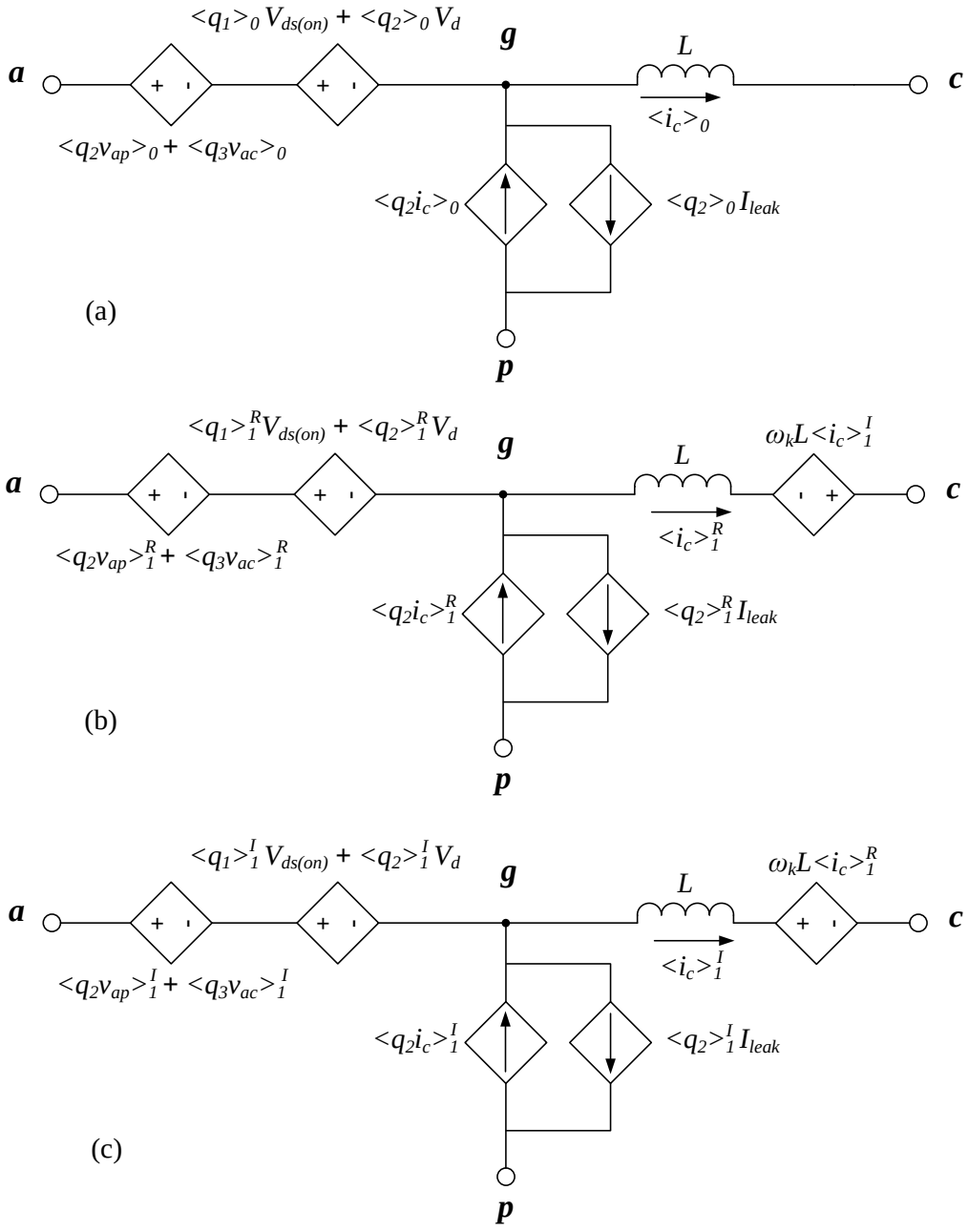


Fig. 16. The multi-harmonic model of the three-terminal the switch cell including (a) index-0 average model, (b) the real part of index-1 average model and (c) the imaginary part of index-1 average model

IV.B. Multi-harmonic Model of DC-DC Converters

Apart from the switch cell, we need to derive the index-k model for all other components of the DC-DC converter such as the capacitor and resistors. By the definition of index-k average shown in (4.2), it is easy to verify that $\langle v_R \rangle_k = R\langle i_R \rangle_k$, which in turn implies the index-k average of a resistor has the same branch constitutive relationship as the actual resistor. Like the index-k average of an inductor, the index-k average of a capacitor can be derived by differentiating both sides of (4.2) with respect to time:

$$\langle C\frac{dv_C}{dt}\rangle_k = C\frac{d\langle v_C \rangle_k}{dt} + jk\omega_s C\langle v_C \rangle_k. \tag{4.18}$$

This suggests that in terms of the index-k averages, a physical capacitor can be modeled as an average capacitor model with the same capacitance in parallel with an admittance of $jk\omega_s C$.

Using the multi-harmonic average models for the switch cell in addition to the capacitors and the resistors derived above, we construct an index-0 and index-1 average model of the entire DC-DC converter. This contributes to three coupled circuits, which can be solved for dc and the first-order harmonic responses. Again, besides the tradeoff of speed and accuracy, the same approach can be taken to derive DC-DC converter multi-harmonic models of higher orders.

CHAPTER V

SYSTEM-DECOUPLED MODEL

As illustrated in the previous chapter, solving mutually dependent averages of different orders is a computationally intensive task. In our proposed method, the dc component has the highest priority but pretty coupled by index-1 variables. To decouple the dependent controlled sources, in this chapter, we provide two rules that can remove the dependency of index-1 average models on all higher order models without sacrificing the model accuracy.

Consider the standard buck converter shown in Fig. 11 and its index-0 average model shown in Fig. 17. Our objective is to remove the dependent components from the index-1 average model within VCVS $vs1$ and the CCCS $cs2$. Recall that the index-0 average of a product can be evaluated from the discrete convolution relation of (4.8), given by

$$\langle qx\rangle_0 = \sum_{i=-\infty}^{\infty} \langle q\rangle_{-i}\langle x\rangle_i. \tag{5.1}$$

One natural observation is that if x has a very small variance within one cycle and hence can be viewed as a DC constant, then for any $k \neq 0$, $\langle x\rangle_k = 0$ exits. Thus, we suggest the first rule of system decoupling:

RULE 1. *If x has small variance within one cycle, then $\langle qx\rangle_0 = \langle q\rangle_0 x$ exits. All higher order terms can be removed from the index-0 average calculation.*

In Fig. 16 (a), there are three averages of product terms $\langle q_2 v_{ap} \rangle_0$, $\langle q_3 v_{ac} \rangle_0$ and $\langle q_2 i_c \rangle_0$. In the buck converter, we have $v_{ap} = V_s$ and $v_{ac} = V_s - V_{out}$, where V_s denotes the input voltage supply and V_{out} dc component of the output voltage. Thus the voltage swing in v_{ap} or v_{ac} is small and can be neglected. Similar conclusions can be made for boost and buck-boost converters. Therefore, we can apply rule 1 to $\langle q_2 v_{ap} \rangle_0$ and $\langle q_3 v_{ac} \rangle_0$ in the index-0 model In Fig. 16 (a). This results in the removal of $vs1$ in Fig. 17.

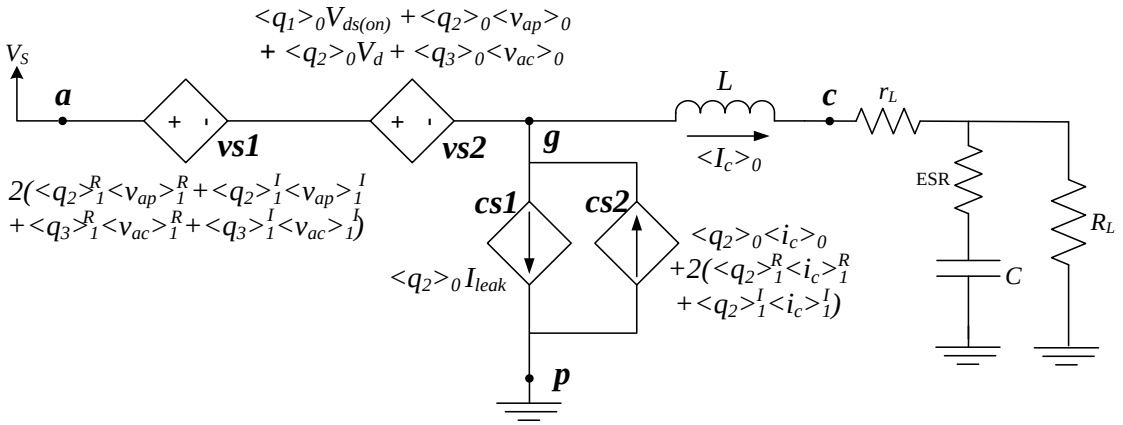


Fig. 17. The index-0 average model of the buck converter with controlled sources $vs1$ and $cs2$ depend on the index-1 average model

On the other hand, $\langle q_2 i_c \rangle_0$ cannot be simplified by rule 1 due to the large variance of i_c shown in Fig. 12. To remove index-1 terms from $\langle q_2 i_c \rangle_0$, we need to consider the waveform shapes of i_c and q_2 shown in Fig. 18. We denote the peak value of i_c by I_{peak} the index-0 average value of i_c is the dc value of the inductor current:

$$\langle i_c \rangle_0 = \bar{\imath}_c = \frac{1}{2}(d_1 + d_2) I_{peak}, \tag{5.2}$$

where $d_1 = \langle q_1 \rangle_0$ and $d_2 = \langle q_2 \rangle_0$. Similarly, the index-0 average value of $q_2 i_c$ is

$$\langle q_2 i_c \rangle_0 = \bar{\imath}_p = \frac{1}{2} d_2 I_{peak}, \tag{5.3}$$

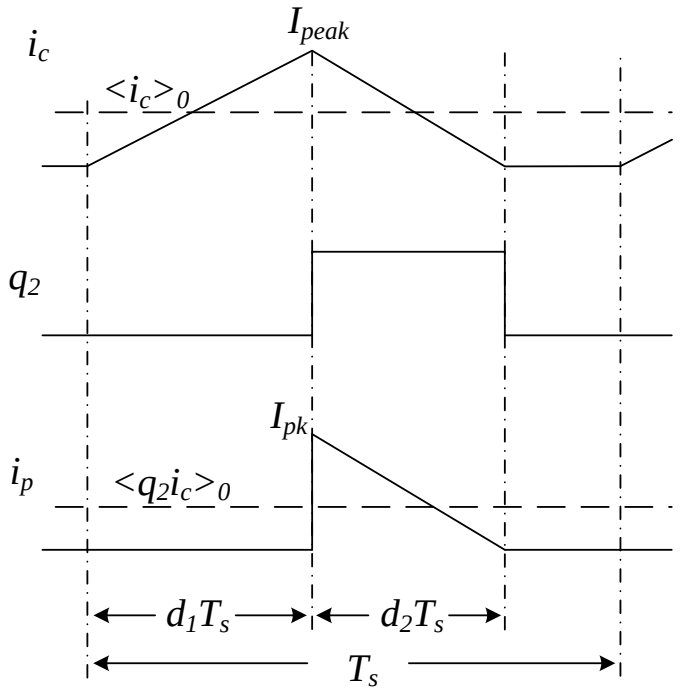


Fig. 18. Illustration of $\langle q_2 i_c \rangle_0$calculation

Substituting (5.2) into (5.3) allows us to rewrite $\langle q_2 i_c \rangle_0$ as a function of $\langle i_c \rangle_0$

$$\langle q_2 i_c \rangle_0 = \frac{d_2}{d_1 + d_2} \langle i_c \rangle_0, \tag{5.4}$$

which does not depend on any index-1 value. In fact, (5.4) is the actual calculation of the

product term with 100% accuracy, equivalent to

$$\langle q_2 i_c \rangle_0 = \sum_{i=-\infty}^{\infty} \langle q_2 \rangle_{-i} \langle i_c \rangle_i, \tag{5.5}$$

which has infinite terms of product and is not practical to compute. For example, in state-space averaging, only one term $\langle q_2 \rangle_0 \langle i_c \rangle_0$ is used as an approximation of (2.34). In the multi-frequency model presented in [8], the average of a product is approximated by

$$\langle q_2 i_c \rangle_0 = \langle q_2 \rangle_0 \langle i_c \rangle_0 + \langle q_2 \rangle_1 \langle i_c \rangle_{-1} + \langle q_2 \rangle_{-1} \langle i_c \rangle_1. \tag{5.6}$$

Compared with both methods, (5.4) is both more efficient and more accurate.

Now we suggest the second rule of system decoupling:

RULE 2. *For the inductor current* i_c *,*$\langle q_2 i_c \rangle_0 = \frac{d_2}{d_1+d_2} \langle i_c \rangle_0$ *exits. All higher order terms can be removed from the index-0 average calculation.*

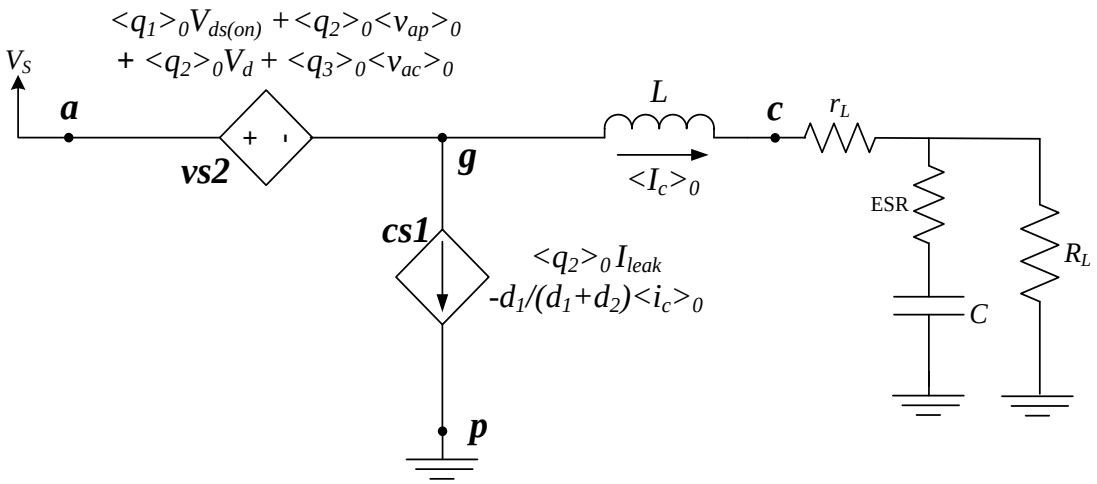


Fig. 19. The index-0 average model of the buck converter with controlled sources $vs1$ and $cs2$ depend on the index-1 average model

Applying rule 2 to the removal of $cs2$ in Fig. 17 as well as changing the current source of $\langle q_2 \rangle_0 \langle i_c \rangle_0$ into $\frac{d_2}{d_1+d_2}\langle i_c \rangle_0$. Fig. 19 summarizes the decoupled model where all of the components can be evaluated independently of high-order averages. Combining this model with the index-1 average model results in a more efficient and accurate multi-harmonic model.

CHAPTER VI

EXPERIMENTAL RESULTS

To demonstrate and test the accuracy and efficiency of our proposed generalized model, we performed a couple of open-loop and closed-loop transient simulations on different DC-DC converters. In every case, we compare the simulation results of our proposed model with conventional models and the real transistor-level simulation. All models and circuits are implemented in Cadence Virtuoso and Verilog-A, simulated by Spectre. Our proposed model is described in transistor-level netlists using industry-standard BSIM4 models.

The simulation accuracy of our proposed model is quantified using the following error metric compared with respect to transistor-level simulation results:

$$\sigma = \frac{\sqrt{\sum_{k=1}^{n}(V_{model}(T \cdot k) - V(T \cdot k))^2}}{\sqrt{\sum_{k=1}^{n} V(T \cdot k)^2}}. \tag{6.1}$$

In (6.1), $V$is a targeted output voltage obtained by real transistor-level simulation while V_{model} is the corresponding output voltage in our proposed model. T is the sampling step size which is set to one tenth of the switching period of a given converter circuit.

VI.A. Boost Converter Open-loop Simulation

A test is performed on the standard PWM boost converter shown in Fig. 20. To better demonstrate the output ripple, we choose a small capacitance value. Similarly, a low frequency is applied in this case to show the effects of harmonics.

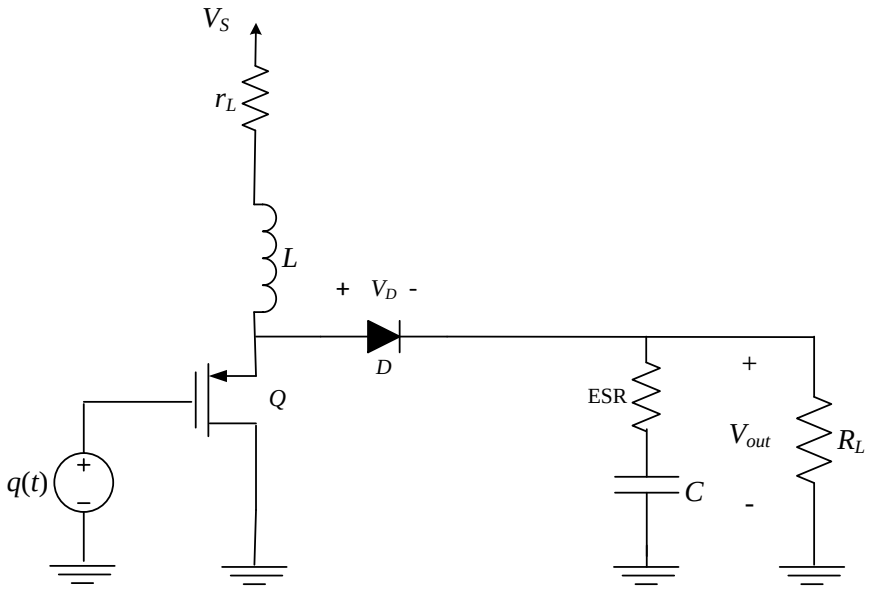


Fig. 20. A standard boost converter with $V_s = 2\text{V}, L = 300\mu\text{H}$, $C = 1\mu\text{F}$ and $R_L = 50\Omega$

We leave the boost converter operating in CCM with a switching frequency $f_s = 50k\text{Hz}$. For this case, the converter simulation starts with a duty ratio of $d = 0.4$ at time $t = 0ms$. This ratio is maintained until $t = 0.4ms$ at which the duty ratio ramps up to 0.5 and remains at this level for the remainder of the simulation. Fig. 21 shows a comparison of transistor-level simulation, our proposed model, and the averaged model obtained using the conventional SSA techniques [12]. As previously mentioned in Chapter V, the SSA model approximates $\langle q_2 i_c \rangle_0$ by $\langle q_2 i_c \rangle_0 = \langle q_2 \rangle_0 \langle i_c \rangle_0$, which can lead to significant errors. Moreover, the SSA model does not consider the effect of device nonidealities. As a result, the SSA model shows visible errors in both the steady state and the transient state. On the other hand, the output voltage and the inductor current waveforms predicted by our proposed method match very well with the transistor level

simulation of the boost converter. The percentage errors for the output voltage are found to be $\sigma_v = 3.46\%$ using (6.1). Furthermore, in this case, our proposed model achieved 6× runtime speedup with respect to the transistor-level simulation.

To further investigate the accuracy of our proposed model, we now take a closer look at the waveforms of Fig. 21 and make cycle-to-cycle comparisons of our proposed model with the transistor-level circuit. Fig. 22 shows a magnified view of the waveforms of Fig. 21 between time $t = 0.4ms$ and $t = 0.5ms$. As can be seen, the responses predicted by our proposed model demonstrate excellent accuracy in capturing the ripple current of the converter. Notice, however, that the sharp transitions due to the switching activities are not present in our proposed model since it only captures the first order harmonics of the ripple. We expect that by extending our model to account for higher order harmonics, which is rather straightforward, we can further improve our model's ability to capture the fine details of the ripple.

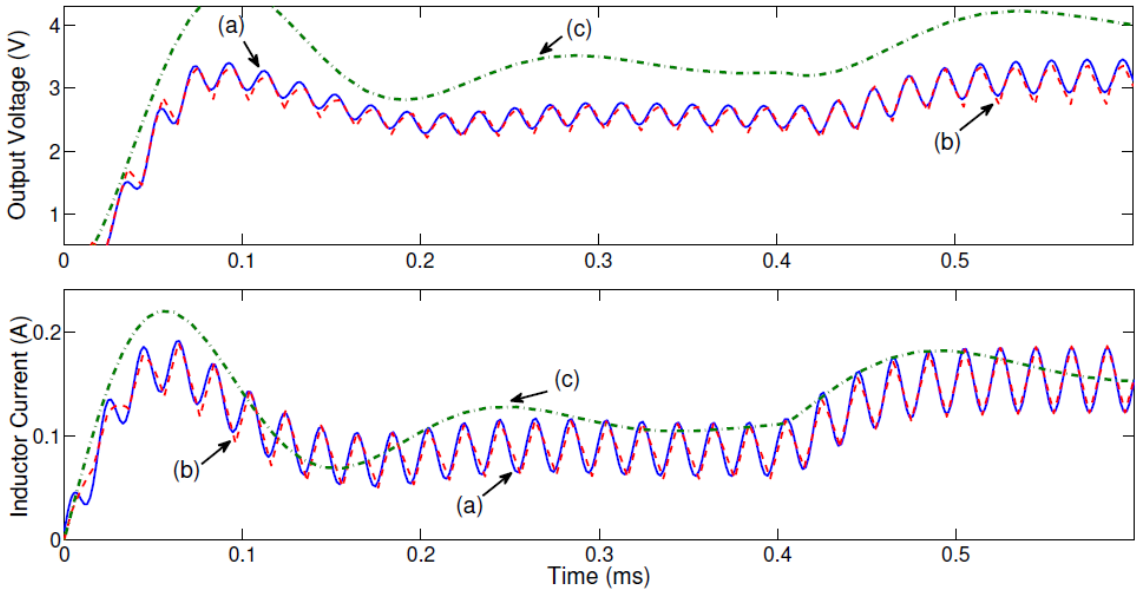


Fig. 21. Boost converter open-loop simulation with varying duty ratio using our proposed model (a), transistor-level circuit (b), and conventional SSA (c)

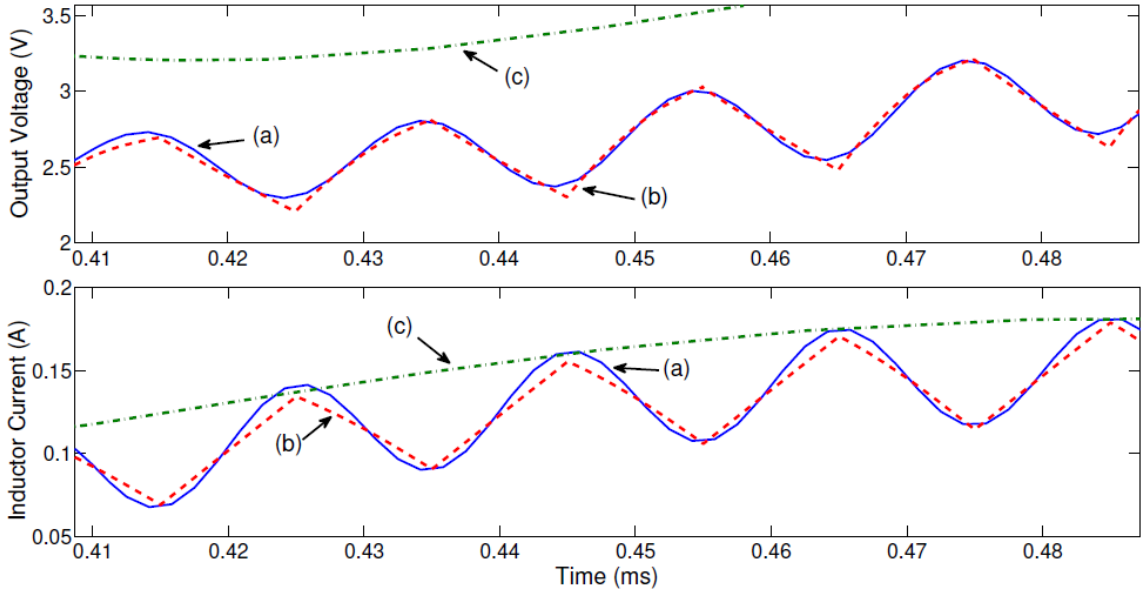


Fig. 22. Magnified comparison of our proposed model (a) and transistor-level boost converter (b)

VI.B. Buck Converter Open-loop Simulation

We now test our proposed model on a buck converter shifting operation modes between CCM and DCM. The transient response of the proposed model is investigated by varying the duty ratio over a wide range. The standard buck converter circuit modeled is shown in Fig. 11 with $L = 100\mu\text{H}$, $C = 500n\text{F}$, $R_L = 10\Omega$ and $f_s = 50k\text{Hz}$. Starting from an initial value of 0.6, the duty ratio of the buck converter is increased to 0.7 at $t = 0.1ms$ and then linearly ramped down to 0.2 at $t = 0.3ms$, which is at the end of the 15^{th} switching cycle. The simulation results for the output voltage and inductor current of the transistor-level circuit, our proposed model and a model derived by multi-frequency averaging [10] are shown in Fig. 23. The multi-frequency average model is modified to account for the nonidealities and parasitics of devices. As a result, both our model and the multi-frequency model make good predictions of the voltage and current responses in the first $0.2ms$ of simulation when the converter is operating in CCM. However, as the duty ratio continues to drop and the converter enters into DCM, the multi-frequency average model significantly deviates from the true response. Our proposed model, on the other hand, successfully detects the presence of the discontinuity of the inductor current and therefore closely tracks the actual circuit response. The major reason for the large errors observed when using the multi-frequency average model in this example is due to the fact that the model is unable to capture the circuit behavior in the zero-current interval of q_3, which is fundamentally different from that in q_2.

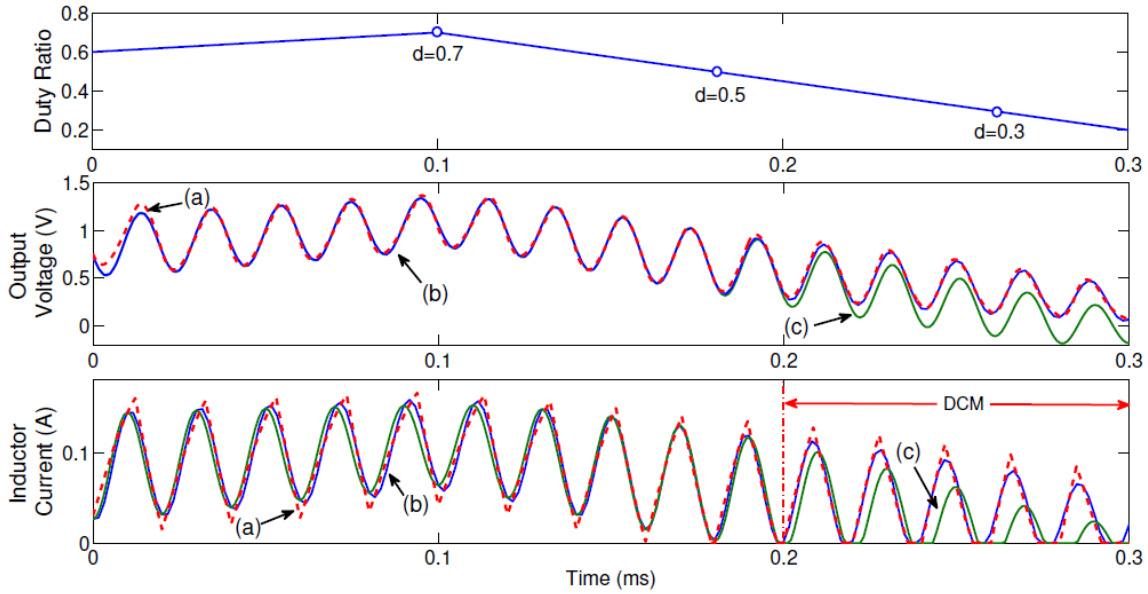


Fig. 23. Buck converter open loop simulation of the transistor-level circuit (a), our proposed model (b), and the multi-frequency average model (c)

In this case, the simulation of the actual transistor-level circuit using transient analysis can be very inefficient and time consuming due to the highly nonlinear switching behaviors in DCM. However, our proposed model replaces the discontinuous inductor current with continuous averaged currents of multiple orders, which in turn results in a 10× speedup with respect to the simulation of the transistor-level circuit. Moreover, no other modeling method by now can show the large current ripples in DCM, which is crucial for discontinuous current design. The output voltage error in this case is found to be $\sigma_v = 3.97\%$, which once again demonstrates the high accuracy of our proposed model. In comparison, the multi-frequency average model shows an error of 18.13%.

VI.C. Buck Converter Closed-loop Simulation

In this last case, our proposed model is tested in closed-loop simulation of buck converter. The buck converter circuit of the previous example is used but is now driving a load capacitance of 20μF. In addition, a voltage feedback loop is added to the circuit with a reference voltage at $V_{ref} = 500m$V. The load resistance of the buck converter starts at 8Ω and then linearly decreases to 4Ω over 10 switching cycles before increasing to 5Ω over the next 5 switching cycles. A comparison of the simulation results of the transistor-level converter with our model is shown in Fig. 24. Both the output voltage and inductor current simulated by our model are in good agreement with the actual buck converter responses. A speedup of $10\times$ is obtained based on our model with respect to the transistor-level circuit. The voltage response errors are found to be $V_\sigma = 0.61\%$.

Based on the above case, a worst-case simulation is developed to test the efficiency of our proposed model in complicated simulation environments. Besides a slow varying load resistor, a time-varying duty ratio is added to see the stability in a lengthy run time. Several resistors and capacitors are inserted around the gate, source and drain of the transistor to model the parasitics and time skews, which also produces additional nodes. With these simulation setups, the actual transistor-level simulation run time is as long as one hour. The output voltage and inductor current obtained by our model can also capture the transistor-level results throughout the entire simulation interval. The relative voltage response errors grow less than 1% and a speedup of $9\times$ is achieved.

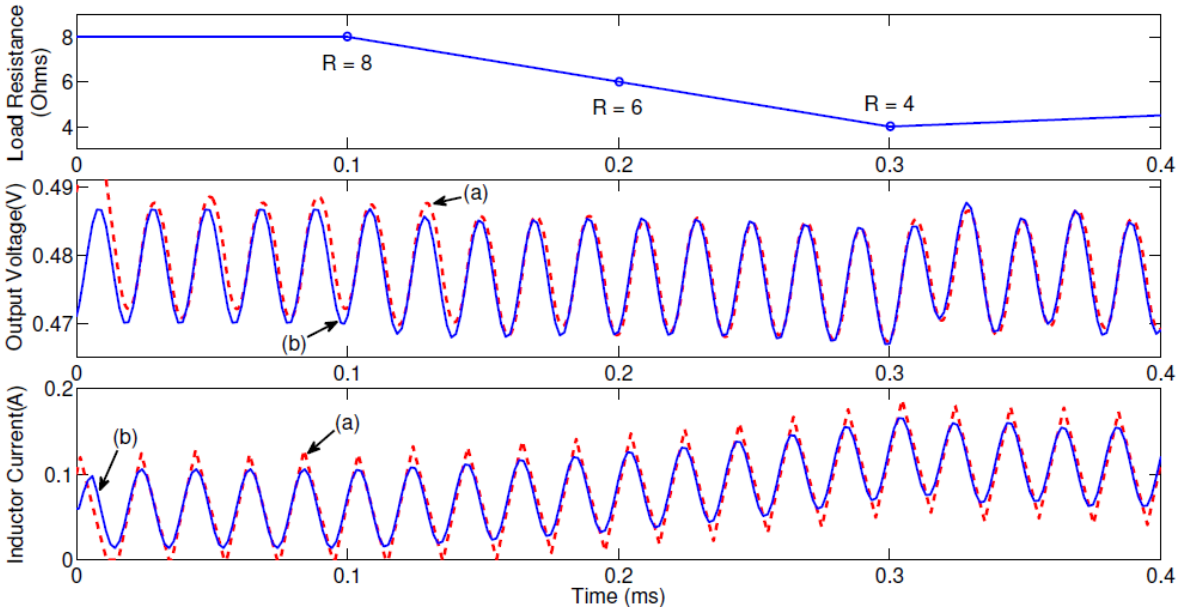


Fig. 24. Buck converter open-loop simulation with varying duty ratio using our proposed model (a), transistor-level circuit (b), and conventional SSA (c)

CHAPTER VII

CONCLUSIONS

In this research work we present a generalized multi-harmonic model for PWM DC-DC converters, which is applicable for various topologies. Our proposed model can capture the dc response as well as higher-order harmonics. As a full order model, it retains the inductor current as a state variable and predicts accurately even when the converter is in transient state. Our model can transition between CCM and DCM continuously and seamlessly during the simulation. Moreover, we suggest two rules for system decoupling in order to achieve better efficiency without compromising accuracy. Our model was tested on three different DC-DC converters and speedups of about 10× were achieved with respect to transistor-level simulations.

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