JITTER TRACKING BANDWIDTH OPTIMIZATION USING ACTIVE-INDUCTOR-BASED BANDPASS FILTERING IN HIGH-SPEED FORWARDED CLOCK TRANSCEIVERS

A Thesis

by

YANG LIU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Samuel Palermo
Committee Members,	Jose Silva-Martinez
	Peng Li
	William M. Lively
Head of Department,	Costas Georghiades

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ABSTRACT

Jitter Tracking Bandwidth Optimization Using Active-Inductor-Based Bandpass Filtering in High-Speed Forwarded Clock Transceivers. (May 2011)

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Chair of Advisory Committee: Dr. Samuel Palermo

Inter-chip input-output (I/O) communication bandwidth demand, which rapidly scaled with integrated circuit scaling, requires high performance I/O links to achieve a per pin data rate as high as multi-Gb/s. The design of high-speed links employing forwarded-clock architecture enables jitter tracking between data and clock from low to high frequencies. Considering the impact of clock to data skew, high frequency sampling clock jitter and data jitter become out of phase at receiver, which reduces the timing margin and limits the data rate. The jitter tracking bandwidth (JTB) between data and clock should be optimized to compensate the clock to data skew. System level analysis shows that the wide tunable range of JTB is needed to compensate different amounts of skews.

The implementation of bandpass filtering on forwarded-clock path is able to control the JTB through the controlling of Q. This work introduces a method using bandpass filtering to optimize the JTB in high-speed forwarded-clock transceivers, followed by the implementation of active-inductor-based bandpass filter as clock receiver, which has advantages of low-voltage operation, low power as well as low area

consumption. Simulation results shows that the designed filter provides controllable JTB over 40 - 600MHz. The bandpass filter is implemented in IBM 90nm CMOS process.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

First, I would like to thank my advisor, Dr. Samuel Palermo, for his guidance, encouragement, motivation and support from the initial stages of research to the completion of the thesis. His technical expertise, insightful thinking and attention have been of great value and helped me to shape the thesis through the various discussions. I would like to thank all my committee members, Dr. Jose Silva-Martinez, Dr. Peng Li, Dr. Lively, for their time, support and valuable suggestions. I thank Younghoon Song and Ahmed Ragab for their help on pin sharing and interconnection of the chip. I would also like to thank all my friends, especially Shan Huang, Heng Zhang, Yung-chung Lo, Chao Zhang, Hongbo Chen, Xuan Zhao, Jiayi Jin, Jackie Zou, Jun Yan, for all the valuable technical discussions and encouragements. Finally and most importantly, I thank my parents for their love, sacrifice, encouragement and constant support, which made this graduate school journey possible.

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CHAPTER I

INTRODUCTION

Integrated circuit technology scaling has incredibly improved the on-chip processing and computational power, which enabled the evolution from single core processor to multi-core and many core processers. These architectures will require an on-chip communication bandwidth extending from hundreds of GB/s into the TB/s range [1], and thus necessitates a corresponding increase in the inter-chip input-output (I/O) communication bandwidth. Figure 1.1 shows the trend of I/O bandwidth scaling over years.

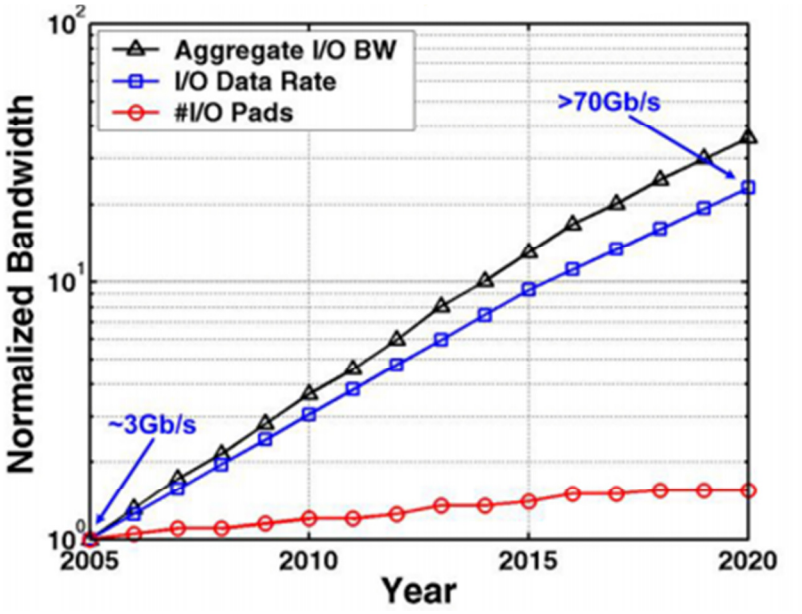

Figure 1.1 I/O Scaling Projections [2]

However, the electrical channel bandwidth lags behind this rapidly increasing

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This thesis follows the model of *IEEE Transactions on Circuit and Systems*.

inter-chip communication bandwidth requirement due to severe high frequency channel losses and non-idealities such as reflections due to impedance discontinuities and crosstalk. In addition, the pin count does not scale with the I/O bandwidth requirement from Figure 1.1, which will require huge improvement on per pin data rate. Therefore, the development of high performance I/O link is required.

The design of multi-Gb/s data links requires both advanced equalization of channel and sufficient optimization of clock quality to balance the goals of performance, power efficiency and cost. It has been demonstrated that the maximum achievable data rate is sensitive to the high frequency TX jitter as well as RX sampling jitter [3]. The process technology scaling has increased the transistor bandwidth dramatically and enabled more advanced equalization. However, increased integration and bandwidth demands brought in more challenges on clock quality optimization [3].

The two most important classes of high speed clock architectures are forwarded clock and embedded clock. Compared to the embedded clock architecture, a forwarded clock architecture is more power and area efficient since clock and data recovery (CDR) circuitry and an inherent phase-locked loop (PLL) are not required. In an ideal scenario, the jitter on forwarded clock is correlated to the jitter on the data in that both signals are generated by the same transmitter. Thus, the sampling quality is improved by retiming the data with a clock that tracks the data jitter. Practically, since the delay of data and clock paths has several UI offset, very high frequency jitter will appear out-of-phase at the receiver and should not be tracked [4]. Therefore, the jitter tracking bandwidth (JTB) on the clock path should be adjustable. There are several methods providing adjustable

JTB like PLL, Injection-locking and bandpass filtering, as is discussed in [5]. This thesis focuses on the method of active inductor-based bandpass filtering on forwarded clock.

1.1 Organization of Thesis

Chapter II presents the introduction about high speed I/O link architectures, jitter and electrical channels, followed by the jitter analysis methods that are used in this thesis. Moreover, the jitter tracking in forwarded-clock system is discussed in this chapter.

In Chapter III, the analysis about how bandpass filtering provides low-pass jitter filtering is given. Based on the relationship between Q of bandpass filtering and the bandwidth of jitter transfer function it provides, jitter tracking optimization using bandpass filtering is discussed.

Chapter IV proposed a design of low voltage active inductor-based bandpass filter that is able to optimize jitter tracking in forwarded clock system. The designs of on-chip voltage regulator and output buffer for testing are included in this chapter as well.

Chapter V provides the post-layout simulation results which characterizes the performance of bandpass filter itself and the jitter tracking bandwidth range it can provide.

Finally Chapter VI concludes the thesis with comparisons of stand-alone filter and jitter tracking optimization methods. An automatic frequency tuning scheme is proposed for system-level application of the designed bandpass filter.

CHAPTER II

BACKGROUND

2.1 High-speed Link Architectures

There are two primary architectures that are used in high speed I/O transceivers design. One is forwarded-clock architecture; the other is embedded-clock architecture. The operations and characteristics are introduced in the following subsections.

2.1.1 Forwarded-clock Architecture

The typical forward-clock architecture is shown in Figure 2.1. This architecture requires an extra channel to transmit the clock signal from the transmitter to receiver for data sampling. Since the low-pass channel will attenuate the clock signal, a good received clock amplifier is needed to compensate the filtering effect of the channel. At each receiver, clock deskew is employed to align the sampling clock phase to data center.

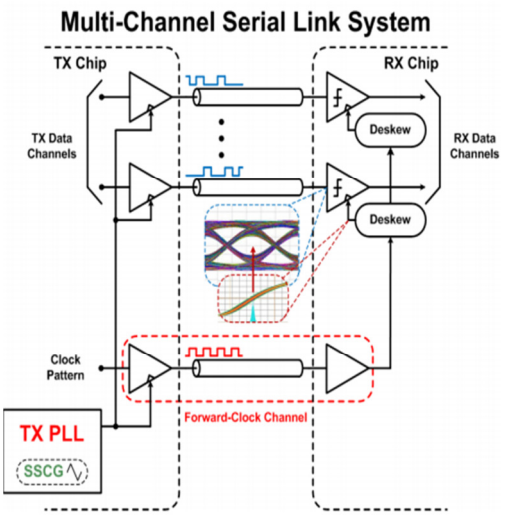

Figure 2.1 Forwarded-clock Architecture [6]

The clock and data transmitters are sharing the same design and triggered by the same TX PLL such that the circuit induced jitter for clock and data signals are identical. On the receiver side, the data will be sampled by the received clock signal with the same phase variation, which improves the sampling quality. The clock and data jitter tracking over a wide frequency range is one of the primary differences between forwarded-clock and embedded clock systems.

2.1.2 Embedded-clock Architecture

Figure 2.2 shows the architecture of embedded-clock system. There is no clock channel used for sending the clock from transmitter to receiver. At each receiver, there is a CDR circuit which is used to extract the sampling clock phase from incoming data. Each CDR circuit on the receiver side has to be driven by an RX PLL. The clock and data jitter tracking also exists in an embedded-clock system. However, it is limited by the CDR bandwidth. In addition, embedded-clock requires more hardware than forwarded-clock does.

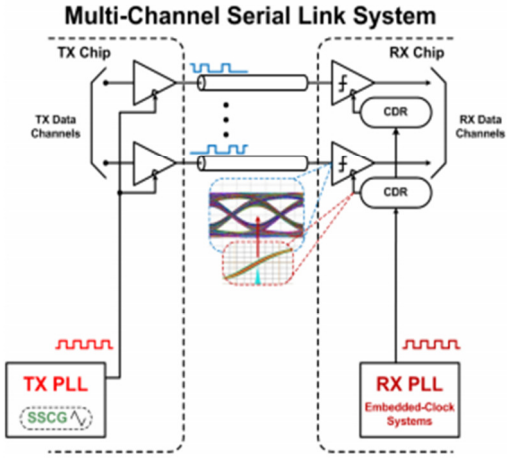

Figure 2.2 Embedded-clock Architecture [6]

2.2 Jitter

Jitter is defined as the deviation of significant timing instants of a signal from their ideal positions in time. For a clock signal, the significant timing instants are zero-crossing times of rising and falling edges.

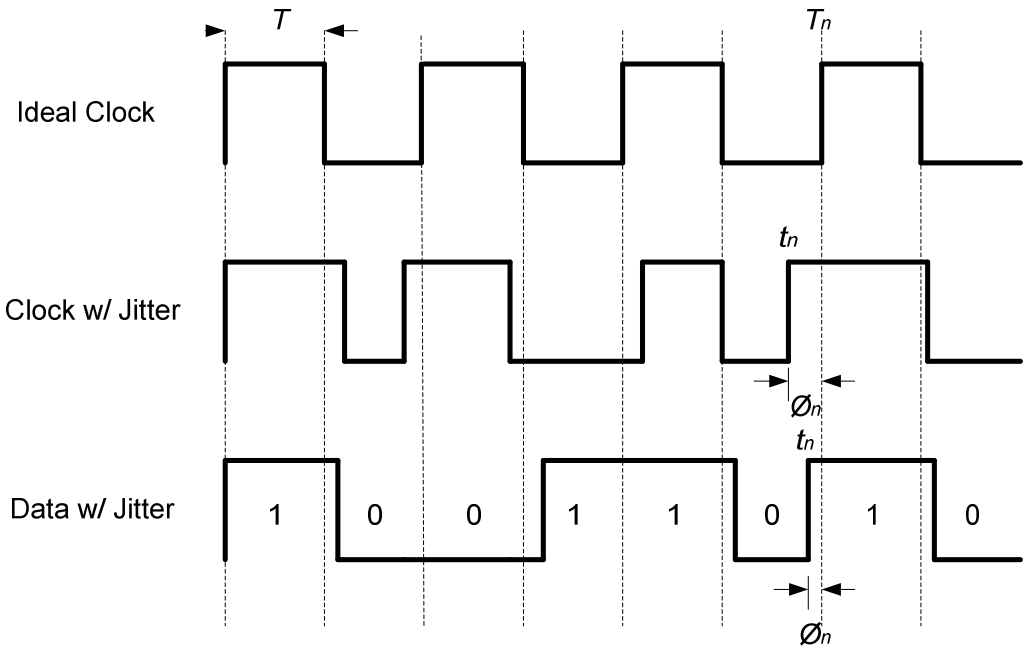

Figure 2.3 Clock and Data Jitter

For a data signal, the significant timing instants are the logic transition times or edges. Figure 2.3 illustrates both clock and data jitter, where T is the bit period of data and half the clock period. The vertical dash lines are the ideal timing positions of the significant instants of signal. T_n denotes the nth ideal timing instants and

$$T_n = nT \tag{2.1}$$

while t_n represents the nth actual timing instants. For both clock and data signal, the jitter at the nth bit period is $\emptyset_n = t_n - nT$, which is also called "cumulative jitter". A general function of a pulse-train signal is defined as

$$s(t) = D_n P\big(\emptyset(t)\big), \tag{2.2}$$

where D_n represents the logic value (either '1' or '0') of the nth bit, and *P* is the pulse function with phase function $\emptyset(t)$ as the argument. This phase function sets the nth bit width as W_n that satisfies

$$W_n = t_n - t_{n-1}, \tag{2.3}$$

$$\emptyset(t_n) - \emptyset(t_{n-1}) = 2\pi. \tag{2.4}$$

A data stream with jitter can be expressed as

$$s(t) = D_n P\big(2\pi f_d t + \varphi(t)\big), \tag{2.5}$$

where $f_d = 1/T$ and $\varphi(t)$ denotes the phase noise, which is a continuous quantity and cause jitter. The nth transition is trigger according to the argument $2\pi f_d t_n + \varphi(t_n)$ in real system. In ideal system, there is no phase noise term and the argument is $2\pi f_d T_n$. As discussed in [7]

$$2\pi f_d t_n + \varphi(t_n) = 2\pi f_d T_n \tag{2.6}$$

$$|\varphi(t_n)| = 2\pi f_d |(t_n - T_n)| = 2\pi f_d |\emptyset_n| \tag{2.7}$$

Thus, the jitter at the nth significant timing instants can be written in terms of phase noise,

$$|\emptyset_n| = \frac{|\varphi(t_n)|}{2\pi f_d} \tag{2.8}$$

Similarly, the clock jitter can be written in terms of phase noise as

$$|\emptyset_n| = \frac{|\varphi(t_n)|}{2\pi f_c} \tag{2.9}$$

where f_c is the frequency of clock.

2.2.1 Jitter Categories

Random Jitter

The random jitter originates from device noise such as thermal noise, shot noise as well as flicker noise. The central limit theorem of probability and statistics can be used to describe random jitter. The probability density function (PDF) of random jitter follows a Gaussian distribution,

$$RJ(t) = \frac{1}{\sqrt{2\pi\sigma_{RJ}}} e^{\frac{-t^2}{2\sigma_{RJ}^2}}, \tag{2.10}$$

where σ_{RJ} is the standard deviation of the distribution. Figure 2.4 shows an example of the PDF of random jitter. It is unbounded, which means it does not have a well-defined peak-to-peak value. The magnitude of random jitter is characterized by its rms value, σ_{RJ}.

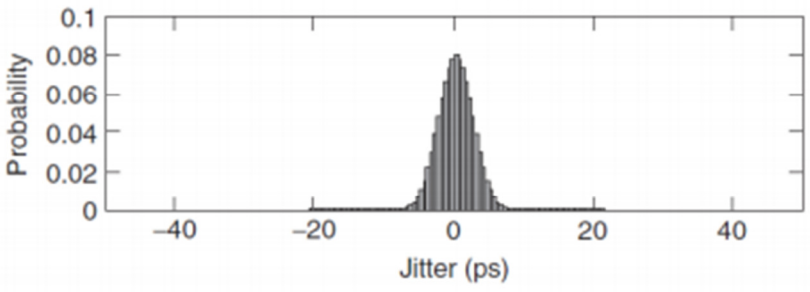

Figure 2.4 Probability Density Function of Random Jitter [8]

Duty Cycle Distortion (DCD)

DCD is caused by duty cycle errors. The ratio of signal pulse width to the period is no longer ½ due to DC offset, rise/fall time mismatch and device mismatch. In half-rate system, duty cycle errors are troublesome since both the rising and falling edges of clock are used to sample the data.

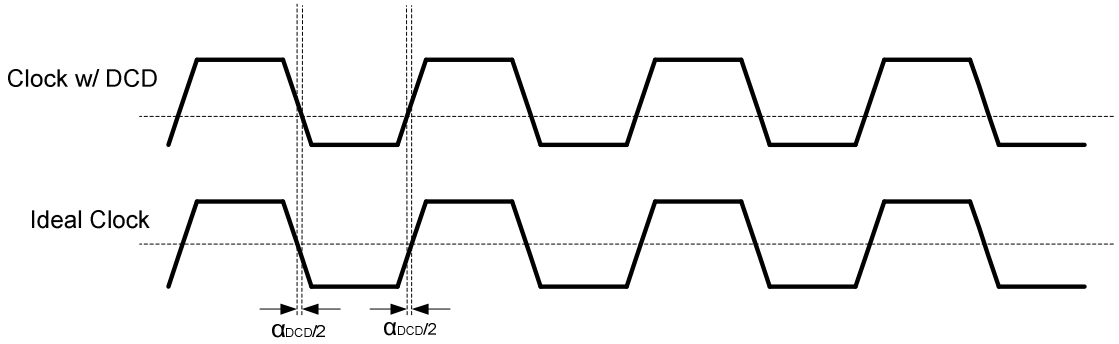

Figure 2.5 Duty-Cycle Distortion Induced Jitter

An example of DCD induced jitter is illustrated in Figure 2.5. The horizontal dash line is the threshold level. This figure shows a clock signal whose falling edges are $\alpha_{DCD}/2$ later than their ideal positions while whose rising crossings are $\alpha_{DCD}/2$ earlier, where α_{DCD} is the peak-to-peak duty cycle distortion jitter. Since the numbers falling and rising edges of a clock are the same, the jitters are evenly distributed at $t = \alpha_{DCD}/2$ and $t = -\alpha_{DCD}/2$. The PDF of DCD jitter is

$$PDF_{DCD}(t) = \frac{1}{2}\left[\delta\left(t - \frac{\alpha_{DCD}}{2}\right) + \delta\left(t + \frac{\alpha_{DCD}}{2}\right)\right]. \quad (2.11)$$

Figure 2.6 shows the PDF of DCD. DCD is deterministic jitter and thus bounded in amplitude.

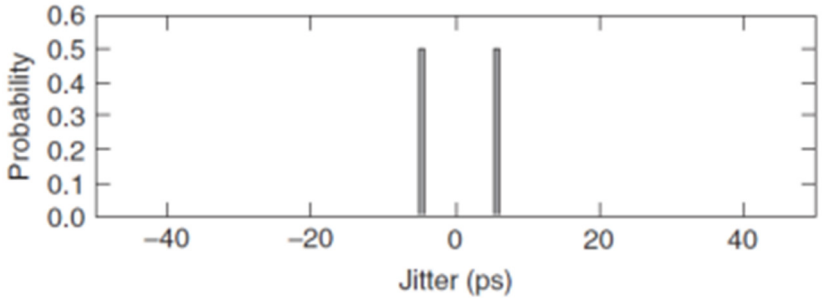

Figure 2.6 Probability Density Function of DCD Induced Jitter [8]

Sinusoidal Jitter (SJ)

SJ has a periodic form due to modulating effects such as PLL reference clock feed-through. Other possible sources are power supply variation and interference from the signals that are related to the data pattern. Due to its periodic nature, SJ can be decomposed in to a Fourier series of sinusoids as

$$SJ(t) = \sum_i A_i cos(\omega_i t + \theta_i). \tag{2.12}$$

The jitter distribution produced by an individual sinusoid is

$$PDF_{SJ}(t) = \begin{cases} \dfrac{1}{\pi\sqrt{A^2 - t^2}}, & A > |t| \\ 0, & A \leq |t| \end{cases}. \tag{2.13}$$

Figure 2.7 illustrates the PDF of SJ.

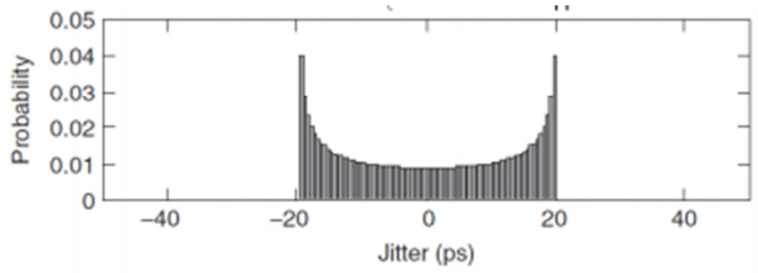

Figure 2.7 Probability Density Function of Sinusoidal Jitter [8]

2.2.2 Jitter Impulse Response and Jitter Transfer

Jitter transfer is an important metric that is used to characterize the system response on input jitter. In analogy to the magnitude frequency response, jitter transfer is expressed by the ratio of output to input jitter as a function of frequency. In order to obtain the frequency response of a system, the system impulse response can be extracted in time domain through simulation or measurement and then Fourier transform is applied on the extracted impulse response to generate the jitter transfer function. The same idea is applicable on obtaining jitter transfer of the system. The required time domain information is called jitter impulse response which is a discrete time sequence, since that jitter is only measured at every clocking moment (either the rising or falling clock edge or both). Then jitter transfer of a system can be obtained by applying FFT on those discrete time jitter samples. Figure 2.8 shows how the discrete time jitter impulse response can be extracted [3]. The jitter impulse is induced at certain clocking edge by advancing or retarding the edge with small percentage of clock cycle, which is descripted in (a). Due to the filtering effect of the band-limited system, the output clock waveform becomes sinusoidal as shown in (b). The solid line is the output clock waveform with ideal clock input while the dash line is the output clock waveform with input clock containing a jitter impulse at one clocking edge. The resultant jitter samples can be extracted by taking the time difference of every clocking edge between the output clocks with and without jitter impulse input, as shown in (c).

It is introduced in [3] that the typical jitter transfer and jitter impulse response classes associated with different frequency responses, as shown in Figure 2.9. The jitter

transfer and jitter impulse response method will be employed to prove the effect of channel and bandpass filtering on input clock jitter in the following sections.

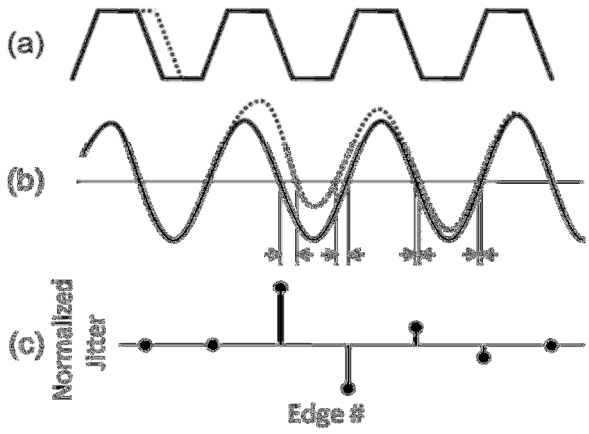

Figure 2.8 (a) Ideal Clock Waveform with Jitter Impulse Stimulus (b) Output Clock Waveform Due to Input Clock with (Dash Line) or without (Solid Line) Jitter Impulse Stimulus (c) Discrete Time Jitter Impulse Response Sequence [3]

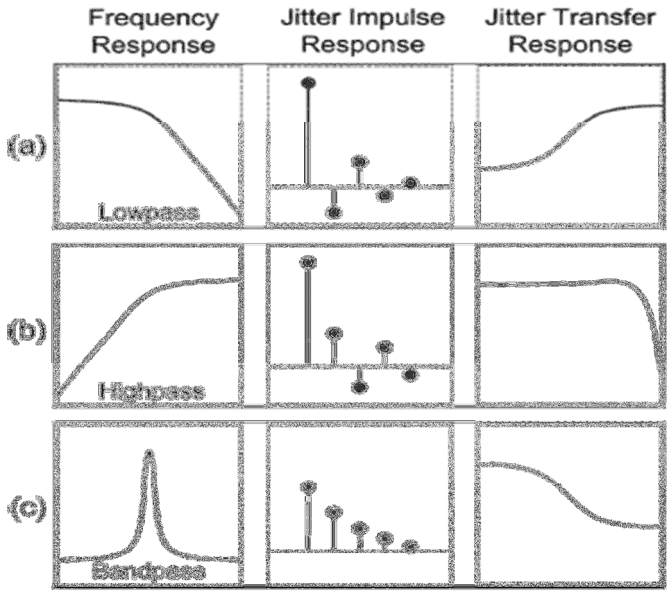

Figure 2.9 Jitter Transfer Functions of (a) Low-Pass, (b) High-Pass and (c) Band-Pass Systems [3]

2.3 Electrical Channel

This section will introduce where the channel loss comes from and how the channel loss affects the transmitted signal and jitter.

2.3.1 Channel Loss

Realistic transmission lines suffer from high-frequency loss caused by skin effect and dielectric loss.

Skin effect describes the process that high-frequency current flows primarily on the surface of a conductor, producing the resistive loss tem which is proportional to the square-root of signal frequency. The cross section of a rectangular conductor is shown in Figure 2.10. δ is skin depth, where current falls by e^{-1} relative to full conductor and

$$\delta = \sqrt{\frac{\rho}{2\pi f \mu}}. \tag{2.14}$$

ρ is the resistivity of the conductor while μ is the absolute magnetic permeability of conductor. Define f_s as the critical frequency where skin depth equals half conductor height, then

$$f_s = \frac{\rho}{\pi\mu(\frac{h}{2})^2}. \tag{2.15}$$

The resistive loss term due to skin effect is given by

$$\alpha_R = \frac{R_{DC}}{2Z_0}(\frac{f}{f_s})^{\frac{1}{2}}, \tag{2.16}$$

where Z_0 is the characteristic impedance of the conductor.

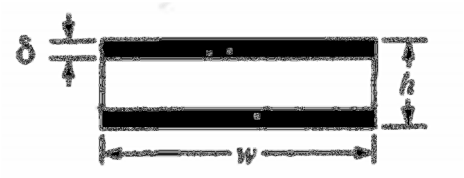

Figure 2.10 Rectangular Conductor Cross-Section [9]

Dielectric loss describes the process that energy is absorbed from an alternating electric field and converted to heat by the insulating material of the transmission line, producing the dielectric loss term which is proportional to signal frequency,

$$\alpha_D = \frac{\pi\sqrt{\varepsilon_r}tan\delta_D}{c} f, \tag{2.17}$$

where ε_r is the relative permittivity, c is the speed of light, and $tan\delta_D$ is the loss tangent of the material.

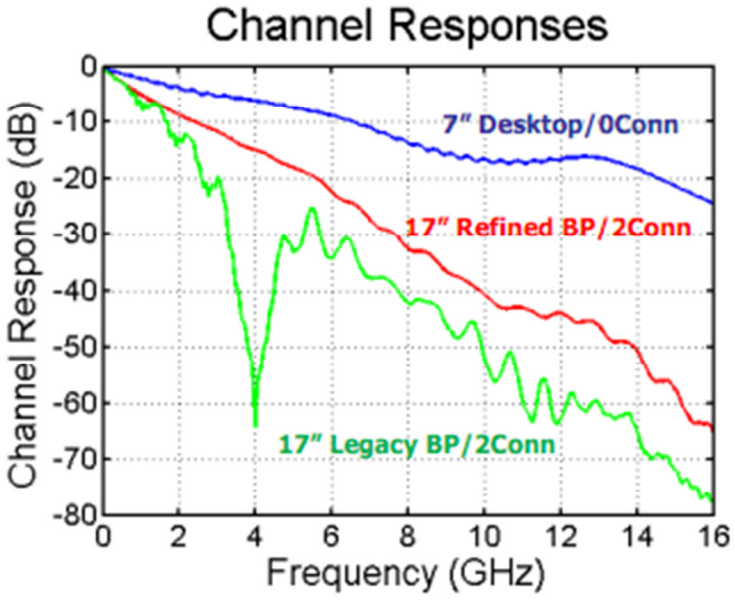

Figure 2.11 Frequency Response of Channels [10]

The frequency dependent loss term results in a low-pass characteristic of electrical channels, as shown in Figure 2.11. The attenuation increases with distance [10]. When a pulse passes through the channel, its high frequency components are distorted, resulting in an attenuated receive pulse whose energy has been spread over time, as shown in Figure 2.12. If a bit-stream is transmitted across the channel, the residual state of the previous bit can interfere with the current bit, resulting in Inter-symbol Interference (ISI).

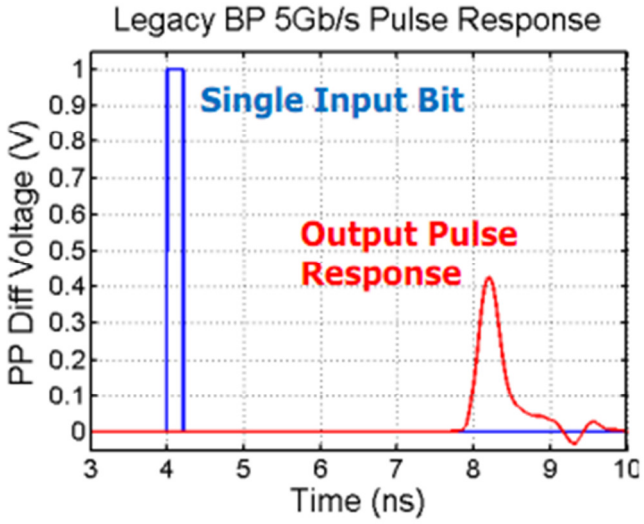

Figure 2.12 Output Channel Pulse Response of Single Input Bit [10]

2.3.2 Impact of Channel Loss on Transmitted Data and Clock Jitter

Low-pass Channel Impacts on Data Jitter

It is well known that the low-pass channel spreads the energy of a bit over several bit periods, which distorts the previous or following bits. The distortions on each bit are different since the data pattern is random, which means that the logic transitions might deviate from their ideal positions by different time periods.

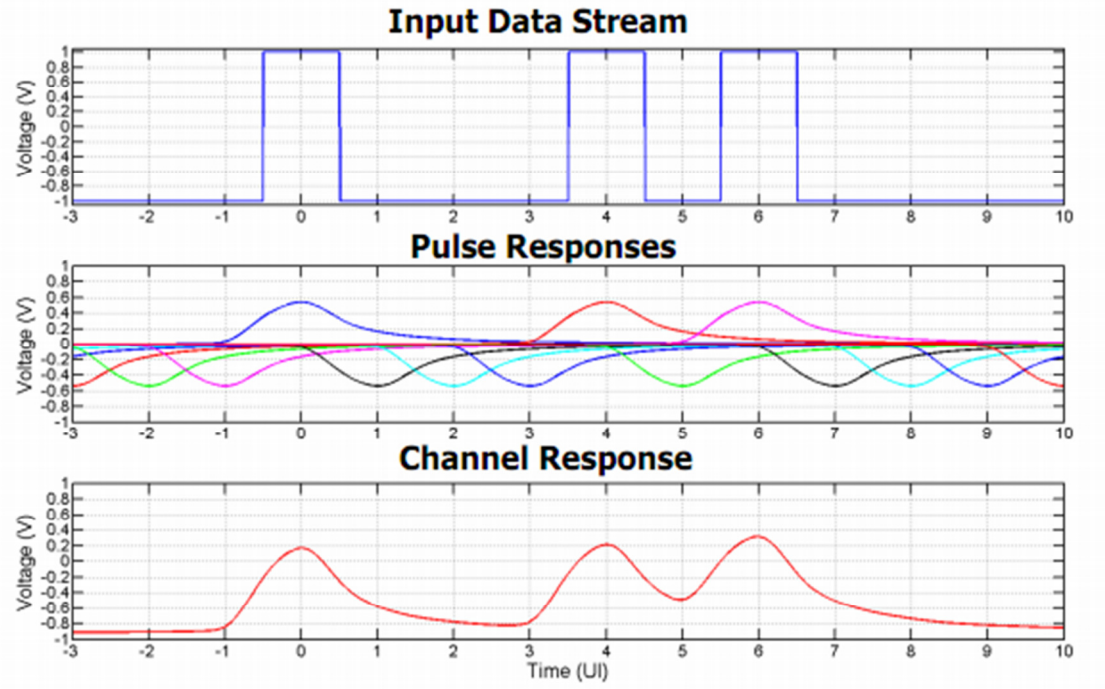

Figure 2.13 Channel Response of Input Data Stream [10]

The channel data stream response can be generated by applying superposition on the channel pulse response of individual bit of the data stream, as shown in Figure 2.13. The channel data stream response can be chopped into equal periods and overlaid into one plot, producing the eye diagrams as shown in Figure 2.14. It is clear that the distribution of logic transitions occupies certain percentage of bit period, degrading the timing margin. These logic transitions deviations are also ISI induced jitter. This kind of jitter is data dependent and deterministic.

The ISI induced jitter increases as data rate increases, as shown in Figure 2.15.

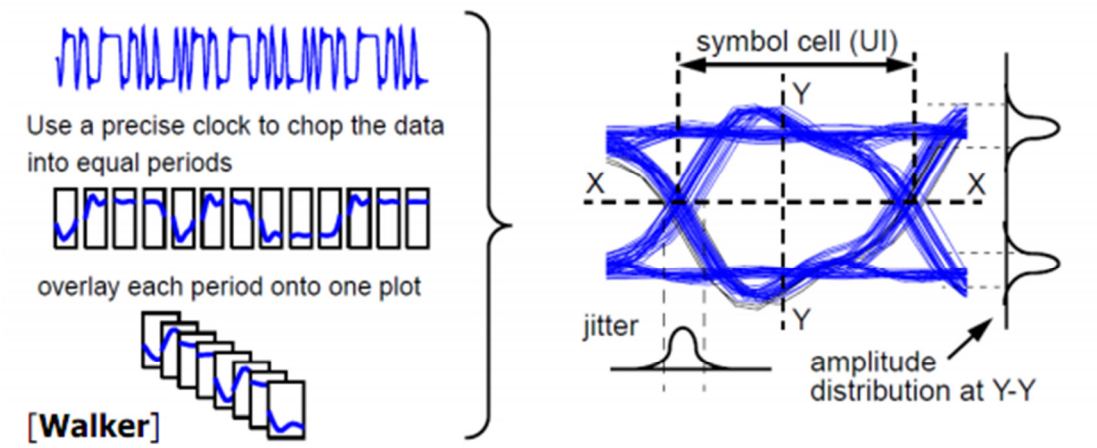

Figure 2.14 Eye Diagram Extraction [11]

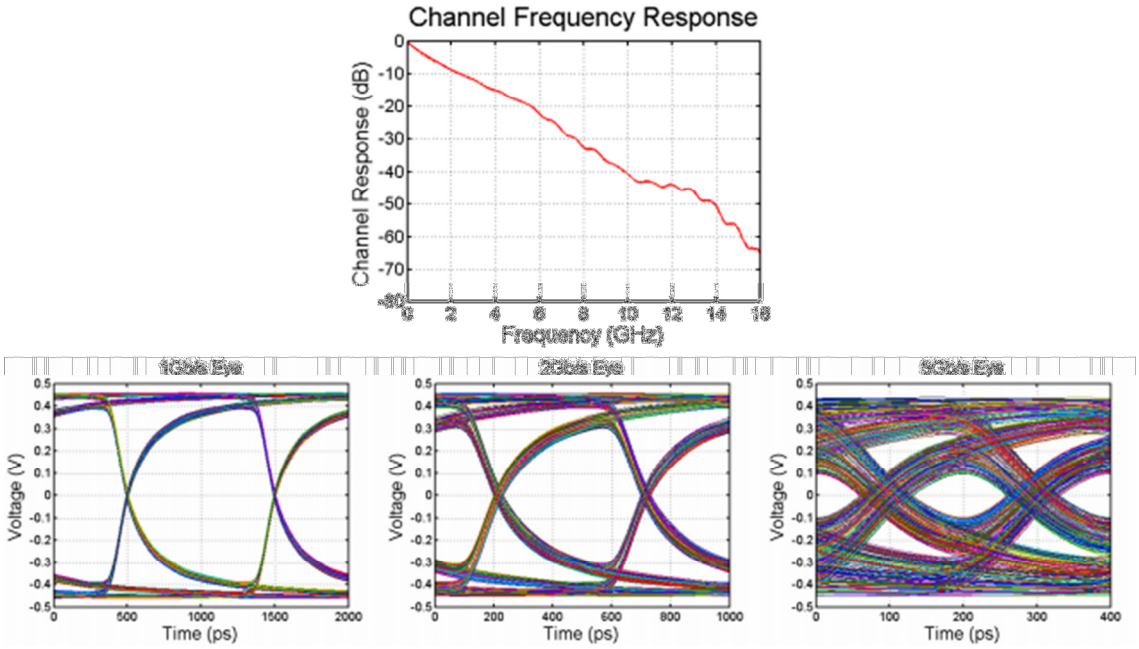

Figure 2.15 Eye Diagram vs. Data Rate [12]

Low-pass Channel Impacts on Clock Jitter

To simplify the analysis, the clock signal with jitter can be approximated as a sinusoidal wave which is frequency modulated and expressed as,

$$c(t) = Acos(2\pi f_c t + \beta sin2\pi f_m t), \tag{2.18}$$

where f_c is the clock frequency, $\beta sin2\pi f_m t$ is the simplified frequency modulated term modeling the phase noise and jitter and β represents the phase noise amplitude while f_m the modulation frequency [13]. For small β, the clock expression can be simplified as

$$c(t) \approx Acos(2\pi f_c t) - \frac{\beta A}{2}\{cos[2\pi(f_c - f_m)t] - cos[2\pi(f_c + f_m)t]\}. \tag{2.19}$$

The Fourier transform of $c(t)$ is given by

$$C(f) \approx \frac{A}{2}\delta(f - f_c) - \frac{\beta A}{4}\{\delta[f - (f_c - f_m)] - \delta[f - (f_c + f_m)]\}. \tag{2.20}$$

Therefore, the spectrum is symmetric around f_c, as shown in Figure 2.16. In the figure, $f_L = f_c - f_m$ and $f_H = f_c + f_m$. Figure 2.17 shows the frequency response of B12 channel [14]. The received clock spectrum is given by multiplying the input clock spectrum with the channel frequency response as

$$S(f) = \frac{\alpha_c A}{2}\delta(f - f_c) - \frac{\beta A}{4}[\alpha_L \delta(f - f_L) - \alpha_H \delta(f - f_H)], \tag{2.21}$$

where α_L, α_c and α_H are the channel response at f_L, f_c and f_H, respectively. The received signal can be expressed in time domain as

$$s(t) = A_r co\, s(2\pi f_c t + \beta_r sin2\pi f_m t), \tag{2.22}$$

where A_r is the amplitude of received clock, β_r is the amplitude of phase noise after low-pass channel. Similarly, the Fourier transform of $s(t)$ can be given in assumption that β_r is small enough,

$$S(f) = \frac{A_r}{2}\delta(f - f_c) - \frac{\beta_r A_r}{4}[\delta(f - f_L) - \delta(f - f_H)]. \tag{2.23}$$

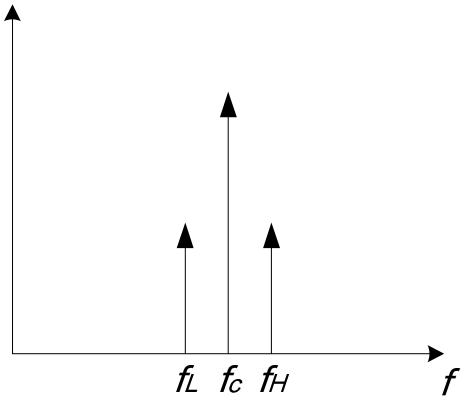

Figure 2.16 Spectrum of Clock Signal with Jitter

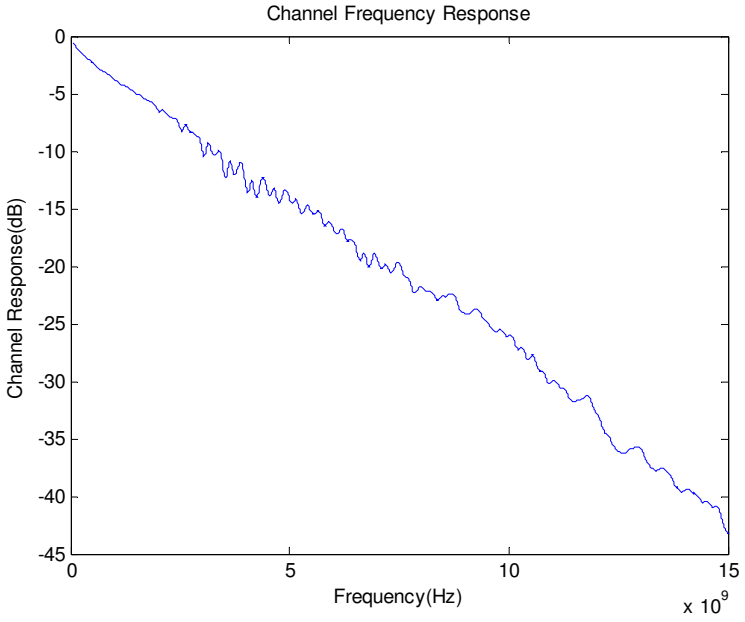

Figure 2.17 Channel Frequency Response

Equating equation (2.21) and (2.23), it can be approximated that

$$A_r \approx \alpha_c A, \tag{2.24}$$

$$\beta_r \approx \left(\frac{\alpha_L + \alpha_H}{2\alpha_c}\right)\beta. \tag{2.25}$$

Equation (2.25) is established for small f_m such that $\alpha_L \approx \alpha_c \approx \alpha_H$. The clock jitter transfer function (JIF) of the low-pass channel can be expressed as

$$JTF_{CH}(j\omega f) = \frac{\beta_r}{\beta}(j\omega f) = \frac{|H(j\omega(f_c - f))| + |H(j\omega(f_c + f))|}{2|H(j\omega f_c)|}, \tag{2.26}$$

where H is the channel frequency response and f is the frequency offset from f_c, and the jitter frequency. If the channel response has a strong frequency roll-off near clock frequency [13], for instance,

$$H(j\omega f) \approx e^{-\gamma f} \; for \; f \approx f_c, \tag{2.27}$$

then,

$$JTF_{CH}(j\omega f) = \frac{e^{-\gamma(f_c - f)} + e^{-\gamma(f_c + f)}}{2e^{-\gamma f_c}} = \frac{e^{-\gamma f} + e^{\gamma f}}{2} = cos\, h(\gamma f). \tag{2.28}$$

Therefore, jitter will get amplified at all frequency offsets by the low-pass channel. To justify this deduction, equation (2.28) can be applied on the channel frequency response as shown in Figure 2.18. The input clock frequency is 5 GHz. It can be found that the jitter amplification factor of low-pass channel increases as the jitter frequency becomes higher.

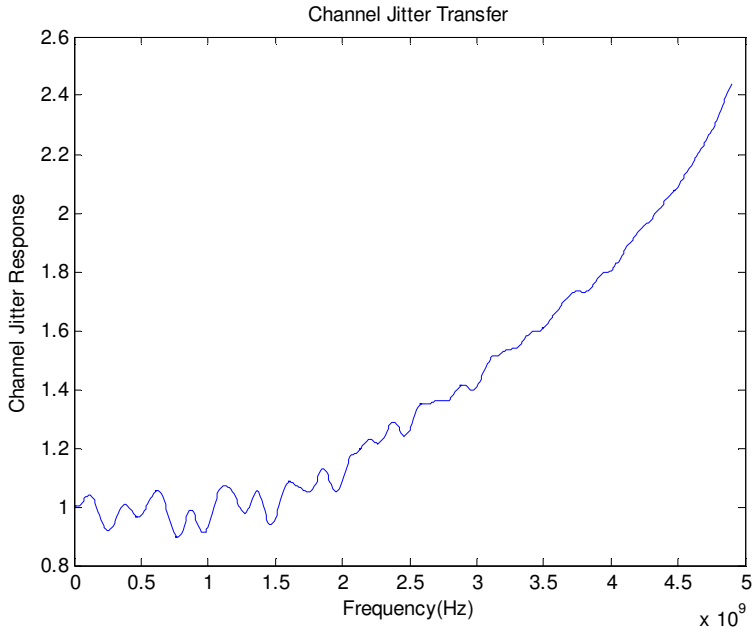

Figure 2.18 Channel Jitter Transfer Based on Equation 2.28

In section 2.2.2, jitter transfer and jitter impulse response method has been introduced. This method can be applied to analyze the effect of a low-pass channel on transmitted jitter as well. The normalized jitter impulse response associated with frequency response in Figure 2.17 is extracted as shown in Figure 2.19. Jitter transfer is generated by applying FFT on the jitter impulse response in Figure 2.20, which is given in Figure 2.20. The jitter transfer demonstrates that jitter gets amplified at higher frequency as well. In addition, it exhibits similar characteristics as the jitter amplification factor generated according to (2.28).

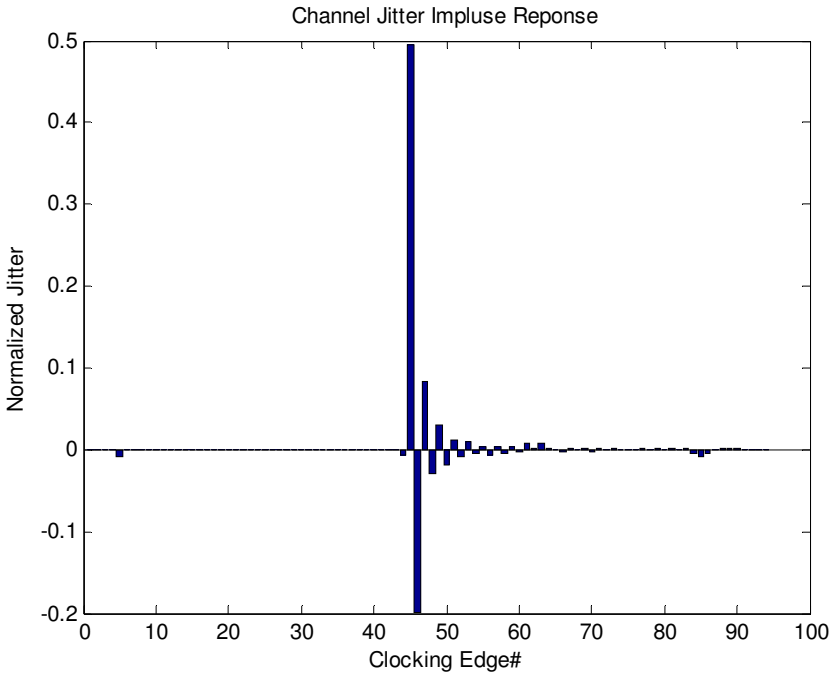

Figure 2.19 Jitter Impulse Response of B12 Channel

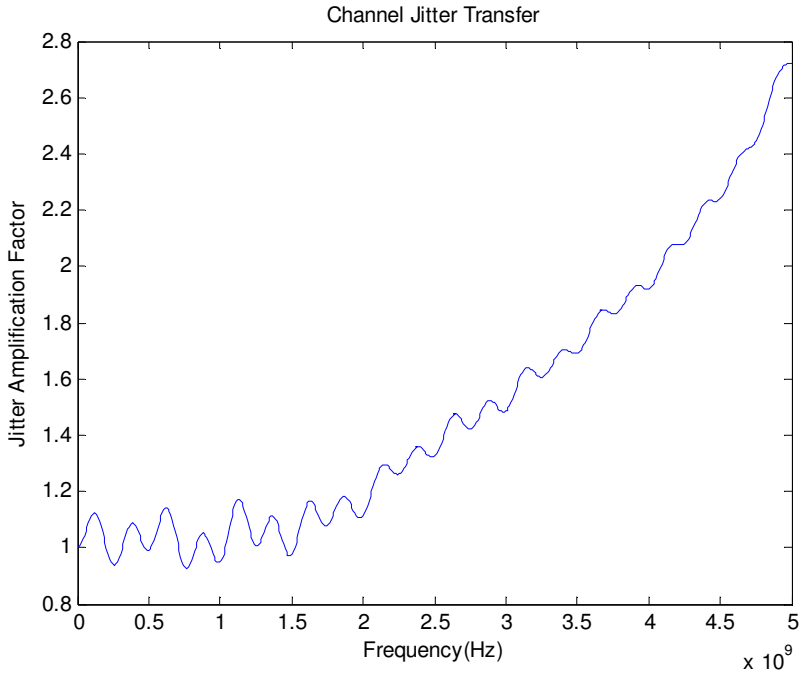

Figure 2.20 Jitter Transfer Function of B12 Channel

2.4 Jitter Tracking in Forwarded-clock System

This section introduces the concept of jitter tracking in a forwarded-clock system and the practical problem inherent in a forwarded-clock architecture, which is clock to data skew. In addition, a method to quantify jitter tracking is presented, followed by the impact of clock to data skew on jitter tracking.

2.4.1 Definitions

Jitter Tracking

As mentioned in section 2.1.2, the equivalent design of clock and data TX circuits creates correlation between clock and data jitter. In this way, the variation of sampling clock phase can always follow the variation of data transition time, indicating that the clock is able to sample the data optimally. It is also a process called jitter tracking.

Clock-to-data Skew

In practice, the latencies of the data and clock paths are not identical due to the mismatch between data and clock channels, strength of drivers and loadings. Thus, the clock and data signals fail to reach the receiver at the same time, which is called clock to data skew. The typical skew value for high speed forwarded clock system is 5 to 10 UI.

Differential Jitter

A data jitter sequence is given by

$$J_D = J_P sin\left(2\pi f_j UI \cdot n\right), \tag{2.29}$$

J_P is the peak value of jitter, UI is the bit period of data and f_j is the jitter frequency. The clock jitter is expressed as

$$J_C = J_P sin\left(2\pi f_j UI \cdot n\right), \tag{2.30}$$

which is the same as data jitter if perfect data and jitter tracking is assumed. If the clock and data paths suffer from skew of mUI. The clock jitter sequence becomes

$$J_C = J_P sin\left(2\pi f_j UI(n+m)\right). \tag{2.31}$$

The differential jitter is given by

$$J_{diff} = J_D - J_C. \tag{2.32}$$

If no clock-to-data skew exist, $J_D = J_C$ and $J_{diff} = 0$, which means the system provides ideal data and clock jitter tracking. An example of differential jitter is shown in Figure 2.21. The frequency of both clock and data jitter is 100MHz and 0.3UI jitter amplitude is assumed. The latency mismatch between clock and data is 5UI, where UI = 100ps for 10Gb/s data link system.

Jitter Tracking Bandwidth (JTB)

JTB descripts how fast the phase variation can be tracked by the system. In forwarded-clock system, the JTB can be defined as how fast the variation of received data transition phase can be tracked by the phase of received sampling clock.

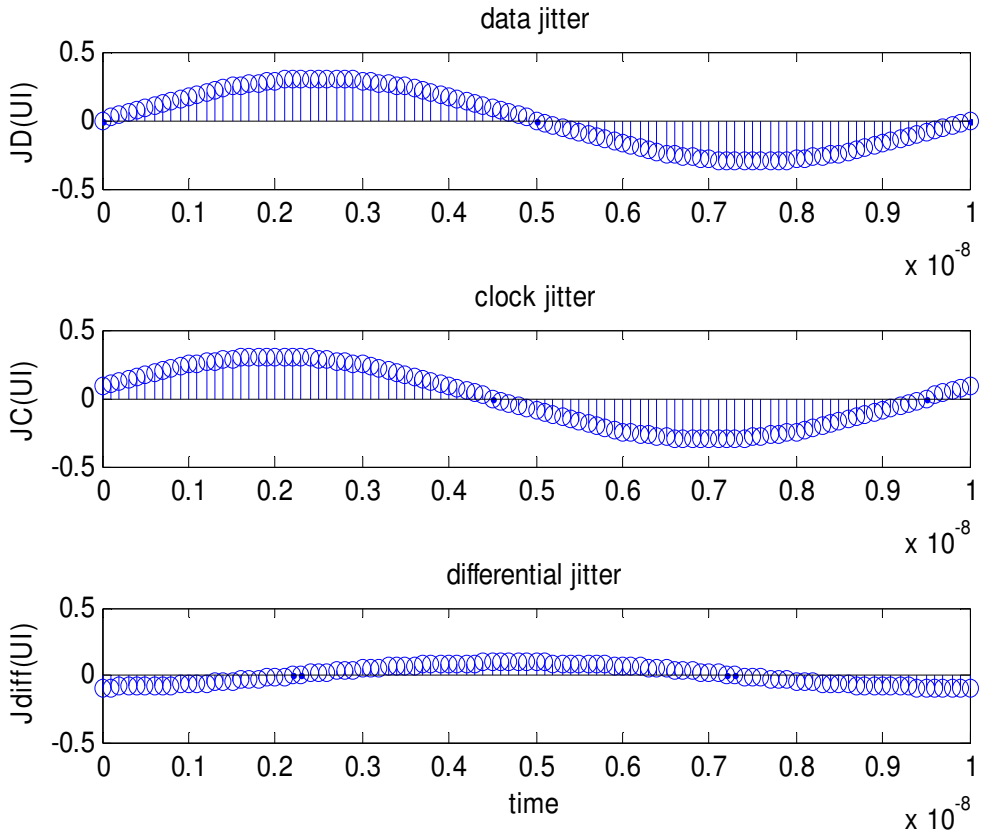

Figure 2.21 Example of 100MHz Differential Jitter with 5UI Clock-to-Data Skew

2.4.2 Impact of Clock Skew on a Forwarded-clock System

Based on the example in Figure 2.21, 200MHz and 400MHz jitter is applied as well. The resultant differential jitter sequences are shown in Figure 2.22. It is shown that the higher the jitter frequency, the larger the differential jitter amplitude. It is because for higher frequency jitter, certain clock-to-data skew produces larger phase difference between clock, resulting in larger differential jitter between data and clock. In order words, the offset between sampling clock phase and data center goes up and the bit error rate will be increases.

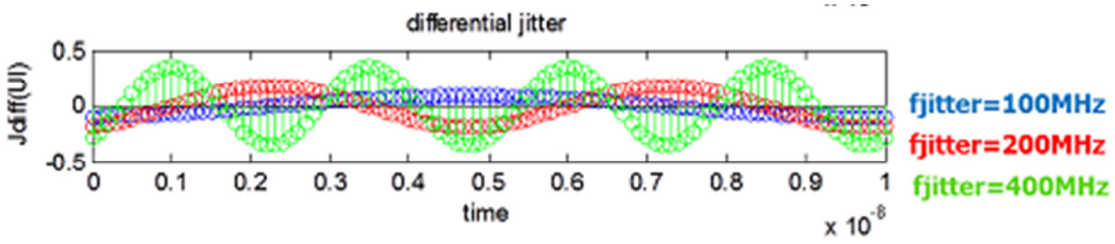

Figure 2.22 Differential Jitter Sequences of Clock and Data Jitter Frequencies of 100MHz, 200MHz and 400MHz

Normalized differential jitter can be defined as normalizing the differential jitter to either data or clock jitter according to

$$J_{NOR} = \frac{\sum_{N}^{i=1} J_{diff,i}^2}{\sum_{N}^{i=1} J_{D,i}^2}. \tag{2.33}$$

Figure 2.23 illustrates the behavior of normalized differential jitter as jitter frequency varies from low to high with clock-to-data skew over 1 to 5 UI, assuming that clock jitter tracks the data jitter over all frequency. It is clear that a larger offset between clock and data paths increases the differential jitter at lower jitter frequencies. All frequency jitter tracking is not desired if clock skew exists.

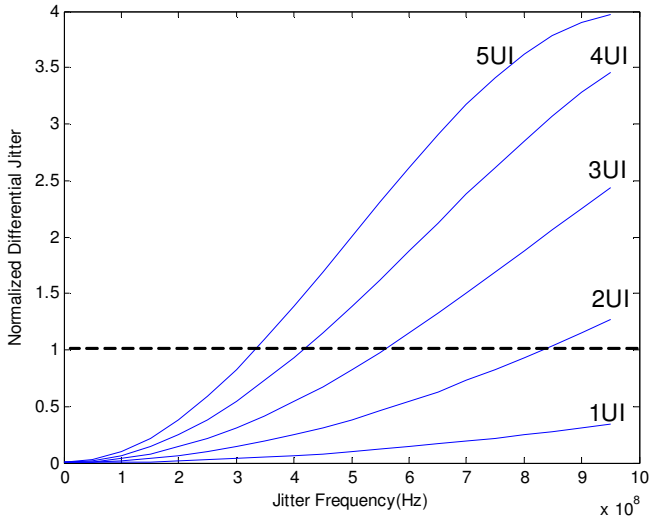

Figure 2.23 Normalized Differential Jitter with Clock-to-Data Skew over 1 to 5 UI

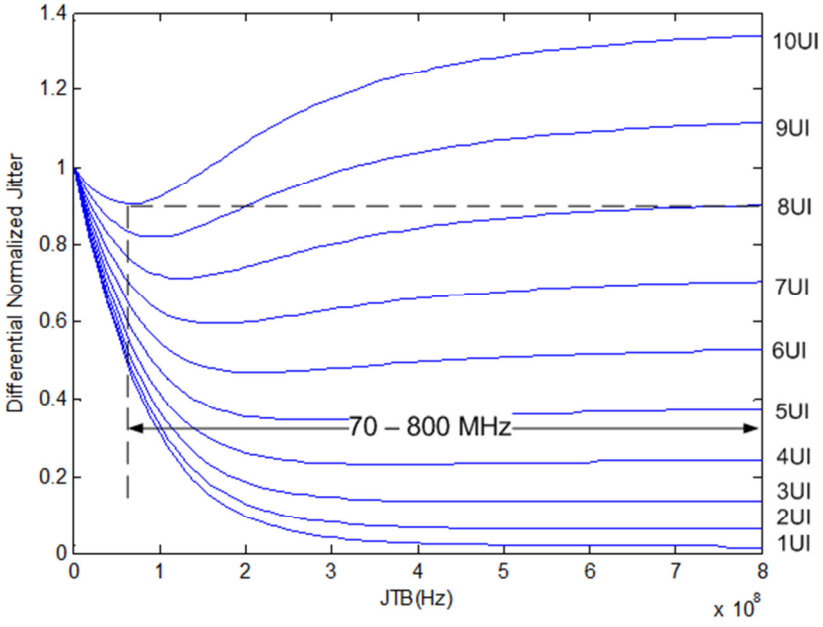

Figure 2.24 Normalized Differential Jitter for 200MHz Jitter Frequency and JTB from 0 to 800MHz

The JTB in a forwarded-clock system can be limited by attenuating the clock jitter amplitude using the amplitude response of a low-pass function with the bandwidth of JTB, as given by

$$J_C = J_P' sin\left(2\pi f_j UI(n+m)\right), \tag{2.34}$$

where

$$J_P' = J_P \left| \frac{1}{1+\frac{jf_j}{JTB}} \right|. \tag{2.35}$$

For 200MHz jitter frequency, JTB affects the differential jitter as shown in Figure 2.24. For different amounts of clock-to-data skews, there is an optimum JTB which yields the minimum differential jitter. The objective of jitter tracking optimization is to minimize the differential jitter between clock and data. Thus, the JTB must be controllable to compensate the effect of different amounts of skews. From Figure 2.24, the jitter tracking optimization for clock-to-data skews over 1 to 10 UI requires an adjustable JTB over 70 to 800MHz.

CHAPTER III

JITTER TRACKING OPTIMIZATION USING BANDPASS FORWARDED CLOCK FILTERING

This chapter focuses on a jitter tracking optimization method using bandpass forwarded clock filtering. It begins with the fundamentals of bandpass filtering. Next, the jitter transfer function of bandpass filtering is discussed. Finally, the requirements of a proposed implementation of a bandpass filter that has the capability for jitter tracking bandwidth optimization is presented.

3.1 Basic of Bandpass Filtering

The objective of bandpass filtering is to pass the desired signal within a certain frequency range while rejecting the un-wanted signal out of that range. An ideal bandpass filter would have unity gain at passband and infinite attenuation out of the passband. In addition, the transitions at upper and lower cut-off frequencies should be instantaneous. The solid line in Figure 3.1 displays the transfer function of an ideal bandpass filter, where f_L and f_H represent the lower and upper cut-off frequencies, respectively. In reality, bandpass filters are not ideal. They cannot reject the signal outside the passband completely. The slope of the transition between passband and stop-band is finite, like the dash lines in Figure 3.1. The cut-off frequencies are the frequencies at which the gains are 3dB lower than the passband gain. In the real case, the passband gain of a bandpass filter is not necessary unity, especially in the design of

active filter. Certain gain at passband is required to prevent the desensitizing effect of device noise.

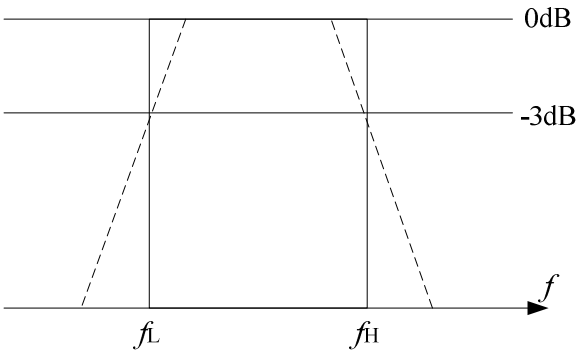

Figure 3.1 Bandpass Transfer Function

3.2 Bandpass Filtering Effect on Jitter

In last chapter, the frequency domain analysis method is applied to analyze the jitter amplification effect of low pass channel. This method can be applied to understand how bandpass filtering impacts clock jitter as well. The time domain and frequency domain expressions of a jittery clock signal are given by

$$c(t) = Acos(2\pi f_c t + \beta sin 2\pi f_m t) \tag{3.1}$$

and

$$S(f) = \frac{\alpha_c A}{2}\delta(f - f_c) - \frac{\beta A}{4}[\alpha_L \delta(f - f_L) - \alpha_H \delta(f - f_H)], \tag{3.2}$$

respectively. In Figure 3.2, (a) shows the frequency components of clock while (b) displays the transfer characteristic of a bandpass system that centers at the clock frequency.

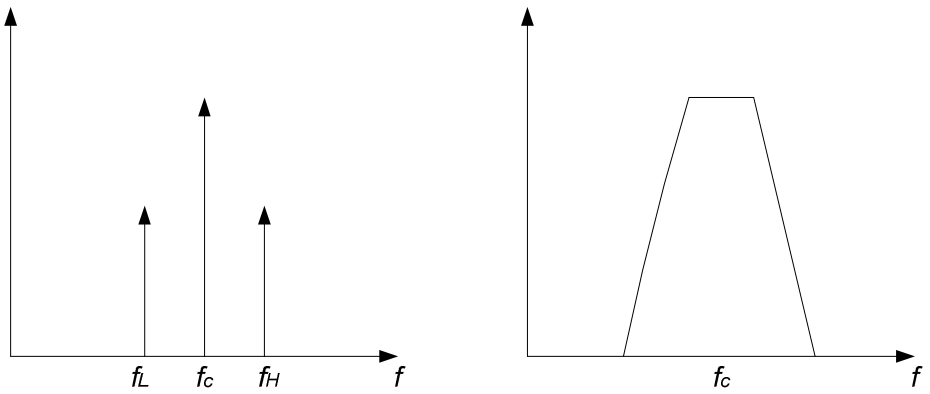

Figure 3.2 (a) Jittery Clock Spectrum (b) Bandpass Transfer Function Centering at Clock Frequency

The bandpass filtering process of clock signal is graphically shown in Figure 3.3, resulting in a frequency modulated clock with lower side bands. The frequency domain expression of the received clock signal can be written as,

$$S(f) = \frac{A_r}{2}\delta(f - f_c) - \frac{\beta_r A_r}{4}[\delta(f - f_L) - \delta(f - f_H)], \tag{3.3}$$

, and

$$\mathrm{A_r} \approx \alpha_c \mathrm{A} \tag{3.4}$$

$$\beta_r \approx \left(\frac{\alpha_L + \alpha_H}{2\alpha_c}\right)\beta, \tag{3.5}$$

where α_c, $\alpha_L$and α_H are the gain of the bandpass function at frequencies of f_c, f_L and f_H, respectively. For typical bandpass filtering,

$$\alpha_c \geq 1 \tag{3.6}$$

$$\alpha_L = \alpha_H < \alpha_c. \tag{3.7}$$

Thus, it is always the case that $\beta_r < \beta$, that is, the jitter of the transmitted clock is filtered by bandpass filtering. Since that the bandpass function is symmetrical and center

at f_c, the transfer function can be approximated as a low-pass function with respect to the frequency offset from f_c,

$$\left|H\left(j2\pi(f_c - f)\right)\right| = \left|H\left(j2\pi(f_c + f)\right)\right| = \frac{|H(j2\pi f_c)|}{|1 + \frac{jf}{f_p}|}, \tag{3.8}$$

where f is the offset frequency from f_c while f_p is the pole frequency and the low-pass function here is assume as first order. If the bandwidth of the bandpass function is BW_{3dB}, then $f_p = (1/2)BW_{3dB}$. The JTF of bandpass filtering is given by

$$JTF_{BP}(j2\pi f) = \frac{|H\left(j2\pi(f_c - f)\right)| + |H\left(j2\pi(f_c + f)\right)|}{2|H(j2\pi f_c)|} = |\frac{1}{1 + \frac{jf}{f_p}}|. \tag{3.9}$$

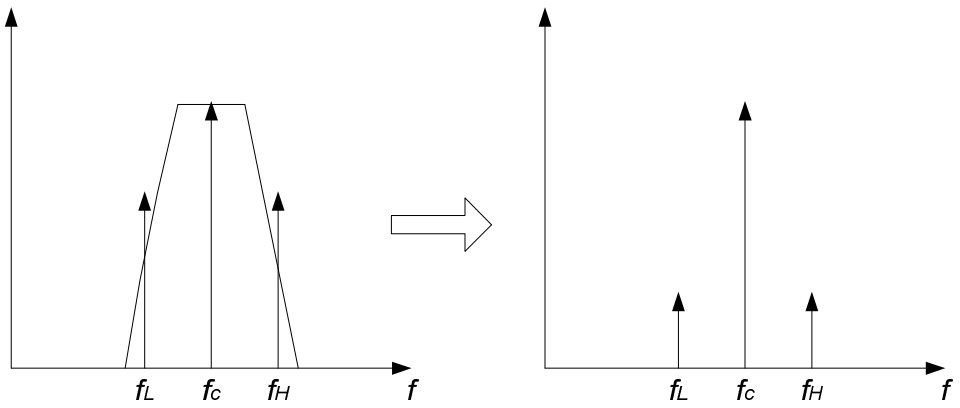

Figure 3.3 Clock Spectrum after Bandpass Filtering

It is very interesting to found that the higher the Q of bandpass filtering, the lower the bandwidth, resulting in higher jitter filtering. This statement is proved graphically in Figure 3.4. To further verify the discussion above, the jitter impulse response method is employed to generate the jitter transfer of bandpass filtering as well.

Figure 3.5 is the extracted discrete time jitter impulse response of a bandpass system. The correspondent jitter transfer is shown in Figure 3.6.

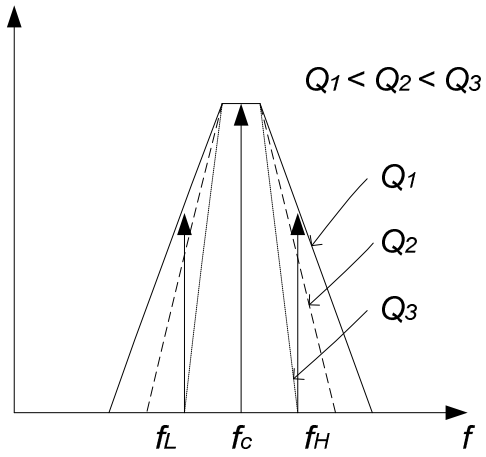

Figure 3.4 Variation of Bandpass Shape for Different Q Values

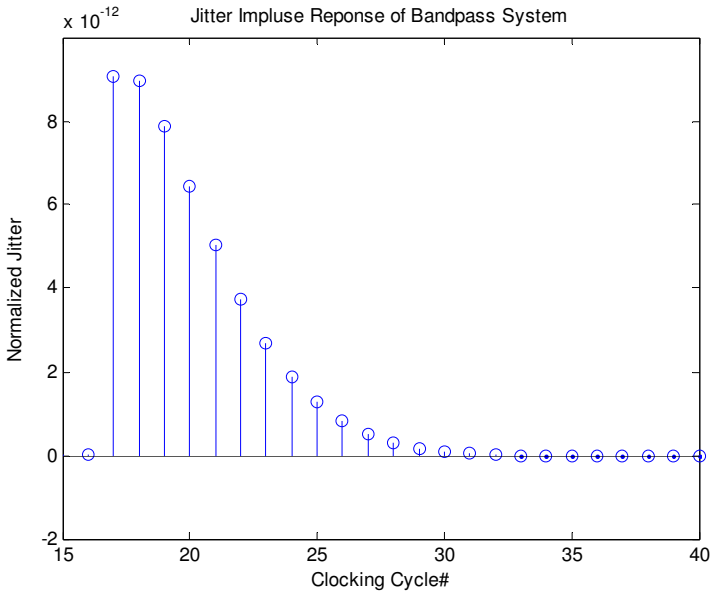

Figure 3.5 Jitter Impulse Response Sequence of Bandpass System

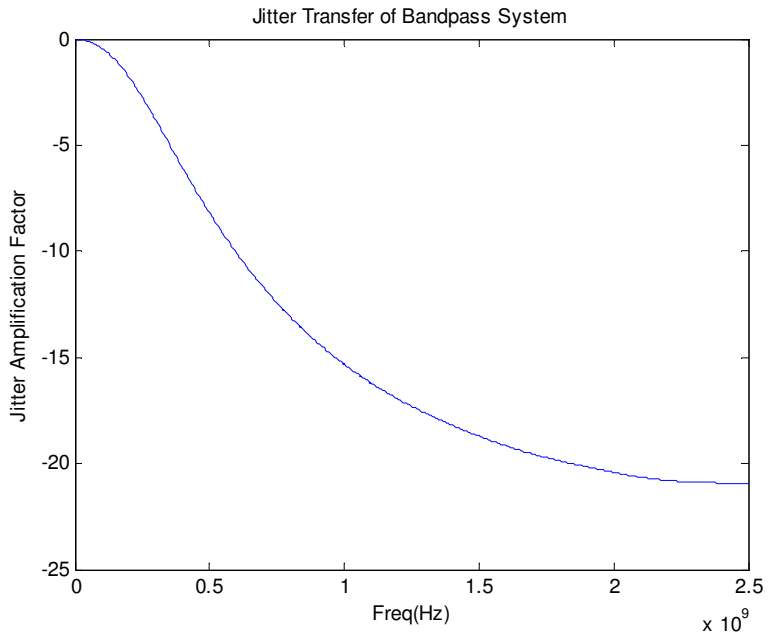

Figure 3.6 Jitter Transfer Function of Bandpass System

It is also valuable to analysis the jitter transfers of bandpass systems with different Q through extracting the jitter impulse response of each system. Figure 3.7 displays the jitter transfers of bandpass systems with Q from 3 to 30. It is clear higher Q of the bandpass filtering results in more attenuation of transmitted jitter at higher frequency and thus lower jitter tracking bandwidth (JTB).

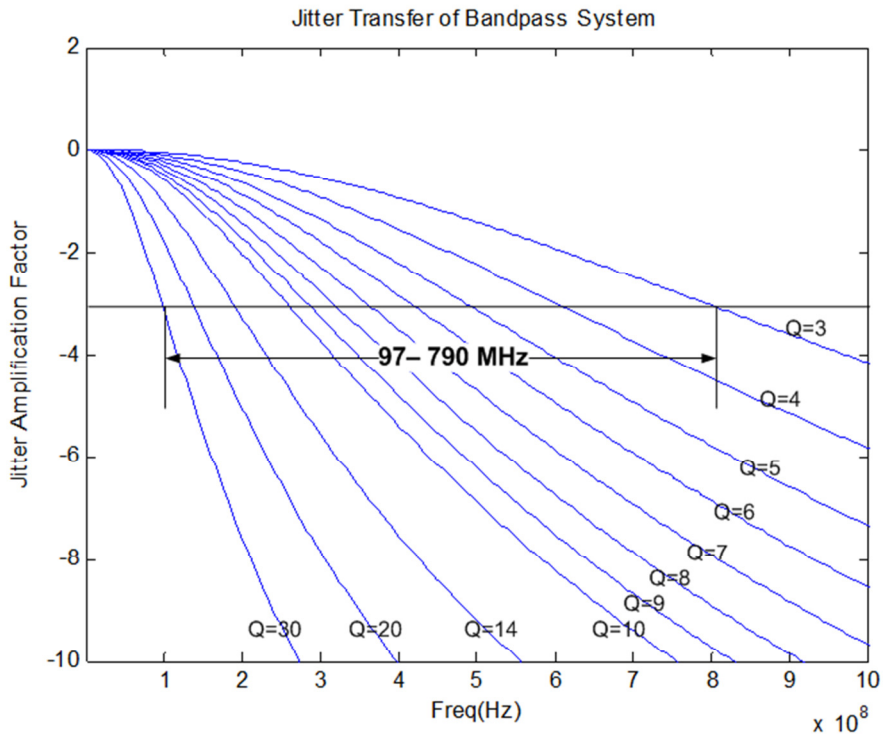

Figure 3.7 Jitter Transfer Functions of Bandpass Systems with Q over 3 – 30

3.3 Jitter Tracking Optimization by Bandpass Filtering

It is introduced in last chapter that the JTB of forwarded-clock system can be controlled by limiting the clock jitter amplitude using the low-pass function. In this chapter, the low-pass jitter transfer characteristic provided by bandpass system is introduced. The JTB is the bandwidth of clock jitter transfer function. In order to minimize the differential jitter amplitude when clock-to-data skew exists, the JTB must be controllable over wide frequency range. From Figure 3.7, a bandpass filter has controllable Q range over 3 to 30 provides JTB range over 97 – 790MHz. Based on Figure 2.24, to compensate the clock-to-data skew as high as 10 UI, 70MHz JTB must be achievable, which means higher tunable Q is required. Therefore, the proposed

bandpass filter design requires high tunable Q range, providing wide enough controllable JTB.

CHAPTER IV

ACTIVE INDUCTOR-BASED

BANDPASS FILTER

Compared to passive LC filter, the bandpass filter using active inductor consumes much less die area and has a large tunable Q range, as proved in [15]. This chapter introduces the active inductor basics and transistor-level implementation of active inductor, followed by the design of proposed bandpasss filter. Besides, the designs of an on-chip voltage regulator and a output buffer are discussed in this chapter.

4.1 Gyrator Basics

4.1.1 Basic Gyrator Operation

An ideal gyrator is a two-port network that converts the voltage (or current) on one port to the current (or voltage) on the other and vice visa. As shown in Figure 4.1, the voltage on port 1 is converted to current flowing into port 2 with transconductance gain of gm, while the voltage on port 2 is converted to current flowing into port 1 with the identical transconductance gain with a minus sign. The currents and voltages associated with port 1 and port 2 is related as:

$$i_2 = g_m v_1$$

$$i_1 = -g_m v_2.$$

If port 2 is loaded with a resistor of R, then the current-voltage characteristic associated with port 2 is regulated by R as:

$$i_2 = -\frac{v_2}{R}.$$

Therefore, the voltage-current characteristic associated with port 1 is given by

$$\frac{v_1}{i_1} = \frac{1}{g_m^2}\frac{1}{R} = \frac{1}{g_m^2}\left(-\frac{i_2}{v_2}\right). \tag{4.1}$$

Based on the derivation above, the gyrator inverts the current-voltage characteristic on one port and presents the inverted characteristic on the other port, which is an important property of the gyrator network. For instance, the resistance on port 2 behaves conductively on port 1 according to the equation above. Similarly, gyrator can make the capacitive circuit behave inductively, which is the basic idea of synthesizing an inductor using capacitive-loaded gyrator.

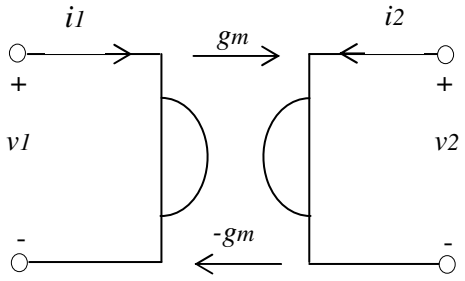

Figure 4.1 Gyrator Network

4.1.2 Gyrator-C Inductor

An ideal gyrator loaded with capacitor at one port can be modeled as shown in the Figure 4.2. The feed-forward GM stage with a minus sign converts the voltage at port 1 to the current charging the capacitor at port 2. The current flowing into port 1 is controlled by the voltage at port 2 through the feedback GM stage once *v2* is charged up. The voltage-current characteristic associated with port 1 can be derived using both time domain and frequency domain equations, as follow:

Time domain:

$$i_2 = g_m v_1 = C\frac{dv_2}{dt}$$

$$i_1 = g_m v_2$$

$$\therefore \mathrm{v_1} = \frac{\mathrm{C}}{\mathrm{g_m^2}}\frac{\mathrm{di_1}}{\mathrm{dt}} \tag{4.10}$$

Frequency domain:

$$i_2 = g_m v_1$$

$$i_1 = g_m v_2$$

$$v_2 = i_2 \cdot sC$$

$$\therefore \frac{v_1}{i_1} = \frac{sC}{g_m^2}. \tag{4.11}$$

From equations 4.10 and 4.11, port 1 exhibits a synthesized inductor of $\frac{C}{g_m^2}$.

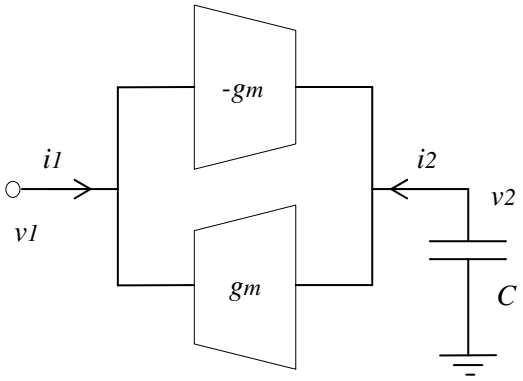

Figure 4.2 Block Diagram of Capacitive-Load Gyrator

Consider the finite output impedance (r_{o1}) of the GM stage from port 1 to 2 (GM1) and the mismatch of transconductances (gm), a realistic model of gyrator-C

inductor is shown in Figure 4.3. The equivalent input impedance of the gyrator-C network is given as

$$Z(s) = \frac{sC + \frac{1}{r_{o1}}}{g_{m1}g_{m2}} = sL_{eq} + R_{eq}, \tag{4.12}$$

where

$$L_{eq} = \frac{C}{g_{m1}g_{m2}} \tag{4.13}$$

$$R_{eq} = \frac{1}{g_{m1}g_{m2}} \cdot \frac{1}{r_{o1}}. \tag{4.14}$$

It can be found that finite output impedance of the GM stage results in an equivalent resistor in series with the synthesized inductor and degrades the quality factor of the inductor. Recall the property that the gyrator inverts the current-voltage characteristic on one port and presents the inverted characteristic on the other port, it can be explained intuitively that parallel combination of loaded capacitor and output impedance of stage GM1 behaves as series combination of their inverted quantities multiplied by a coefficient at the other port, where the coefficient is the inversion of the product of the two transconductance gains.

Therefore, the higher the output impedance of the transconductance stage, the lower the equivalent series resistor and the active inductor approaches the ideal inductor. Higher transconductance gain helps to reduce the series resistor value but probably consumes more power.

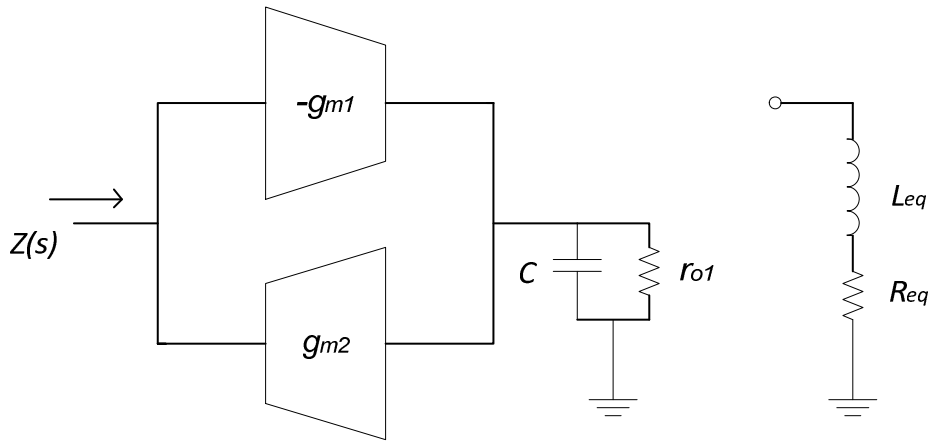

Figure 4.3 Realistic Model of Capacitive-Loaded Gyrator

4.1.3 Active Resonator Based on Gyrator-C Inductor

Figure 4.4 shows an LC resonator, where the inductor is synthesized by the capacitive-loaded gyrator network discussed in the last section. The parallel resistor dissipates the energy and cause loss of LC resonator. In passive resonator, this term is dominated by the series resistor of the real inductor. In active resonator, this term is contributed by the finite output impedance of the forwarded transconductance stage (GM1), which produces the equivalent resistor of synthesized inductor, and the finite output impedance of the feedback transconductance stage (GM2) that is in parallel with LC network.

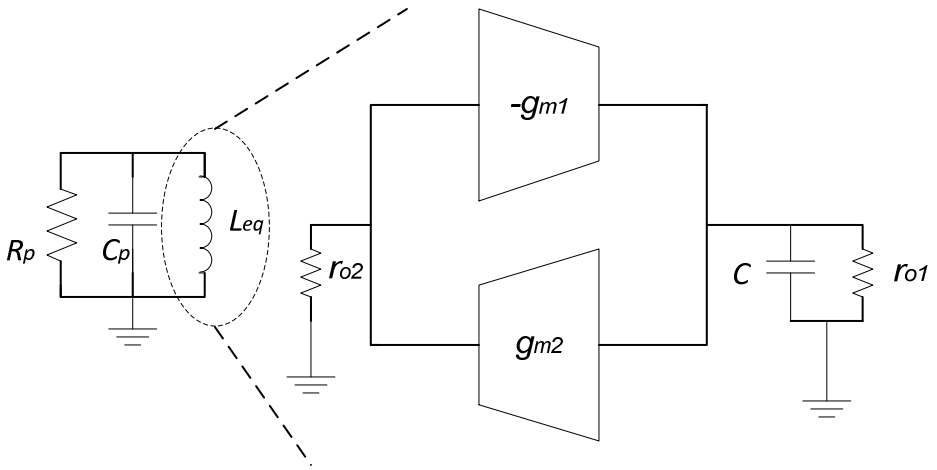

Figure 4.4 Active-Inductor Based LC Resonator

In active resonator, R_p can be defined as

$$R_p = R_{p,ro1} \| r_{o2}, \tag{4.15}$$

where $R_{p,ro1}$is the equivalent dissipating resistor due to $r_{o1}$and given by (4.14), while r_{o2} is the output impedance of stage GM2.

$$R_{p,ro1} = R_{eq}(Q^2 + 1) \tag{4.16}$$

$$L_p = L_{eq}\left(\frac{Q^2 + 1}{Q^2}\right), \tag{4.17}$$

,where

$$Q = \frac{\omega_o L_{eq}}{R_{eq}} = \frac{R_p}{\omega_0 L_p}, \tag{4.18}$$

where ω_o is the resonant frequency and given by

$$\omega_0 = \frac{1}{\sqrt{L_p C_p}}. \tag{4.19}$$

The equations above are derived to match the parameters of active resonator to its passive counterpart and provides with intuitive understanding. A more explicit

configuration of active resonator is shown in Figure 4.5, which is more straightforward to give the resonator impedance with respect to frequency. Assume that $g_{o1} = 1/r_{o1}$ and $g_{o2} = 1/r_{o2}$, the resonator impedance is given by

$$Z_{in}(s) = \left(\frac{1}{sC_p + g_{o2}}\right) \Big\| \left(\frac{sC_L + g_{o1}}{g_{m1}g_{m2}}\right) \tag{4.20}$$

$$= \frac{\frac{1}{C_p}(s + \frac{g_{o1}}{C_L})}{s^2 + s\left(\frac{g_{o1}}{C_L} + \frac{g_{o2}}{C_p}\right) + \frac{g_{m1}g_{m2} + g_{o1}g_{o2}}{C_L C_p}}. \tag{4.21}$$

The denominator of a second order function is

$$s^2 + s\frac{\omega_0}{Q} + \omega_0^2. \tag{4.22}$$

Thus,

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2} + g_{o1}g_{o2}}{C_L C_p}}, \tag{4.23}$$

and

$$Q = \frac{\sqrt{\frac{g_{m1}g_{m2} + g_{o1}g_{o2}}{C_L C_p}}}{\frac{g_{o1}}{C_L} + \frac{g_{o2}}{C_p}}. \tag{4.24}$$

From (4.23), if g_{o1}, g_{o2} are zero then Q becomes infinite and the resonator is ideal with

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{L_p C_p}}, \tag{4.25}$$

and

$$L_p = \frac{C_L}{g_{m1}g_{m2}}. \tag{4.26}$$

The inductor value is depended on loaded capacitor value and transcondcutance gains of GM stages only.

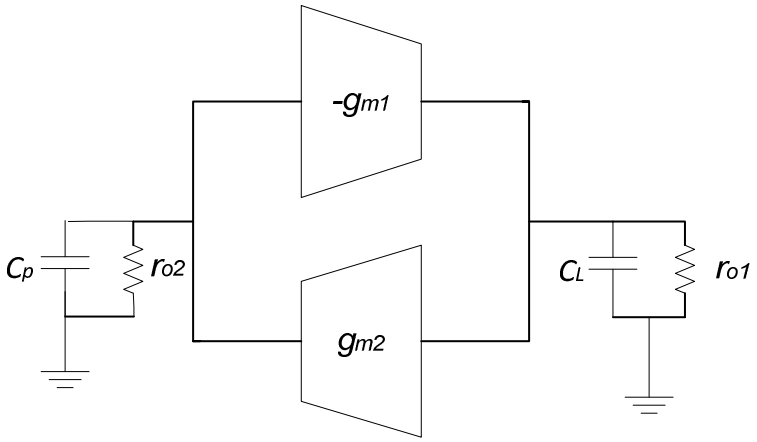

Figure 4.5 Realistic Model of Active Inductor

4.1.4 Noise Analysis

The noise analysis of active resonator has been introduced by A.A. Abidi in [16]. The noise model of active resonator in is shown in Figure 4.6. v_{n1} and v_{n2} are the input referred noise voltage of stages GM1 and GM2, respectively.

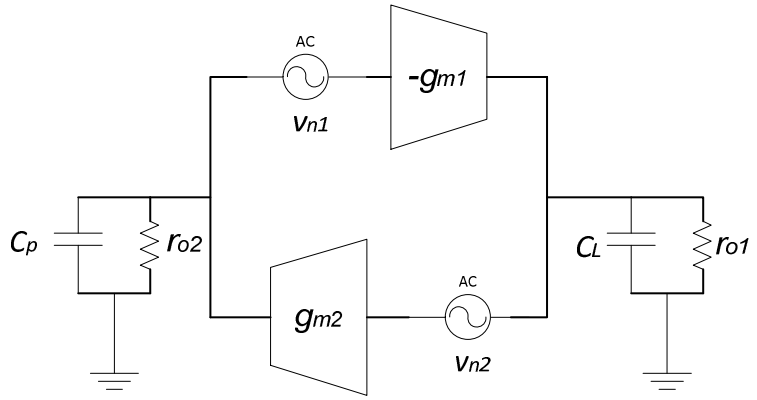

Figure 4.6 Noise Model of Active Resonator

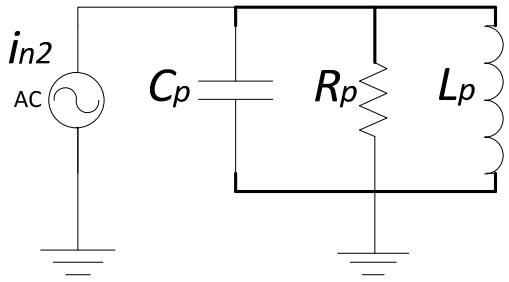

Figure 4.7 Noise Analysis Model for Stage GM2

The noise contributions of GM1 and GM2 are invested independently. The total noise is the superposition of the effect of both sources. The impact of v_{n2} on the resonator is analyzed first and the equivalent noise model using equivalent parallel inductor and resistance is shown in Figure 4.7. i_{n2} is the shunt equivalent noise current and

$$i_{n2} = g_{m2} v_{n2}. \tag{4.27}$$

The expressions of R_p and L_p have been given by equations (4.15) and (4.25), respectively. At resonant frequency, the noise current is fully applied on the parallel resistor. The resonator noise density is given by

$$v_{n,gm2}^2 = i_{n2}^2 R_p^2 = 4kT\gamma g_{m2} R_p^2. \tag{4.28}$$

The noise contribution of g_{m1} can be model as its input referred noise voltage source in series with the synthesized inductor. The parallel RL combination can be transferred to a series RL combination with the same Q in the equivalent RLC network as shown in Figure 4.8 (a) and (b). (c) shows the noise model associated with GM1. Consider the

voltage amplification effect of series RLC network, the noise voltage across C_p due to $v_{n1}$is Q times of v_{n1}, the noise density is given by

$$v_{n,gm1}^2 = Q^2 v_{n1}^2 = Q^2 \frac{4kT\gamma}{g_{m1}}. \tag{4.29}$$

Since that v_{n1} and v_{n2} are two independent noise sources, the total noise density is

$$v_n^2 = 4kT\gamma g_{m2} R_p^2 + \frac{4kT\gamma}{g_{m1}} Q^2 \tag{4.30}$$

From equation (4.23), $g_{m1}g_{m2} \gg g_{o1}g_{o2}$ in most cases,

$$\omega_0 \approx \sqrt{\frac{g_{m1}g_{m2}}{C_L C_p}}. \tag{4.31}$$

Take (4.31) into (4.30),

$$v_n^2 = \frac{4kT\gamma}{g_{m1}} Q^2 \left(1 + \frac{C_L}{C_p}\right).$$

Assume that the noise bandwidth is equal to the 3dB bandwidth of the resonator, ω_0/Q, the average noise voltage is given as

$$\overline{v_n^2} = v_n^2 \frac{\omega_0}{Q} = \frac{4kT\gamma}{g_{m1}} \omega_0 Q \left(1 + \frac{C_L}{C_p}\right). \tag{4.32}$$

Take (4.31) into (4.32), then

$$\overline{v_n^2} = \frac{4kT\gamma}{C_p} \sqrt{\frac{g_{m2}}{g_{m1}}} Q \left(\sqrt{\frac{C_p}{C_L}} + \sqrt{\frac{C_L}{C_p}}\right). \tag{4.33}$$

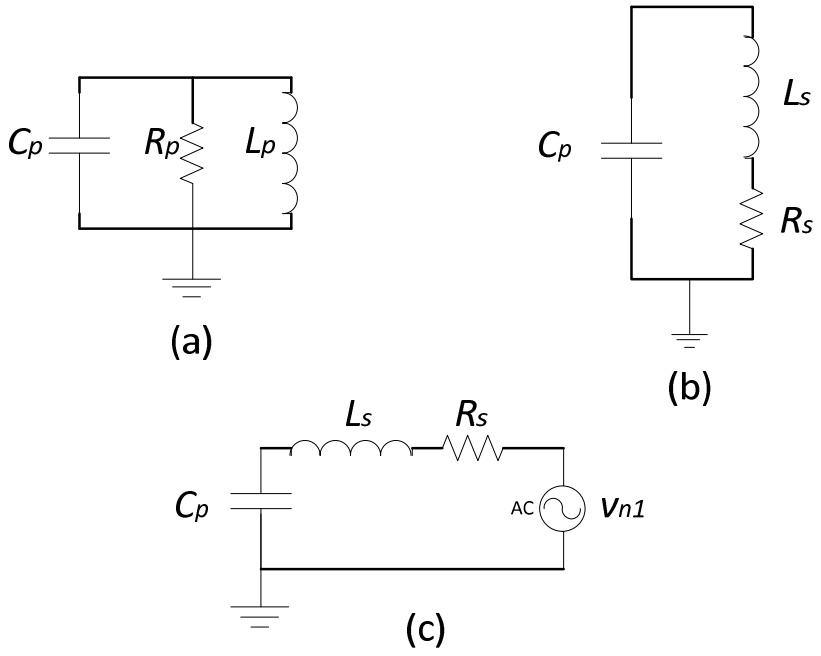

Figure 4.8 Noise Analysis Model for Stage GM1

4.2 Transistor-Level Implementation of Active Inductor

4.2.1 Xiao's Active Inductor Implementation

Figure 4.9 shows an active inductor implementation in transistor proposed in [15]. The signal path from node 2 to 1 consists of a source flower provided by M1, followed by a common gate stage of M3. They share the same current source M6. There is no signal inversion through this path. The path from node 1 to 2 is an active loaded common source stage M2 and thus it provides signal inversion, while M5 is the current source basing M3. Node 1 is loaded by a capacitor C_1 Therefore, V_2 controls the current charging C_1, resulting in V_1, which feedback controls the current sunk by M2. The equivalent impedance of the topology is

$$L_{eq} = \frac{C_1}{0.5 g_{m1} g_{m2}}, \tag{4.34}$$

the 0.5 coefficient is because the impedance looking at the source of M3 degenerates M1 and $g_{m1} = g_{m3}$.

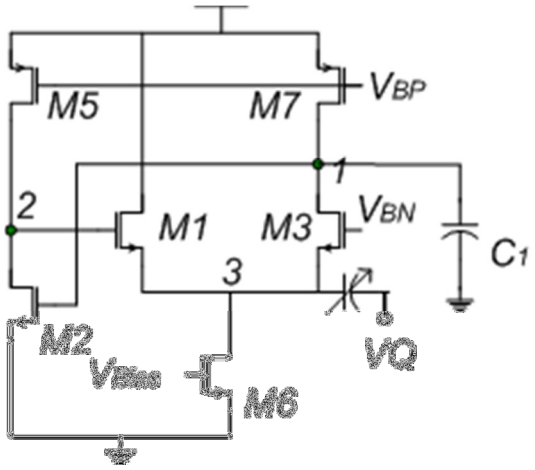

Figure 4.9 Xiao's Active Inductor Topology

The voltage headroom at node 2 is given by

$$VDSAT_6 + VTH_1 + VOV_1 < V_2 < VDD - VDSAT_5. \tag{4.35}$$

In IBM 90nm CMOS process, supply voltage is 1.2V while the threshold voltage of minimum length NFET is around 600mV, which constrains the voltage swing of this topology severely. The threshold voltage can be reduced by using larger length NFET. However, this way increases the parasitic capacitor at node 2 and reduces the resonant frequency.

4.2.2 Propose Active Inductor Implementation

To solve the voltage limitation problem discussed above, a low voltage active inductor topology is proposed and shown in Figure 4.10. The path from 2 to 1

experiences two signal inversion stages provided by M1 and M6, respectively. Thus this path serves as a GM stage without signal inversion. The path from 2 to 1 is a common source stage of M2, operating as a GM stage with signal inversion. Therefore, equivalent inductor and series resistor looking at node 2 are given by

$$L_{eq} = \frac{C_1}{g_{m1}g_{m2}} \tag{4.36}$$

$$r_{loss} = \frac{g_{05} + g_{06}}{g_{m1}g_{m2}}, \tag{4.37}$$

where C_1 is the capacitor loaded at node 1, while g_{05} and g_{06} are the conductances associated with the output impedances at node 1.

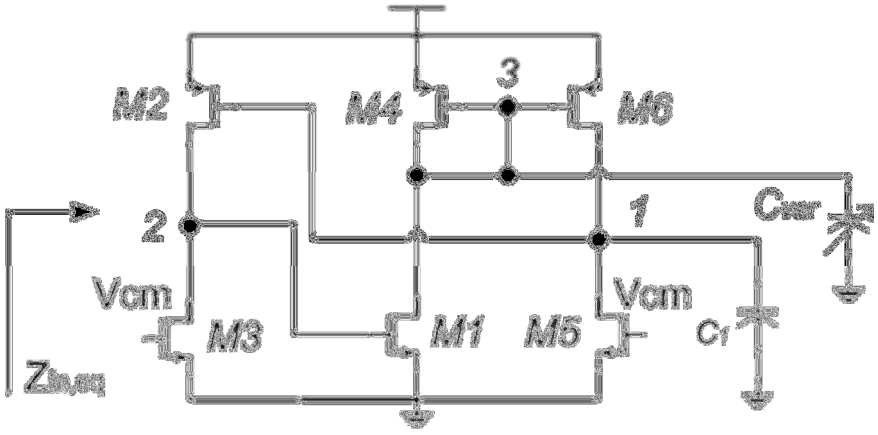

Figure 4.10 Low-Voltage Active Inductor

The voltage headroom at node 2 limited by

$$VTH_1 + VOV_1 < V_2 < VDD - VDSAT_2, \tag{4.38}$$

which is one VDSAT larger than that given by (4.35). It is easier to be implemented in low supply voltage and relatively high threshold voltage process compared to Xiao's topology

Consider the output impedance and parasitic capacitor associated with node 2, the small signal model of Figure 4.10 is shown in Figure 4.11, which is equivalent to a resonant network as shown in Figure 4.12. L_{eq} and r_{loss} is given by (4.36) and (4.37). The resonant frequency is

$$\omega_0 \approx \frac{1}{\sqrt{L_{eq}C_{P2}}} = \sqrt{\frac{g_{m1}g_{m2}}{C_1 C_{P2}}}. \tag{4.39}$$

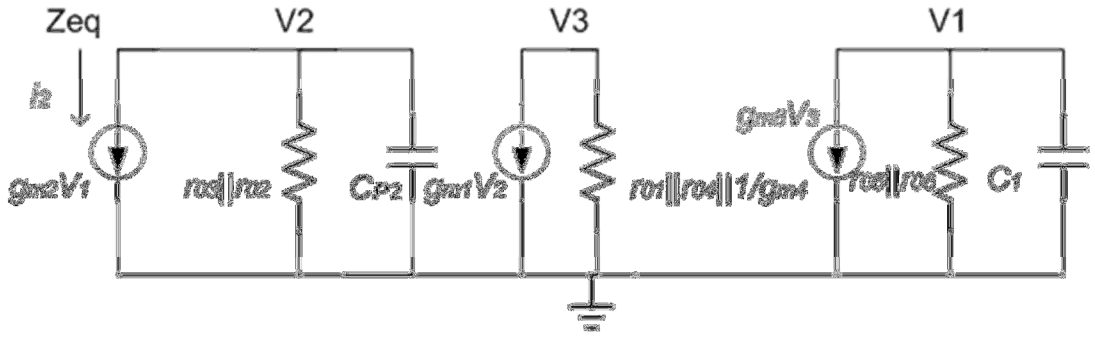

Figure 4.11 Small Signal Model of Proposed Active Inductor Topology

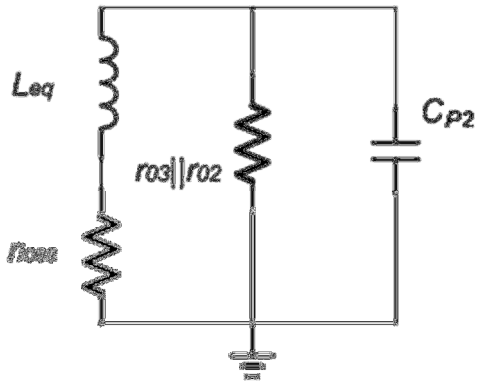

Figure 4.12 Equivalent RLC Circuit of Proposed Active Inductor Topology

In Figure 4.10, consider the effect of total capacitor associated with node 3, C_3. It creates an high frequency pole at node 3 and

$$\omega_{p3} = \frac{g_{m4} + 1/r_{01} + 1/r_{04}}{C_3} \approx \frac{g_{m4}}{C_3}. \tag{4.40}$$

Then

$$Z_{eq,2} = \frac{j\omega_0\left(C_1 + \frac{g_{05}+g_{06}}{\omega_{p3}}\right) + g_{05} + g_{06} - \omega_0^2\frac{C_1}{\omega_{p3}}}{g_{m1}g_{m2}}, \tag{4.41}$$

where ω_0 is the operating frequency. Because

$$\omega_{p3} \gg \frac{g_{05}+g_{06}}{C_1},$$

then,

$$L_{eq} \approx \frac{C_1}{g_{m1}g_{m2}}, \tag{4.42}$$

and

$$r_{loss} = \frac{1}{g_{m1}g_{m2}}\left(g_{05} + g_{06} - \omega_0^2\frac{C_1}{\omega_{p3}}\right). \tag{4.43}$$

Form (4.40) and (4.43), $r_{loss} = 0$ if

$$C_3 = \frac{g_{m4}(g_{05} + g_{06})}{\omega_0^2 C_1}. \tag{4.44}$$

Therefore, if C_3 is chosen properly, an ideal equivalent inductor can be provided.

4.3 Low-voltage Active Inductor-based Bandpass Filter

4.3.1 Bandpass Filter Design

Transfer Function

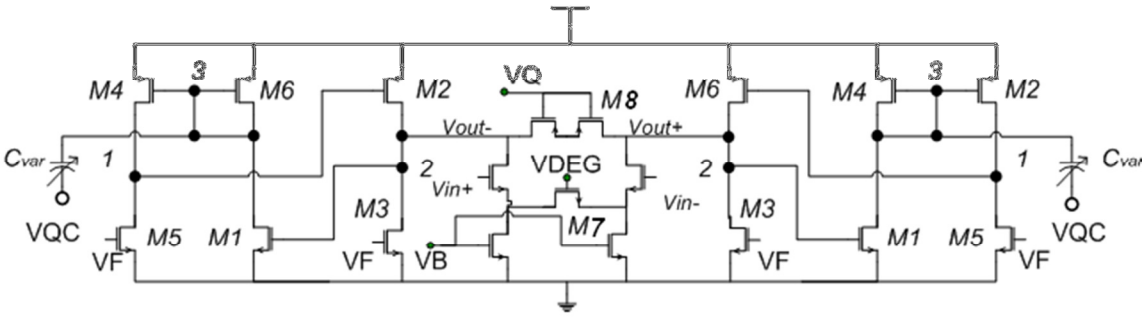

Figure 4.13 Proposed Active-Inductor Based Bandpass Filter Topology

Figure 4.13 shows the topology of proposed active inductor-based bandpass filter. It is designed by loading the source-degenerated differential pairs with the proposed active inductor and effective parallel resistors of M8. The supply voltage is 1V. After simplification, the transfer function is given by

$$H(s) \approx \frac{\frac{G_m}{C_2}s}{s^2 + s\left(\frac{g_1}{C_1} + \frac{g_2}{C_2} + \frac{C_3}{g_{m4}}\frac{g_1}{C_1}\frac{g_2}{C_2} - \omega_0^2\frac{C_3}{g_{m4}}\right) + \frac{g_{m1}g_{m2}}{C_1C_2}}, \tag{4.45}$$

where g_1, g_2 are the conductance associated with node 1 and 2, respectively. C_1, C_2 and C_3 are the total capacitors at node 1 and 2, including the parasitic capacitors. G_m is the effective transconductance of input source-degenerated differential pairs. The resonant frequency and Q of the filter are given by

$$\omega_0 = \sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}, \tag{4.46}$$

and

$$Q = \frac{\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}}{\left[\frac{g_1}{C_1} + \frac{g_2}{C_2} - \frac{C_3}{g_{m4}}\left(\omega_0^2 - \frac{g_1}{C_1}\frac{g_2}{C_2}\right)\right]}. \tag{4.47}$$

Frequency Tuning

From equation (4.46), the frequency of filter is depended on the transconductance gains and the capacitors loaded at node 1 and 2. To minimize power, no external capacitors are added at node 1 and 2, thus $C_1 = C_{p1}$ and $C_2 = C_{p2}$, where C_{p1} and C_{p2} are the parasitic capacitors associated with node 1 and 2, respectively. g_{m1} and g_{m2} can be changed by varying the current biasing M1 and M2. The DC current through M2 can adjusted through changing the gate voltage of M3, VF. The current through M1 is controlled by its gate voltage, which is also the output common-mode voltage. Biasing the gate voltage of M5 using VF, the output common-mode voltage is locked by VF through the negative feedback path through M1, M6, M4 and M2. Therefore, the

frequency tuning is achieved by varying VF. Figure 4.14 shows the frequency tuning range of designed filter based on small signal simulation. This bandpass filter can operate at frequencies over 4.5 to 5.5GHz. Q varies from 27.5 to 50 during frequency tuning from Figure 4.14.

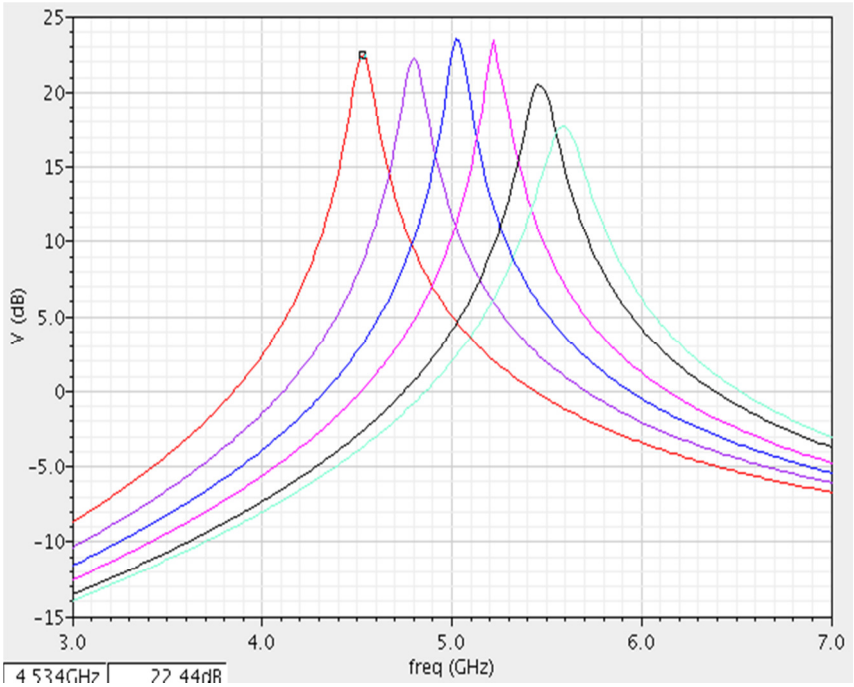

Figure 4.14 Frequency Tuning of Designed Filter

Q Tuning

The Q tuning is completed by two steps. The first step is to modify C_3 through varying varactor at node 3 by VQC to eliminate the loss term due to finite impedance at node 1 based on equation (4.43) and (4.47). In this way, an effective inductor without loss can be provided such that the Q of resonant network is dominated by the effective resistor values of M8, which can be achieved by varying the gate voltage of M8, VQ.

Adjusting VQ is the second step of Q tuning. If C_{var} is tuned properly, in (4.13) the effect of g_1 is eliminated and equation (4.13) becomes

$$Q = \frac{\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}}}{\frac{g_2}{C_2}}, \tag{4.48}$$

where $g_2 = 1/r_{02} + 1/r_{03} + 1/r_{in} + 1/R_{on8}$. r_{02}, r_{03} and r_{in} are the output impedances of M2, M3 and the source-degenerated input stage. R_{on8} is the effective resistor of M8 and

$$R_{on8} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS8} - V_{TH8})}. \tag{4.49}$$

Since, $R_{on8} \ll r_{02}, r_{03}, r_{in}$, so $g_2 \approx 1/R_{on8}$. Figure 4.15 shows the Q tuning of the designed bandpass filter based on small signal simulation. It covers a range from 3.4 to 568.5.

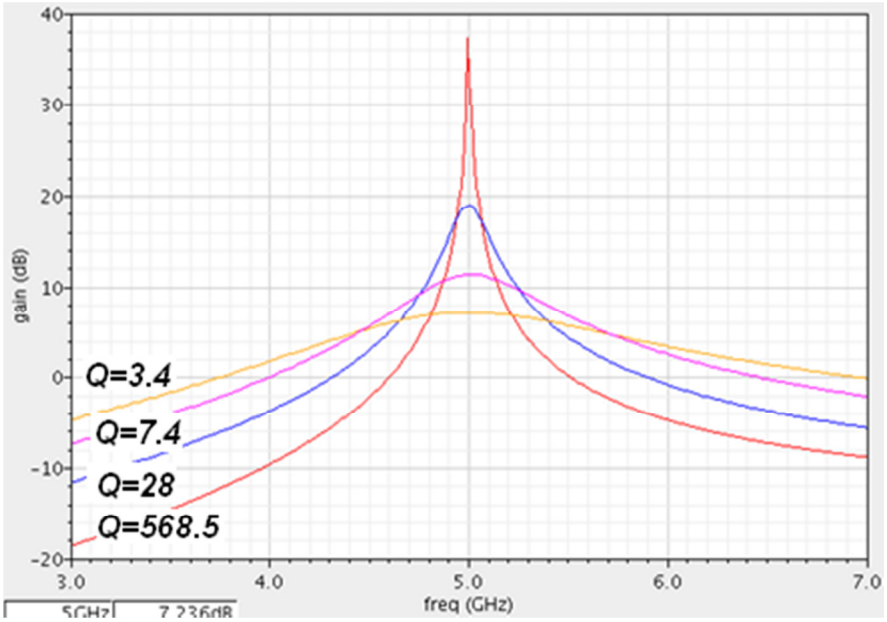

Figure 4.15 Q Tuning of Designed Filter

Stability

From equation (4.45), it must be ensured that

$$\frac{g_1}{C_1}+\frac{g_2}{C_2}+\frac{C_3}{g_{m4}}\frac{g_1}{C_1}\frac{g_2}{C_2}-\omega_0^2\frac{C_3}{g_{m4}}>0. \tag{4.50}$$

Otherwise, the circuit is not stable. Therefore, over tuning of C_{var} should be avoided.

4.3.2 Impact of Mismatch on Bandpass Filter

The transfer function given by (4.45) is based on the assumption that $g_{m1}=g_{m6}=g_{m4}$, and the circuit is perfect symmetrical. Figure 4.16 shows the single-end circuit of the bandpass filter. Consider the impact if $g_{m1}\neq g_{m6}\neq g_{m4}$, and the transconductance gain of GM path without signal inversion is

$$G_m=\frac{g_{m1}g_{m6}}{g_{m4}}. \tag{4.51}$$

Replace g_{m1} by (4.51) in (4.45), and the transfer function is affected by the value of g_{m4} and g_{m6} as

$$H(s)\approx\frac{\frac{G_{m,in}}{C_2}s}{s^2+s\left(\frac{g_1}{C_1}+\frac{g_2}{C_2}+\frac{C_3}{g_{m4}}\frac{g_1}{C_1}\frac{g_2}{C_2}-\omega_0^2\frac{C_3}{g_{m4}}\right)+\frac{g_{m1}g_{m6}g_{m2}}{g_{m4}C_1C_2}}, \tag{4.52}$$

where $G_{m,in}$ is the effective transconductance of input source-degenerated stage. C_1, C_2 and C_3 are the total capacitors at node 1, 2 and 3, respectively. g_1 and g_2 are the conductance associated with node 1 and 2. The frequency and Q are given by

$$\omega_0=\sqrt{\frac{g_{m1}g_{m6}g_{m2}}{g_{m4}C_1C_2}}, \tag{4.53}$$

and

$$Q = \frac{\sqrt{\frac{g_{m1}g_{m6}g_{m2}}{g_{m4}C_1C_2}}}{\left[\frac{g_1}{C_1} + \frac{g_2}{C_2} - \frac{C_3}{g_{m4}}\left(\omega_0^2 - \frac{g_1}{C_1}\frac{g_2}{C_2}\right)\right]}. \tag{4.54}$$

.

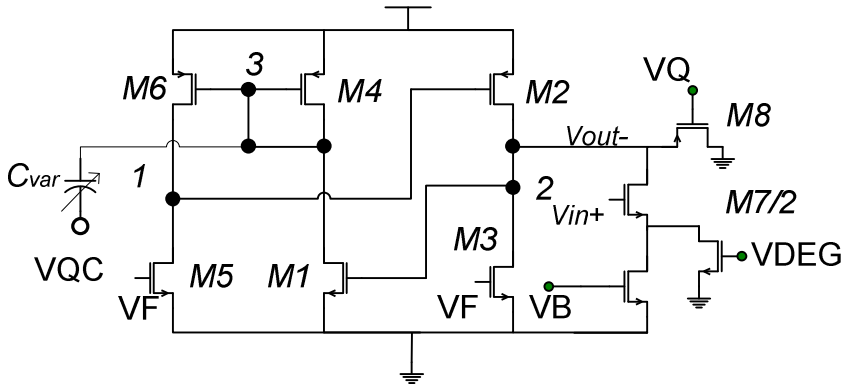

Figure 4.16 Half-Circuit of Designed Filter

If this differential bandpass filter is not perfect symmetrical. The transfer function of one single-end circuit is differential from that of the other one. The overall transfer function is given by

$$H(s)_{tot} = \frac{1}{2}(H(s)_{half} - H(s)'_{half}) \tag{4.55}$$

$$= \frac{1}{2}\left(\frac{\frac{G_{m,in}}{C_2}s}{s^2 + s\left(\frac{g_1}{C_1} + \frac{g_2}{C_2} + \frac{C_3}{g_{m4}}\frac{g_1}{C_1}\frac{g_2}{C_2} - \omega_0^2\frac{C_3}{g_{m4}}\right) + \frac{g_{m1}g_{m6}g_{m2}}{g_{m4}C_1C_2}}\right.$$

$$\left. + \frac{\frac{G_{m,in}{}'}{C_{2'}}s}{s^2 + s\left(\frac{g_{1'}}{C_{1'}} + \frac{g_{2'}}{C_{2'}} + \frac{C_{3'}}{g_{m4'}}\frac{g_{1'}}{C_{1'}}\frac{g_{2'}}{C_{2'}} - \omega_0{}'^2\frac{C_{3'}}{g_{m4'}}\right) + \frac{g_{m1'}}{g_{m4'}}\frac{g_{m6'}}{C_{1'}}\frac{g_{m2'}}{C_{2'}}}\right). \tag{4.56}$$

It is the combination of two bandpass function with different center frequency, Q and gain. Figure 4.17 illustrates that the overall transfer function has two resonances. If the two resonances are far from each other, the one has larger gain and higher Q can be used to filter the clock signal. However, the noise around the other resonance will be amplified and converted to jitter at the output. If the two resonances are closed to each other, a lager bandwidth will be provided, and the overall Q becomes smaller. Figure 4.18 and Figure 4.19 show the distribution of resonant frequency and Q from mote carlo simulation. The Q is 24 if no mismatch effect. The sigma value for center frequency is 373.3MHz. Most Qs are concentrated in the region over 3 to 40.

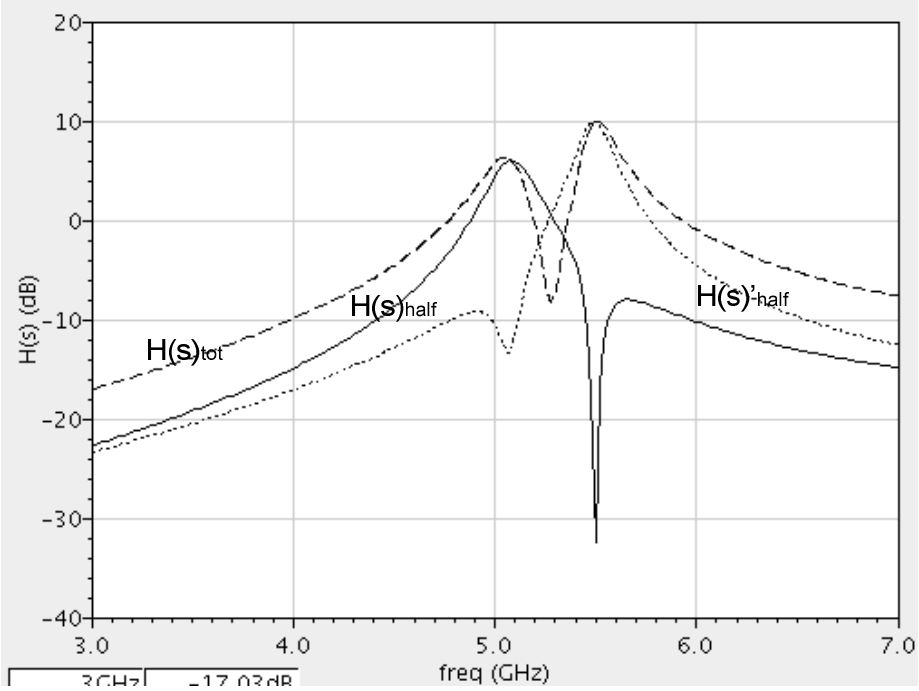

Figure 4.17 Effect of Mismatch on Transfer Function

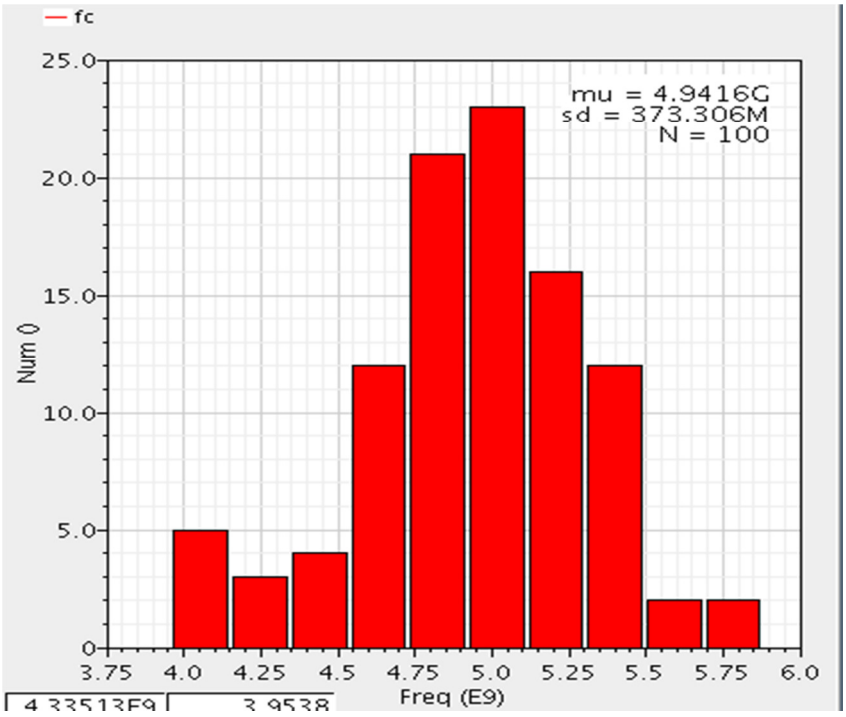

Figure 4.18 Distribution of Center Frequency

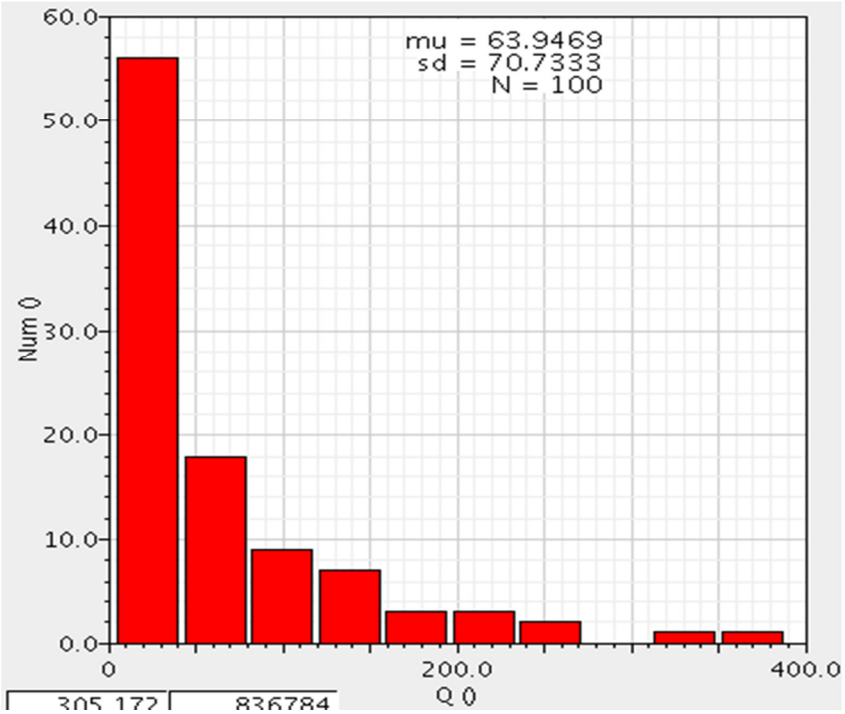

Figure 4.19 Distribution of Q

4.3.3 Impact of PVT Variations

In this section, the impact of PVT variations on frequency and Q is analysis based on the corner simulations.

In Figure 4.20, the solid line shows the simulated transfer function at typical-typical corner, while the dash line shows that at slow-slow corner. The frequency goes down from 5GHz to 4.34GHz and the Q changed from 25 to 21. The frequency can be tuned back to 5GHz by increase the current, the achievable Q range is 3.5 to 12.5 as shown in Figure 4.21. The Q range reduced a lot since that increase the current reduced the output impedance of the transistors and thus creates larger loss term of the active inductor. The varying of VQC fails to provide high Q inductor such that the filter Q is limited.

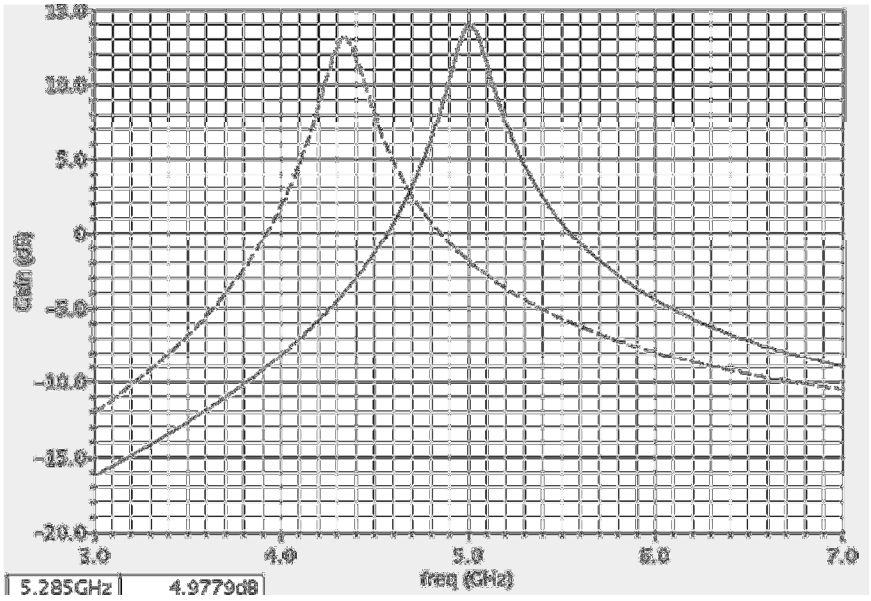

Figure 4.20 Transfer Function Based on TT (Solid Line) and SS (Dash Line) Simulations

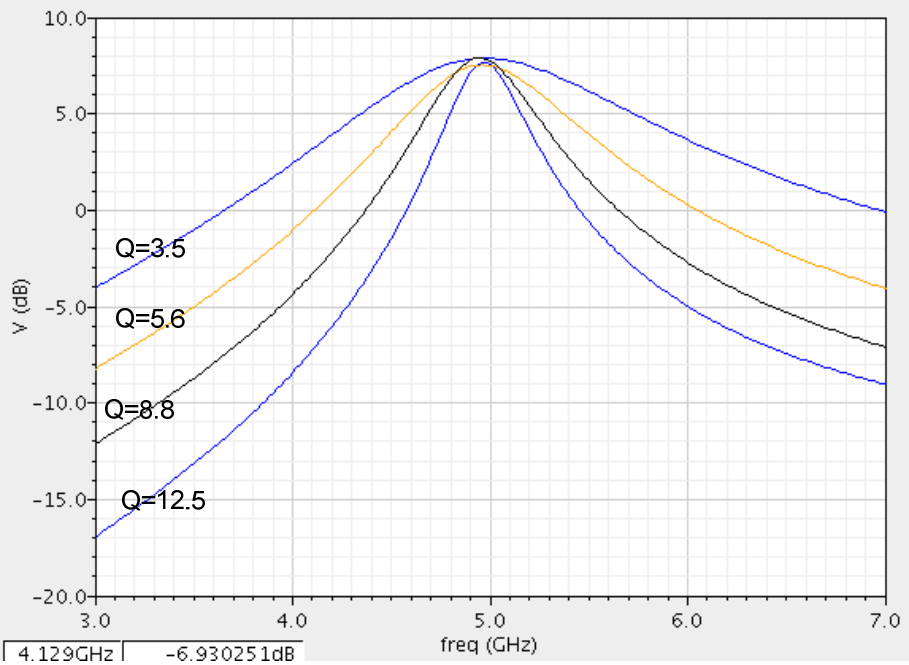

Figure 4.21 Q Tuning from SS Simulation

In Figure 4.22, the solid line shows the simulated transfer function at typical-typical corner, while the dash line shows that at fast-fast corner. Frequency goes up from 5GHz to 5.71GHz, while Q changes from 34 to 26. The frequency can be adjusted to 5GHz by reducing the current of active inductor. The Q range is from 3.4 to 288 as shown in Figure 4.23.

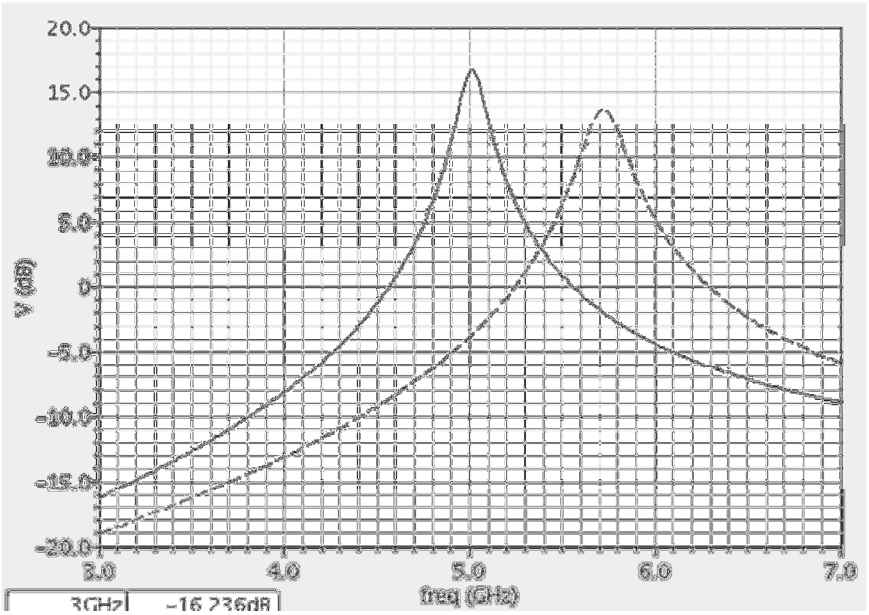

Figure 4.22 Transfer Function Based on TT (Solid Line) and FF (Dash Line) Simulations

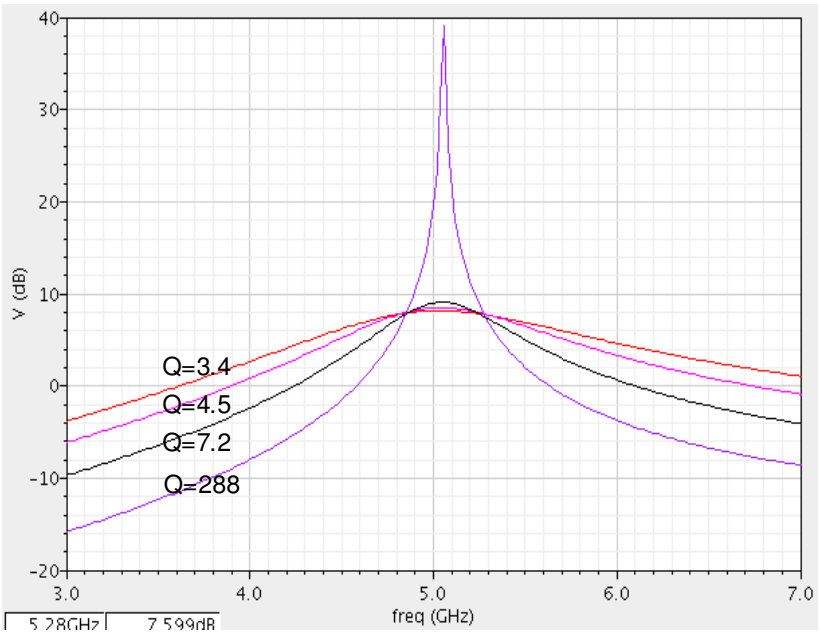

Figure 4.23 Q Tuning from FF Simulation

4.4 Design of On-chip Voltage Regulator

The active inductor-based bandpass filter is quite sensitive to the power supply noise, because it is loaded with active elements. In high speed applications, the typical power supply variation is +/- 5% of VDD with frequency of 200MHz, which results in jitter even though there is an ideal clock input. Also, this supply-induced jitter is uncorrelated with the data jitter. A voltage regulator is required to isolate the supply of the bandpass filter supply from the power supply and provides high power supply rejection (PSR) over wide frequency range that cover frequencies around 200MHz.

Replica Compensated Linear Regulator

[17] discussed the design of replica compensated linear regulator that can provide high supply rejection at high frequency. This Topology is shown in Figure 4.24. The replica loop creates an additional negative feedback loop to extend the bandwidth of the regulator's amplifier such that the output pole becomes dominant. In addition, it creates a replica signal Vrep indicative of supply noise at Vreg in the local feedback path such that the amplifier make use of all its available gain to reject the supply noise. From Figure 4.24, the actual load current is M times of the replica load current. Thus, the effective resistor of the replica load should M times of that of actual load to match the replica and actual I-V curves.

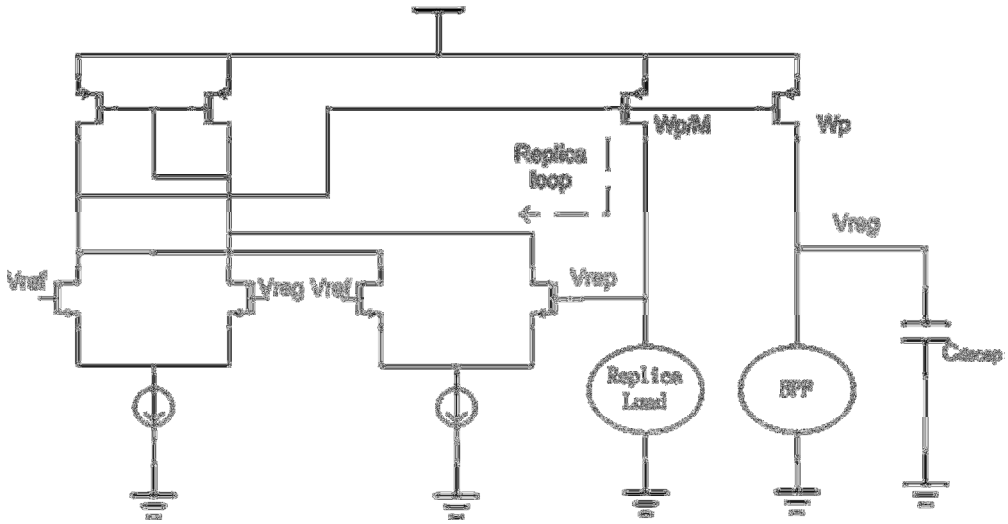

Figure 4.24 Replica Compensated Linear Regulator

Replica Load Design

The proposed replica load should track the I-V characteristic of the design bandpass filter. Analysis the common-mode characteristic of the bandpass filter, and the circuit in Figure 4.13 can be simplified as shown in Figure 4.25. It has been mentioned in the last section that $V_2 \approx V_F$, so $V_1 \approx V_3$. The common-mode circuit can be simplified by combing the branches (M5, M6), (M3, M4) and (M1, M2). Take certain faction of the transistor sizing in bandpass filter, and design the replica load as shown in Figure 4.26. Figure 4.27 displays the PSR of the designed regulator. It provides supply rejection of 24 dB at DC and 30 dB at 200MHz.

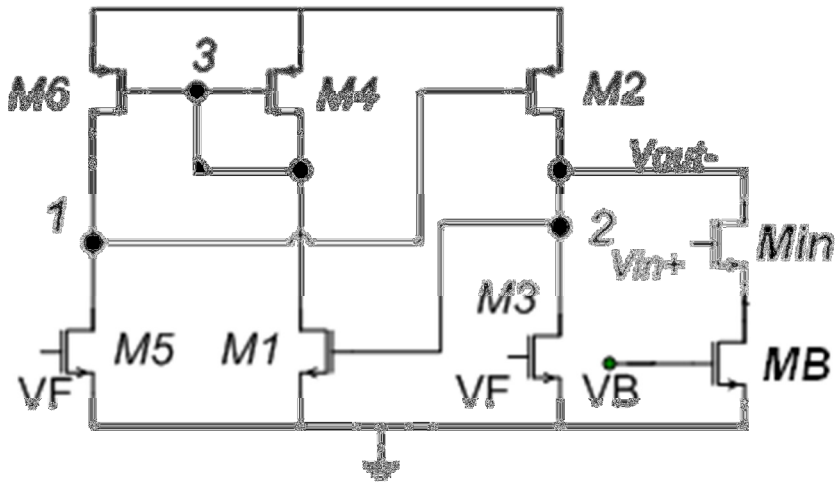

Figure 4.25 Common-Mode Analysis of Designed Bandpass Filter

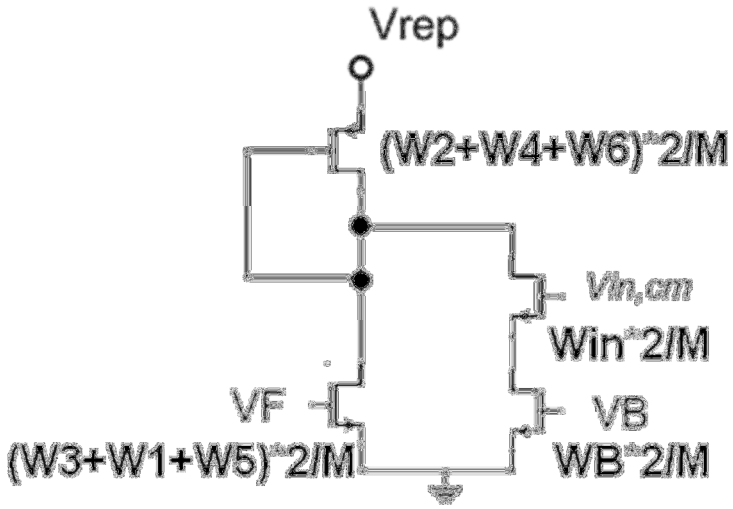

Figure 4.26 Design of Replica Load

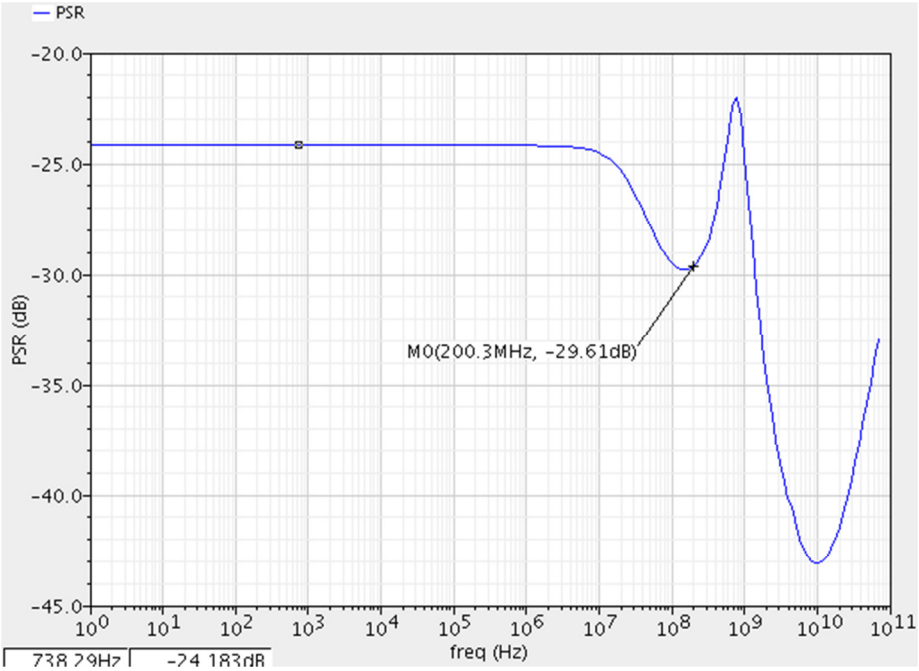

Figure 4.27 PSR of Designed Voltage Regulator

4.5 Design of Output Buffer

There are two major concerns on the design of output buffer. One is that large size input transistor will load the output of the bandpass filter and reduce the resonant frequency. The other is that output impedance of the buffer must be 50Ω to match 50Ω characteristic impedance of the probe that will be used in testing the output signal.

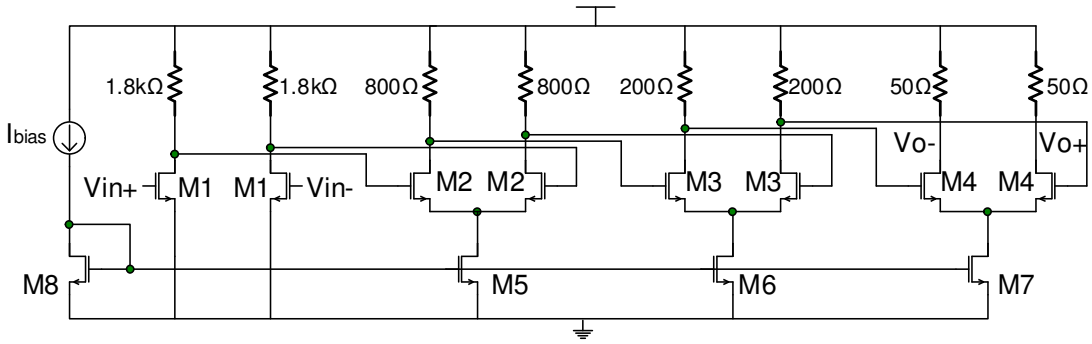

Figure 4.28 Output Buffer Schematic

Figure 4.28 shows the topology of the designed output buffer. To avoid the loading effect of AC coupling capacitor parasitics, Pseudo-differential pairs (M1 pairs) are used as the input stage of the output buffer such that filter output can be DC coupled to the input of buffer. The size of M1 pairs should be as small as possible to avoid loading the filter output effectively. The load resistors of the first stage should be chosen properly to ensure the gain of the stage at least 1 and output common-mode voltage around 900mV – 1V to bias the second. The second, third and fourth stages employ the resistive loaded fully differential structure. The input pairs and biasing current is scaled up by four while the load resistor is scaled down by four from stage to stage. In this way, the pole associated with output of each stage can be pushed to frequency much higher the 5GHz to reduce the filtering effect on the signal to be tested. Moreover, the load of last stage can be scaled down to 50Ω for matching with the probe impedance. Meanwhile, the total gain of the buffer can be retained by scaling up the transconductance and scaling down the load impedance stage by stage. Figure 4.29 displays the simulated transfer function of the output buffer. The gain at 5GHz is larger than 0dB. Figure 4.30 shows the output swing with 200mVpp single-end 5GHz input. The single-end output swing is a litter bit larger than 200mVpp.

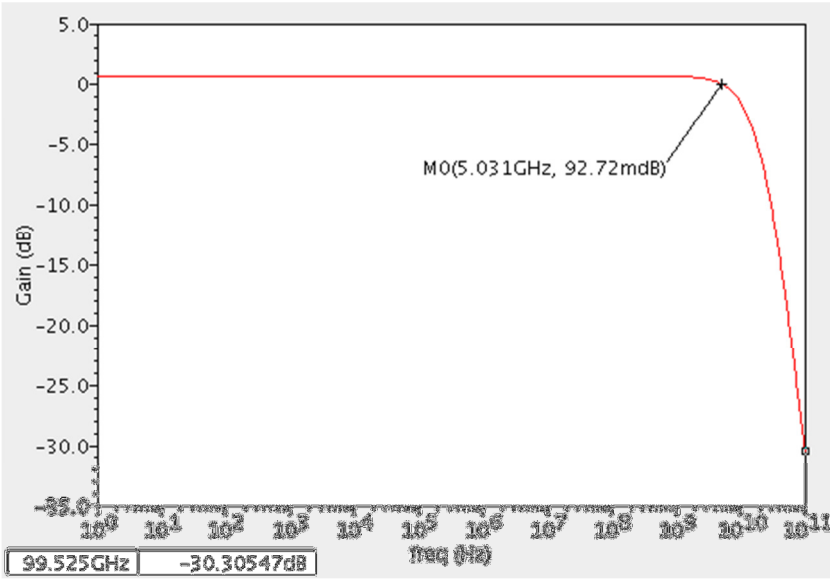

Figure 4.29 Transfer Function of Output Buffer

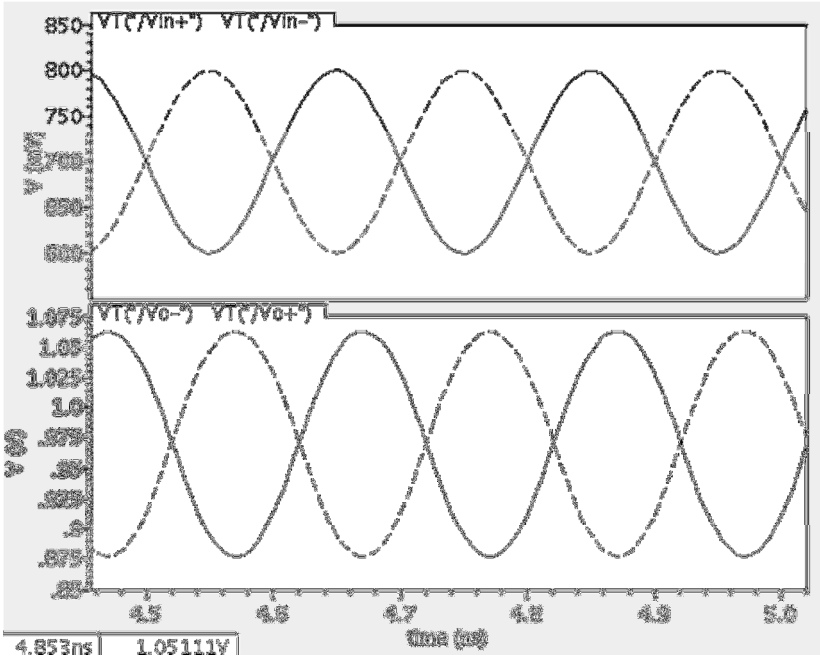

Figure 4.30 Input and Output Swing of Buffer

CHAPTER V

POST-LAYOUT

SIMULATION RESULTS

The final layout of the circuit with pads is shown in Figure 5.1, including bandpass filter, voltage regulator and output buffer. Figure 5.2 is the zoom-in area of circuit layout. The simiulation results are presented in the following subsections.

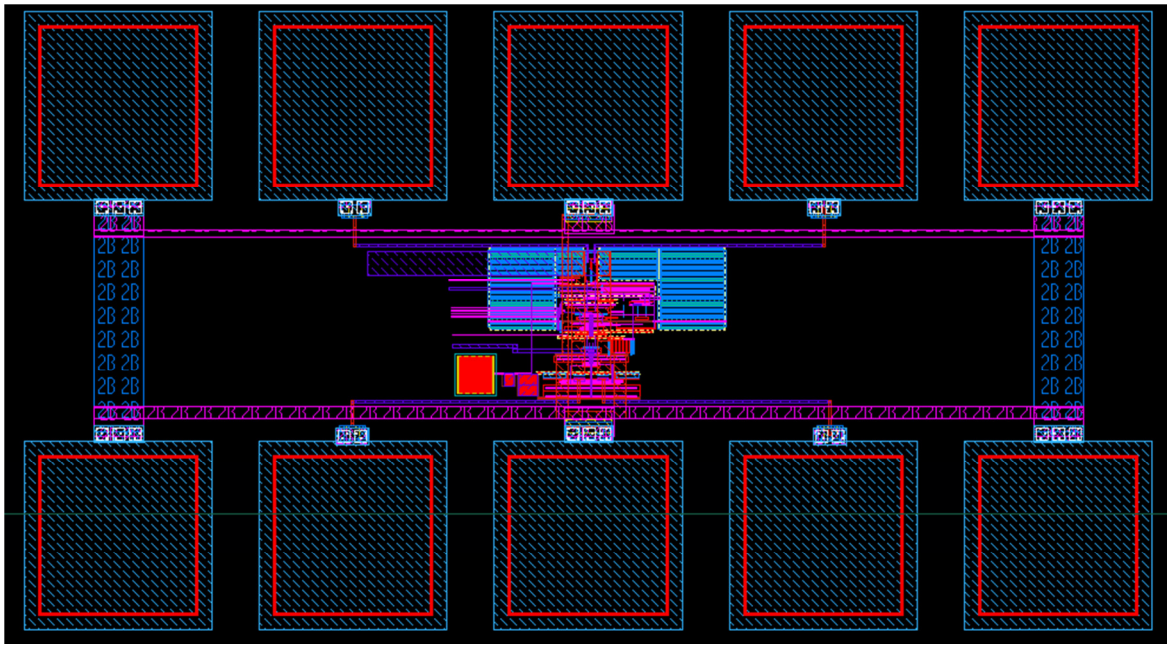

Figure 5.1 Layout with Pads

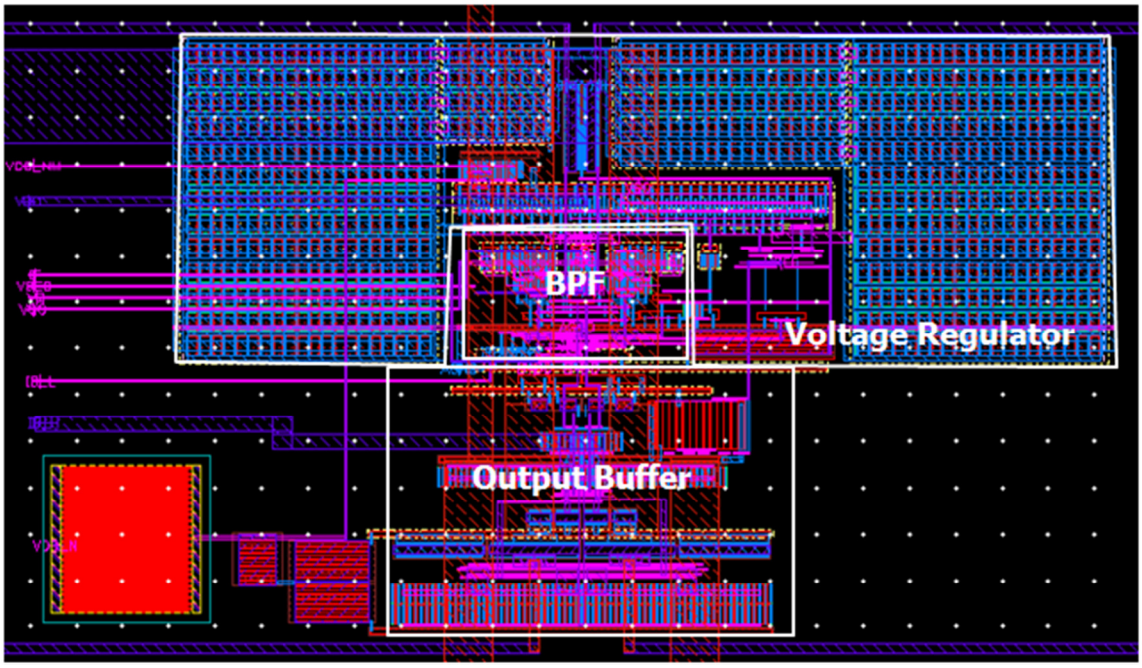

Figure 5.2 Zoom-In of the Circuit Layout

5.1 Frequency and Q Tuning

The input swing level impacts the linearity of circuit. The frequency and Q are simulated in different input swing levels.

100 mVpp Differential Input

100mVppd sinusoidal wave is input, and the frequency and Q tuning plots are shown in Figure 5.3 and Figure 5.4, respectively. The achieved frequency tuning range is from 4.4 to 5.6 GHz. The Q varies from 5.6 to 6.5 in Figure 5.3. Q is adjustable from 3.6 to 14.5. The lowest achievable JTB correspond to Q of 14.5 is 180MHz, as shown in Figure 5.5. The highest JTB is around 600MHz, which corresponds to Q of 3.4 and can be found in Figure 3.7.

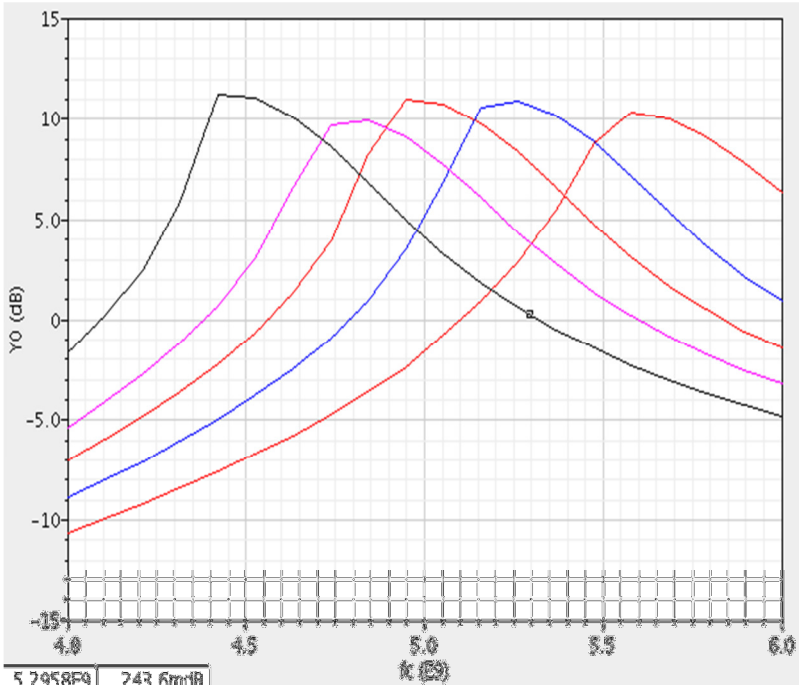

Figure 5.3 Frequency Range for 100mVppd Input

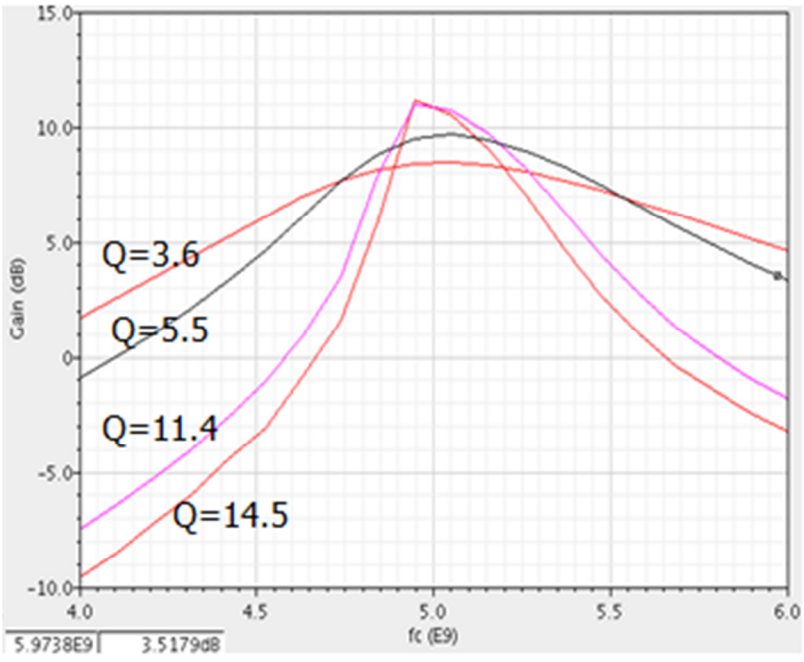

Figure 5.4 Q Range of 100mVppd Input

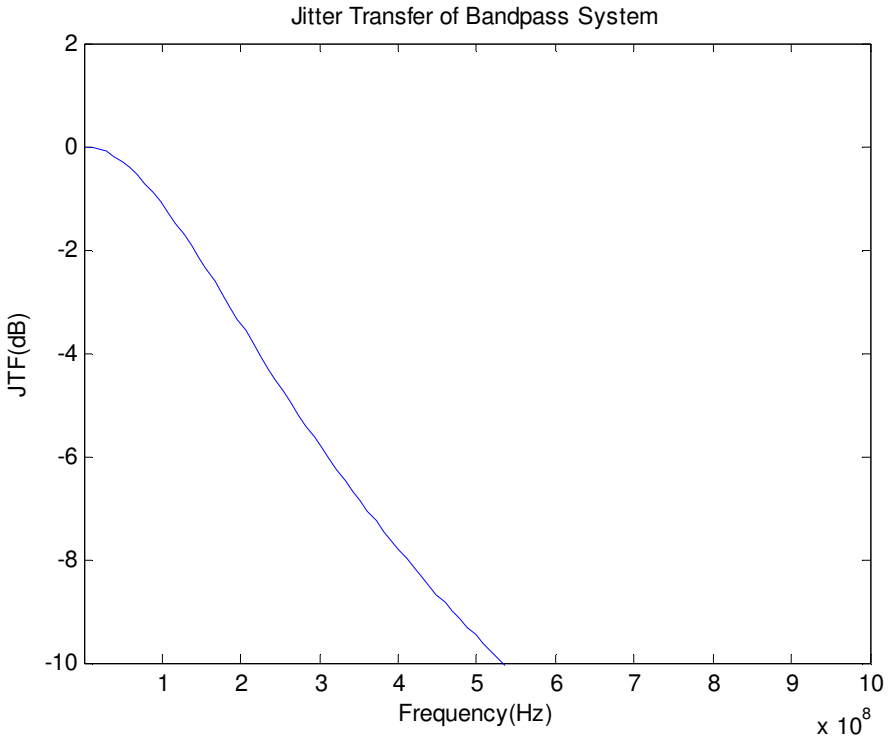

Figure 5.5 JTF of Q =14.5

40mVpp Differential Input

If 40mVppd sinusoidal wave is input, the circuit can operate more linearly. It can achieve higher Q. Q range of 40mVppd input is shown in Figure 5.6, which shows that the highest achievable Q is 26.4. It provides lowest JTB of 107MHz as shown in Figure 5.7. The frequency range is similar to that shown in Figure 5.3.

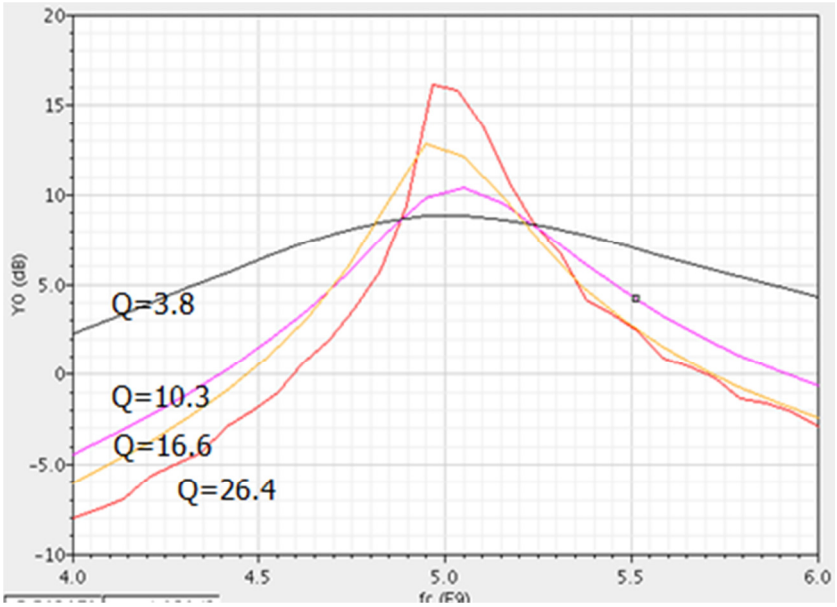

Figure 5.6 Q Range of 40mVppd Input

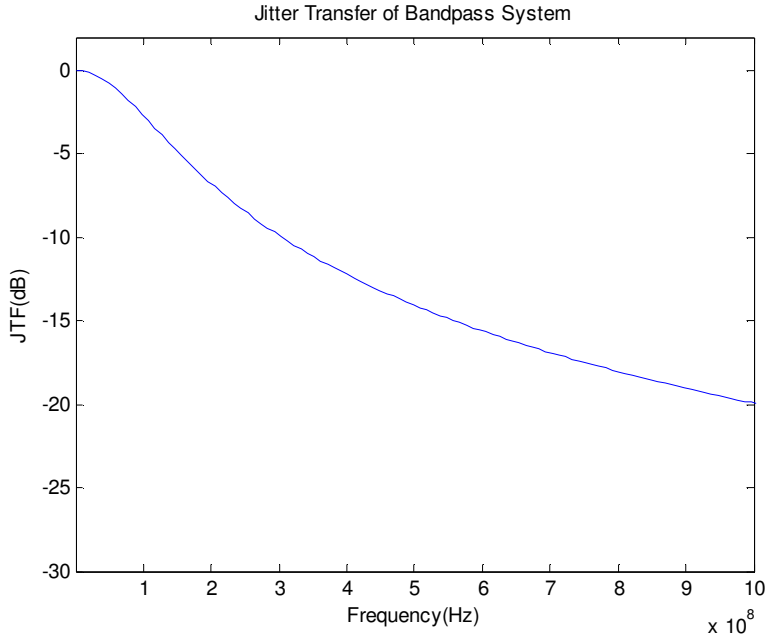

Figure 5.7 JTF of Q = 26.4

Small Signal Input

If the input signal is very small, the filter is always operating in linear region. The ideal Q tuning range is shown in Figure 5.8, which show the highest Q of 568.5. The lowest JTB is 40MHz from the JTF in Figure 5.9. Ideally, the designed filter can provide the JTB that is able to minimize differential jitter for 10 UI clock-to-data skew, as mentioned in 0.

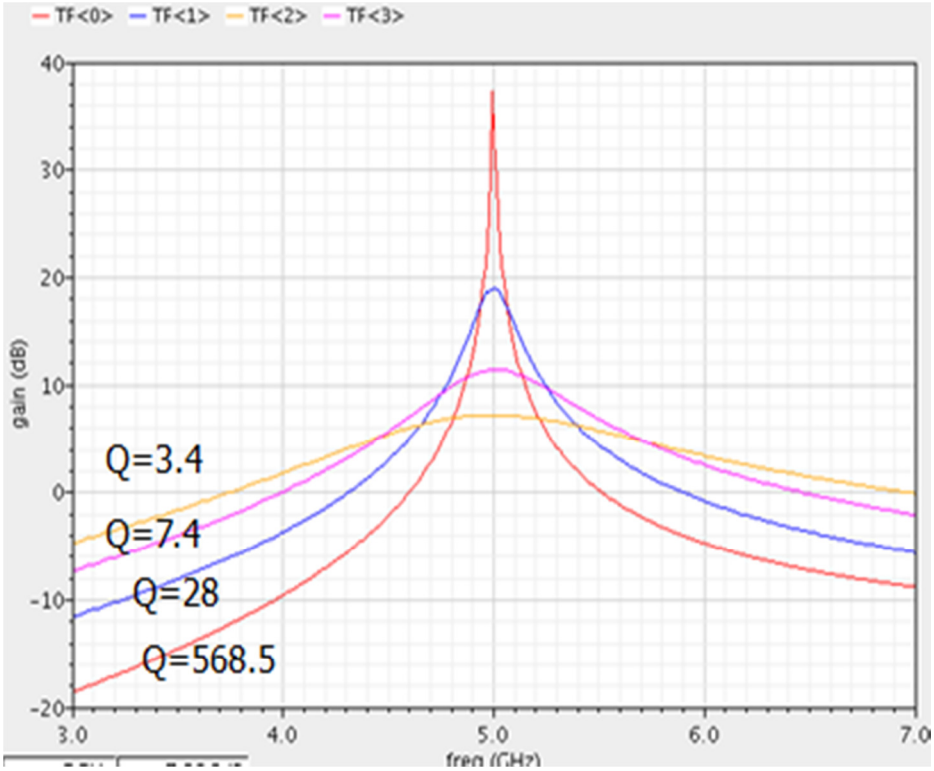

Figure 5.8 Q Range of Small Signal Input

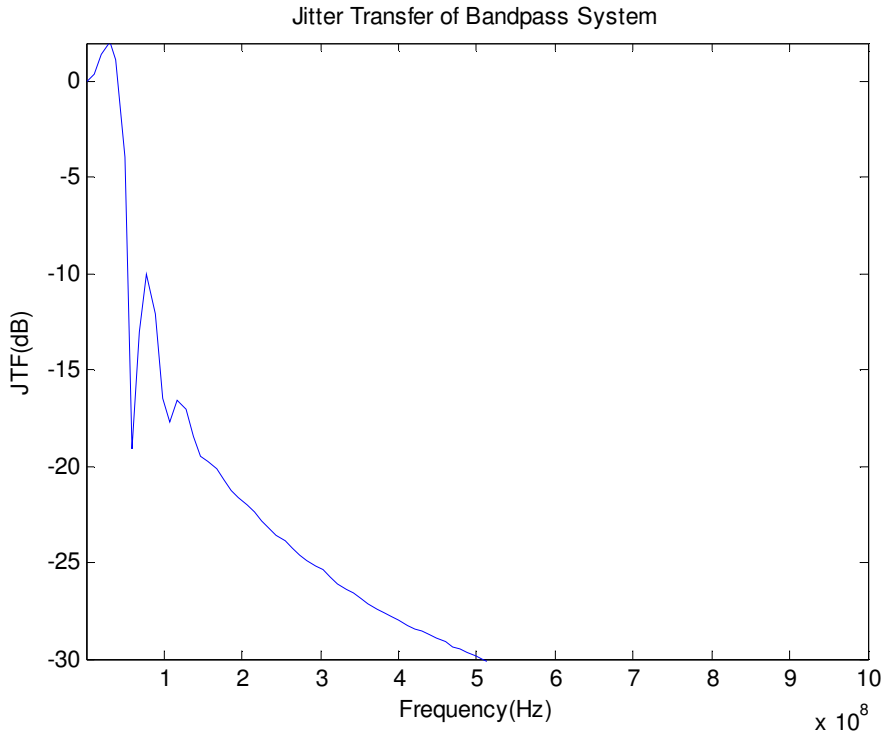

Figure 5.9 JTF for Q = 568.5

5.2 Supply Sensitivity

The supply noise affects the operation of active inductor and induces jitter. The supply sensitivity is used to quantify how much jitter is induced by each mV supply noise. In high speed application, the typical supply noise level is +/- 5% of supply voltage (1.2 V). In this simulation, 120mVpp noise is applied around 1.2V supply of the voltage regulator. The noise frequency is swept non-linearly from DC to 300MHz, and the simulated supply induced jitter and supply sensitivity is shown in Table 5.1.

Table 5.1 Supply Induced Jitter and Supply Sensitivity at Different Frequencies

Frequency (MHz)	Total Induced Jitter (ps)	Supply Sensitivity (fs/mV)
DC	2.4	20
10	2.0	16.7
20	1.6	13.3
50	1.06	8.8
100	0.717	5.9
200	0.567	4.7
300	0.544	4.5

It can be found that the supply sensitivity decreases and frequency increases, which follows the similar behavior as shown in PSR simulation of Figure 4.27.

5.3 Equivalent RMS Input Jitter Due to Thermal Noise

The thermal noise of circuit also induced jitter at the output, which can be referred to input as input referred noise. The simulated input referred RMS noise voltage is from 500uV to 600uV. The equivalent input RMS jitter is given by divided the input referred noise by the input slop at zero-crossing as

$$J_{rms} = \frac{1}{2\pi}\frac{V_n}{V_p}T_{clk} \tag{5.1}$$

, where V_n is the input referred RMS noise voltage while V_p is the input amplitude. T_{clk} is one clock cycle and 200ps for 5GHz clock. For 100mVppd input, the clock amplitude is 50mV and the equivalent input RMS jitter is from 0.32 to 0.38ps. For 40mVppd input, the equivalent input RMS jitter is from 0.8 to 0.96ps. To minimize the input RMS jitter,

large input clock swing should be applied. However, it degrades the linearity of filter and limits the highest achievable Q value.

5.4 Performance Summary

The bandpass filter performance is summarized in the Table 5.2.

Table 5.2 Performance Summary of Designed Bandpass Filter

Parameters	**Value**
Frequency	5GHz
Frequency Tuning Range	4.4 – 5.6 GHz
Q Tuning Range	3.4 – 568.5
JTB Range	40 – 600 MHz
Supply Sensitivity@200MHz	4.7 fs/mV
Input RMS Jitter	0.32 – 0.38 ps w/ 100mVppd Input 0.8 – 0.96 ps w/ 40mVppd Input
Power	1.184mW
Area	23.3um × 8.2um w/o Voltage Regulator 100um × 36um w/ Voltage Regulator

CHAPTER VI

CONCLUSION AND FUTURE WORK

Table 6.1 compares the designed active inductor-based bandpass filter with other bandpass filters in [15] and [5]. Compared to Xiao's filter, which uses active inductor as well, the designed filter can operated at the environment with much lower supply voltage to threshold voltage ratio. In addition, it consumes much less area compared to the passive bandpass filter introduced in [5].

Table 6.1 Performance Comparison with Other Bandpass Filter

Specifications	**[15]**	**[5]**	**This work**
Frequency	5.4GHz	5GHz	5GHz
Frequency Range	3.34-5.72GHz	2.38-8.53GHz	4.4 – 5.6GHz
Q Range	2 - 665	2.622	3.4 – 568.5
Gain at fc	n/a	7.9dB	7.6dB – 11dB
Area	26.6um×30um	85um×85um (Inductor alone)	23.3um×8.2um w/o Voltage regulator 100um×36um w/ Voltage Regulator
VDD	1.8V (Vt ~320mV)	1.2V	1.0V 1.2V w/Voltage Regulator (Vt~600mV)
Power	4.4mW	5.695mW	1.184mW
Power Supply Sensitivity	n/a	6fs/mV	4.7fs/mV
Technology	0.18um CMOS	90nm CMOS	90nm CMOS

Table 6.2 compares the controllable JTB range using the designed filter with that using other techniques. The proposed solution can provide jitter tracking at higher frequencies. Also, the lowest achievable JTB is able to minimize clock to data differential jitter with 10 UI clock-to-data skew.

Table 6.2 Comparison of Achievable JTB Range over Different Technique

Specifications	**[Agrawal '08]**	**[Hu '09]**	**[Hossain '10]**	**This work**
Architecture	DLL	ILO	MILO_ILO	BPF
Data Rate	5Gb/s	7.3Gb/s	7.4Gb/s	10Gb/s
Clock frequency	¼ rate	¼ rate	¼ rate	½ rate
JTB	All passes	30M – 100MHz	25MHz – 200MHz	40MHz – 600MHz

Note:
DLL – Delay-Locked Loop
ILO – Injection-Locked Oscillator
MILO_ILO – Frequency-Multiplying Injection- Locked Oscillator and Per Pin Local Injection-Locked Oscillators
BPF – Bandpass Filter

In system applications, the frequency tuning should be completed automatically. The automatic tuning scheme is proposed and shown in Figure 6.1. The output of bandpass filter is passed into two paths, where the buffers are used to isolate the tuning circuitry and the filter output. The path with frequency divider is used to generate three sampling phases Ø1, Ø2 and Ø3. The other path passes the clock output to a rectifier followed by a low-pass filter to generate the DC voltage proportional to the output swing

level. The DC voltages at Ø1 and Ø2 are sampled and passed to the comparator controlled by Ø3. Based on the comparison between voltages at Ø1 and Ø2, the comparator output the UP/DN signal for the following counter. The current DAC convers the code from counter to voltage to control the center frequency of the bandpass filter. The phase difference between Ø1 and Ø2 should be long enough such that the waveform has enough time to settle after the change of VF. Before the bandpass filter reaches its peak swing, the counter would counts in one direction and thus the VF is adjusted in one direction. If the peak swing is achieved, the comparator will output '1' and '0' alternatively. Then the counter outputs a code varying by its LSB. Thus, VF is settled.

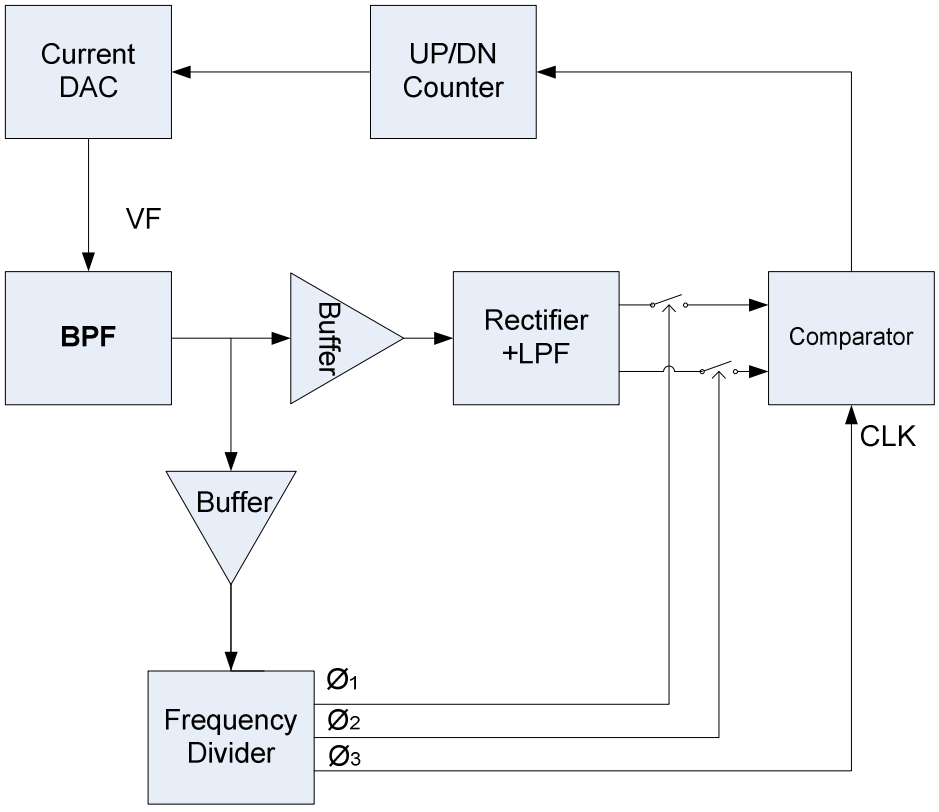

Figure 6.1 Block Diagram of Automatic Frequency Tuning

In summary, the optimum jitter tracking is achievable through bandpass filtering of forwarded clock signal in forwarded-clock systems. Wide range of controllable JTB is required to compensate the impact of different amount of clock-to-data skew. The designed active inductor-based bandpass filter can provide JTB over 40 – 600 MHz with low-voltage, low power consumption as well as low area.

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